测试

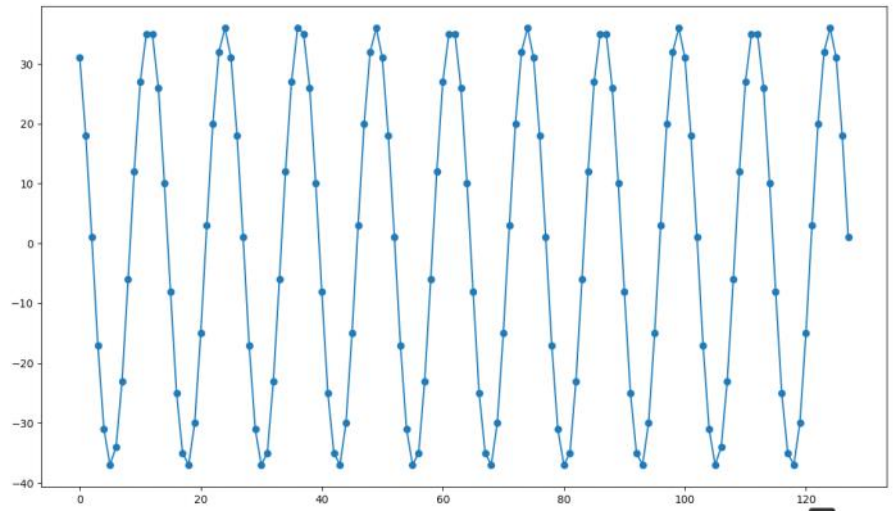
2023年6月8日　22:45

Adc16使用mlib_devel-ebdc

主mlib_devel-lijian

只替换@xps_adc16

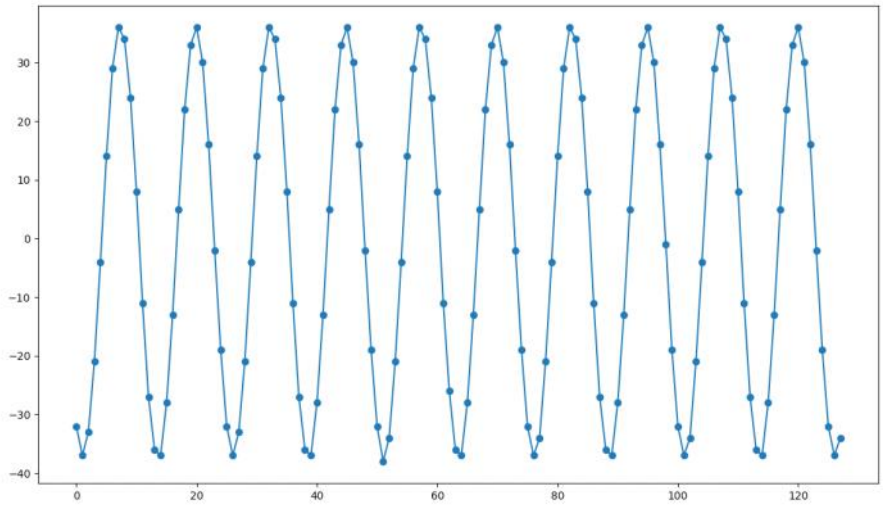
```
(env1) [observer@cylctrl bin]$ ruby adc16_status.rb roach8
roach8: Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
roach8: Gateware supports demux modes (currently using demux by 1)
roach8: ZDOK0 clock OK, ZDOK1 clock OK
roach8: AAAABBBBCCCCDDDDEEEEFFFFGGGGHHHH
roach8: 12341234123412341234123412341234
roach8: ................................ deskew
roach8: ................................ sync
(env1) [observer@cylctrl bin]$
```



试试整体

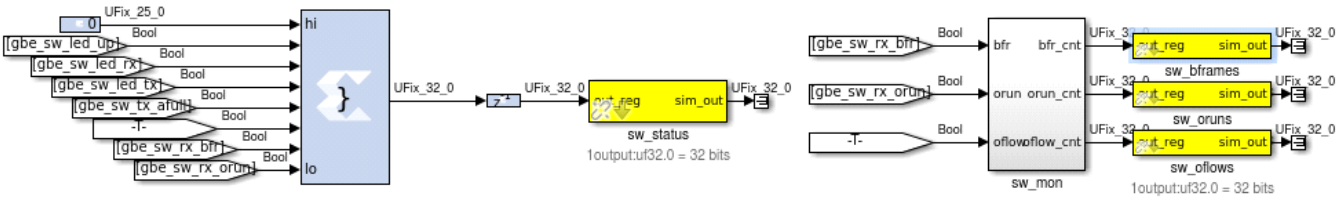
```
Bitstream generation is complete.
========================================================================
Flow run time summary: (01:02:32 seconds total)
    System update............00:00:22
    Design Rules Check.......00:00:04
    Xilinx System Generator..00:01:36
    Base system copy.........00:00:00
    IP creation..............00:00:00
    EDK files creation.......00:00:19
    IP elaboration...........00:00:00
    Software creation........00:00:00
    EDK/ISE backend..........01:00:08
========================================================================
```

```
Connecting to roach8...
Programming roach8 with roach2_fengine68pmli.bof...
Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
Gateware supports demux modes (using demux by 1)
Resetting ADC, power cycling ADC, and reprogramming FPGA...
ZDOK0 clock OK, ZDOK1 clock OK
Calibrating SERDES blocks...ABCDEFGH
SERDES calibration successful.
Selecting analog inputs...
Using default digital gain of 1...
Done!
Done#########
```



添加噪声源控制后

```
**********************************************************************************
ERROR: 1 constraint not met.

PAR could not meet all timing constraints. A bitstream will not be generated.

To disable the PAR timing check:

1> Disable the "Treat timing closure failure as error" option from the Project Options dialog in XPS.

OR

2> Type following at the XPS prompt:
XPS% xset enable_par_timing_error 0
**********************************************************************************
gmake: *** [implementation/system.bit] Error 1
ERROR:EDK -
   Error while running "gmake -f system.make bits".
: XPS failed.
Backtrace 1: gen_xps_files:708
Backtrace 2: run_Callback:163
Backtrace 3: casper_xps:88
Backtrace 4: @(h0bject,eventdata)casper_xps('run_Callback',h0bject,eventdata,guidata(h0bject)):0
>> system_routed
```



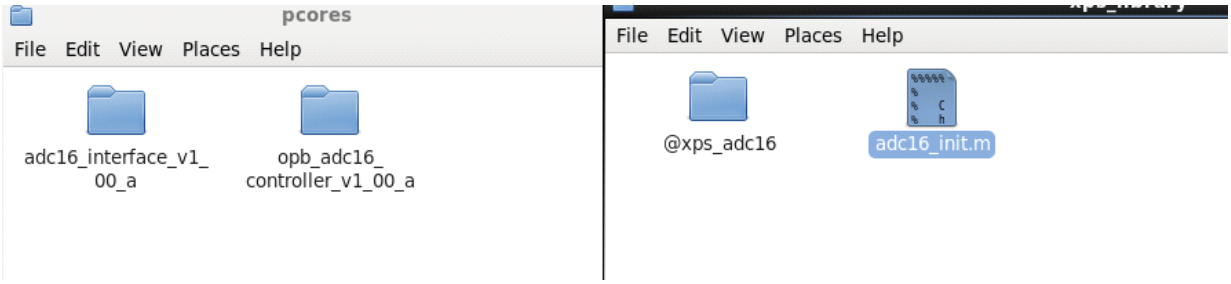
只加这些 发现还是编译有问题

```
xflow done!
touch __xps/system_routed
xilperl /opt/Xilinx/14.7/ISE_DS/EDK/data/fpga_impl/observe_par.pl -error yes implementation/system.par
Analyzing implementation/system.par
********************************************************************************
ERROR: 1 constraint not met.

PAR could not meet all timing constraints. A bitstream will not be generated.

To disable the PAR timing check:

1> Disable the "Treat timing closure failure as error" option from the Project Options dialog in XPS.

OR

2> Type following at the XPS prompt:
XPS% xset enable_par_timing_error 0
********************************************************************************
gmake: *** [implementation/system.bit] Error 1
ERROR:EDK -
   Error while running "gmake -f system.make bits".
: XPS failed.
Backtrace 1: gen_xps_files:708
Backtrace 2: run_Callback:163
Backtrace 3: casper_xps:88
Backtrace 4: @(h0bject,eventdata)casper_xps('run_Callback',h0bject,eventdata,guidata(h0bject)):0
>>
```

怎么回事呢 重新来一遍

Lijian-mlib_devel 与 adc16 的 xpsadc16

Lidevel_mlib 替换所有adc16有关的



先替换 xps_adc16

```
Bitstream generation is complete.
================================================================
Flow run time summary: (00:07:10 seconds total)
    System update.....00:00:01
    Design Rules Check.....00:00:00
    Xilinx System Generator..00:00:20
    Base system copy.....00:00:00
    IP creation.....00:00:00
    EDK files creation.....00:00:02
    IP elaboration.....00:00:00
    Software creation.....00:00:00
    EDK/ISE backend.....00:06:46
================================================================
>>
```

```
(env1) [observer@cylctrl bin]$ ruby adc16_status.rb roach8
roach8: Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
roach8: Gateware supports demux modes (currently using demux by 1)
roach8: ZDOK0 clock OK, ZDOK1 clock OK
roach8: AAAABBBBCCCCDDDDEEEEFFFFGGGGHHHH
roach8: 12341234123412341234123412341234
roach8: ................................ deskew
roach8: ....XXXXXXXX........XXXXXXXXXXXX sync
(env1) [observer@cylctrl bin]$
```

不行

再加一个adc16_init.m

```
(env1) [observer@cylctrl bin]$ ruby adc16_status.rb roach8
roach8: Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
roach8: Gateware supports demux modes (currently using demux by 1)
roach8: ZDOK0 clock OK, ZDOK1 clock OK
roach8: AAAABBBBCCCCDDDDEEEEFFFFGGGGHHHH
roach8: 12341234123412341234123412341234
roach8: ................................ deskew
roach8: XXXX....XXXXXXXXXXXXXXXXXXXX.... sync
(env1) [observer@cylctrl bin]$
```

不行

加一个

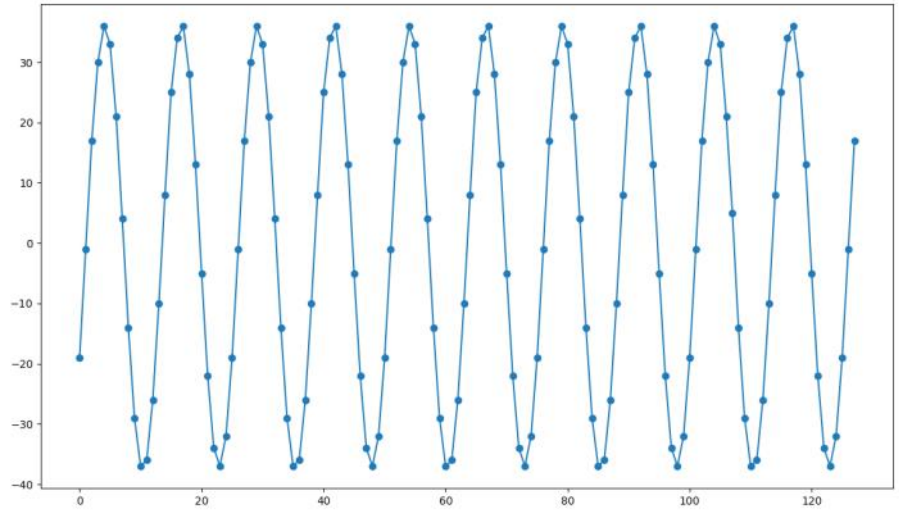
opb_adc16_
controller_v1_00_a

```
Constructing platform-level connectivity ...
ERROR:EDK:4073 - INSTANCE: opb_adc16_controller_0, PORT: adc16_iserdes_bitslip,
   CONNECTOR: adc16_iserdes_bitslip - 64 bit-width connector assigned to 8
   bit-width port -
   /home/wz/mlib_library/mlib_devel-wz/testadc69pm8/XPS_ROACH2_base/system.mhs
   line 58
Completion time: 0.00 seconds
ERROR:EDK:440 - platgen failed with errors!
gmake: *** [implementation/system.bmm] Error 2
ERROR:EDK -
   Error while running "gmake -f system.make bits".
: XPS failed.
Backtrace 1: gen_xps_files:708
Backtrace 2: run_Callback:163
Backtrace 3: casper_xps:88
Backtrace 4: @(h0bject,eventdata)casper_xps('run_Callback',h0bject,eventdata,guidata(h0bject)):0
>>
```

再加一个

adc16_interface_v1_
00_a c

```
(env1) [observer@cylctrl rb_test]$ ./6test.sh
Hellow,It is a nice day,isn't it?
Connecting to roach8...
Programming roach8 with testadc69pm10.bof...
Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
Gateware supports demux modes (using demux by 1)
Resetting ADC, power cycling ADC, and reprogramming FPGA...
ZDOK0 clock OK, ZDOK1 clock OK
Calibrating SERDES blocks...ABCDEFGH
SERDES calibration successful.
Selecting analog inputs...
Using default digital gain of 1...
Done!
Done#########
(env1) [observer@cylctrl rb_test]$
```

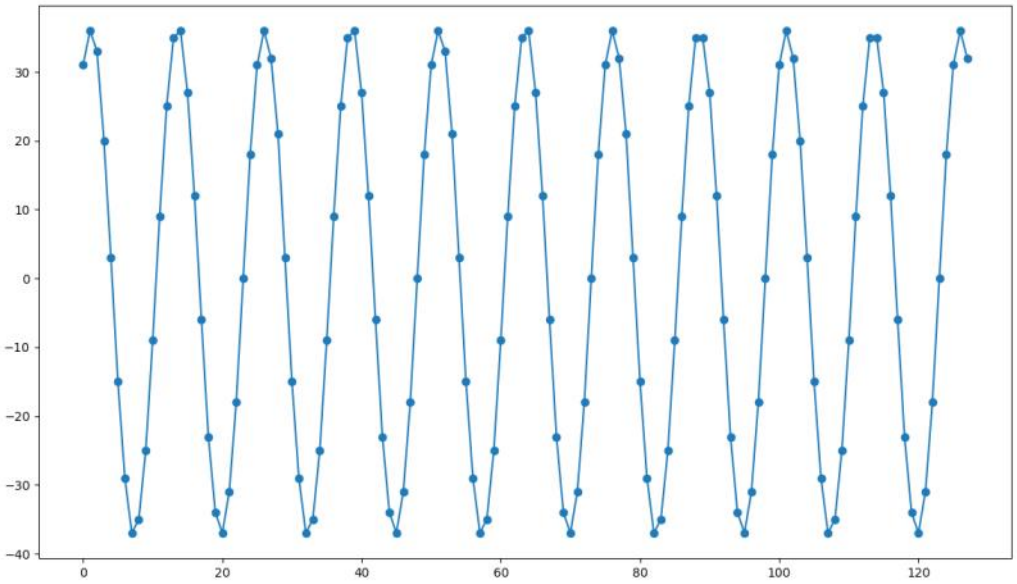


可以

试试整体

```
Detected Linux OS
############################
##      System Update     ##
############################
############################
## Block objects creation  ##
############################
####################
## Checking objects ##
####################
: XPS block must be on the same level as the Xilinx SysGen block
Backtrace 1: drc:32
Backtrace 2: gen_xps_files:312
Backtrace 3: run_Callback:163
Backtrace 4: casper_xps:88
Backtrace 5: @(h0bject,eventdata)casper_xps('run_Callback',h0bject,eventdata,guidata(h0bject)):0
############################
## Block objects creation  ##
############################
####################
## Checking objects ##
####################
Running system generator ...
```

```
(env1) [observer@cylctrl rb_test]$ gedit 6test.sh
(env1) [observer@cylctrl rb_test]$ ./6test.sh
Hellow,It is a nice day,isn't it?
Connecting to roach8...
Programming roach8 with roach2_69.bof...
Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
Gateware supports demux modes (using demux by 1)
Resetting ADC, power cycling ADC, and reprogramming FPGA...
ZDOK0 clock OK, ZDOK1 clock OK
Calibrating SERDES blocks...ABCDEFGH
SERDES calibration successful.
Selecting analog inputs...
Using default digital gain of 1...
Done!
Done#########
(env1) [observer@cylctrl rb_test]$
```

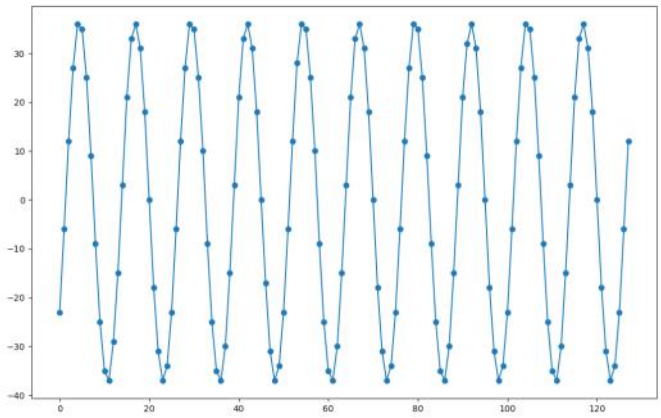


添上溢出啥啥的

```
Bitstream generation is complete.
================================================================
Flow run time summary: (00:59:45 seconds total)
    System update............00:00:24
    Design Rules Check.......00:00:05
    Xilinx System Generator..00:01:46
    Base system copy.........00:00:00
    IP creation..............00:00:00
    EDK files creation.......00:00:25
    IP elaboration...........00:00:00
    Software creation........00:00:00
    EDK/ISE backend..........00:57:01
================================================================
```

```
(env1) [observer@cylctrl bin]$ ruby adc16_status.rb roach8
roach8: Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
roach8: Gateware supports demux modes (currently using demux by 1)
roach8: ZDOK0 clock OK, ZDOK1 clock OK
roach8: AAAABBBBCCCCDDDDEEEEFFFFGGGGHHHH
roach8: 12341234123412341234123412341234
roach8: ................................ deskew
roach8: ................................ sync
(env1) [observer@cylctrl bin]$
```

```
(env1) [observer@cylctrl rb_test]$ ./6test.sh
Hellow,It is a nice day,isn't it?
Connecting to roach8...
Programming roach8 with roach2_6109.bof...
Design built for ROACH2 rev2 with 8 ADCs (ZDOK rev2)
Gateware supports demux modes (using demux by 1)
Resetting ADC, power cycling ADC, and reprogramming FPGA...
ZDOK0 clock OK, ZDOK1 clock OK
Calibrating SERDES blocks...ABCDEFGH
SERDES calibration successful.
Selecting analog inputs...
Using default digital gain of 1...
Done!
Done#########
(env1) [observer@cylctrl rb_test]$
```


30
20
10
0
−10
−20
−30
−40
0
20
40
60
80
100
120