VLSI System Design 2025 Fall

Homework 2

REPORT

Must do self-checking before submission:

◻ Compress all files described in the homework into one tar

◻ All Verilog/System Verilog files can be compiled in VCS

◻ All port declarations comply with I/O port specifications

◻ Organize files according to the File Hierarchy Requirement

◻ No waveform files in deliverables

Submission Due: 2025/10/27,15:00. (+8 GMT)

Please fill out this form!

|  |  |
| --- | --- |
| Simulation results (Pass/Fail) |  |
| Superlint coverage (%) |  |

Student name: \_\_\_\_\_\_\_\_\_\_\_

Student ID: \_\_\_\_\_\_\_\_\_\_

1. Design principles.

A.adder

|  |
| --- |
| Data path diagram: |
|  |
| Explain your design principles. |
|  |

B.comparator

|  |
| --- |
| Data path diagram: |
|  |
| Explain your design principles. |
|  |

C.FPU

|  |
| --- |
| Data path diagram: |
|  |
| Explain your design principles. |
|  |

1. Simulation results.(Provide ur terminal screenshot for every Prob)

|  |
| --- |
| Please provide screenshots of simulation results from the **terminal after fixing the code with Superlint**. |
|  |
| Explain your design behavior using waveforms from “**nWave**” waveform viewer tool. |
|  |

1. Superlint coverage.

|  |
| --- |
| Please provide screenshots of the Superlint Warnings/Errors after fixing. |
|  |
| Coverage definition: |
| warning lines:  total lines:  coverage percentage: |

1. Discussion of problems & solutions (optional).