CLCL-N_MB

Rev: 1.00
Date: 2018/11/20

CAD NOTE:
ALL FOOTPRINT OF SMD PARTS ARE 0402
IF THERE IS ANY DIFFERENT WHICH WILL BE SHOWN.

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016 CPU PCIE
017 CPU MISC
018 CPU POWER
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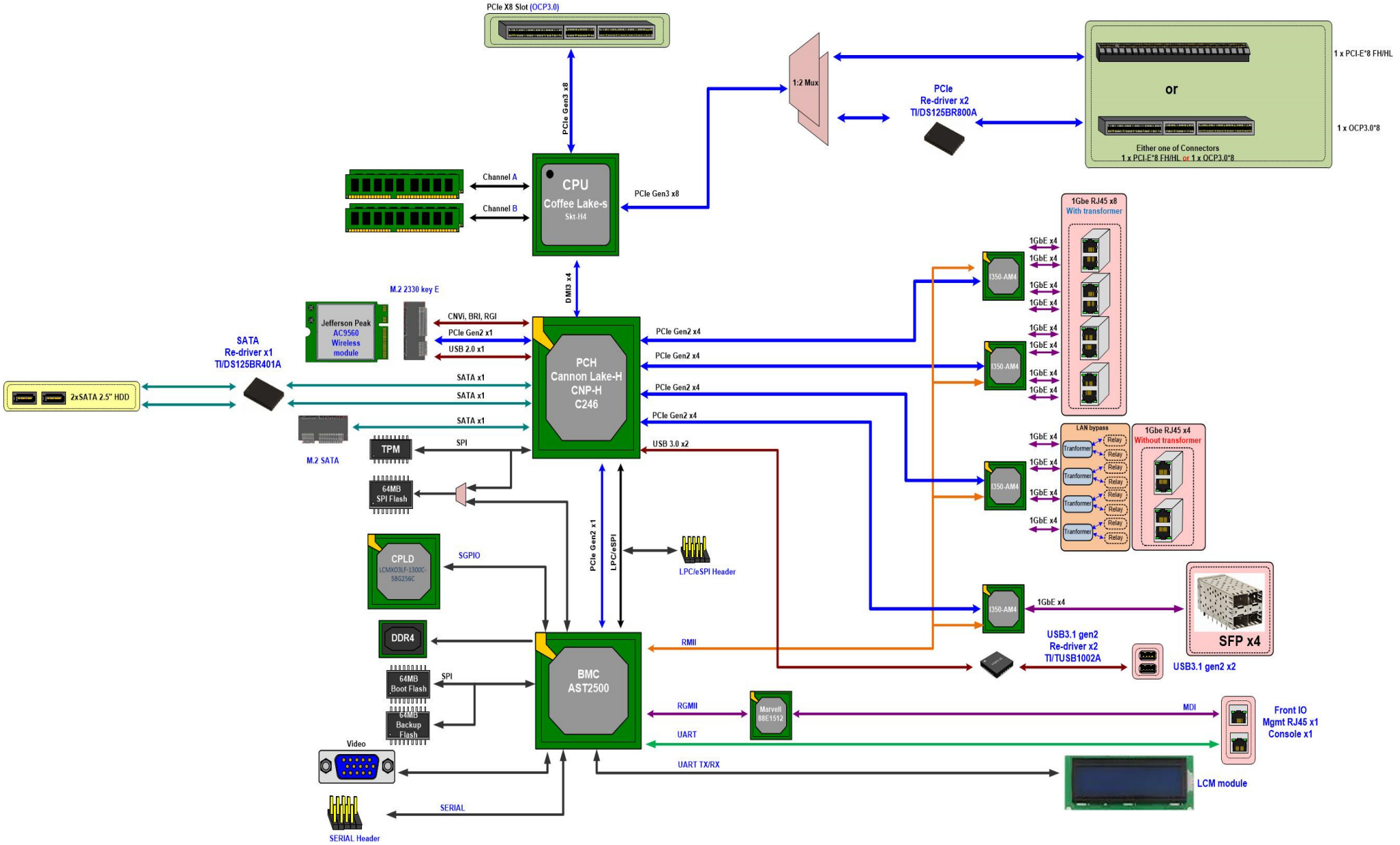
092 VCORE DRIVER 2-1
093 VCORE DRIVER 2-2
094 VCORE CAP
095 VCCGT DRIVER 1-1
096 VCCGT CAP
097 VCCSA
098 VCCIO
099 1P05V_PCH_DUAL
100 VDDQ & VTT
101 VPP
102 VCCST & 5V_RELAY
103 3P3V_DAUL
104 2P5V_DUAL
105 1P2V_DUAL
106 1P15V_DUAL
107 P1V8/3V3_PGPPA
108 P12V_P5V_DUAL
109.+1V_LAN
110. +1P8V_LAN
110. +1P8V_LAN

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 001 TATBLE OF CON
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 1 of 110



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 002 BLOCK DIAGRAM

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 2 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

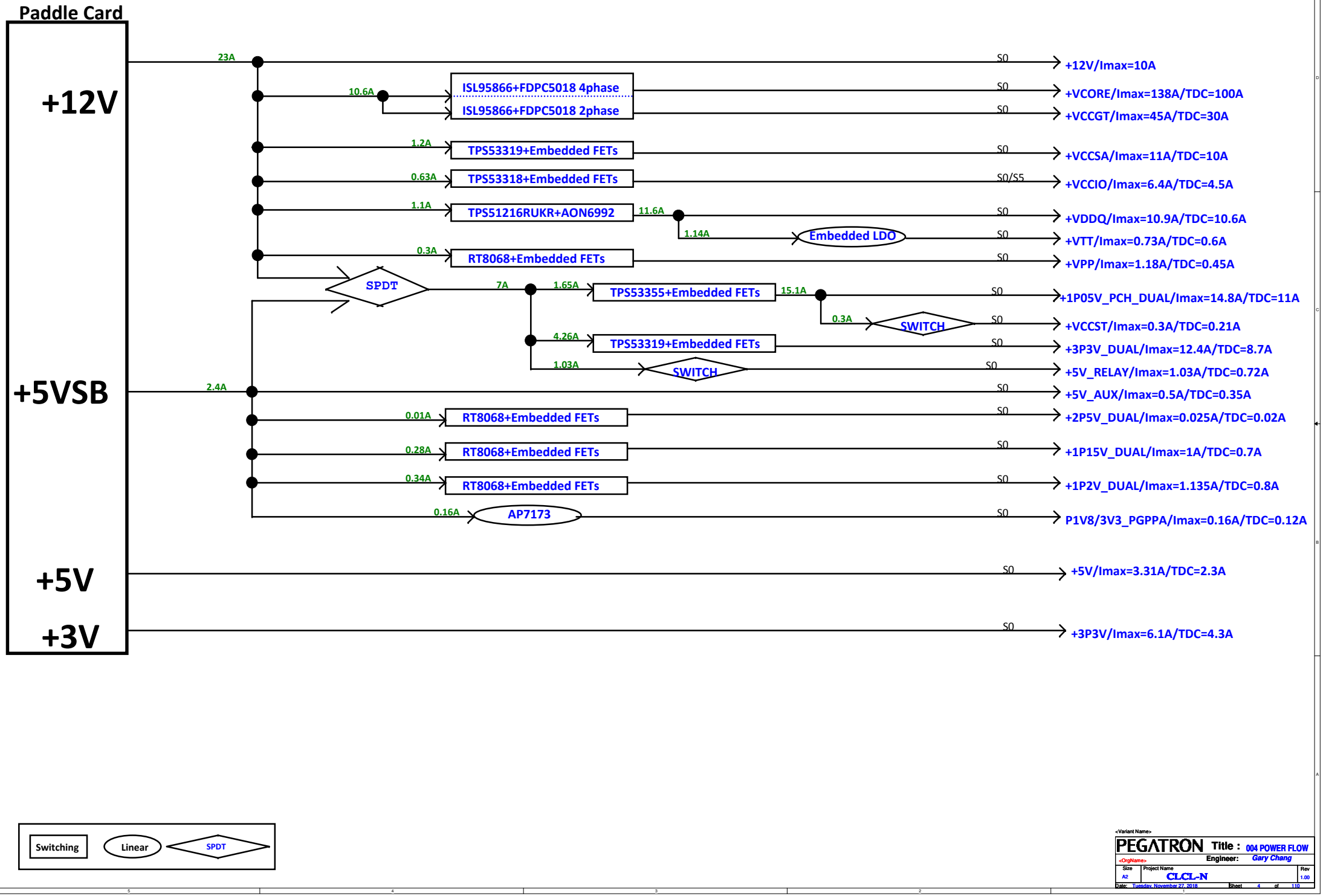
PEGATRON Title : 003 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 3 of 110

Mehlow/CLCL-N Power Flow



Switching | Linear | SPDT

<Variant Name>

PEGATRON Title : 004 POWER FLOW

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A2	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 4 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : 005 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 5 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : 006 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 6 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : 007 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 7 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : 008 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 8 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : 009 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 9 of 110

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 010 PAGE

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 10 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : 012 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 12 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

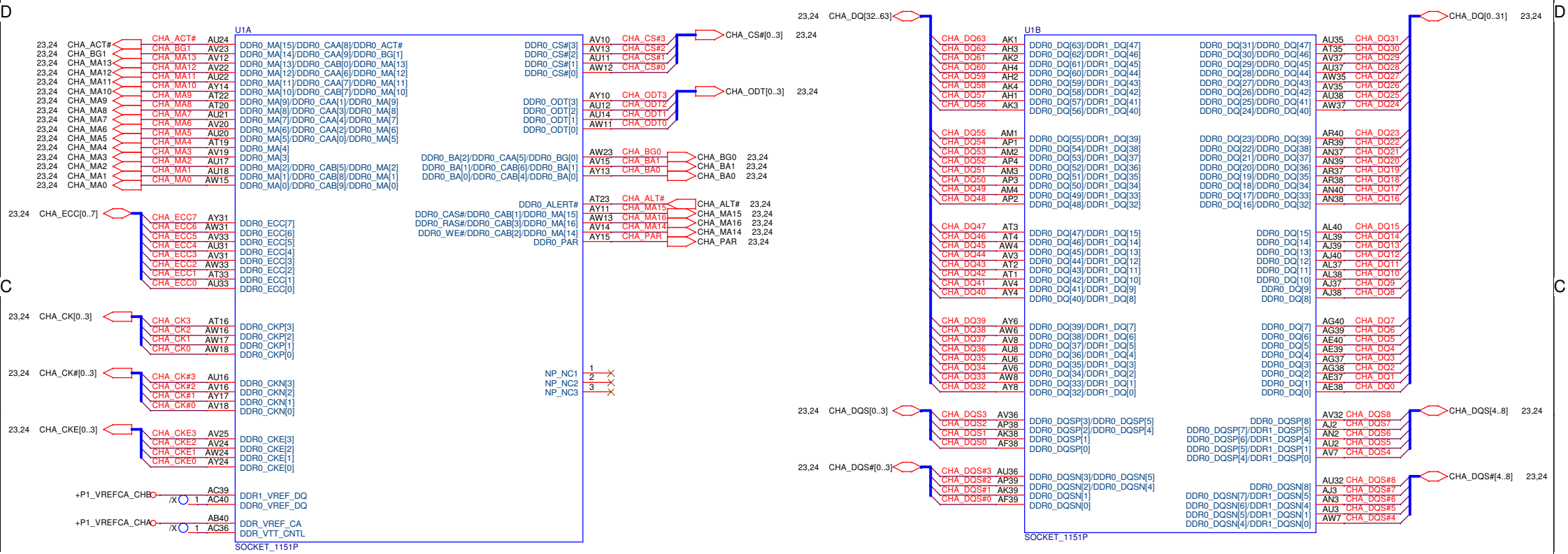
<Variant Name>

PEGATRON Title : 013 PAGE

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 13 of 110



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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

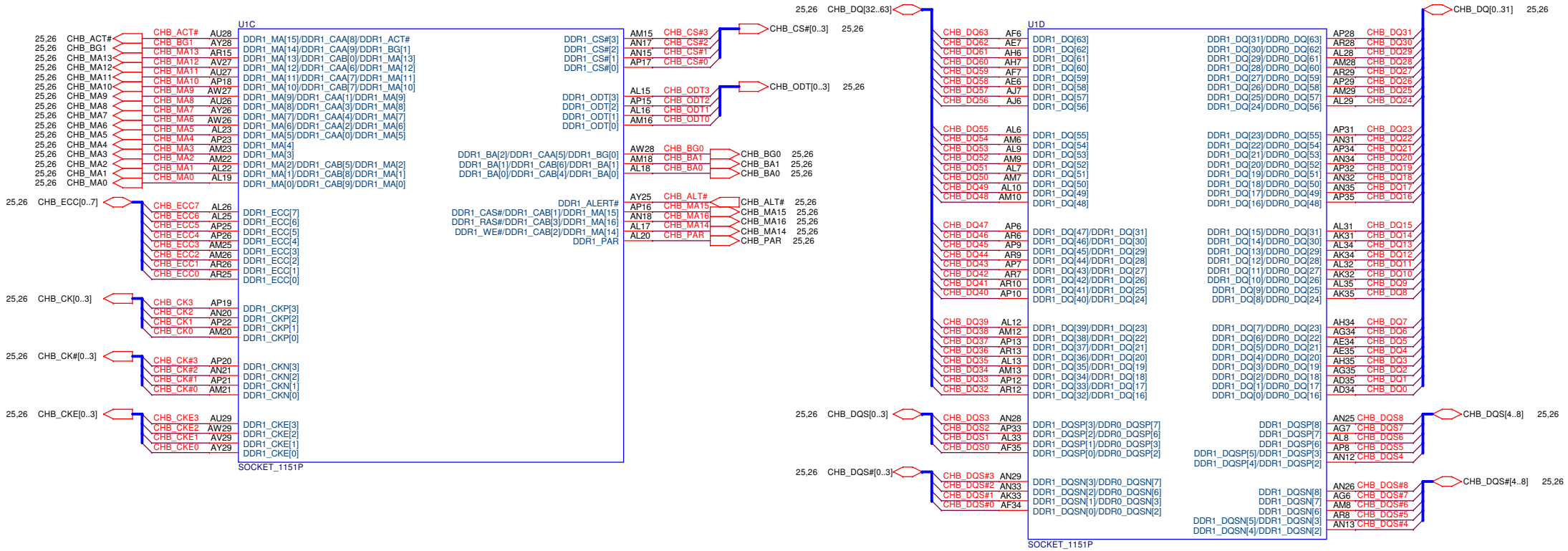
Title : 014 CPU CHA

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 14 of 110



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PEGATRON
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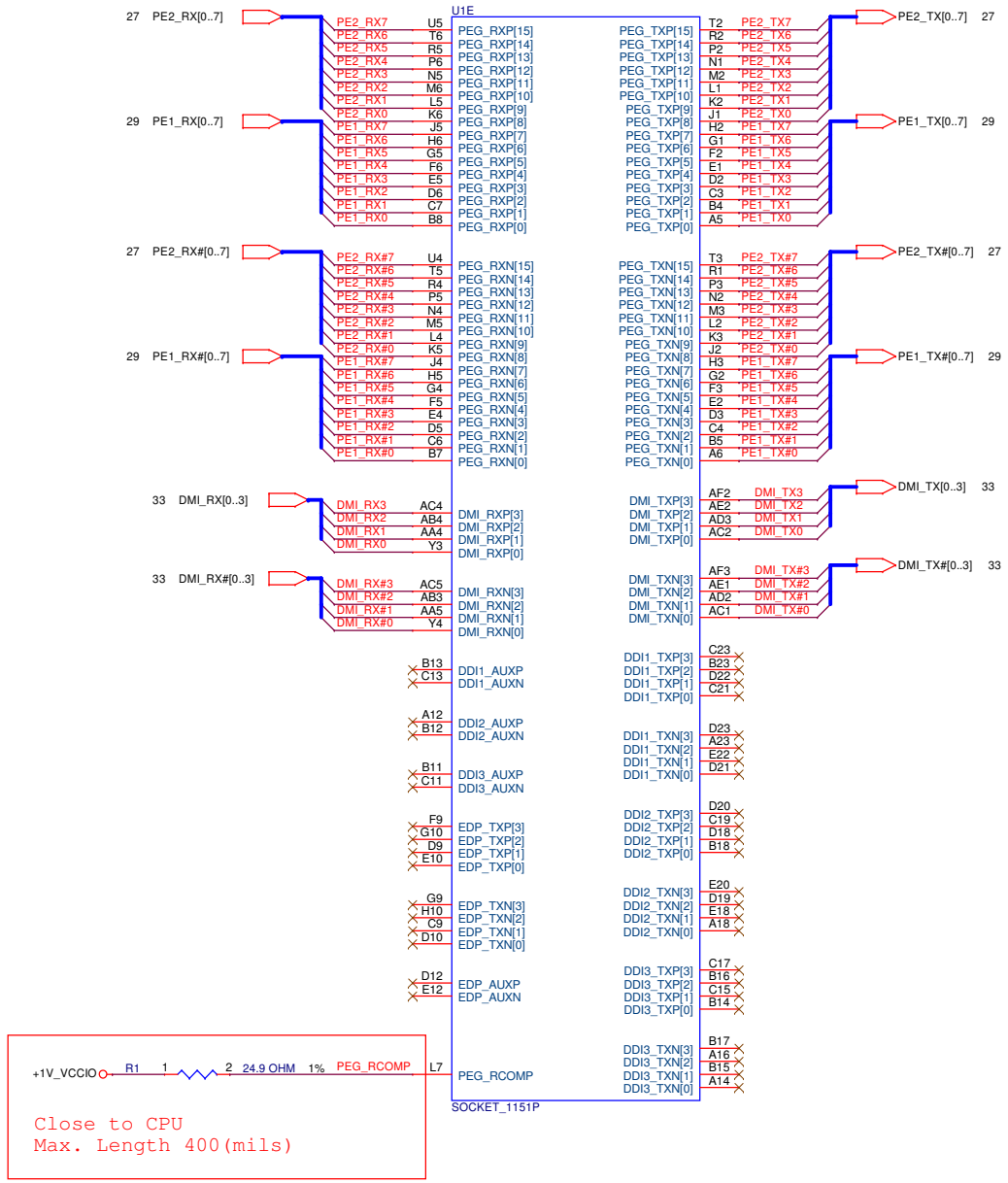
PEGATRON CORPORATION

Title : 015 CPU CHB
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 15 of 110



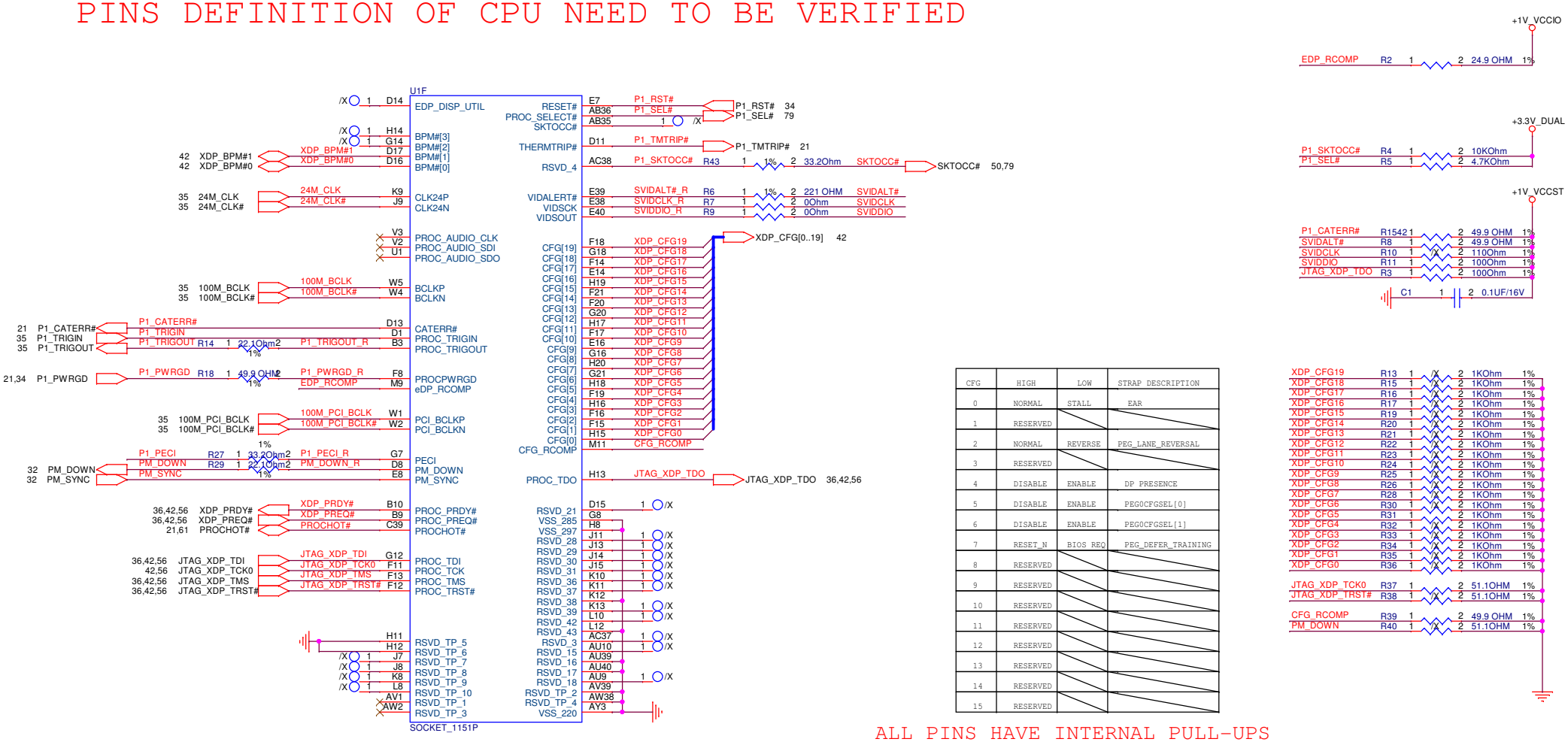
<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 016 CPU PCIE
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 16 of 110

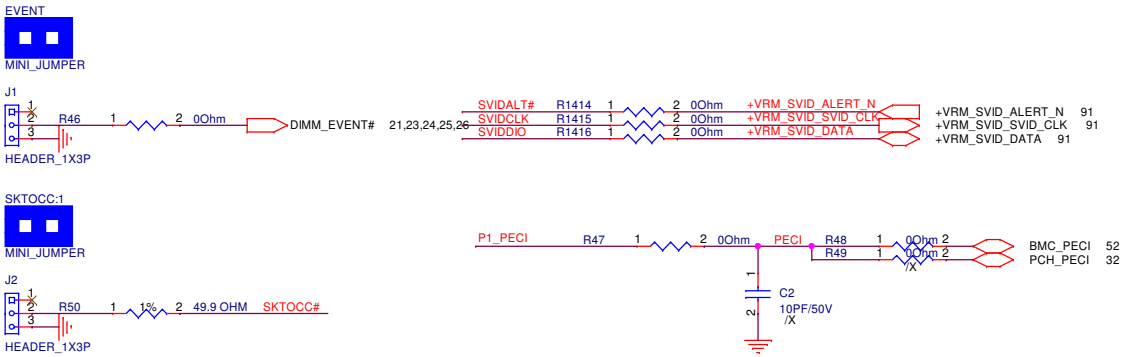
PINS DEFINITION OF CPU NEED TO BE VERIFIED



CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	RESERVED		
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	RESERVED		
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	RESERVED		
9	RESERVED		
10	RESERVED		
11	RESERVED		
12	RESERVED		
13	RESERVED		
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

CFG2	CFG6	CFG5	PCI-E CONFIG
0(REVERSE)	0	0	X8 X4 X4 (DEFUALT)
0(REVERSE)	0	1	RESERVED
1(NORMAL)	1	0	X8 X8
1(NORMAL)	1	1	X16

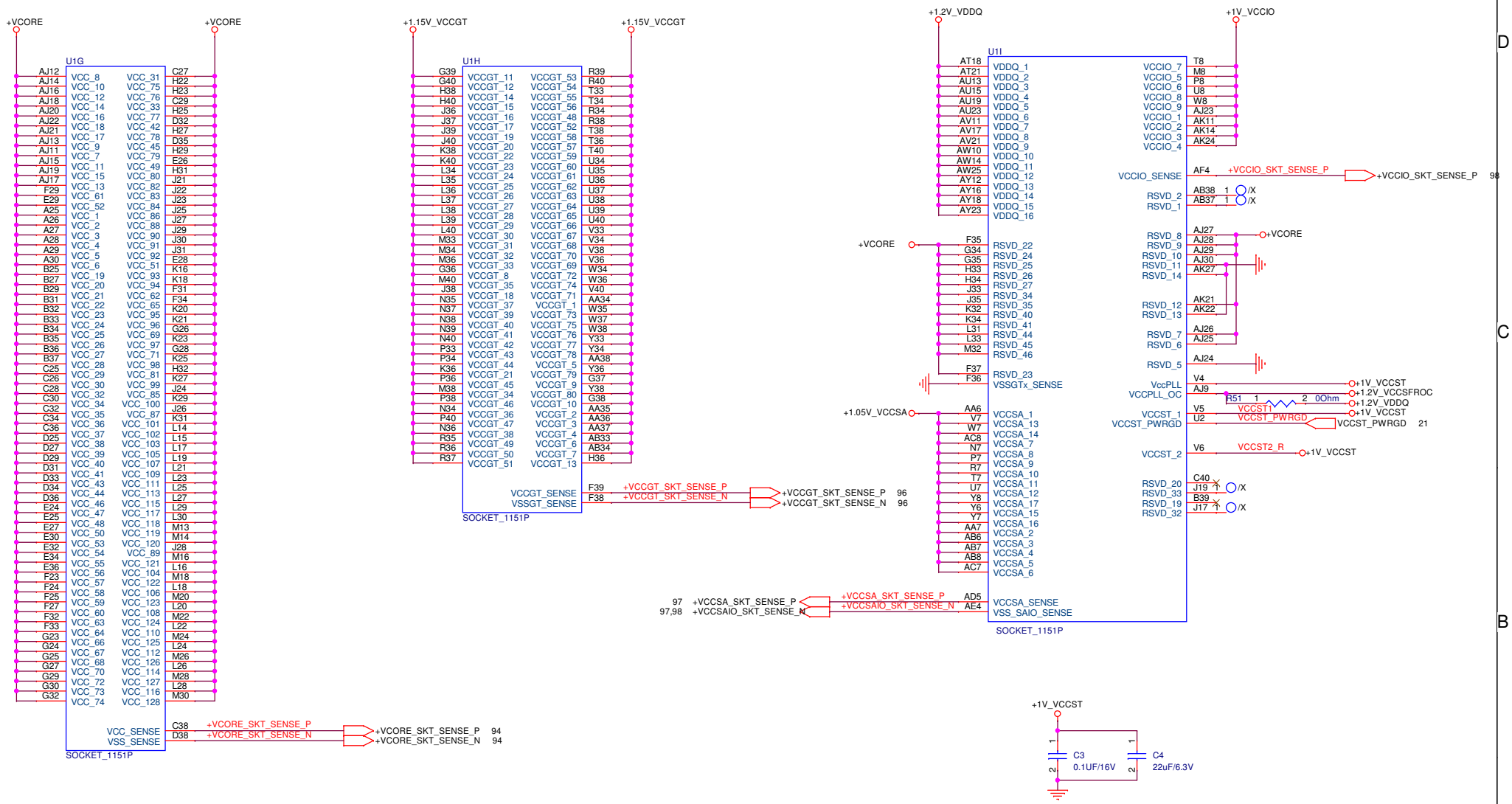


<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 017 CPU MISC
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 17 of 110



<Variant Name>

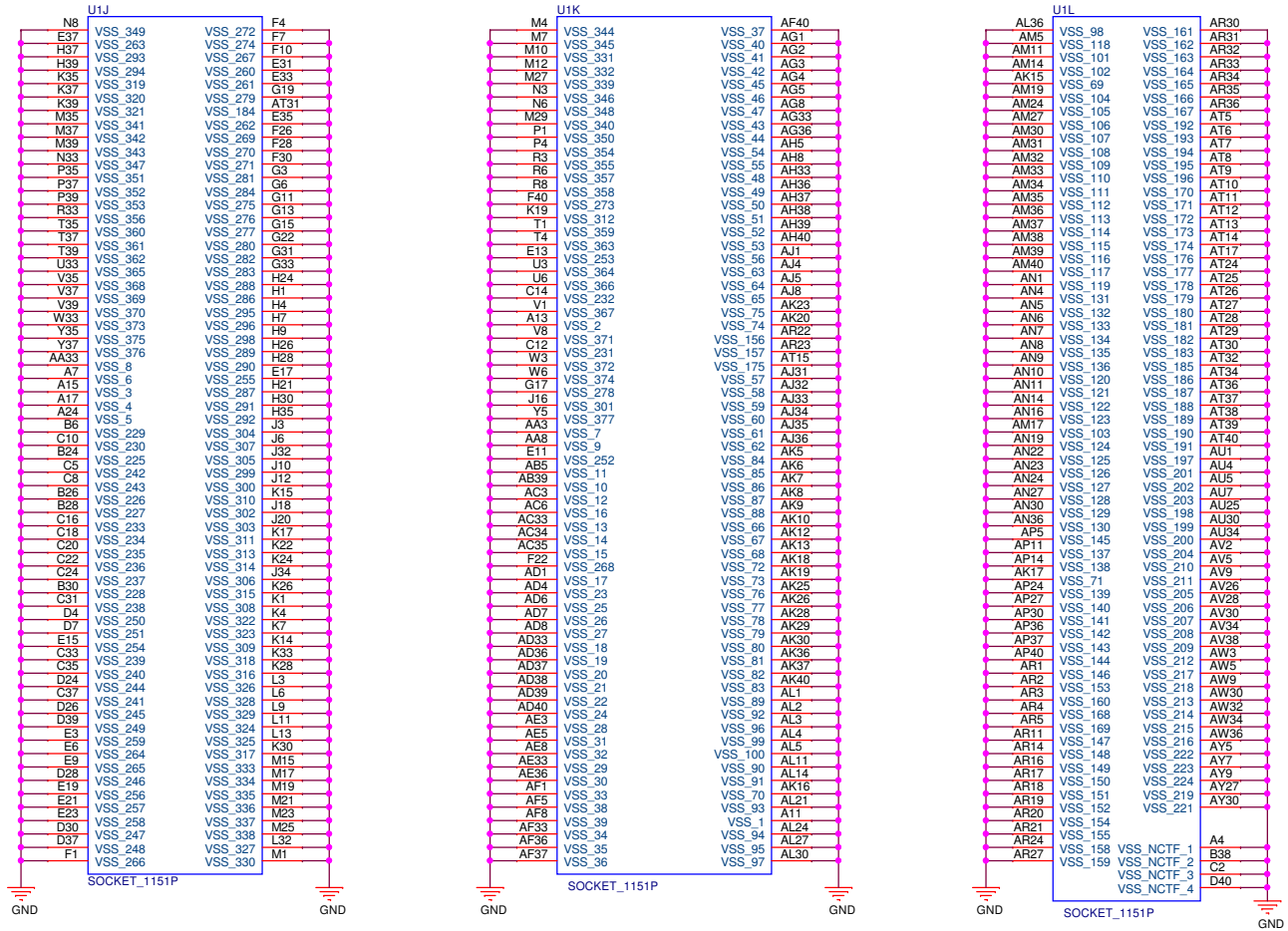
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 018 CPU POWER

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 18 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 019 CPU GND

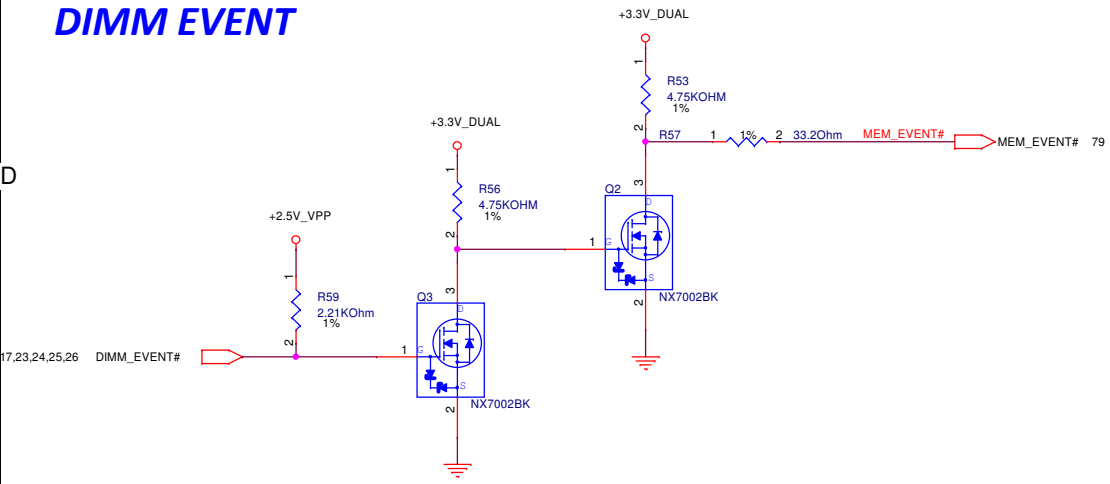
PEGATRON CORPORATION

Engineer: Ryan2_Wang

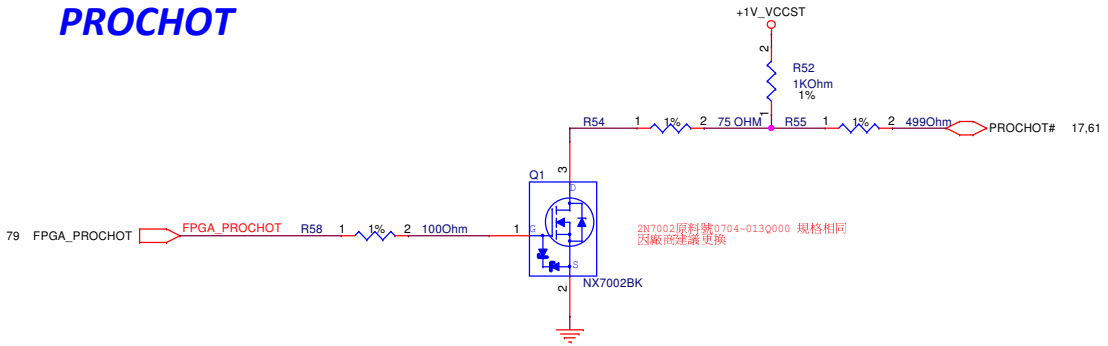
Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 19 of 110

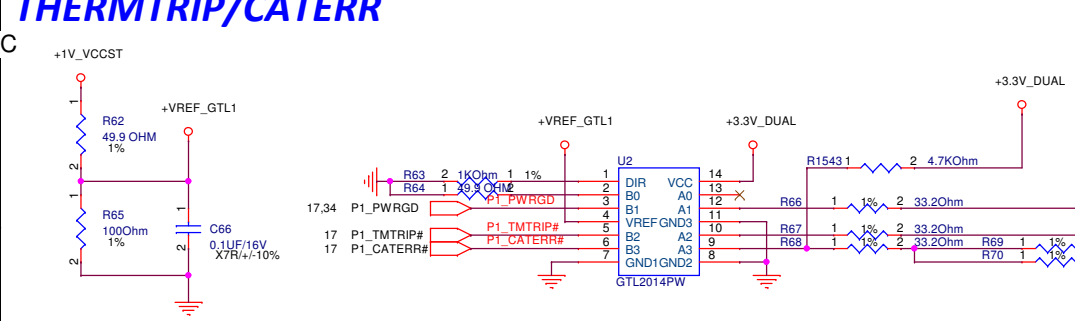
DIMM EVENT



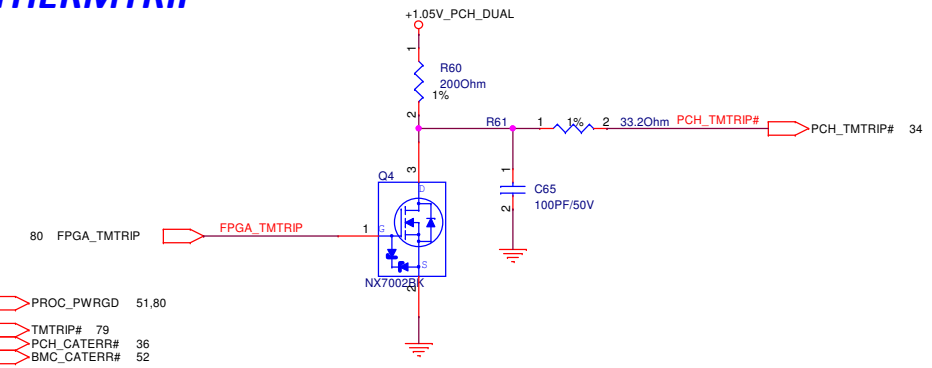
PROCHOT



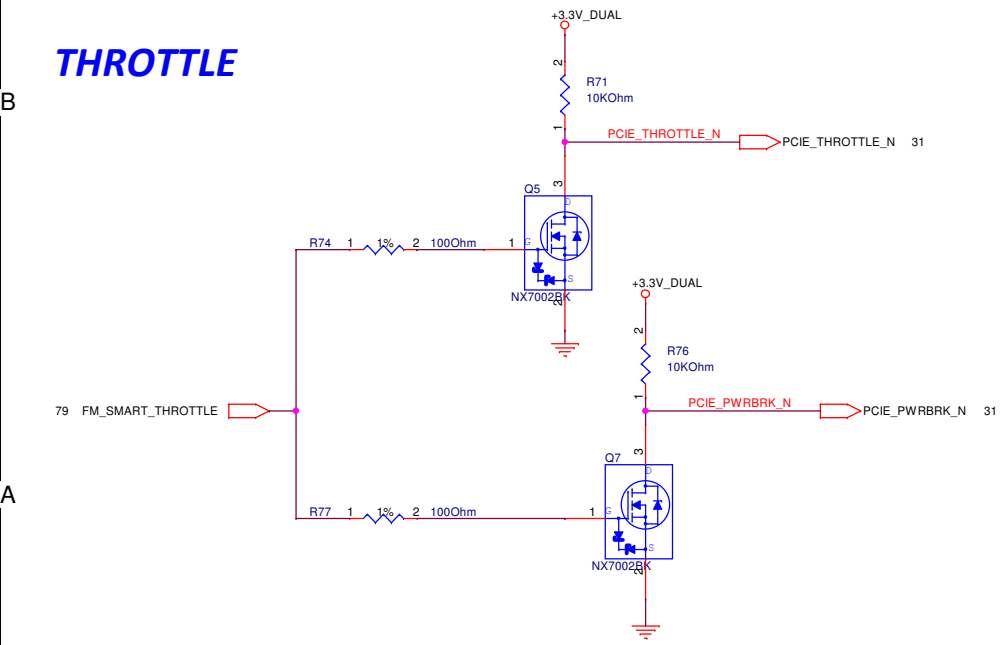
THERMTRIP/CATERR



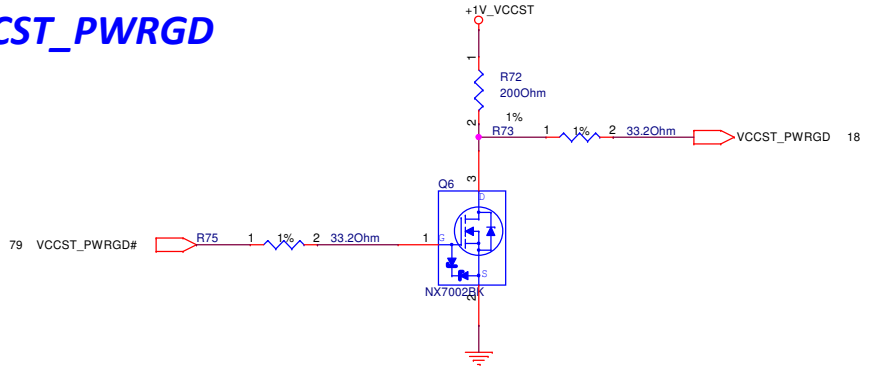
PCH THERMTRIP



THROTTLE



VCCST_PWRGD



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 021 CPU SIDE BAND

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 21 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON

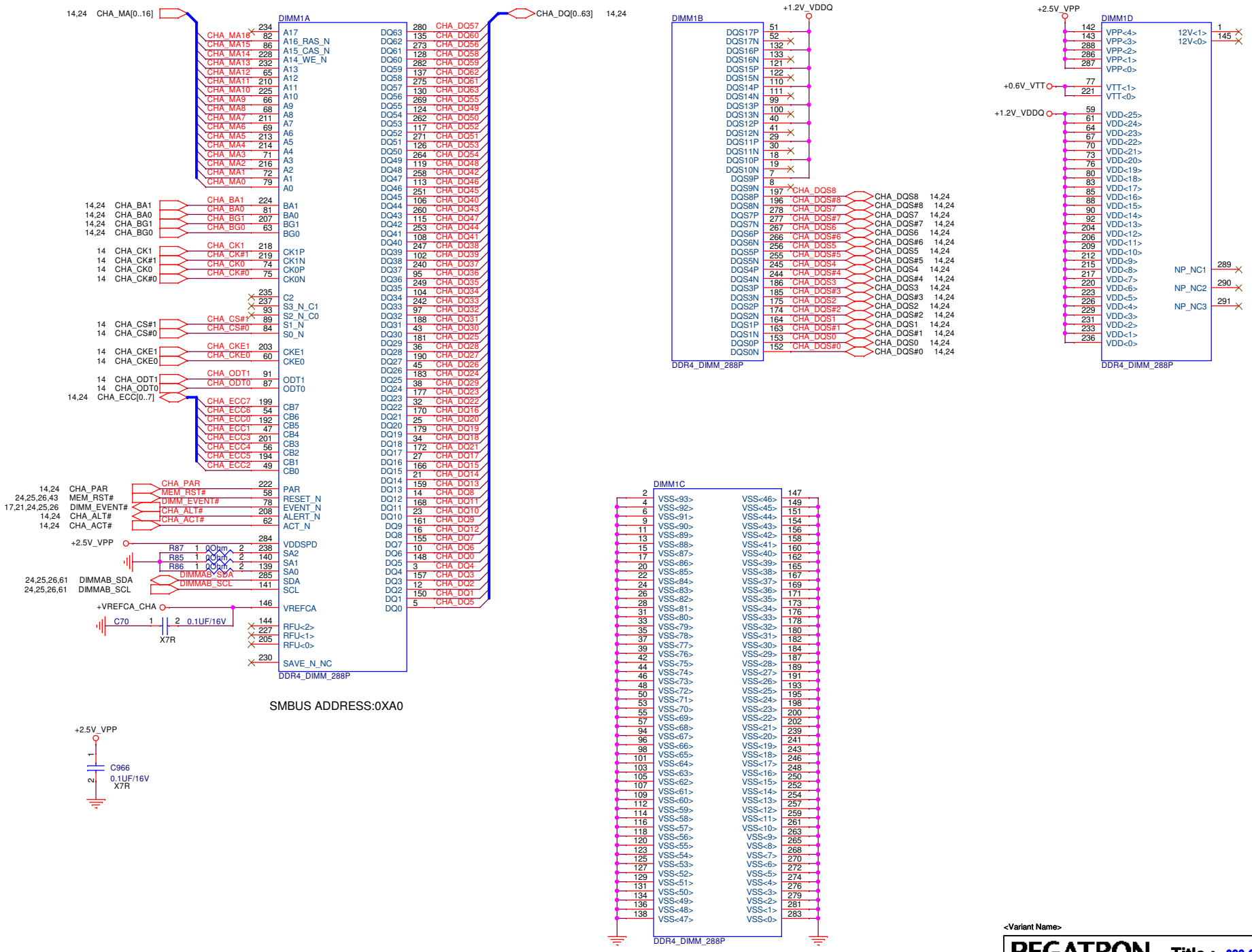
Title : 022 PAGE

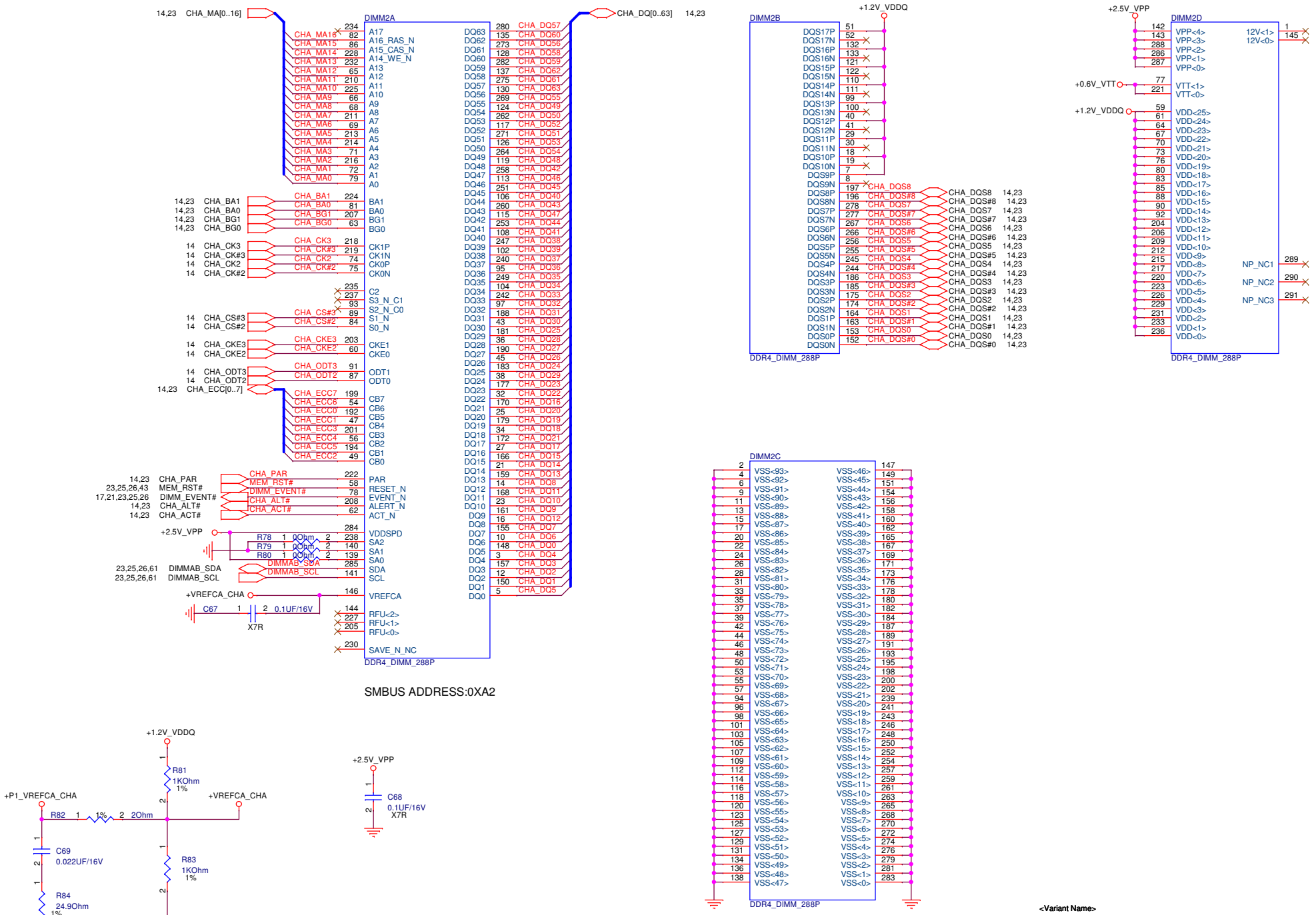
PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 22 of 110


DIMM1A
DDR4_DIMM_288P
CHA_MA[0..16]
CHA_DQ[0..63]
CHA_BA1
CHA_BA0
CHA_BG1
CHA_BG0
CHA_CK1
CHA_CK#1
CHA_CK0
CHA_CK#0
CHA_CS#1
CHA_CS#0
CHA_CKE1
CHA_CKE0
CHA_ODT1
CHA_ODT0
CHA_ECC[0..7]
CHA_PAR
MEM_RST#
DIMM_EVENT#
CHA_ALT#
CHA_ACT#
+2.5V_VPP
R87 1 0Ohm 2
R85 1 0Ohm 2
R86 1 0Ohm 2
DIMMAB_SDA
DIMMAB_SCL
+VREFCA_CHA
C70 0.1UF/16V
X7R
SMBUS ADDRESS:0XA0
C966
0.1UF/16V
X7R
DIMM1B
DDR4_DIMM_288P
+1.2V_VDDQ
CHA_DQS8
DIMM1C
DDR4_DIMM_288P
DIMM1D
DDR4_DIMM_288P
+2.5V_VPP
+0.6V_VTT
+1.2V_VDDQ
NP_NC1
NP_NC2
NP_NC3



<variant_name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

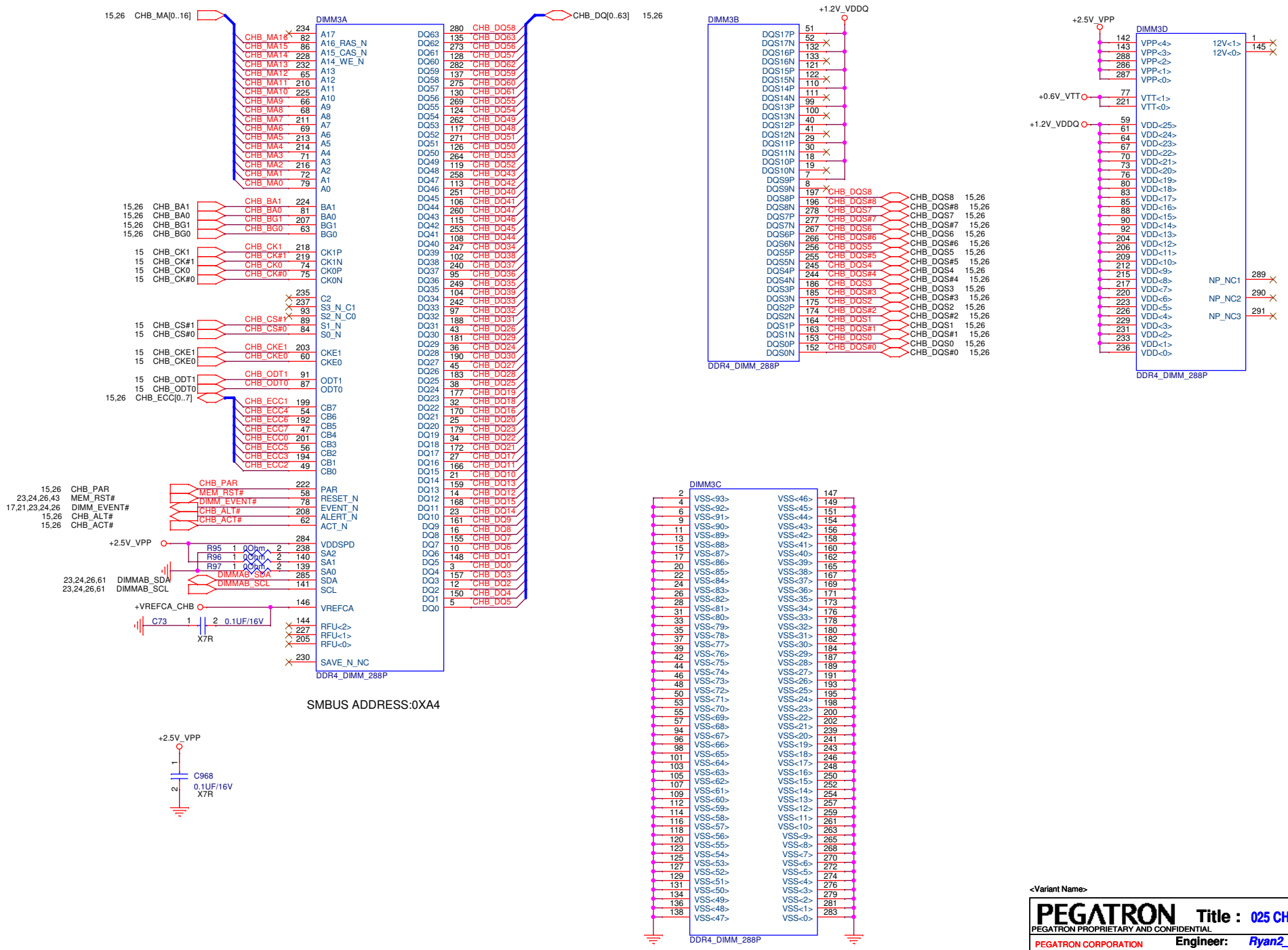
Title : 024 CHA DIMMA1

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 24 of 110



SMBUS ADDRESS:0XA4

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

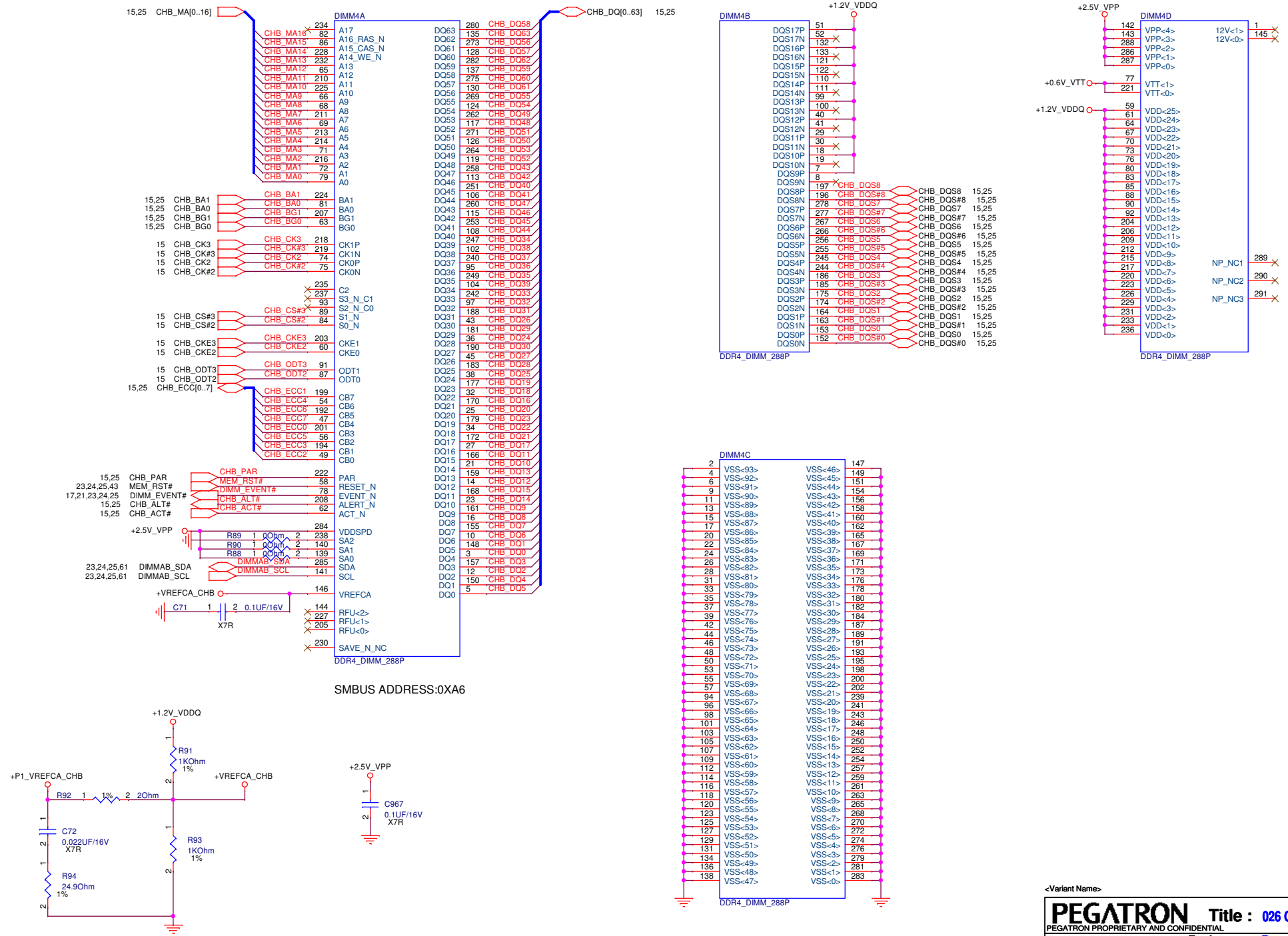
PEGATRON CORPORATION

Title : 025 CHB DIMMB0

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 25 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

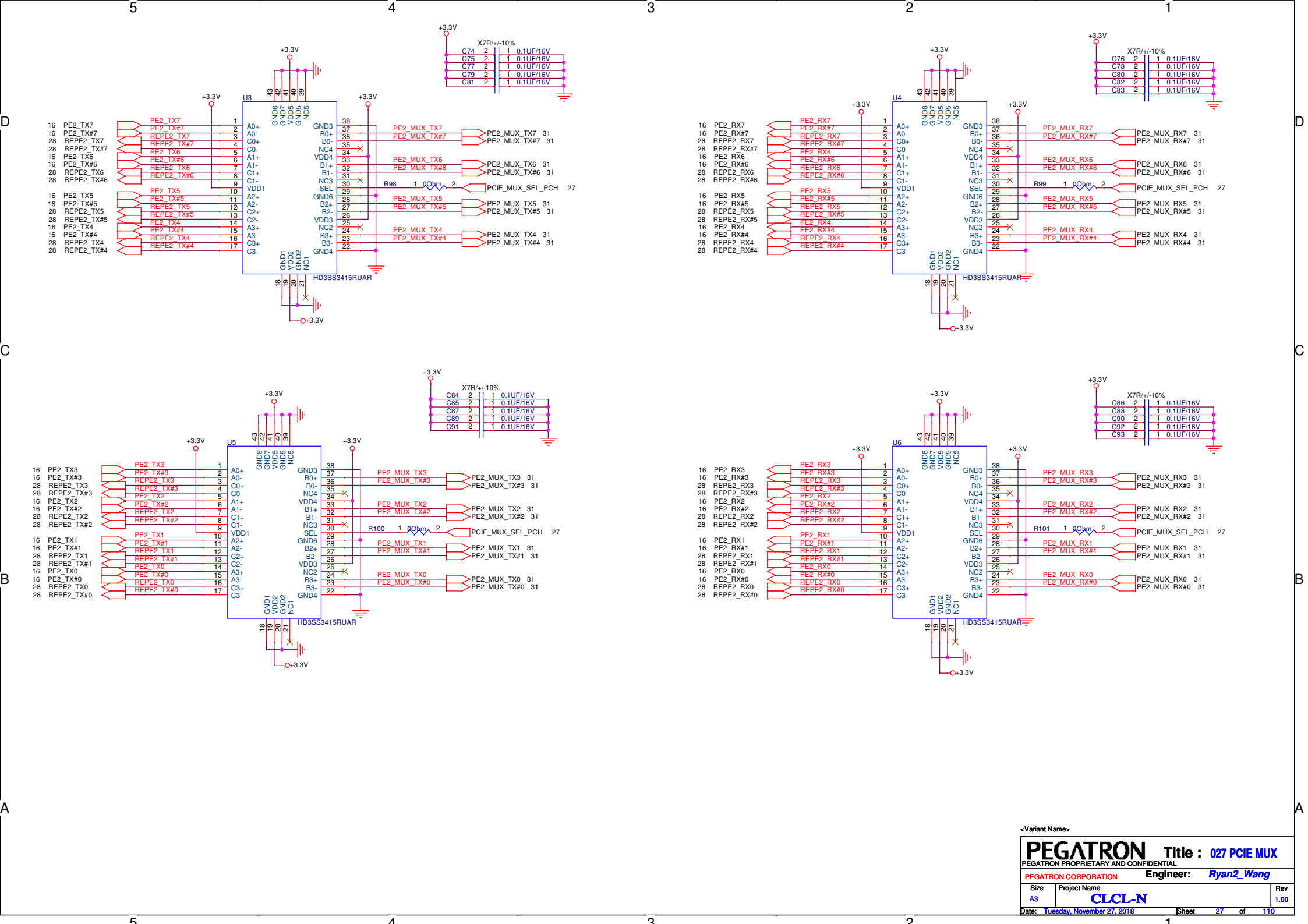
Title : 026 CHB DIMMB1

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 26 of 110



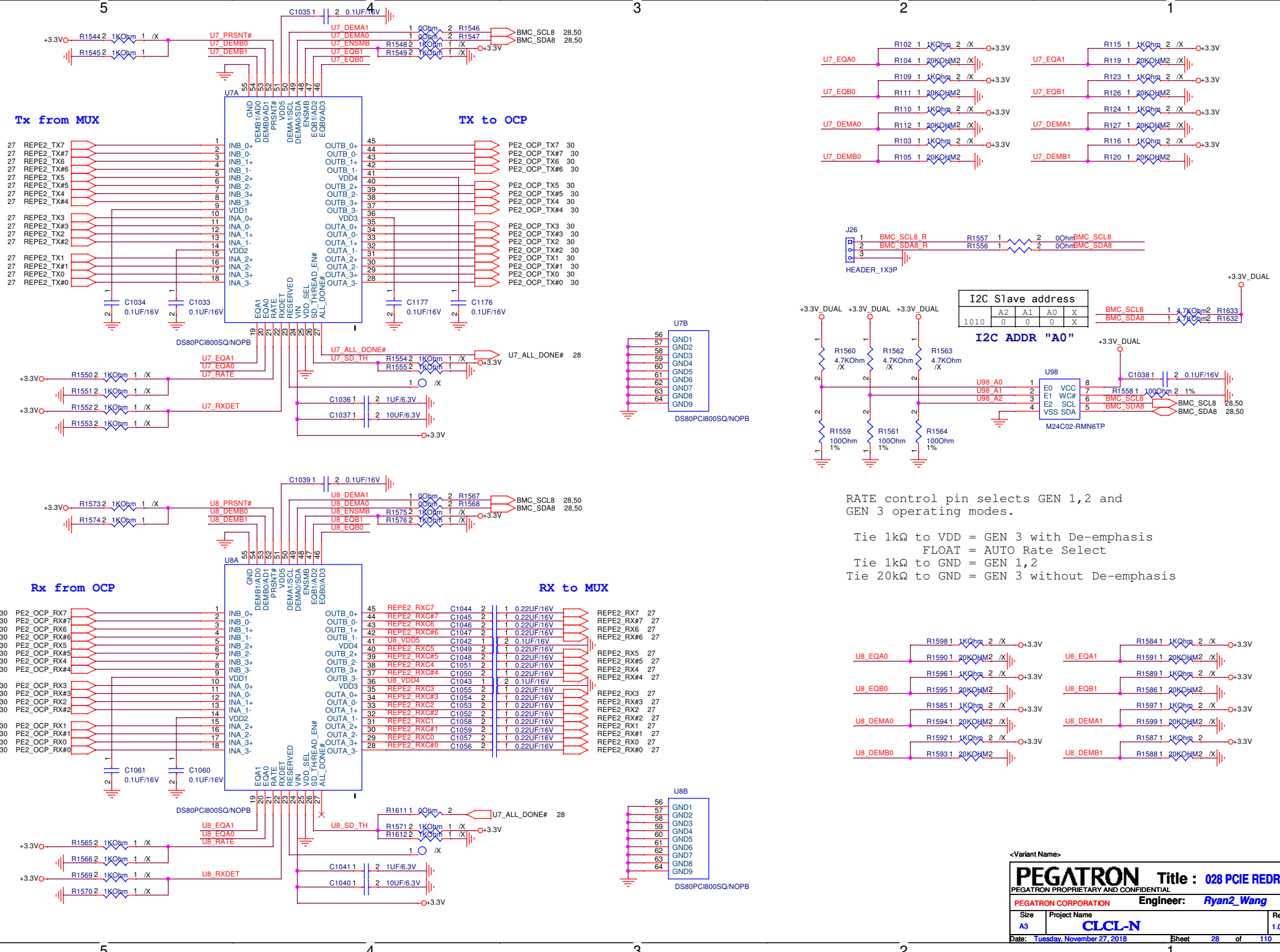
<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

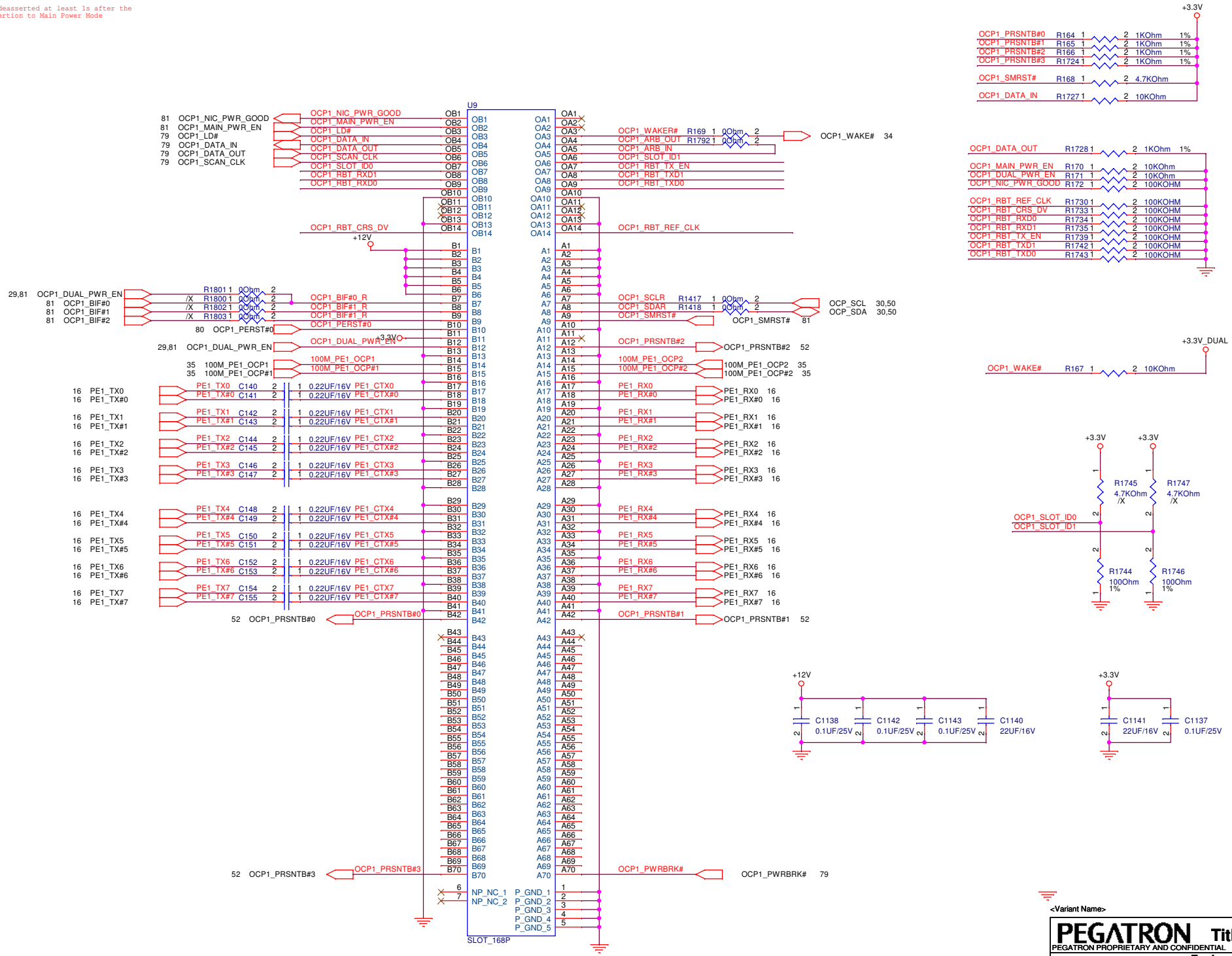
Title : 027 PCIE MUX
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 27 of 110


Tx from MUX
TX to OCP
U7A
DS80PCI800SQ/NOPB
U7B
DS80PCI800SQ/NOPB
Rx from OCP
RX to MUX
U8A
DS80PCI800SQ/NOPB
U8B
DS80PCI800SQ/NOPB
J26
HEADER_1X3P
I2C Slave address
I2C ADDR "A0"
M24C02-RMN6TP
RATE control pin selects GEN 1,2 and
GEN 3 operating modes.
Tie 1kΩ to VDD = GEN 3 with De-emphasis
FLOAT = AUTO Rate Select
Tie 1kΩ to GND = GEN 1,2
Tie 20kΩ to GND = GEN 3 without De-emphasis
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 028 PCIE REDRIVER
PEGATRON CORPORATION
Engineer: Ryan2_Wang
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 28 of 110

PERST# shall be deasserted at least 1s after the NIC_PWR_GOOD assertion to Main Power Mode

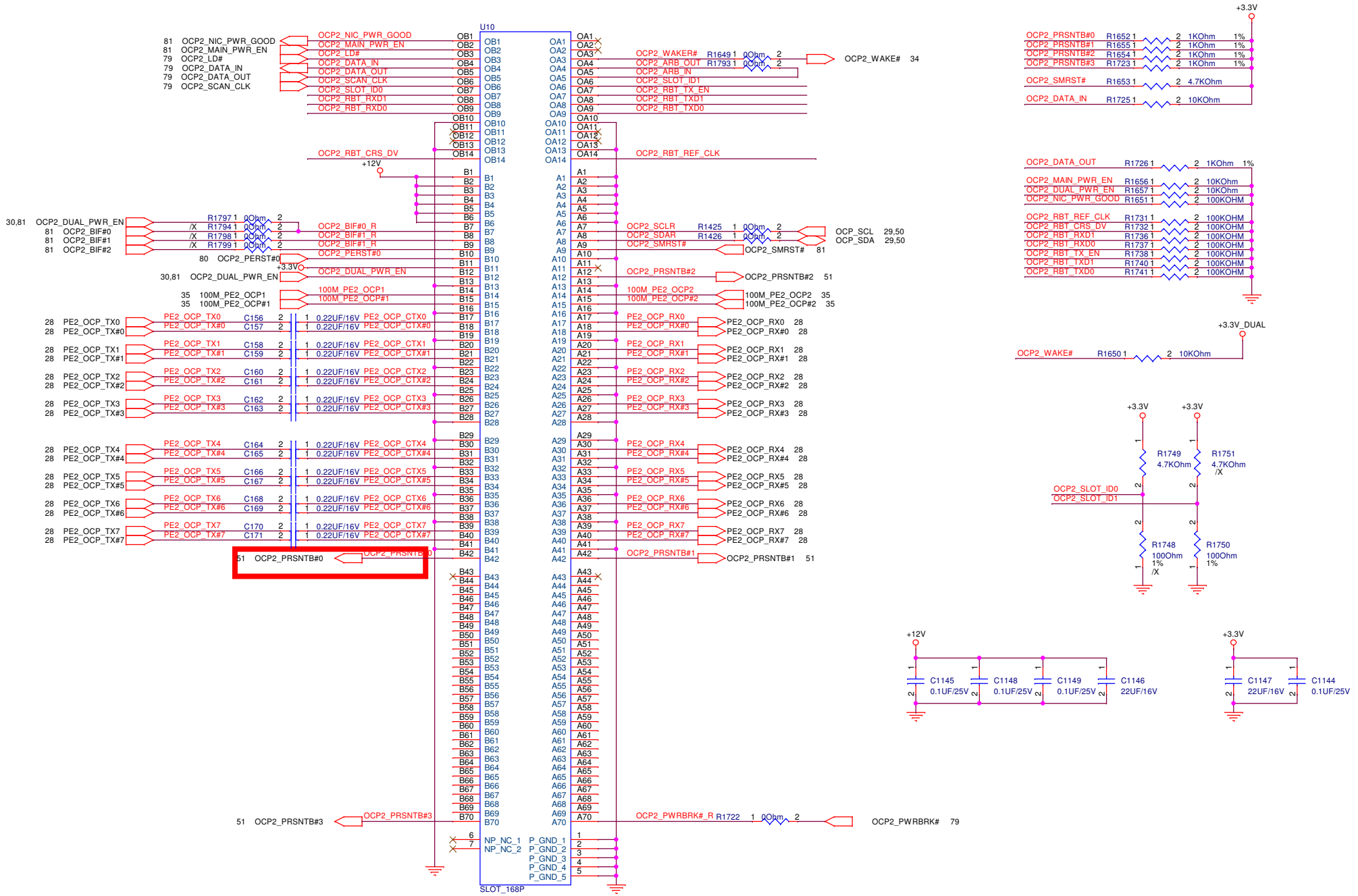


<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 029 PCIE1 X8 OCP 3.
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 29 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

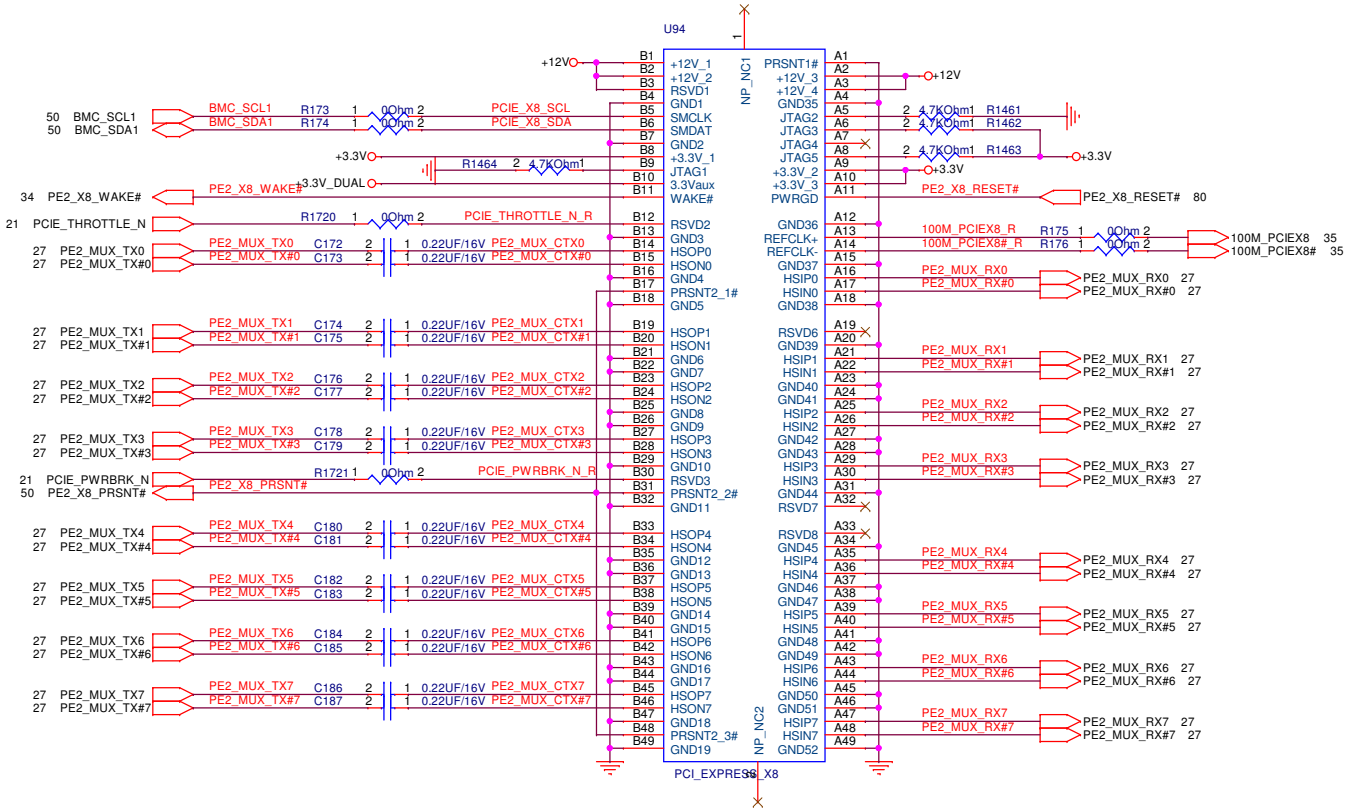
Title : 030 PCIE2 X8 MUX O

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 30 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 031 PCIE2 X8 MUX SI

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 31 of 110

PCH1F

LPC/ESPI

SD

SPI0

HOST

ISH_GP

958988

BOOT HALT

BOOT HALT ENABLED WHEN LOW
DISABLE WHEN HIGH (DEFAULT)

PERSONALITY STRAP (DFX)

0: PERSONALITY STRAP ENABLE WHEN LOW
1: PERSONALITY STRAP DISABLE WHEN HIGH (DEFAULT)

CONSENT STRAP (DFX)

0: CONSENT STRAP ENABLE WHEN LOW
1: CONSENT STRAP DISABLE WHEN HIGH (DEFAULT)

SLOT 7 LINK WIDTH

0: SLOT7 1X2, 2X1 DEFAULT
1: SLOT7 1X4

NOTE:R212,R213,R214,R215,R220 should close to BMC

BOARD REV

	ID1	ID0
BBFV	0	0
SDV	0	1
SIT	1	0
SVT	1	1

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 032 PCH SPI/ESPI
PEGATRON CORPORATION
Engineer: Tom_Liao
Size: A3
Project Name: CLCL-N
Rev: 1.00
Date: Tuesday, November 27, 2018
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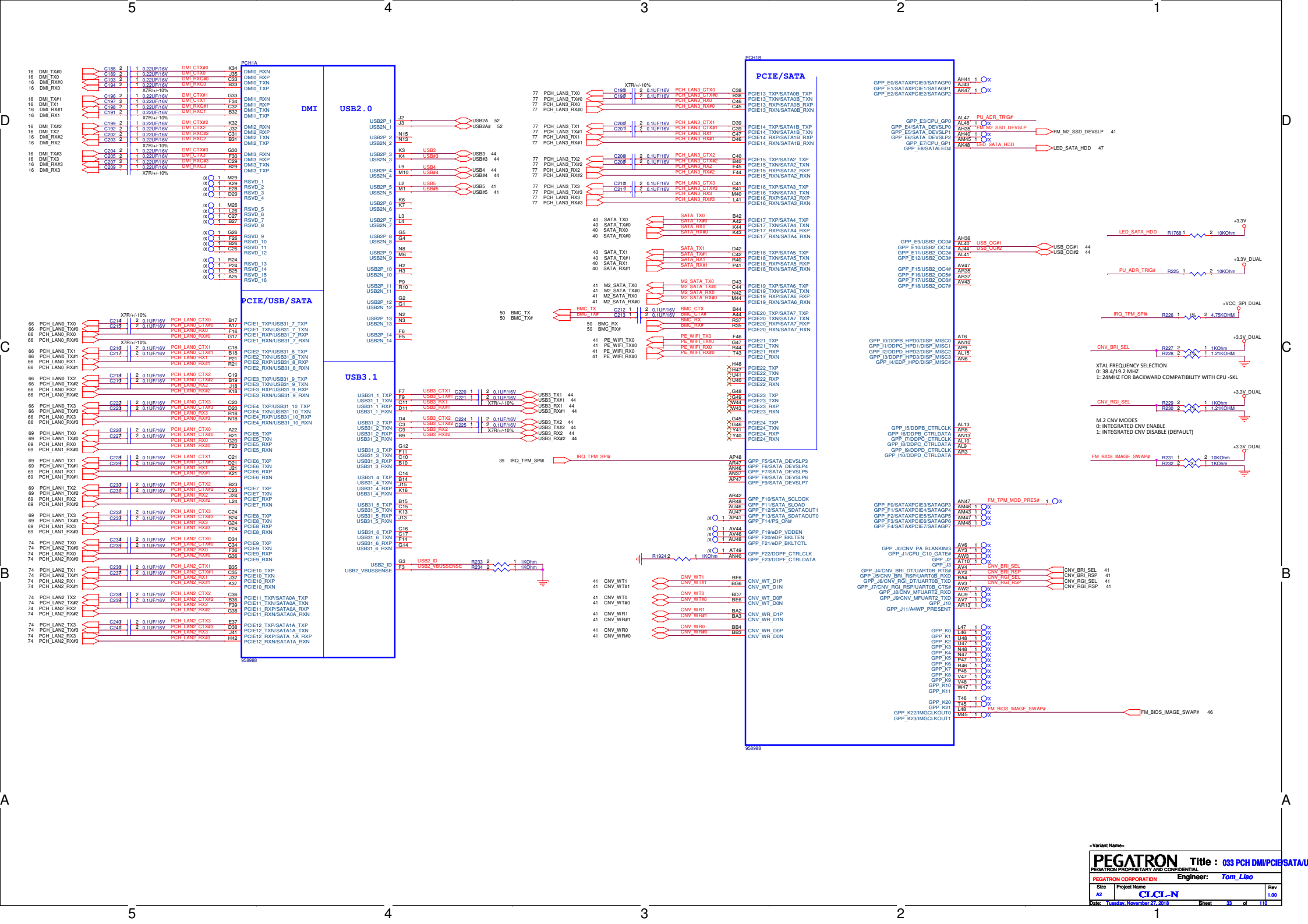
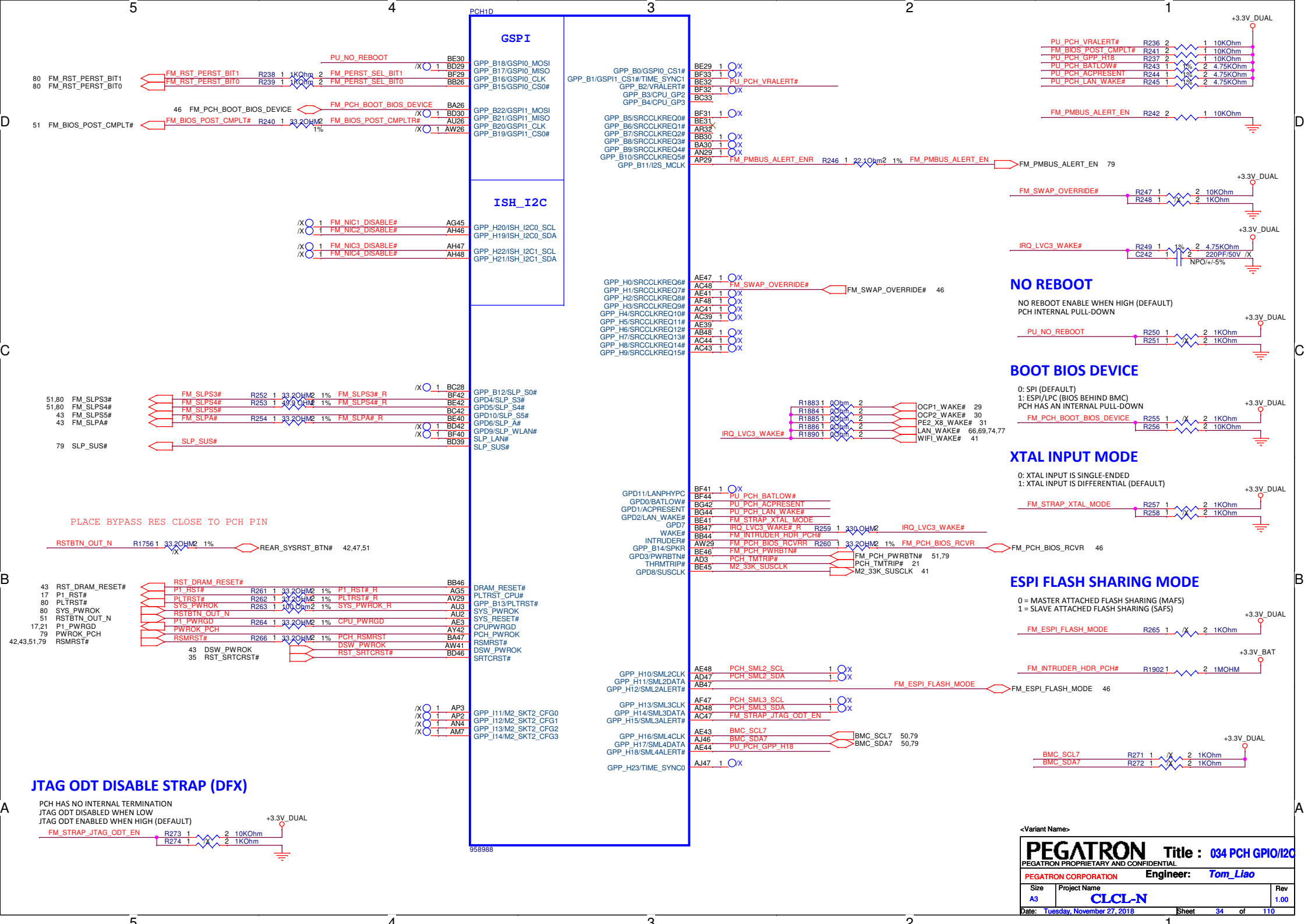
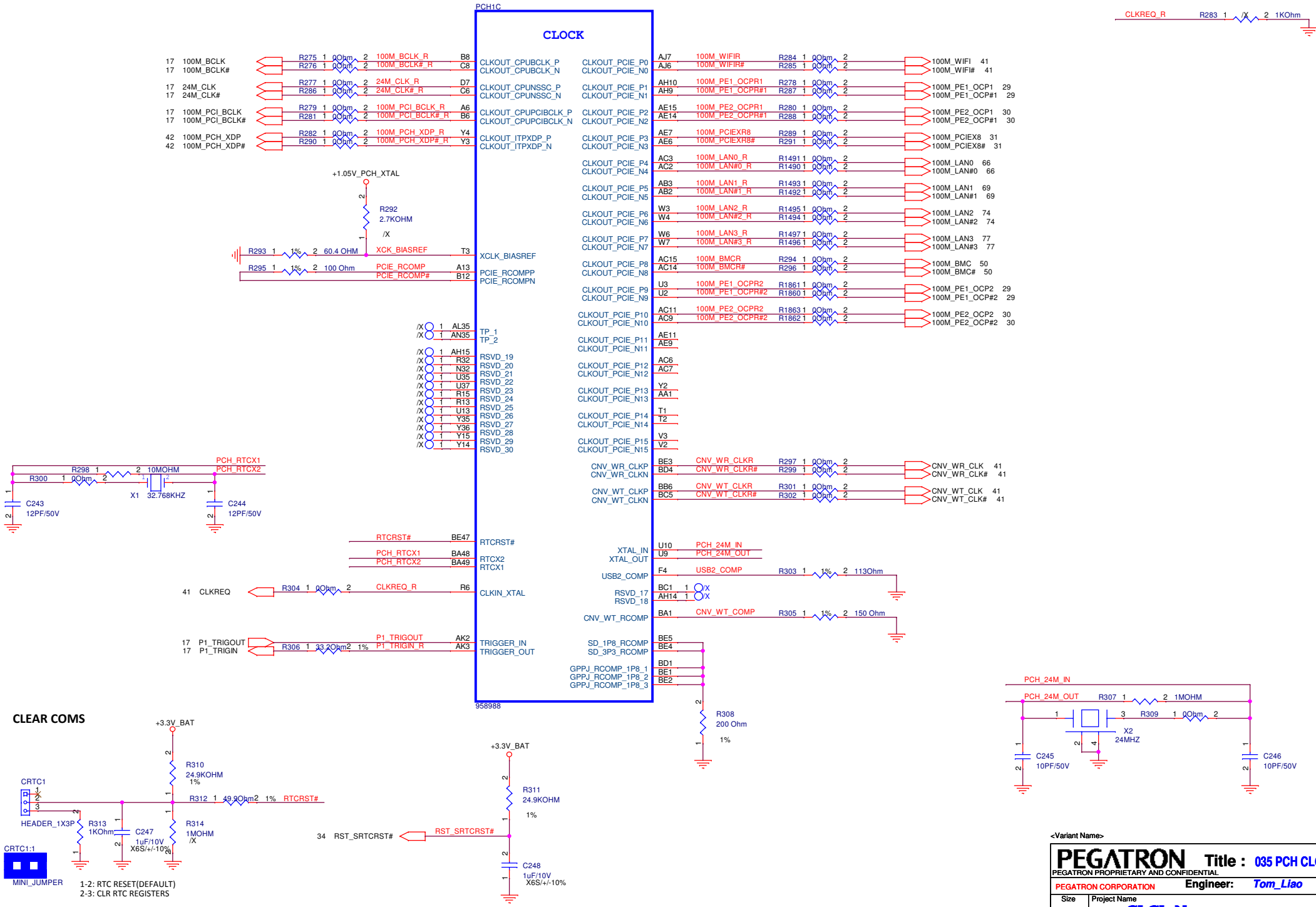

PCH1A
DMI
USB2.0
USB3.1
PCIE/USB/SATA
PCH1B
PCIE/SATA
DMI_CTX#0
DMI_CTX0
DMI_RXC#0
DMI_RXC0
DMI_CTX#1
DMI_CTX1
DMI_RXC#1
DMI_RXC1
DMI_CTX#2
DMI_CTX2
DMI_RXC#2
DMI_RXC2
DMI_CTX#3
DMI_CTX3
DMI_RXC#3
DMI_RXC3
DMI0_RXN
DMI0_RXP
DMI0_TXN
DMI0_TXP
DMI1_RXN
DMI1_RXP
DMI1_TXN
DMI1_TXP
DMI2_RXN
DMI2_RXP
DMI2_TXN
DMI2_TXP
DMI3_RXN
DMI3_RXP
DMI3_TXN
DMI3_TXP
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
USB2P_1
USB2N_1
USB2P_2
USB2N_2
USB2P_3
USB2N_3
USB2P_4
USB2N_4
USB2P_5
USB2N_5
USB2P_6
USB2N_6
USB2P_7
USB2N_7
USB2P_8
USB2N_8
USB2P_9
USB2N_9
USB2P_10
USB2N_10
USB2P_11
USB2N_11
USB2P_12
USB2N_12
USB2P_13
USB2N_13
USB2P_14
USB2N_14
USB3_CTX1
USB3_CTX1#
USB3_RX1
USB3_HX#1
USB3_CTX2
USB3_CTX2#
USB3_RX2
USB3_HX#2
USB2_ID
USB2_VBUSSENSE
PCIE1_TXP/USB31_7_TXP
PCIE1_TXN/USB31_7_TXN
PCIE1_RXP/USB31_7_RXP
PCIE1_RXN/USB31_7_RXN
PCIE2_TXP/USB31_8_TXP
PCIE2_TXN/USB31_8_TXN
PCIE2_RXP/USB31_8_RXP
PCIE2_RXN/USB31_8_RXN
PCIE3_TXP/USB31_9_TXP
PCIE3_TXN/USB31_9_TXN
PCIE3_RXP/USB31_9_RXP
PCIE3_RXN/USB31_9_RXN
PCIE4_TXP/USB31_10_TXP
PCIE4_TXN/USB31_10_TXN
PCIE4_RXP/USB31_10_RXP
PCIE4_RXN/USB31_10_RXN
PCIE5_TXP
PCIE5_TXN
PCIE5_RXP
PCIE5_RXN
PCIE6_TXP
PCIE6_TXN
PCIE6_RXP
PCIE6_RXN
PCIE7_TXP
PCIE7_TXN
PCIE7_RXP
PCIE7_RXN
PCIE8_TXP
PCIE8_TXN
PCIE8_RXP
PCIE8_RXN
PCIE9_TXP
PCIE9_TXN
PCIE9_RXP
PCIE9_RXN
PCIE10_TXP
PCIE10_TXN
PCIE10_RXP
PCIE10_RXN
PCIE11_TXP/SATA0A_TXP
PCIE11_TXN/SATA0A_TXN
PCIE11_RXP/SATA0A_RXP
PCIE11_RXN/SATA0A_RXN
PCIE12_TXP/SATA1A_TXP
PCIE12_TXN/SATA1A_TXN
PCIE12_RXP/SATA_1A_RXP
PCIE12_RXN/SATA1A_RXN
PCIE13_TXP/SATA0B_TXP
PCIE13_TXN/SATA0B_TXN
PCIE13_RXP/SATA0B_RXP
PCIE13_RXN/SATA0B_RXN
PCIE14_TXP/SATA1B_TXP
PCIE14_TXN/SATA1B_TXN
PCIE14_RXP/SATA1B_RXP
PCIE14_RXN/SATA1B_RXN
PCIE15_TXP/SATA2_TXP
PCIE15_TXN/SATA2_TXN
PCIE15_RXP/SATA2_RXP
PCIE15_RXN/SATA2_RXN
PCIE16_TXP/SATA3_TXP
PCIE16_TXN/SATA3_TXN
PCIE16_RXP/SATA3_RXP
PCIE16_RXN/SATA3_RXN
PCIE17_TXP/SATA4_TXP
PCIE17_TXN/SATA4_TXN
PCIE17_RXP/SATA4_RXP
PCIE17_RXN/SATA4_RXN
PCIE18_TXP/SATA5_TXP
PCIE18_TXN/SATA5_TXN
PCIE18_RXP/SATA5_RXP
PCIE18_RXN/SATA5_RXN
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN
PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE21_TXP
PCIE21_TXN
PCIE21_RXP
PCIE21_RXN
PCIE22_TXP
PCIE22_TXN
PCIE22_RXP
PCIE22_RXN
PCIE23_TXP
PCIE23_TXN
PCIE23_RXP
PCIE23_RXN
PCIE24_TXP
PCIE24_TXN
PCIE24_RXP
PCIE24_RXN
CNV_WT1
CNV_WT1#
CNV_WT0
CNV_WT#0
CNV_WR1
CNV_WR#1
CNV_WR0
CNV_WR#0
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_D0P
CNV_WT_D0N
CNV_WR_D1P
CNV_WR_D1N
CNV_WR_D0P
CNV_WR_D0N
SATA_TX0
SATA_TX#0
SATA_RX0
SATA_RX#0
SATA_TX1
SATA_TX#1
SATA_RX1
SATA_RX#1
M2_SATA_TX0
M2_SATA_TX#0
M2_SATA_RX0
M2_SATA_RX#0
BMC_TX
BMC_TX#
BMC_RX
BMC_RX#
PE_WIFI_TX0
PE_WIFI_TX#0
PE_WIFI_RX0
PE_WIFI_RX#0
IRQ_TPM_SPI#
GPP_F5/SATA_DEVSLP3
GPP_F6/SATA_DEVSLP4
GPP_F7/SATA_DEVSLP5
GPP_F8/SATA_DEVSLP6
GPP_F9/SATA_DEVSLP7
GPP_F10/SATA_SCLOCK
GPP_F11/SATA_SLOAD
GPP_F12/SATA_SDATAOUT1
GPP_F13/SATA_SDATAOUT0
GPP_F14/PS_ON#
GPP_F19/eDP_VDDEN
GPP_F20/eDP_BKLTEN
GPP_F21/eDP_BKLTCTL
GPP_F22/DDPF_CTRLCLK
GPP_F23/DDPF_CTRLDATA
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E3/CPU_GP0
GPP_E4/SATA_DEVSLP0
GPP_E5/SATA_DEVSLP1
GPP_E6/SATA_DEVSLP2
GPP_E7/CPU_GP1
GPP_E8/SATALED#
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_F15/USB2_OC4#
GPP_F16/USB2_OC5#
GPP_F17/USB2_OC6#
GPP_F18/USB2_OC7#
GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DDPD_HPD2/DISP_MISC2
GPP_I3/DDPF_HPD3/DISP_MISC3
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F0/SATAXPCIE3/SATAGP3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7
GPP_J0/CNV_PA_BLANKING
GPP_J1/CPU_C10_GATE#
GPP_J2
GPP_J3
GPP_J4/CNV_BRI_DT/UART0B_RTS#
GPP_J5/CNV_BRI_RSP/UART0B_RXD
GPP_J6/CNV_RGI_DT/UART0B_TXD
GPP_J7/CNV_RGI_RSP/UART0B_CTS#
GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD
GPP_J10
GPP_J11/A4WP_PRESENT
GPP_K0
GPP_K1
GPP_K2
GPP_K3
GPP_K4
GPP_K5
GPP_K6
GPP_K7
GPP_K8
GPP_K9
GPP_K10
GPP_K11
GPP_K20
GPP_K21
GPP_K22/IMGCLKOUT0
GPP_K23/IMGCLKOUT1
PU_ADR_TRIG#
FM_M2_SSD_DEVSLP
LED_SATA_HDD
USB_OC#1
USB_OC#2
FM_TPM_MOD_PRES#
CNV_BRI_SEL
CNV_BRI_RSP
CNV_RGI_SEL
CNV_RGI_RSP
FM_BIOS_IMAGE_SWAP#
XTAL FREQUENCY SELECTION
0: 38.4/19.2 MHZ
1: 24MHZ FOR BACKWARD COMPATIBILITY WITH CPU -SKL
M.2 CNV MODES
0: INTEGRATED CNV ENABLE
1: INTEGRATED CNV DISABLE (DEFAULT)
+3.3V
+3.3V_DUAL
+VCC_SPI_DUAL
10KOhm
4.75KOHM
1KOhm
1.21KOHM
X7R/+/-10%
0.22UF/16V
0.1UF/16V
958988


PCH1D
GSPI
ISH_I2C
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD6/SLP_A#
GPD9/SLP_WLAN#
SLP_LAN#
SLP_SUS#
DRAM_RESET#
PLTRST_CPU#
GPP_B13/PLTRST#
SYS_PWROK
SYS_RESET#
CPUPWRGD
PCH_PWROK
RSMRST#
DSW_PWROK
SRTCRST#
GPP_I11/M2_SKT2_CFG0
GPP_I12/M2_SKT2_CFG1
GPP_I13/M2_SKT2_CFG2
GPP_I14/M2_SKT2_CFG3
958988
GPP_B0/GSPI0_CS1#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B2/VRALERT#
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_B11/I2S_MCLK
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
GPD11/LANPHYPC
GPD0/BATLOW#
GPD1/ACPRESENT
GPD2/LAN_WAKE#
GPD7
WAKE#
INTRUDER#
GPP_B14/SPKR
GPD3/PWRBTN#
THRMTRIP#
GPD8/SUSCLK
GPP_H10/SML2CLK
GPP_H11/SML2DATA
GPP_H12/SML2ALERT#
GPP_H13/SML3CLK
GPP_H14/SML3DATA
GPP_H15/SML3ALERT#
GPP_H16/SML4CLK
GPP_H17/SML4DATA
GPP_H18/SML4ALERT#
GPP_H23/TIME_SYNC0
+3.3V_DUAL
+3.3V_BAT
PU_PCH_VRALERT# R236 10KOhm
FM_BIOS_POST_CMPLT# R241 10KOhm
PU_PCH_GPP_H18 R237 10KOhm
PU_PCH_BATLOW# R243 4.75KOhm
PU_PCH_ACPRESENT R244 4.75KOhm
PU_PCH_LAN_WAKE# R245 4.75KOhm
FM_PMBUS_ALERT_EN R242 10KOhm
FM_PMBUS_ALERT_ENR R246 22.1Ohm
FM_PMBUS_ALERT_EN
FM_SWAP_OVERRIDE# R247 10KOhm R248 1KOhm
IRQ_LVC3_WAKE# R249 4.75KOhm C242 220PF/50V NPO/+/-5%
NO REBOOT
NO REBOOT ENABLE WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-DOWN
PU_NO_REBOOT R250 1KOhm R251 1KOhm
BOOT BIOS DEVICE
0: SPI (DEFAULT)
1: ESPI/LPC (BIOS BEHIND BMC)
PCH HAS AN INTERNAL PULL-DOWN
FM_PCH_BOOT_BIOS_DEVICE R255 1KOhm R256 10KOhm
XTAL INPUT MODE
0: XTAL INPUT IS SINGLE-ENDED
1: XTAL INPUT IS DIFFERENTIAL (DEFAULT)
FM_STRAP_XTAL_MODE R257 1KOhm R258 1KOhm
ESPI FLASH SHARING MODE
0 = MASTER ATTACHED FLASH SHARING (MAFS)
1 = SLAVE ATTACHED FLASH SHARING (SAFS)
FM_ESPI_FLASH_MODE R265 1KOhm
FM_INTRUDER_HDR_PCH# R1902 1MOHM
BMC_SCL7 R271 1KOhm
BMC_SDA7 R272 1KOhm
PLACE BYPASS RES CLOSE TO PCH PIN
RSTBTN_OUT_N R1756 33.2OHM
REAR_SYSRST_BTN# 42,47,51
JTAG ODT DISABLE STRAP (DFX)
PCH HAS NO INTERNAL TERMINATION
JTAG ODT DISABLED WHEN LOW
JTAG ODT ENABLED WHEN HIGH (DEFAULT)
FM_STRAP_JTAG_ODT_EN R273 10KOhm R274 1KOhm
FM_PCH_BIOS_RCVR
FM_PCH_PWRBTN#
PCH_TMTRIP#
M2_33K_SUSCLK
BMC_SCL7
BMC_SDA7
PU_PCH_GPP_H18
FM_ESPI_FLASH_MODE
FM_STRAP_JTAG_ODT_EN
FM_PCH_BOOT_BIOS_DEVICE
FM_BIOS_POST_CMPLTR
FM_PERST_SEL_BIT1
FM_PERST_SEL_BIT0
FM_SLPS3#_R
FM_SLPS4#_R
FM_SLPA#_R
P1_RST#_R
PLTRST#_R
SYS_PWROK_R
CPU_PWRGD
PCH_RSMRST
OCP1_WAKE#
OCP2_WAKE#
PE2_X8_WAKE#
LAN_WAKE#
WIFI_WAKE#
FM_PCH_BATLOW#
FM_PCH_ACPRESENT
FM_PCH_LAN_WAKE#
FM_STRAP_XTAL_MODE
IRQ_LVC3_WAKE#_R
FM_INTRUDER_HDR_PCH#
FM_PCH_BIOS_RCVRR
FM_PCH_PWRBTN#
PCH_TMTRIP#
M2_33K_SUSCLK
FM_ESPI_FLASH_MODE
FM_STRAP_JTAG_ODT_EN
BMC_SCL7
BMC_SDA7
PU_PCH_GPP_H18
FM_SWAP_OVERRIDE#
FM_PMBUS_ALERT_EN
FM_PCH_BOOT_BIOS_DEVICE
FM_BIOS_POST_CMPLT#
FM_NIC1_DISABLE#
FM_NIC2_DISABLE#
FM_NIC3_DISABLE#
FM_NIC4_DISABLE#
FM_SLPS3#
FM_SLPS4#
FM_SLPS5#
FM_SLPA#
SLP_SUS#
RST_DRAM_RESET#
P1_RST#
PLTRST#
SYS_PWROK
RSTBTN_OUT_N
P1_PWRGD
PWROK_PCH
RSMRST#
DSW_PWROK
RST_SRTCRST#
IRQ_LVC3_WAKE#
FM_PCH_BIOS_RCVR
FM_PCH_PWRBTN#
PCH_TMTRIP#
M2_33K_SUSCLK
FM_ESPI_FLASH_MODE
FM_INTRUDER_HDR_PCH#
BMC_SCL7
BMC_SDA7
FM_PMBUS_ALERT_EN
FM_SWAP_OVERRIDE#
FM_PCH_BOOT_BIOS_DEVICE
FM_BIOS_POST_CMPLT#
FM_PERST_SEL_BIT1
FM_PERST_SEL_BIT0
FM_SLPS3#_R
FM_SLPS4#_R
FM_SLPA#_R
P1_RST#_R
PLTRST#_R
SYS_PWROK_R
CPU_PWRGD
PCH_RSMRST
OCP1_WAKE#
OCP2_WAKE#
PE2_X8_WAKE#
LAN_WAKE#
WIFI_WAKE#
FM_PCH_BATLOW#
FM_PCH_ACPRESENT
FM_PCH_LAN_WAKE#
FM_STRAP_XTAL_MODE
IRQ_LVC3_WAKE#_R
FM_INTRUDER_HDR_PCH#
FM_PCH_BIOS_RCVRR
FM_PCH_PWRBTN#
PCH_TMTRIP#
M2_33K_SUSCLK
FM_ESPI_FLASH_MODE
FM_STRAP_JTAG_ODT_EN
BMC_SCL7
BMC_SDA7
PU_PCH_GPP_H18
FM_SWAP_OVERRIDE#
FM_PMBUS_ALERT_EN



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 035 PCH CLOCK
Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 35 of 110

PCH1E

AUDIO/I2S

HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDA_BCLK/I2S0_SCLK
HDA_RST#/I2S1_SCLK
HDACPU_SDI
HDACPU_SDO
HDACPU_SCLK
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D7/I2S2_RXD
GPP_D8/I2S2_SCLK

46 FM_FLASH_SECURITY_STRAP — FM_FLASH_SECURITY_STRAP — BF12

41 I2S_WS — I2S_WS — BE16
41 I2S_SD_IN — I2S_SD_IN — BA17
41 I2S_SD_OUT — I2S_SD_OUT — AW18
41 I2S_SCLK — I2S_SCLK — AV18

CLINK

CL_CLK — AR2 CLINK_CLK — CLINK_CLK 41
CL_DATA — AT5 CLINK_DATA — CLINK_DATA 41
CL_RST# — AU4 CLINK_RST# — CLINK_RST# 41

SPI1

GPP_D0/SPI1_CS#/SBK0/BK0
GPP_D1/SPI1_CLK/SBK1/BK1
GPP_D2/SPI1_MISO/SBK2/BK2
GPP_D3/SPI1_MOSI/SBK3/BK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3

BF19 IRQ_PCH_NMI — IRQ_PCH_NMI
BE19 FP_PWR_LED# — FP_PWR_LED#

I2C

GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL

BF23, BC22, BF21, BE21

DBG

GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA

CPU_TRST# — AM4 R328 0Ohm — JTAG_XDP_TRST# — JTAG_XDP_TRST# 17,42,56
PRDY# — AM5 XDP_PRDY# — XDP_PRDY# 17,42,56
PREQ# — AL2 XDP_PREQ# — XDP_PREQ# 17,42,56

SMB

GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

42,50,61,91 HOST_SCL — HOST_SCL R333 10Ohm — PCH_HOST_SCL — BE26
42,50,61,91 HOST_SDA — HOST_SDA R334 10Ohm — PCH_HOST_SDA — BF26
PU_PCH_TLS_ENABLE_STRAP — BE25

61 SML0_SCL — SML0_SCL R336 10Ohm — PCH_SML0_SCL — BF25
61 SML0_SDA — SML0_SDA R337 10Ohm — PCH_SML0_SDA — BE24
46 IRQ_SML0_ALERT# — IRQ_SML0_ALERT# R338 49.9 OHM — IRQ_SML0_ALERT#_R — BF24

50 SML1_SCL — SML1_SCL R339 10Ohm — PCH_SML1_SCL — BF27
50 SML1_SDA — SML1_SDA R340 10Ohm — PCH_SML1_SDA — BE27
43 FM_PCH_THERMTRIP# — FM_PCH_THERMTRIP# — BD33

+3.3V_DUAL
PCH_HOST_SCL R329 1KOhm
PCH_HOST_SDA R330 1KOhm
PCH_SML1_SCL R331 1KOhm
PCH_SML1_SDA R332 1KOhm

UART

GPP_C8/UART0A_RXD
GPP_C9/UART0A_TXD
GPP_C10/UART0A_RTS#
GPP_C11/UART0A_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#

46 FM_PASSWORD_CLEAR# — FM_PASSWORD_CLEAR# R341 33.2Ohm — FM_PASSWORD_CLEAR#_R — BE23
46 FM_MFG_MODE — FM_MFG_MODE — BB24
52,79 FM_THROTTLE_IN_N — FM_THROTTLE_IN_N R1865 33.2Ohm — PCH_THROTTLE_IN_N_R — BA24 / AP24
52,79 FM_NM_THROTTLE# — FM_NM_THROTTLE# R343 33.2Ohm — FM_NM_THROTTLE_PCH#_R — BD20
52 BMC_MUX_RST# — BMC_MUX_RST# R344 33.2Ohm — PCH_MUX_RST# — BE20
50 BMC_LPC_IRQ# — BMC_LPC_IRQ# — AW21
21 PCH_CATERR# — PCH_CATERR# — AV21

ISH_SPI

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI

BA20, BB20, BB16, AN18

ISH_I2C

GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL

BE15, BE14

ISH_UART

GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D16/ISH_UART0_CTS#/CNV_WCEN

BE17, BF17, AR18, BF14

32 FM_BOARD_REV_ID0 — FM_BOARD_REV_ID0 — AU24
32 FM_BOARD_REV_ID1 — FM_BOARD_REV_ID1 — AP21
51 BMC_PCH_SCI# — BMC_PCH_SCI# — AW24
BD21

GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#

958988

JTAG_XDP_TCK1 R322 51.1 OHM 1%
+1V_VCCST
C249 0.1UF/16V X7R/+/-10%
+3.3V_DUAL
FM_NM_THROTTLE_PCH#_R R323 10KOhm
FP_PWR_LED# R324 10KOhm
IRQ_PCH_NMI R321 10KOhm

TLS CONFIDENTIALITY

TLS ENABLED WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-DOWN

+3.3V_DUAL
PU_PCH_TLS_ENABLE_STRAP R326 1KOhm
R327 1KOhm

FLASH SECURITY OVERRIDE

0 = FLASH SECURITY OVERRIDE DISABLE (DEFAULT)
1 = FLASH SECURITY OVERRIDE ENABLE
PCH HAS INTERNAL PULL-DOWN

+3.3V_DUAL
FM_FLASH_SECURITY_STRAP R335 1KOhm

PCH_JTAG_TMS — AJ4 JTAG_XDP_TMS — JTAG_XDP_TMS 17,42,56
PCH_JTAG_TDO — AH3 JTAG_XDP_TDO — JTAG_XDP_TDO 17,42,56
PCH_JTAG_TDI — AH2 JTAG_XDP_TDI — JTAG_XDP_TDI 17,42,56
PCH_JTAG_TCK — AJ3 JTAG_XDP_TCK1 — JTAG_XDP_TCK1 42,56
PCH_JTAGX — AH4 JTAG_XDP_RTCK — JTAG_XDP_RTCK 42
ITP_PMODE — AL3 XDP_ITP_PMODE — XDP_ITP_PMODE 42

DFXTESTMODE ACTIVE

PCH INTERNAL PULL-UP
DFXTESTMODE ENABLED WHEN LOW

XDP_ITP_PMODE R342 1KOhm

DCI DISABLE: EXI BOOT STALLBYPASS (DFX)

0 :DCI ENABLED (DEFAULT)
1 :DCI DISABLED
PCH HAS A 20K INTERNAL PULL-DOWN

+3.3V_DUAL
FM_PCH_THERMTRIP# R345 1MOHM

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 036 PCH XDP
Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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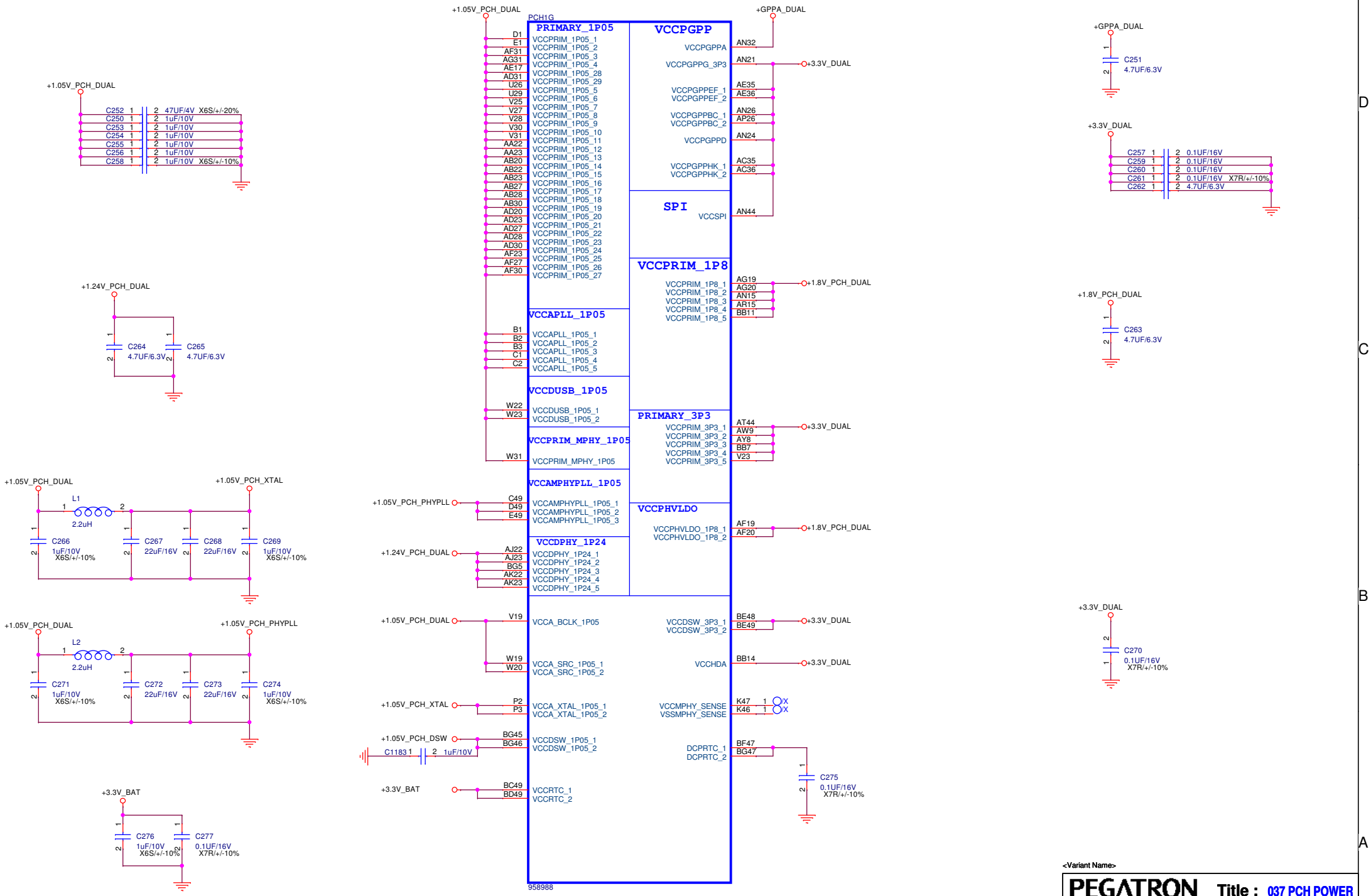
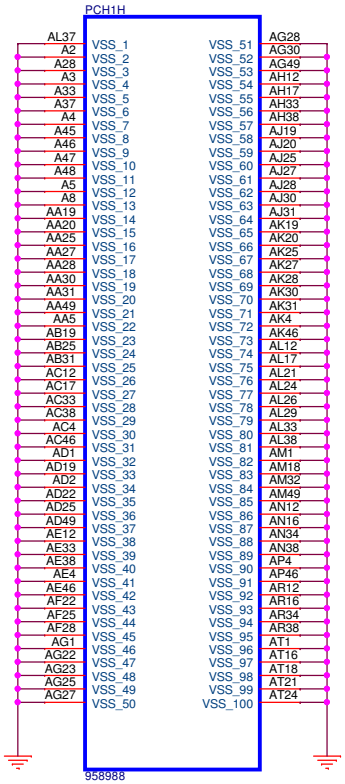


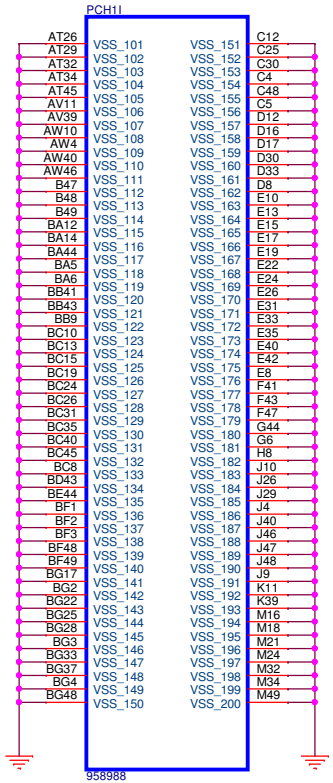
<Variant Name>

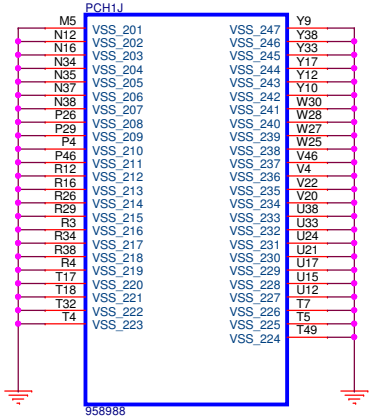
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 037 PCH POWER
PEGATRON CORPORATION
Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 37 of 110







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PEGATRON

Title : 038 PCH GND

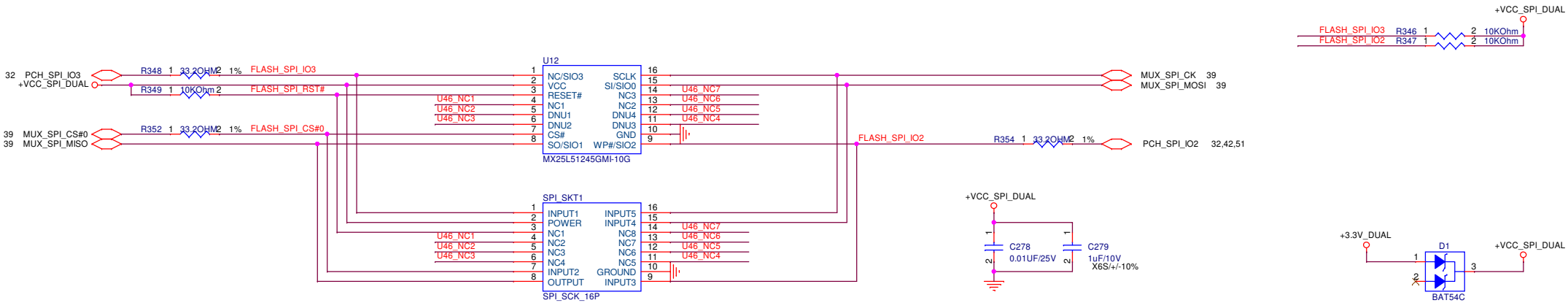
PEGATRON PROPRIETARY AND CONFIDENTIAL

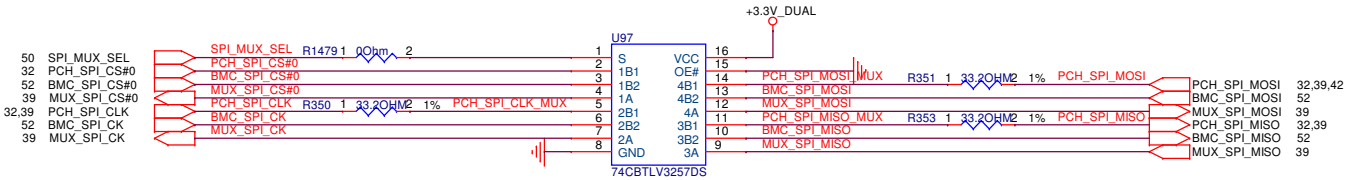
PEGATRON CORPORATION Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

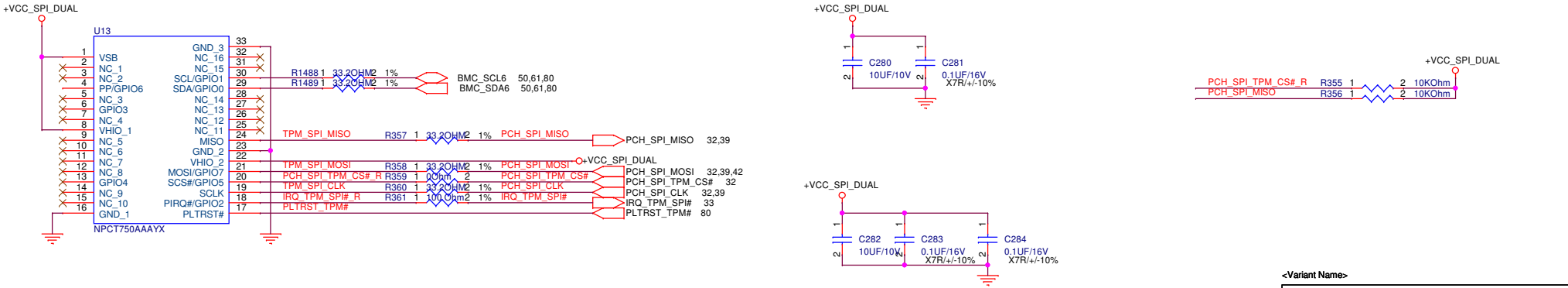
Date: Tuesday, November 27, 2018 Sheet 38 of 110

BIOS FLASH

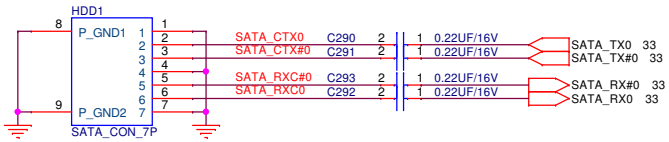


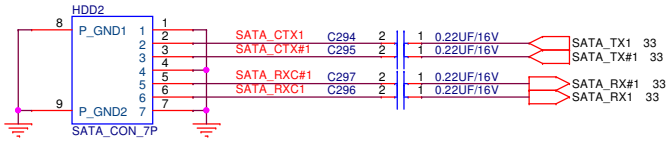


TPM



SATA HDD CONNECTOR





<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 040 SATA 2.5" HDD

PEGATRON CORPORATION Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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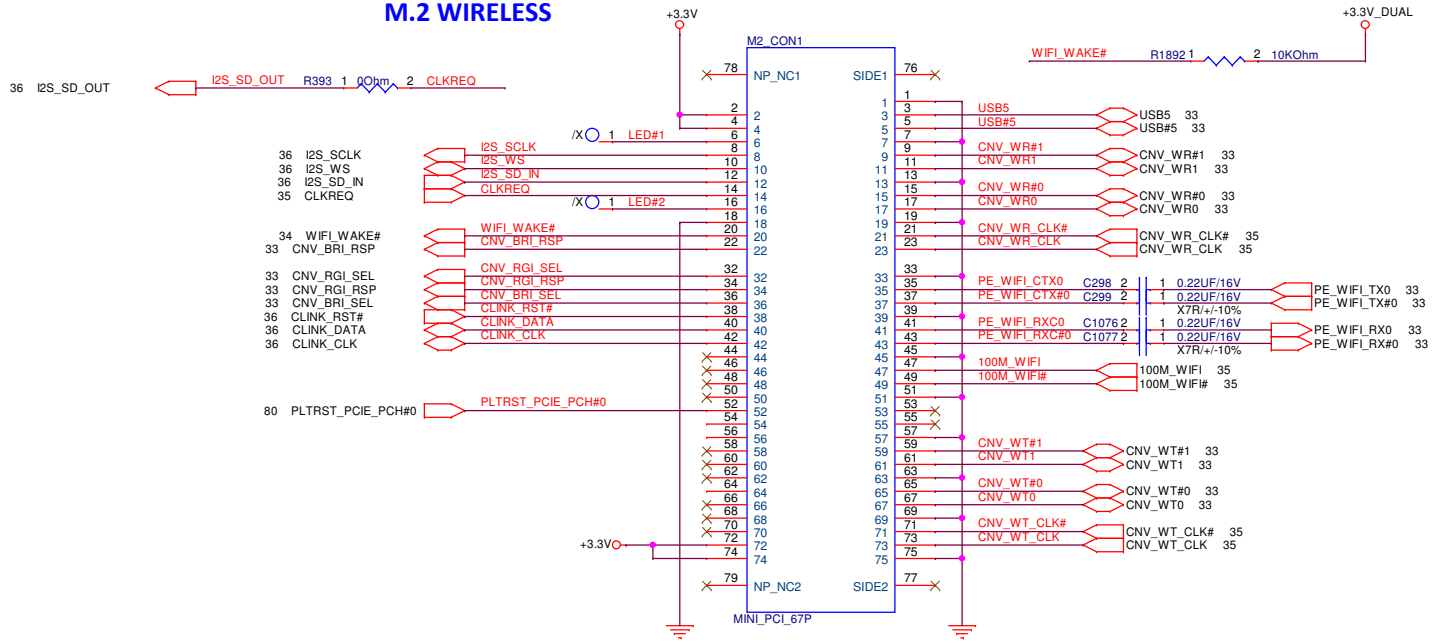
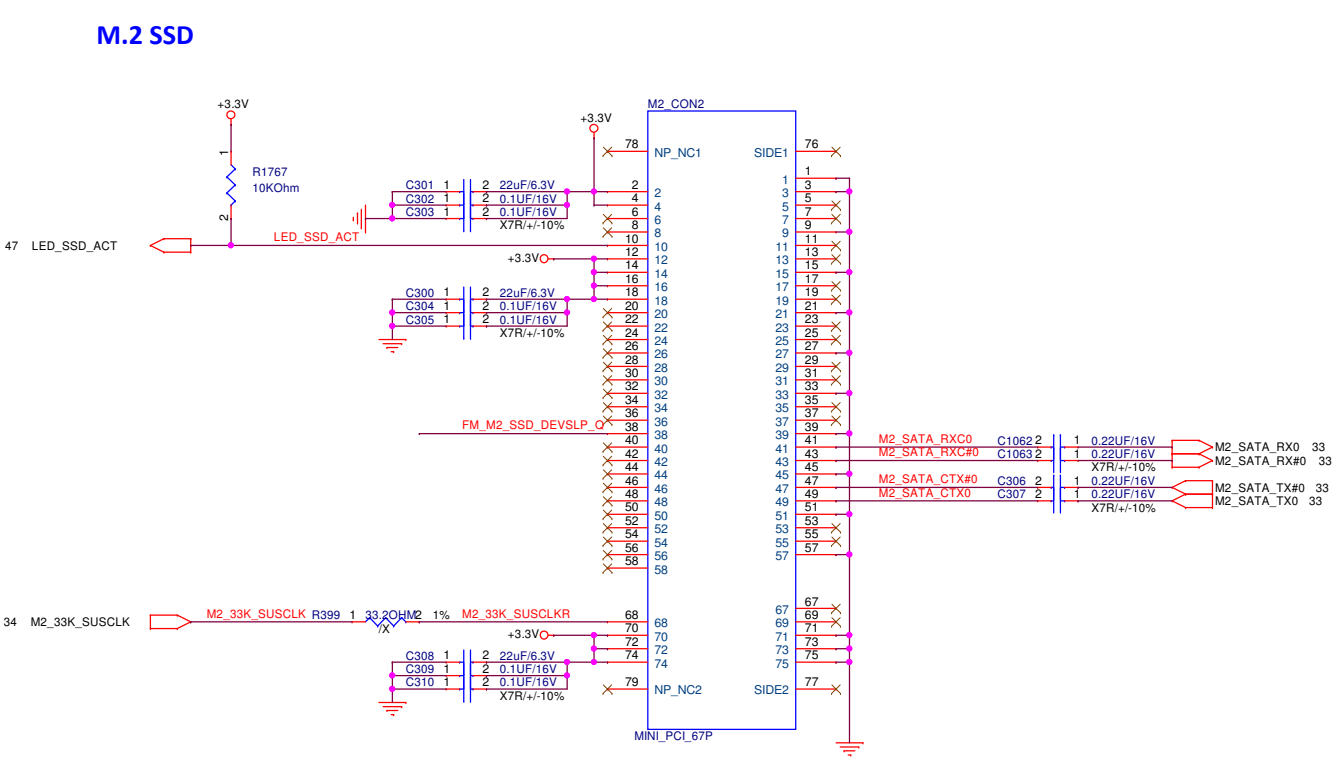
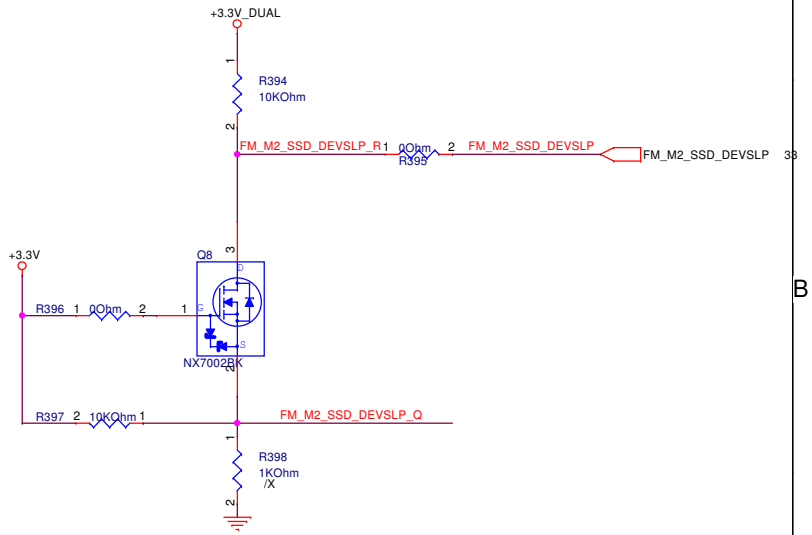
M.2 WIRELESS



M.2 SSD





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 041 M.2 CONN/WIREL

PEGATRON CORPORATION Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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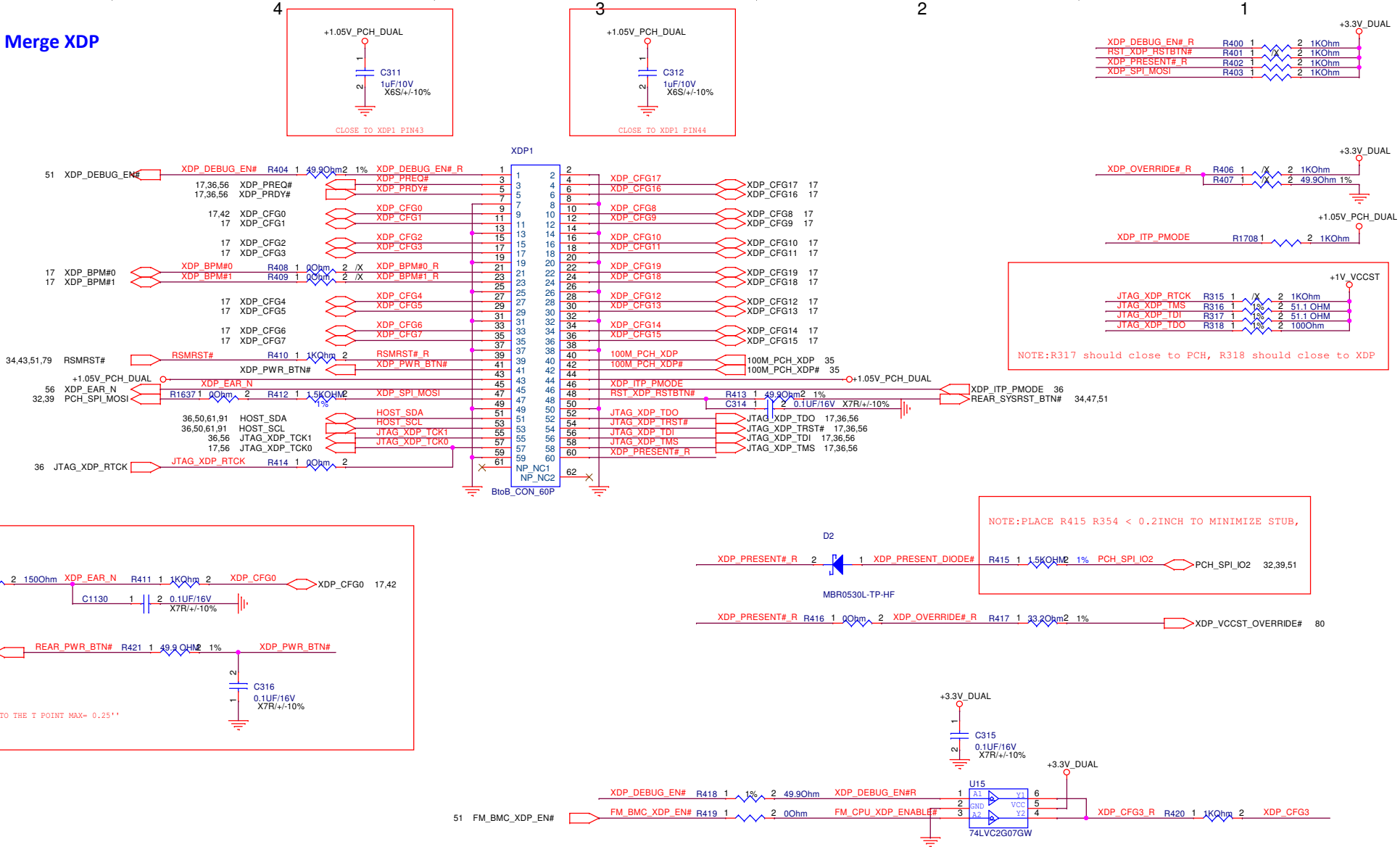
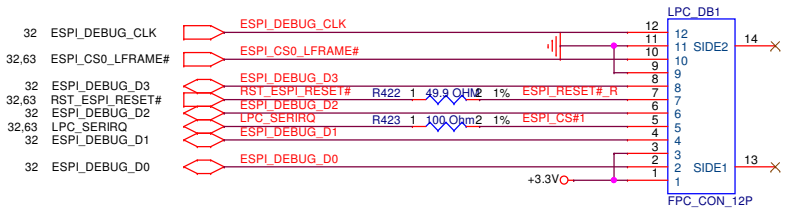
Merge XDP



LPC/ESPI DEBUG PORT



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 042 Merge XDP/DEBU
PEGATRON CORPORATION
Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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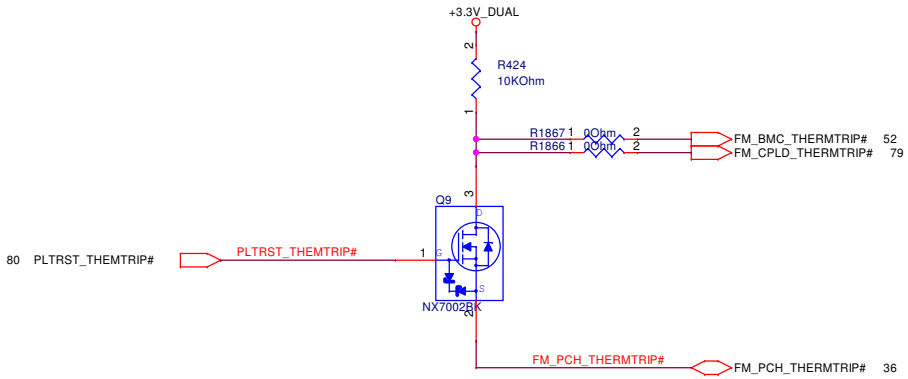
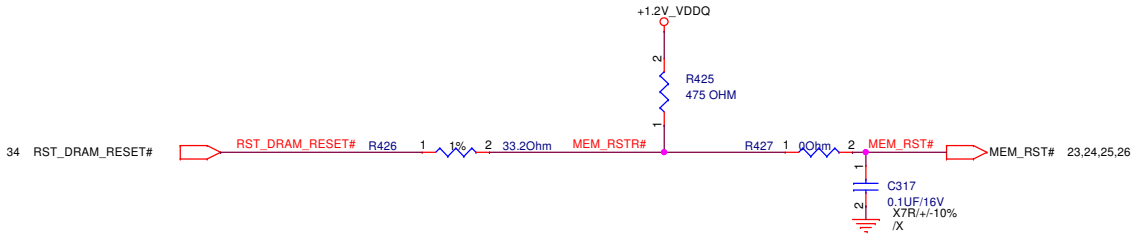
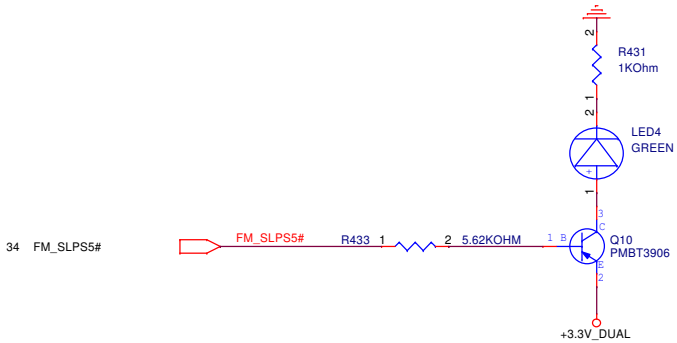
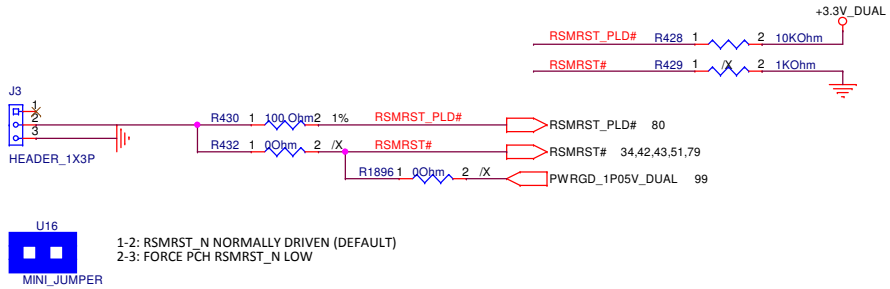
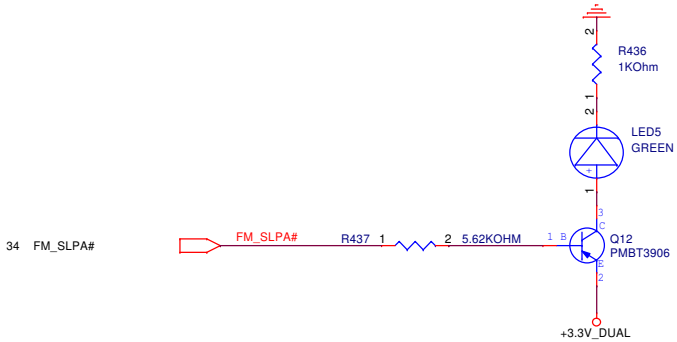


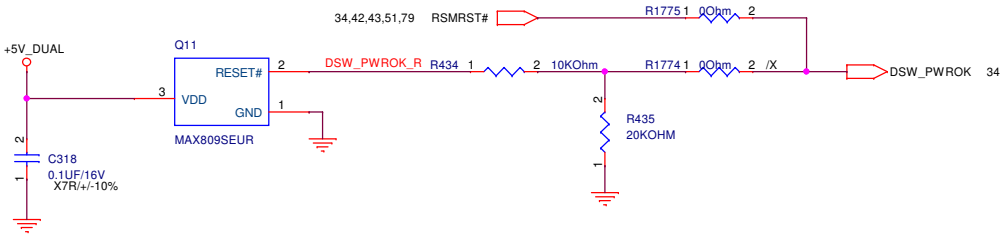








DSW PWROK



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 043 PCH SIDEBAND

PEGATRON CORPORATION Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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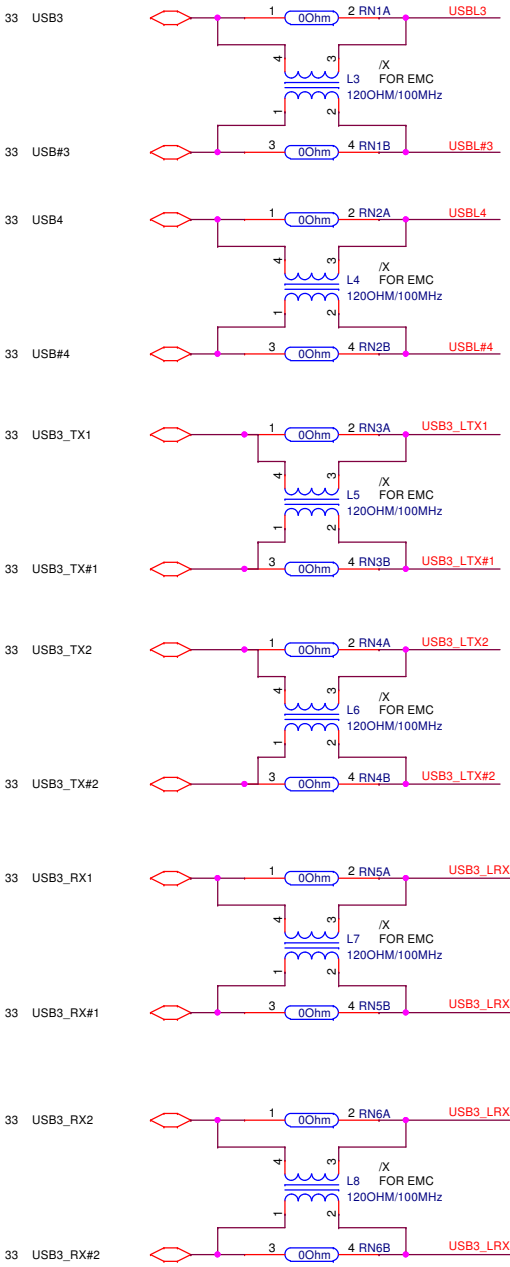
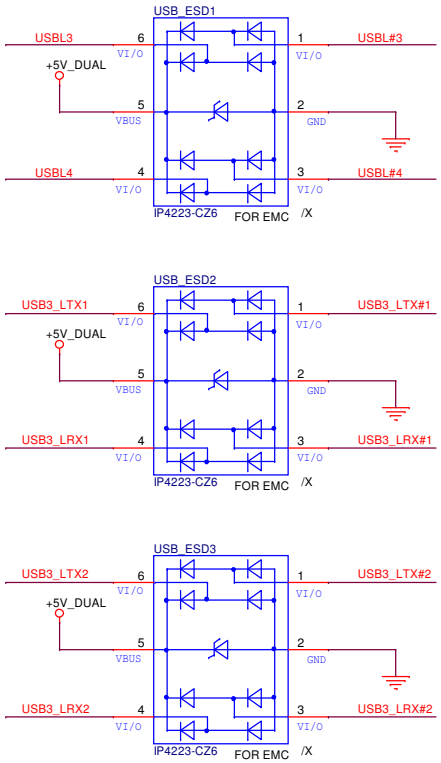
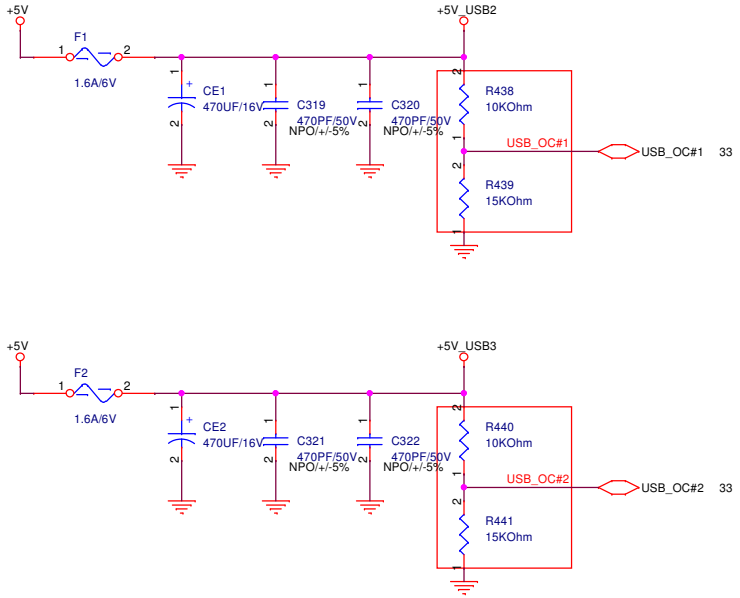
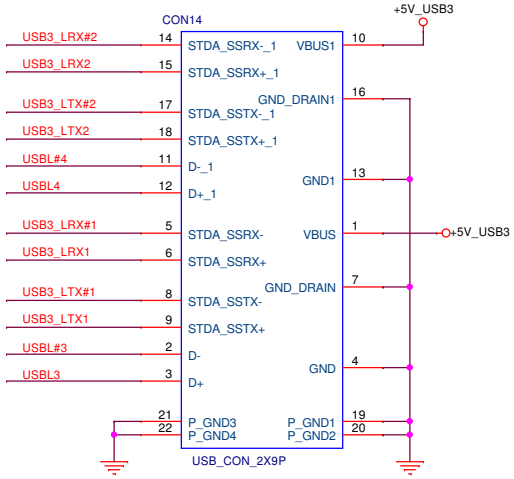




NOTE:R438~R441 CRB use 1% ohm



USB3.0



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 044 USB3
Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 44 of 110

<Variant Name>

PEGATRON

Title : 045 USB3 redriver

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON CORPORATION

Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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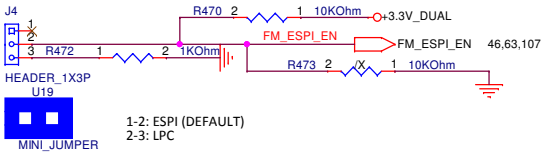
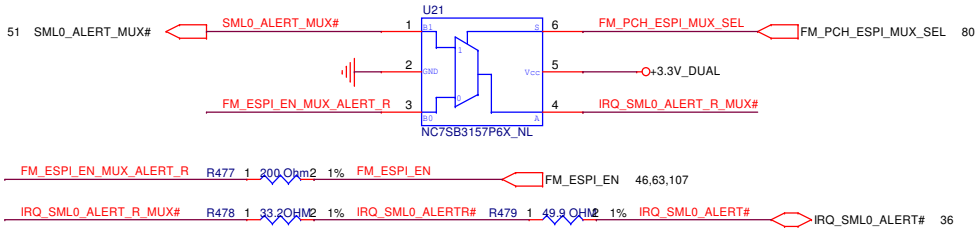
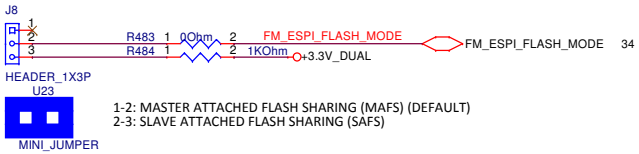
ESPI OR LPC



1-2: ESPI (DEFAULT)
2-3: LPC

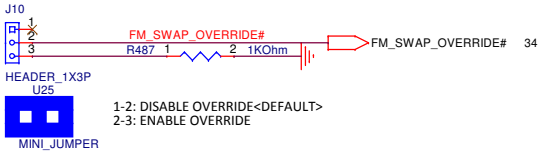


ESPI FLASH SHARING MODE



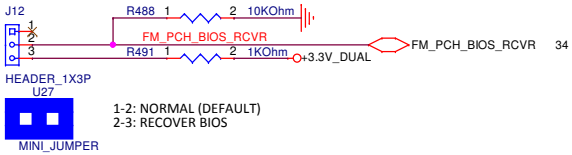
1-2: MASTER ATTACHED FLASH SHARING (MAFS) (DEFAULT)
2-3: SLAVE ATTACHED FLASH SHARING (SAFS)

BIOS SWAP SOFTWARE OVERRIDE JUMPER



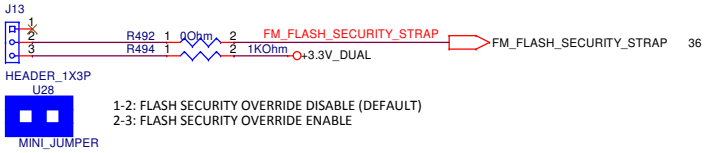
1-2: DISABLE OVERRIDE<DEFAULT>
2-3: ENABLE OVERRIDE

BIOS RECOVERY MODE / TOP SWAP OVERRIDE JUMPER



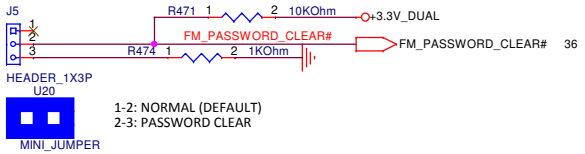
1-2: NORMAL (DEFAULT)
2-3: RECOVER BIOS

FLASH SECURITY OVERRIDE



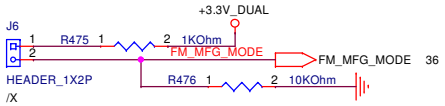
1-2: FLASH SECURITY OVERRIDE DISABLE (DEFAULT)
2-3: FLASH SECURITY OVERRIDE ENABLE

PASSWORD CLEAR JUMPER

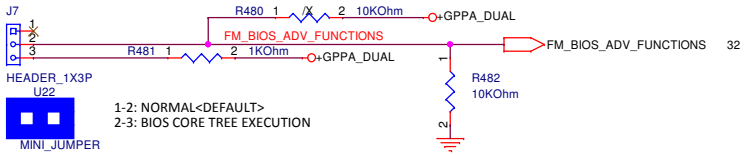


1-2: NORMAL (DEFAULT)
2-3: PASSWORD CLEAR

MANUFACTURING MODE JUMPER

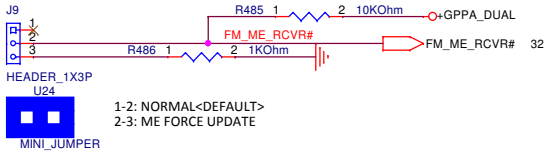


BIOS ADV FUNCTIONS



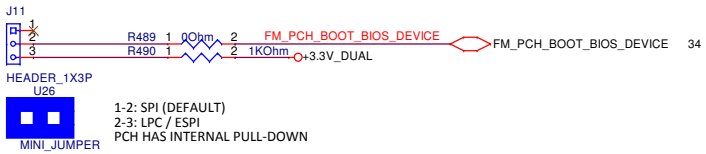
1-2: NORMAL<DEFAULT>
2-3: BIOS CORE TREE EXECUTION

ME FIRMWARE UPDATE



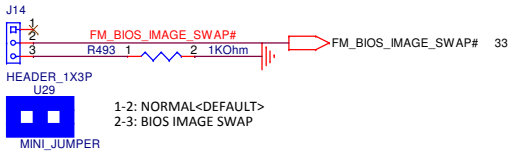
1-2: NORMAL<DEFAULT>
2-3: ME FORCE UPDATE

BOOT BIOS DEVICE



1-2: SPI (DEFAULT)
2-3: LPC / ESPI
PCH HAS INTERNAL PULL-DOWN

BIOS IMAGE SWAP JUMPER



1-2: NORMAL<DEFAULT>
2-3: BIOS IMAGE SWAP

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON CORPORATION

Title : 046 PCH HEADER

Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

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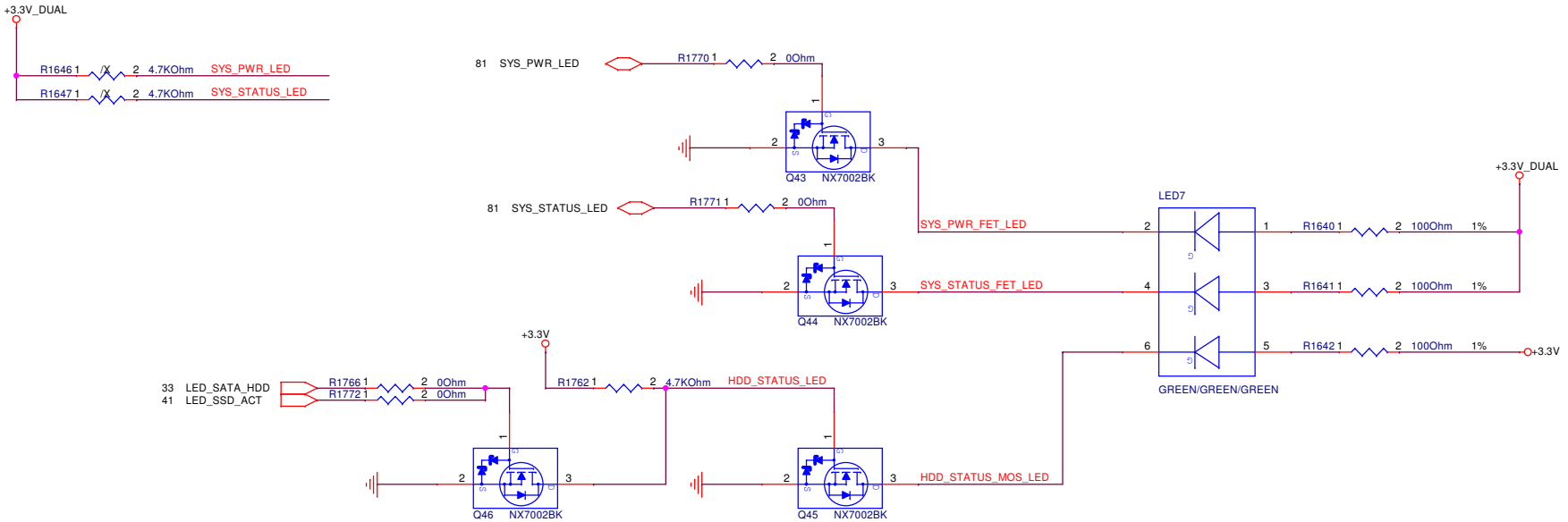
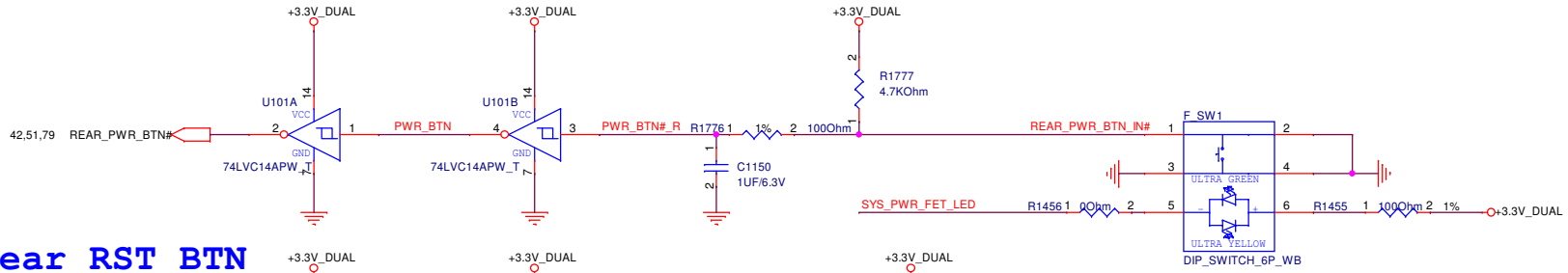
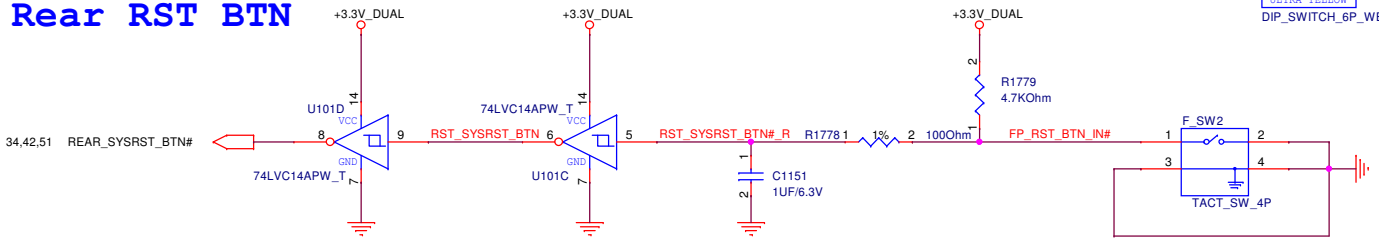
Front LED

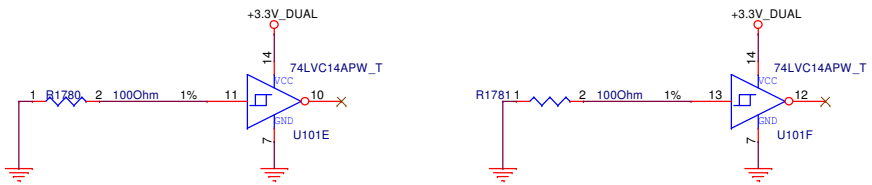


Rear PWR BTN



Rear RST BTN





<Variant Name>

PEGATRON

Title : 047 FP PWR

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON CORPORATION

Engineer: Tom_Liao

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 47 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

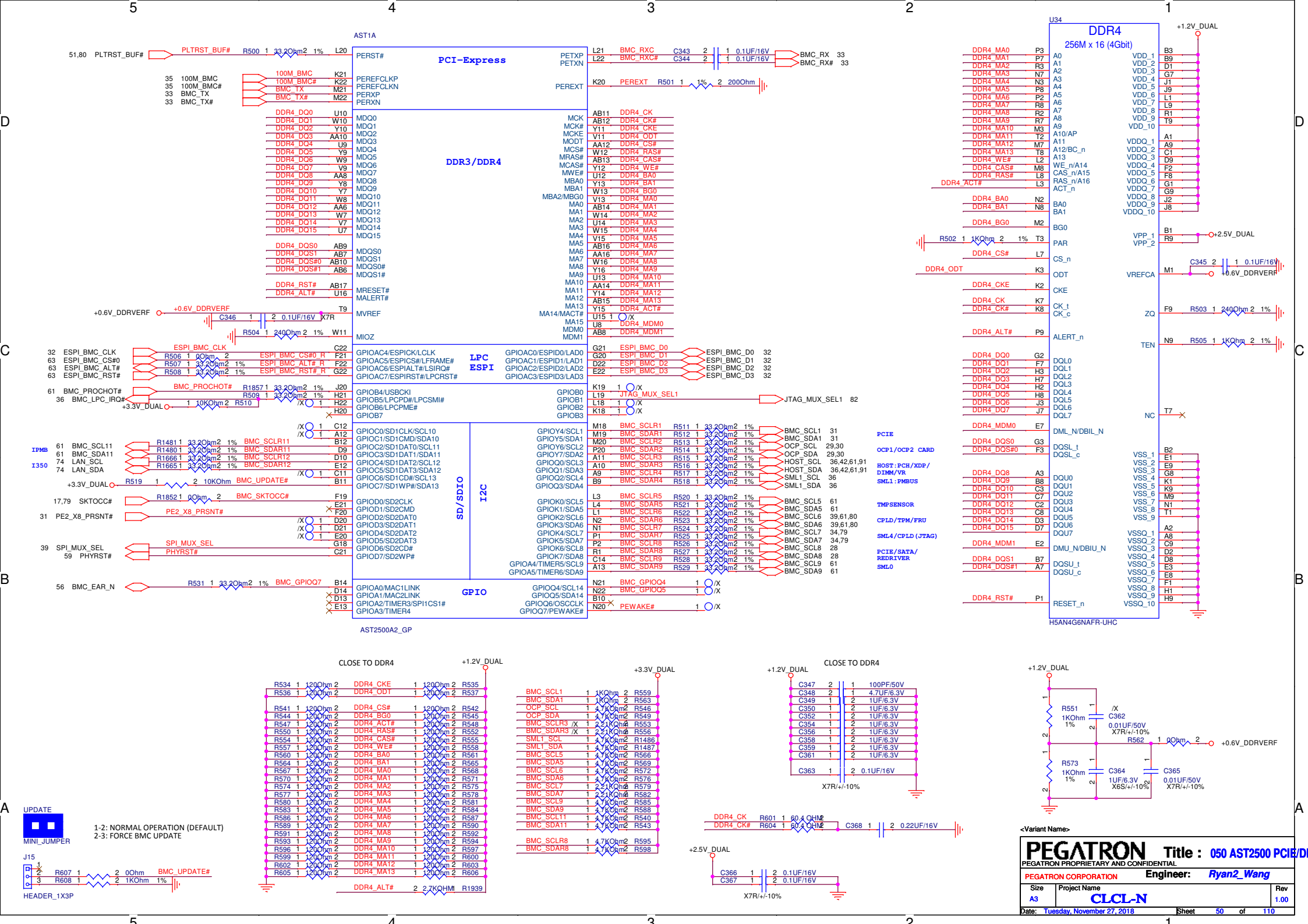
<Variant Name>

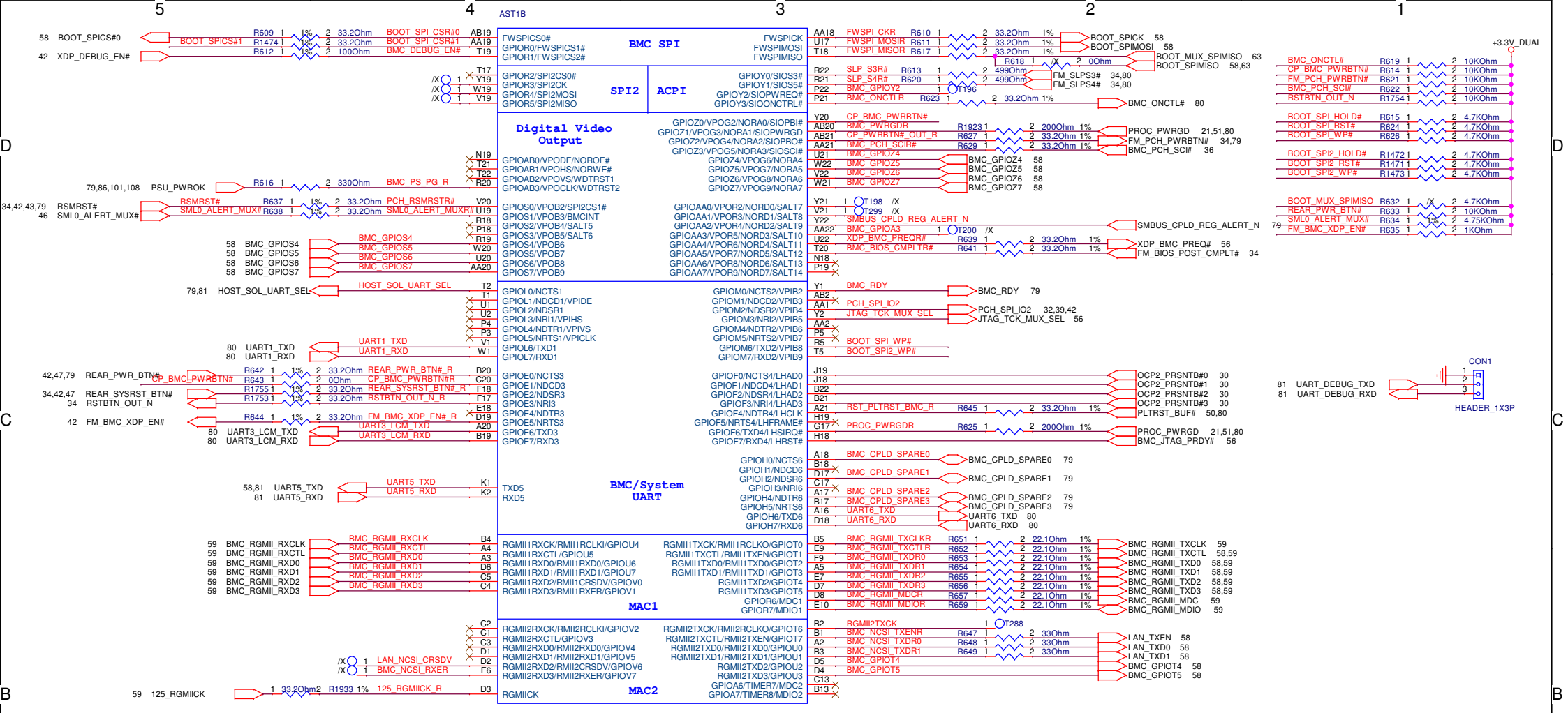
PEGATRON Title : 48

PEGATRON CORPORATION Engineer: Tom_Liao

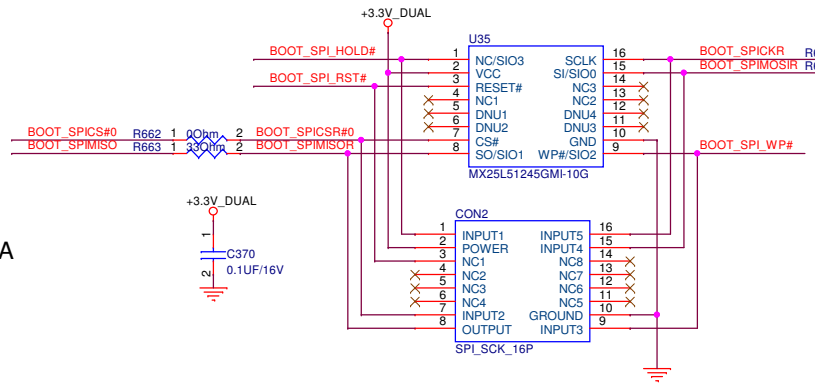
Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 48 of 110

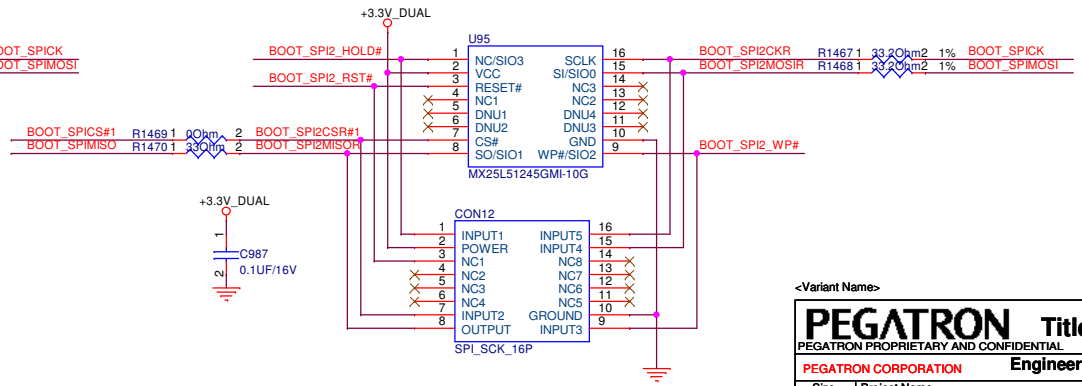

AST1A
PCI-Express
DDR3/DDR4
LPC ESPI
SD/SDIO
I2C
GPIO
AST2500A2_GP
U34
DDR4
256M x 16 (4Gbit)
H5AN4G6NAFR-UHC
CLOSE TO DDR4
+1.2V_DUAL
+3.3V_DUAL
+2.5V_DUAL
+0.6V_DDRVERF
UPDATE
MINI_JUMPER
1-2: NORMAL OPERATION (DEFAULT)
2-3: FORCE BMC UPDATE
J15
HEADER_1X3P
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION
Title : 050 AST2500 PCIE/DI
Engineer: Ryan2_Wang
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 50 of 110



Firmware_SPI_FLASH



Second_Boot_FLASH



<Variant Name>

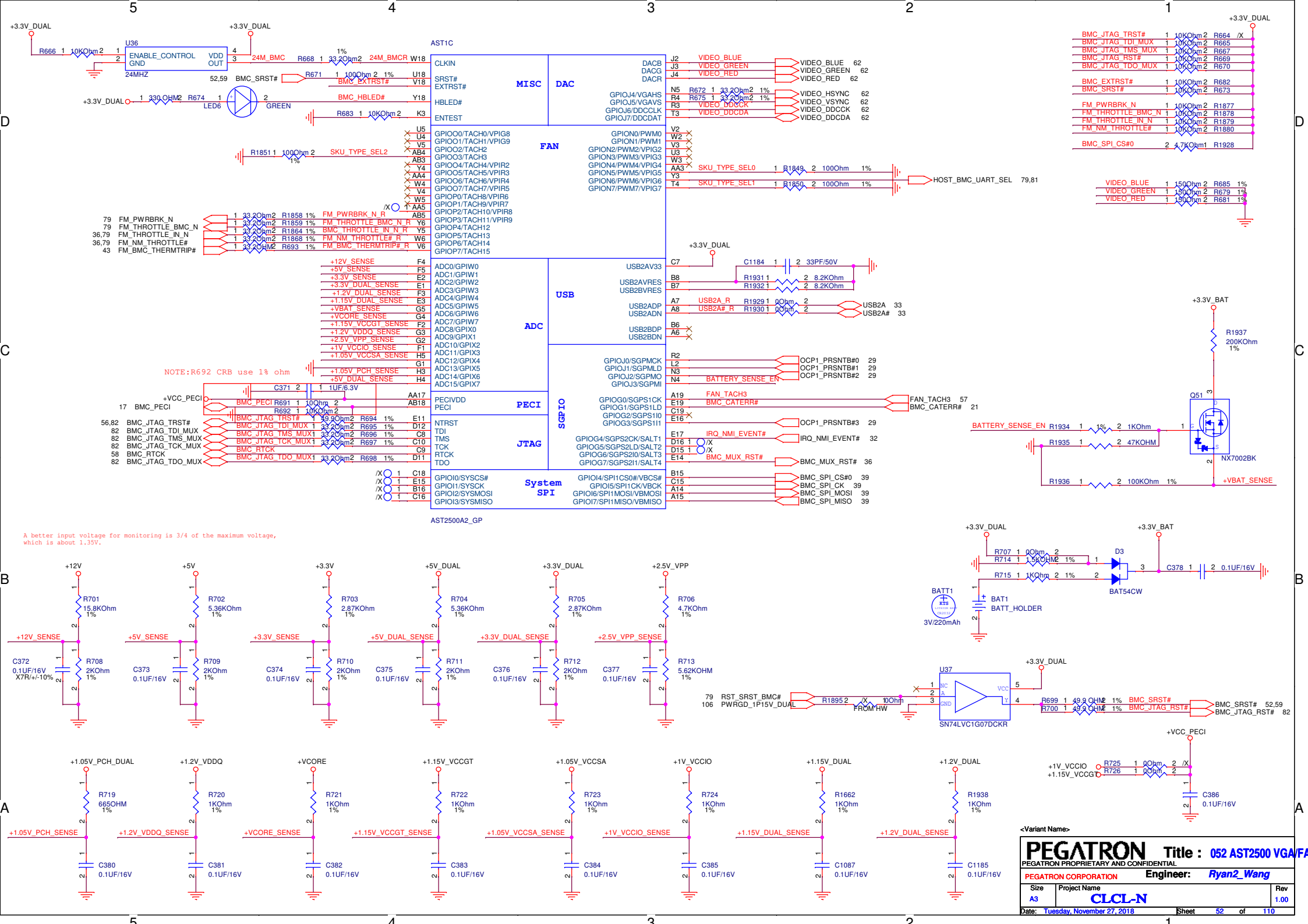
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

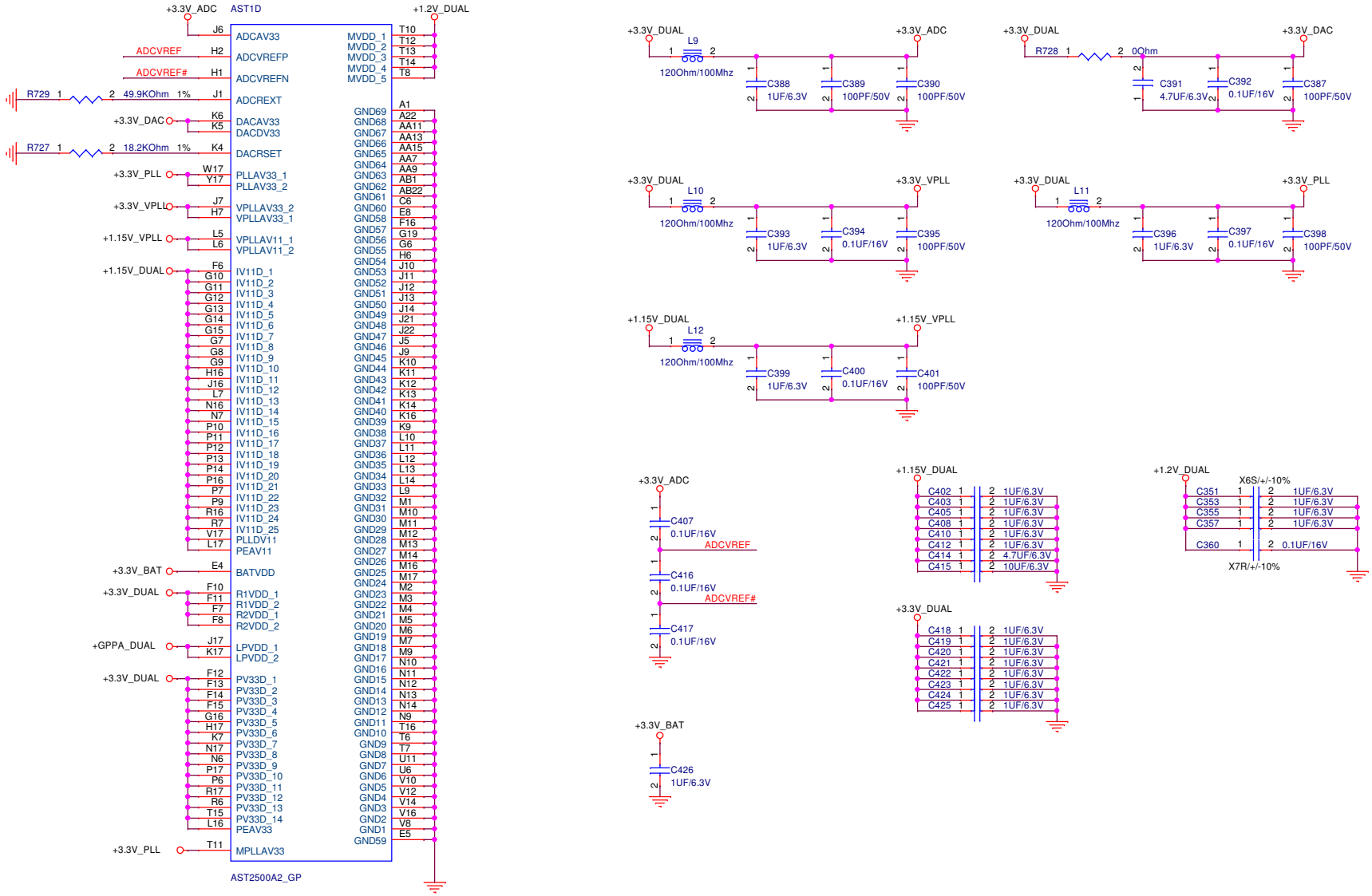
Title : 051 AST2500 SPI/UA

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 51 of 110


AST1C
MISC
DAC
FAN
ADC
USB
PECI
JTAG
SGPIO
System SPI
AST2500A2_GP
NOTE:R692 CRB use 1% ohm
A better input voltage for monitoring is 3/4 of the maximum voltage, which is about 1.35V.
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION
Title : 052 AST2500 VGA/FA
Engineer: Ryan2_Wang
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 52 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

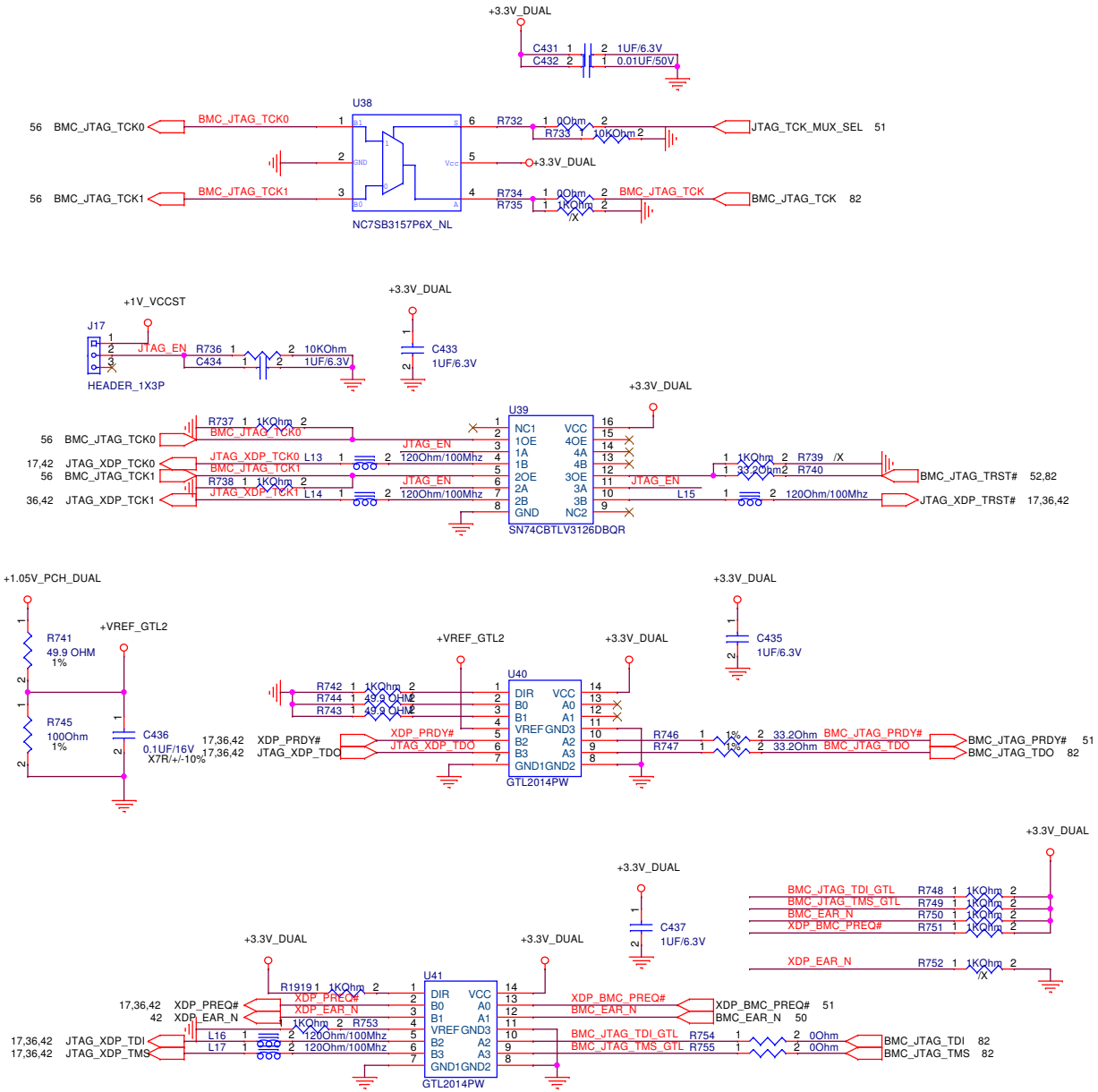
Title : 053 AST2500 POWER

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 53 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 056 AST2500 JTAG

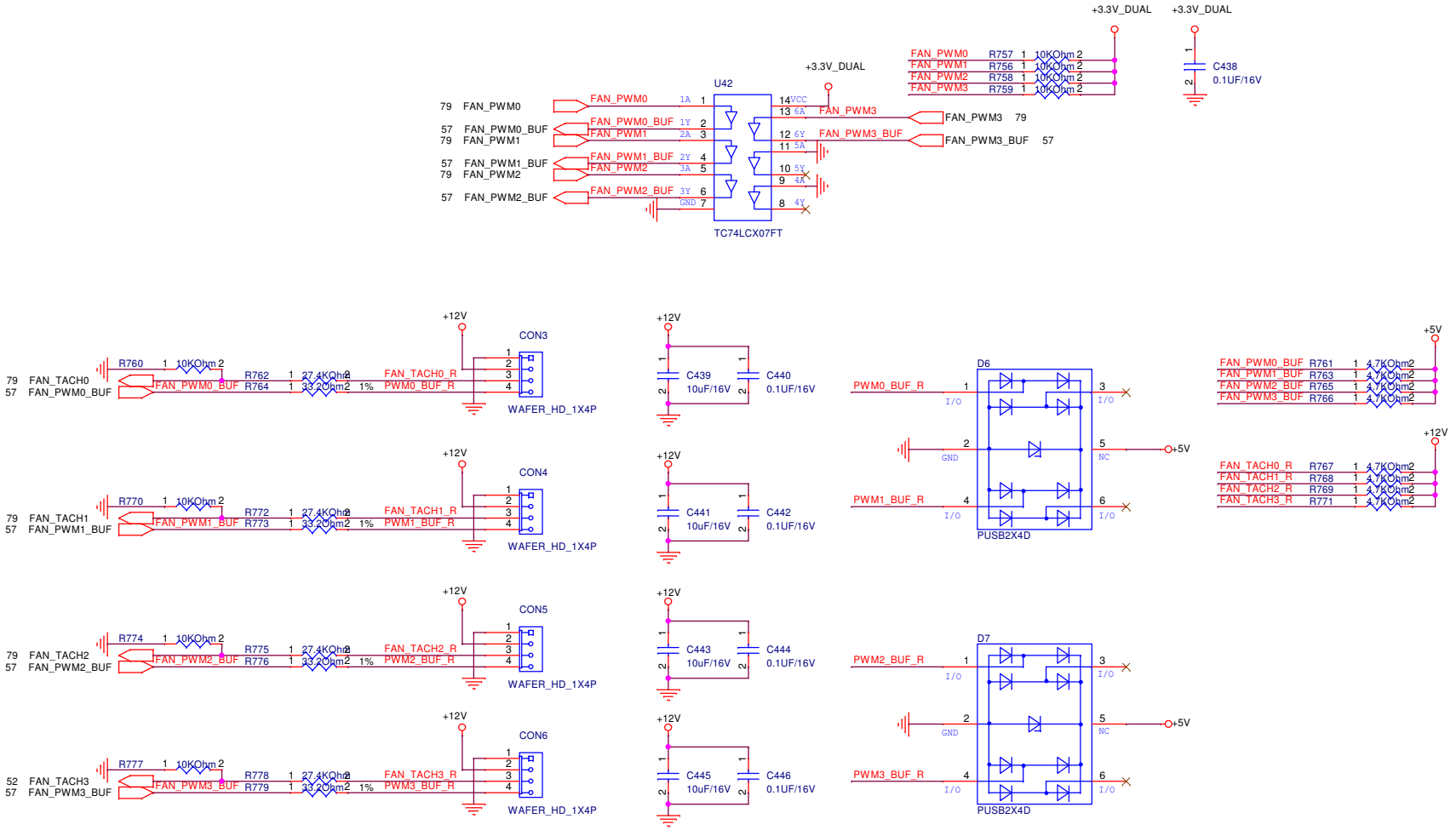
PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 56 of 110

FAN



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 057 AST2500 FAN

PEGATRON CORPORATION

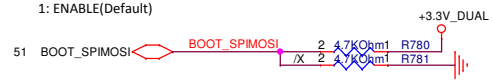
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 57 of 110

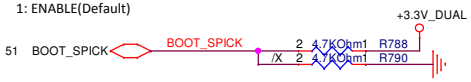
Enable SPI Flash Strap Auto Fetch Mode

0: DISABLE
1: ENABLE(Default)



Enable GPIO Strap Mode

0: DISABLE
1: ENABLE(Default)



Select UART Debug Port

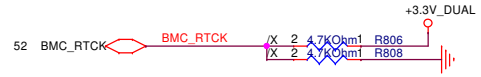
0: Select UART1 as BMC console port
1: Select UART5 as BMC console port(Default)

ENABLE fast reset mode for ARM ICE debugger

0: Long reset mode(Default)
1: Fast reset mode

ENABLE ESPI Flash MODE

0: ESPI respond with no flash attached (Default)
1: ESPI respond with flash attached



Enable ESPI Mode

0: LPC mode
1: eSPI mode (Default)

Select DDR4 SDRAM

0: DDR3 SRAM
1: DDR4 SRAM(Default)

Select Reference clock input mode

0: CLKIN is 24MHz and USBCKI not used(Default)
1: CLKIN is 25MHz and USBCKI=24/48MHz

Enable GPIOE pass-throug mode

0: Disable pass through
1: Enable pass through(Default)

Enable GPIOD pass-throug mode

0: Disable pass through(Default)
1: Enable pass through

Disable LPC to decode SuperIO address

0: ENABLE address decoding(Default)
1: DISABLE address decoding

Enable ACPI function

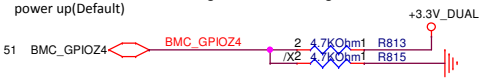
0: Disable ACPI
1: Enable ACPI(Default)

Select USBCKI input frequence

0: 24MHz(Default)
1: 48MHz

Enable BMC 2nd boot watchdog timer

0: DISABLE
1: ENABLE BMC 2nd boot watchdog timer star counting at power up(Default)

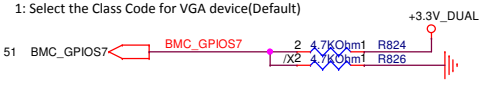


SuperIO configuration address selection

0: Decode 0x2E
1: Decode 0x4E(Default)

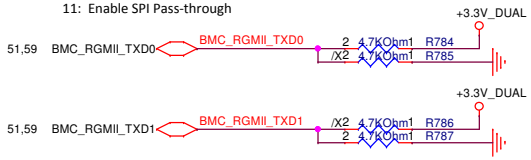
VGA Class Code selection

0: Select the Class Code for video device
1: Select the Class Code for VGA device(Default)



SPI mode selection

00: Disable SPI interface
01: Enable SPI Master(Default)
10: Reserved, enable SPI Master and SPI Slave to AHB
11: Enable SPI Pass-through



Define MAC#2 interface

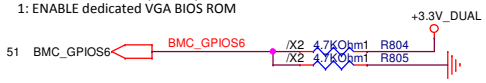
0: RMII/NCSI(Default)
1:RGMII

Define MAC#1 interface

0: RMII/NCSI
1:RGMII(Default)

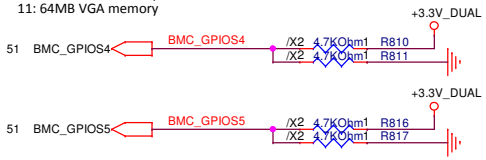
Enable VGA BIOS ROM

0: NO VGA BIOS ROM(Default)
1: ENABLE dedicated VGA BIOS ROM



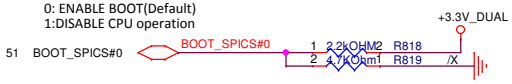
VGA memory size selection

00: 8 MB VGA memory
01: 16MB VGA memory(Default)
10: 32MB VGA memory
11: 64MB VGA memory



Disable CPU boot

0: ENABLE BOOT(Default)
1:DISABLE CPU operation



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 058 AST2500 STRAP
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

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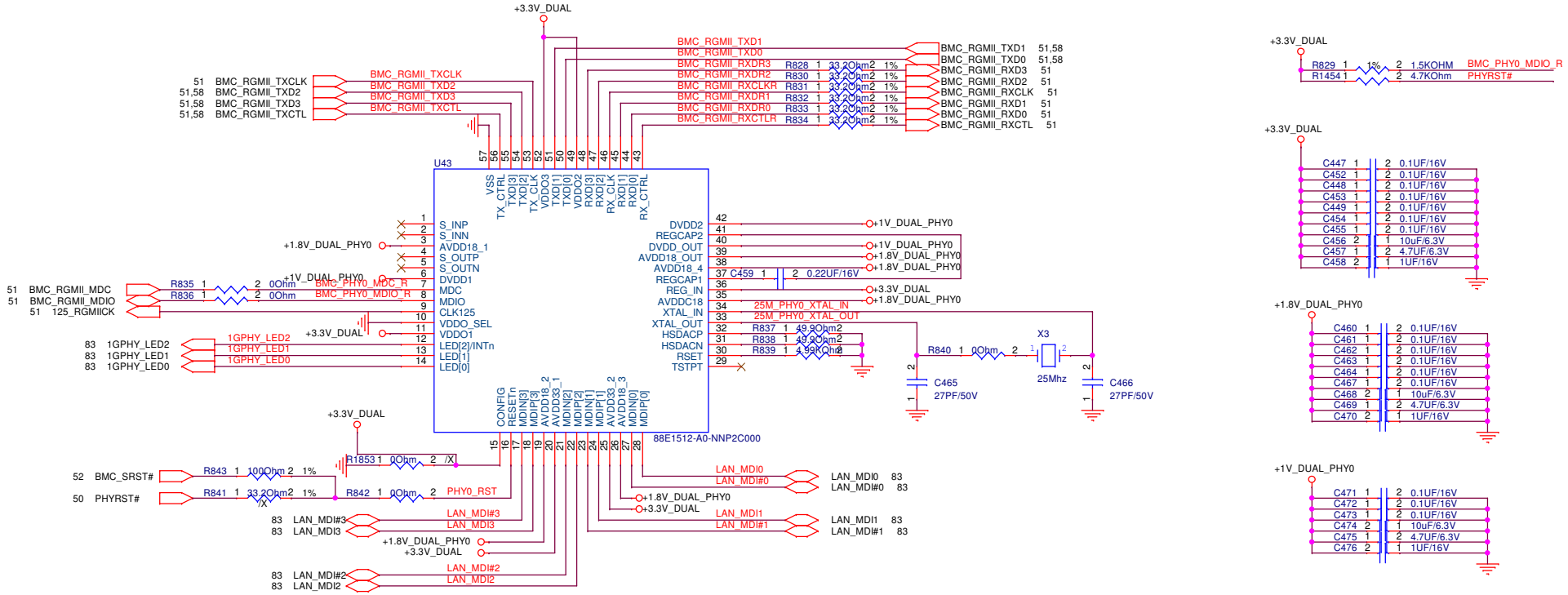
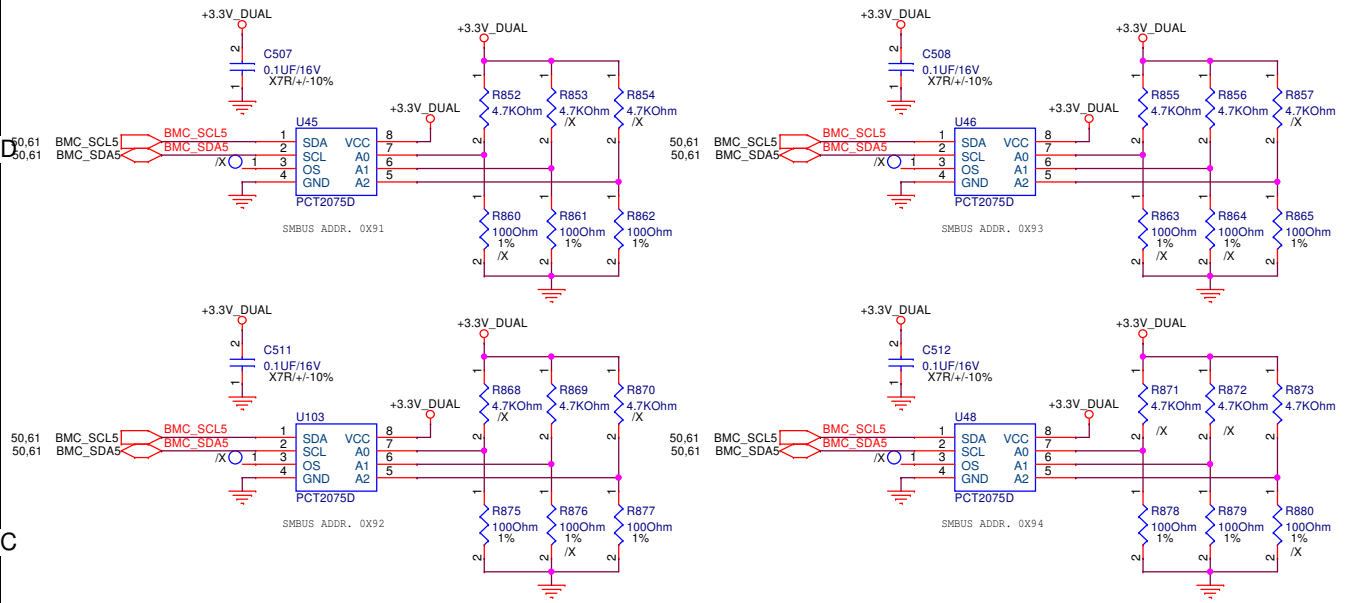
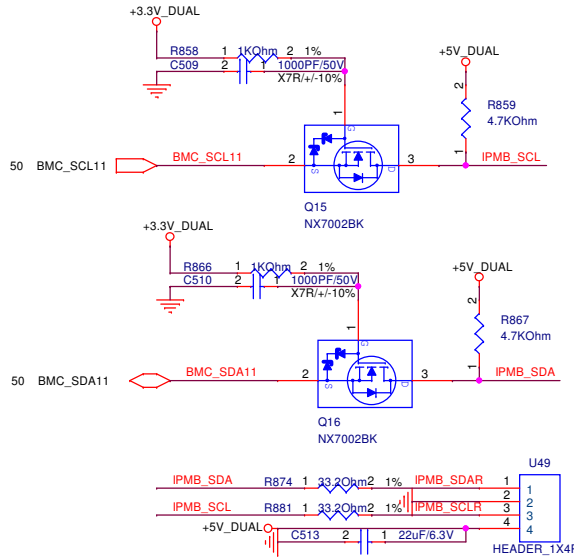

+3.3V_DUAL
U43
88E1512-A0-NNP2C000
BMC_RGMII_TXCLK
BMC_RGMII_TXD2
BMC_RGMII_TXD3
BMC_RGMII_TXCTL
BMC_RGMII_TXD1
BMC_RGMII_TXD0
BMC_RGMII_RXDR3
BMC_RGMII_RXDR2
BMC_RGMII_RXCLKR
BMC_RGMII_RXDR1
BMC_RGMII_RXDR0
BMC_RGMII_RXCTLR
BMC_RGMII_TXD1 51,58
BMC_RGMII_TXD0 51,58
BMC_RGMII_RXD3 51
BMC_RGMII_RXD2 51
BMC_RGMII_RXCLK 51
BMC_RGMII_RXD1 51
BMC_RGMII_RXD0 51
BMC_RGMII_RXCTL 51
+1.8V_DUAL_PHY0
+1V_DUAL_PHY0
+3.3V_DUAL
BMC_RGMII_MDC
BMC_RGMII_MDIO
125_RGMIICK
BMC_PHY0_MDC_R
BMC_PHY0_MDIO_R
1GPHY_LED2
1GPHY_LED1
1GPHY_LED0
25M_PHY0_XTAL_IN
25M_PHY0_XTAL_OUT
25Mhz
C465
27PF/50V
C466
27PF/50V
BMC_SRST#
PHYRST#
PHY0_RST
LAN_MDI0
LAN_MDI#0
LAN_MDI1
LAN_MDI#1
LAN_MDI2
LAN_MDI#2
LAN_MDI3
LAN_MDI#3

+3.3V_DUAL
R829 1% 1.5KOHM BMC_PHY0_MDIO_R
R1454 4.7KOhm PHYRST#
+1.8V_DUAL_PHY0
+1V_DUAL_PHY0

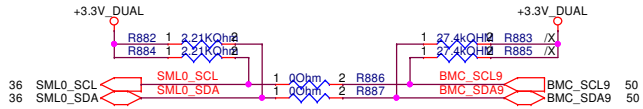
TMPSENSOR_SMBUS



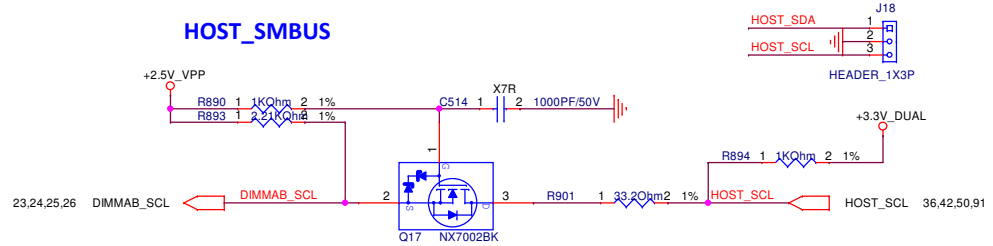
IPMB_SMBUS



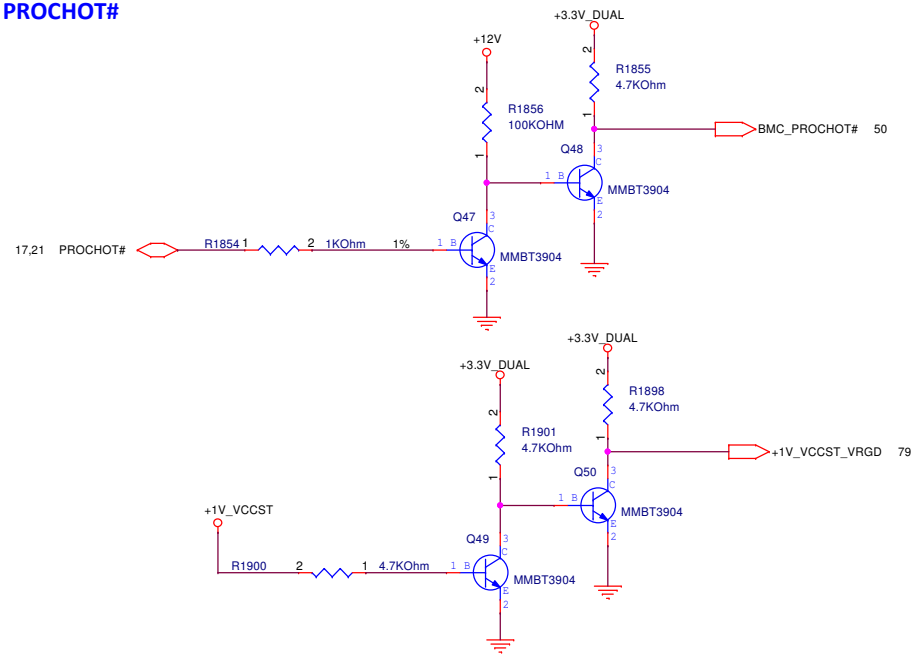
SMLINK0



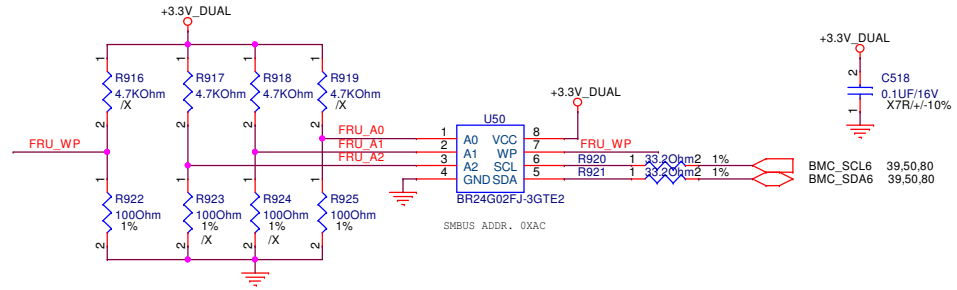
HOST_SMBUS



PROCHOT#



FRU_SMBUS



<Variant Name>

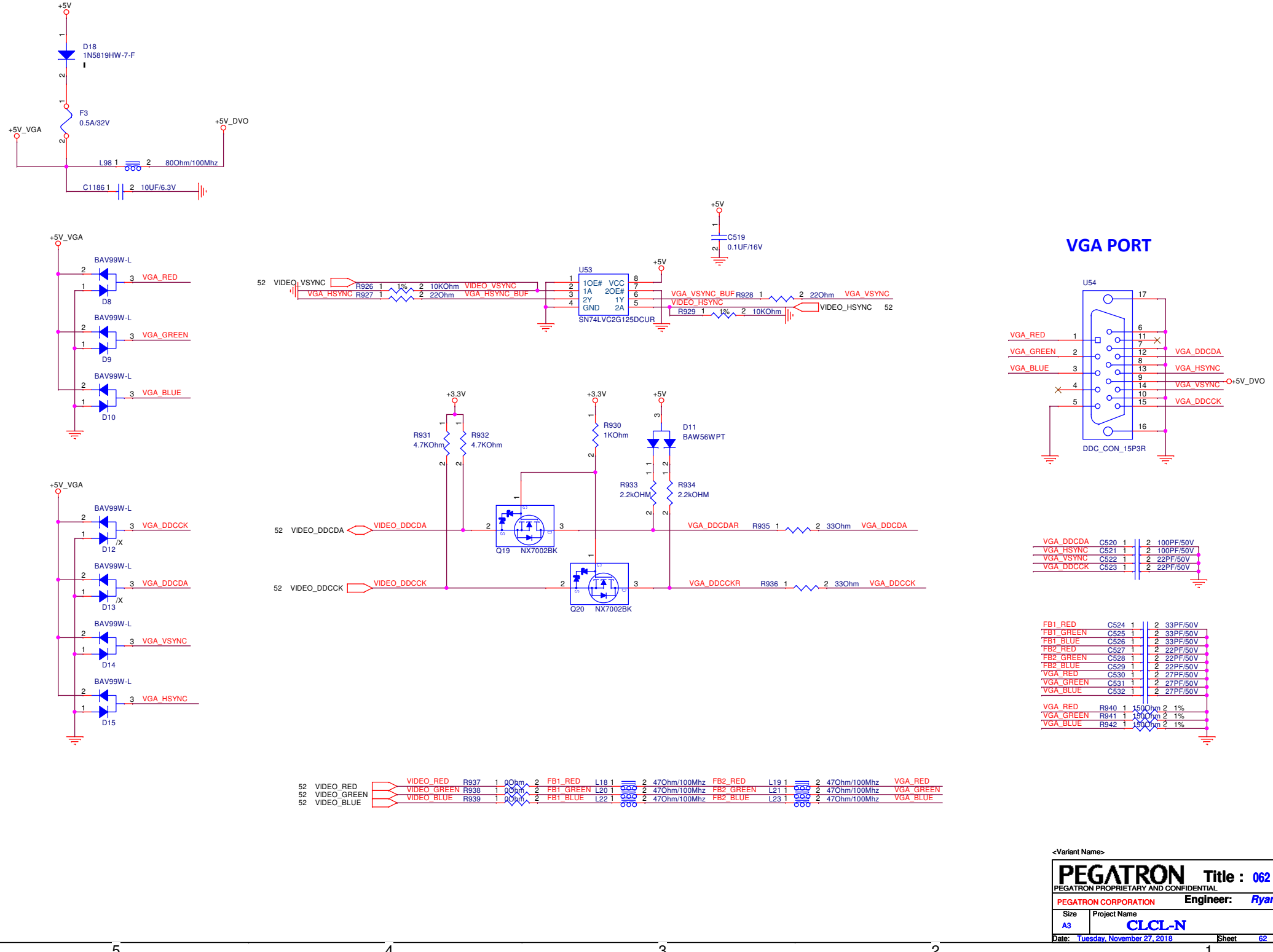
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 061 AST2500 SMBUS
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 61 of 110

VGA PORT



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

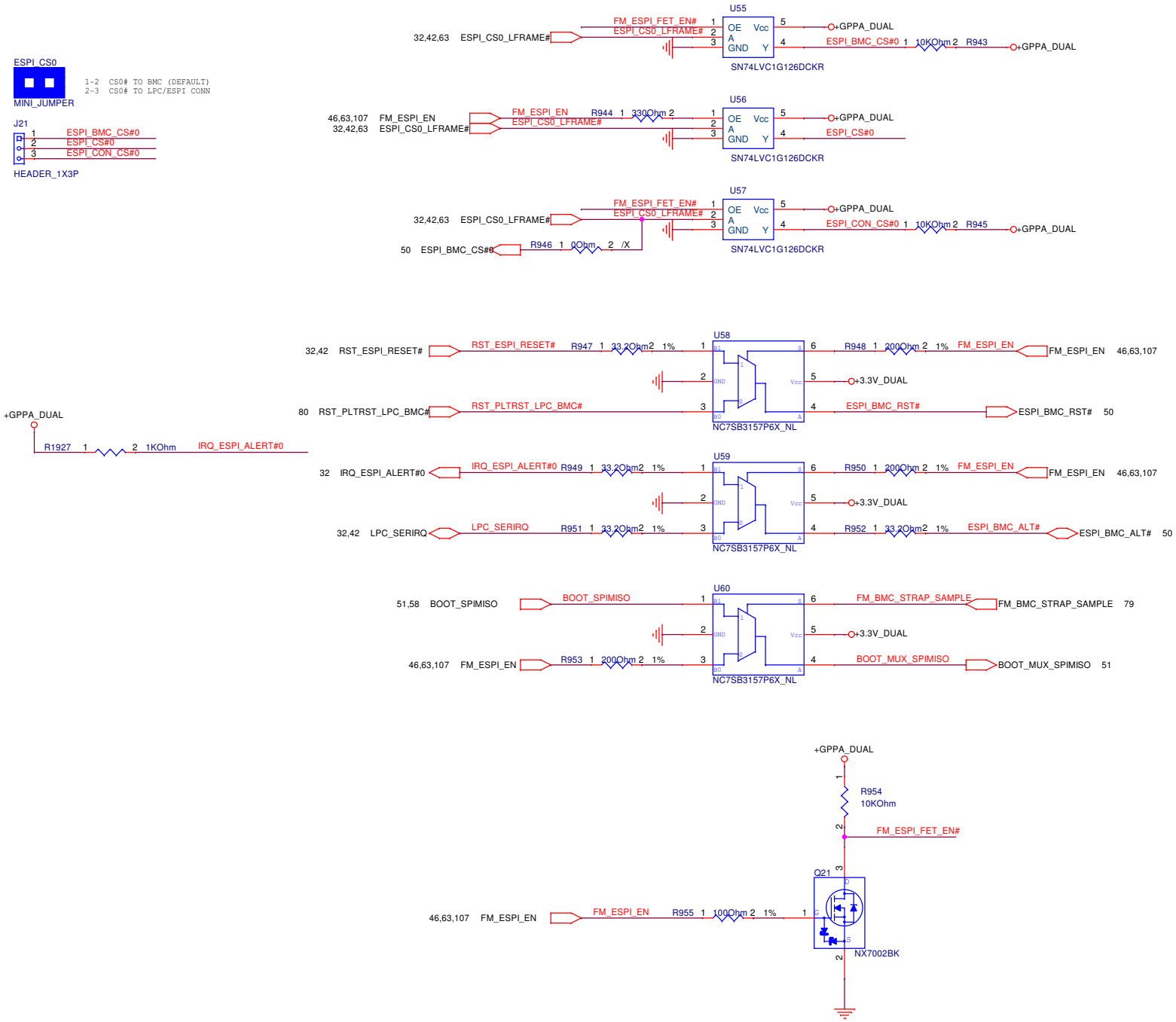
PEGATRON CORPORATION

Title : 062 AST2500 VGA

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 62 of 110



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 063 ESPI

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 63 of 110

PEGATRON PROPRIETARY AND CONFIDENTIAL

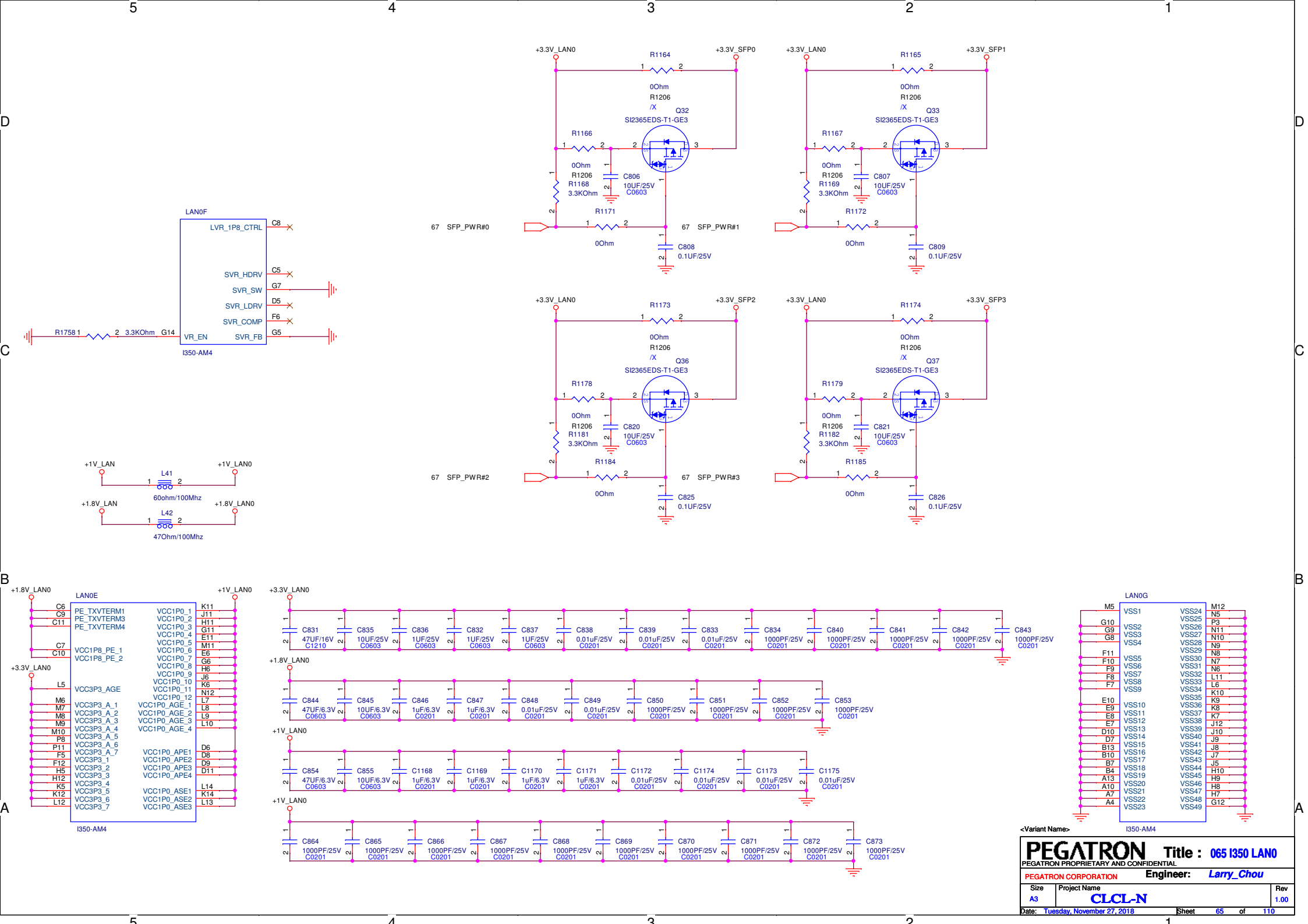
<Variant Name>

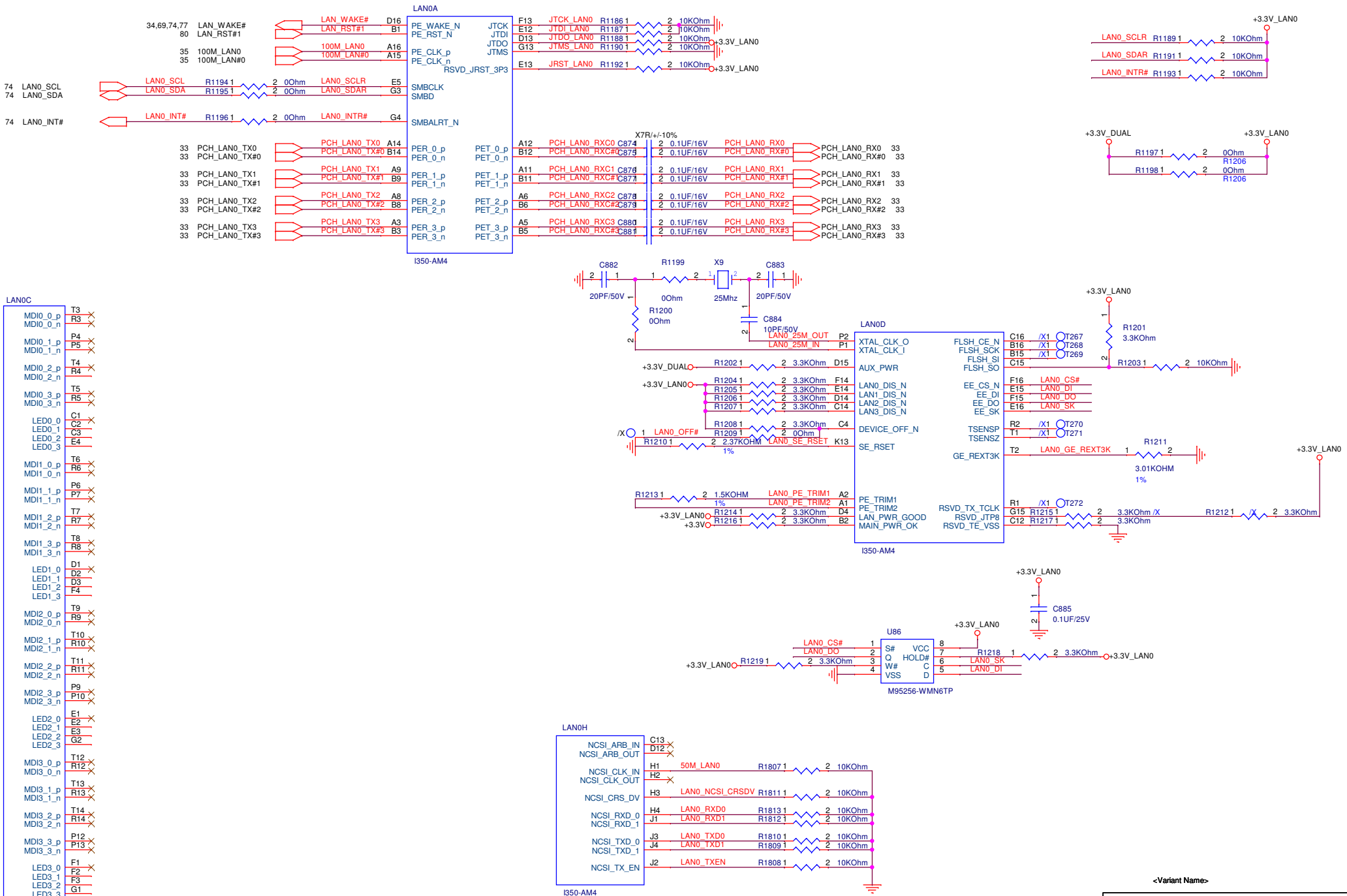
PEGATRON Title : 064 CKMNG

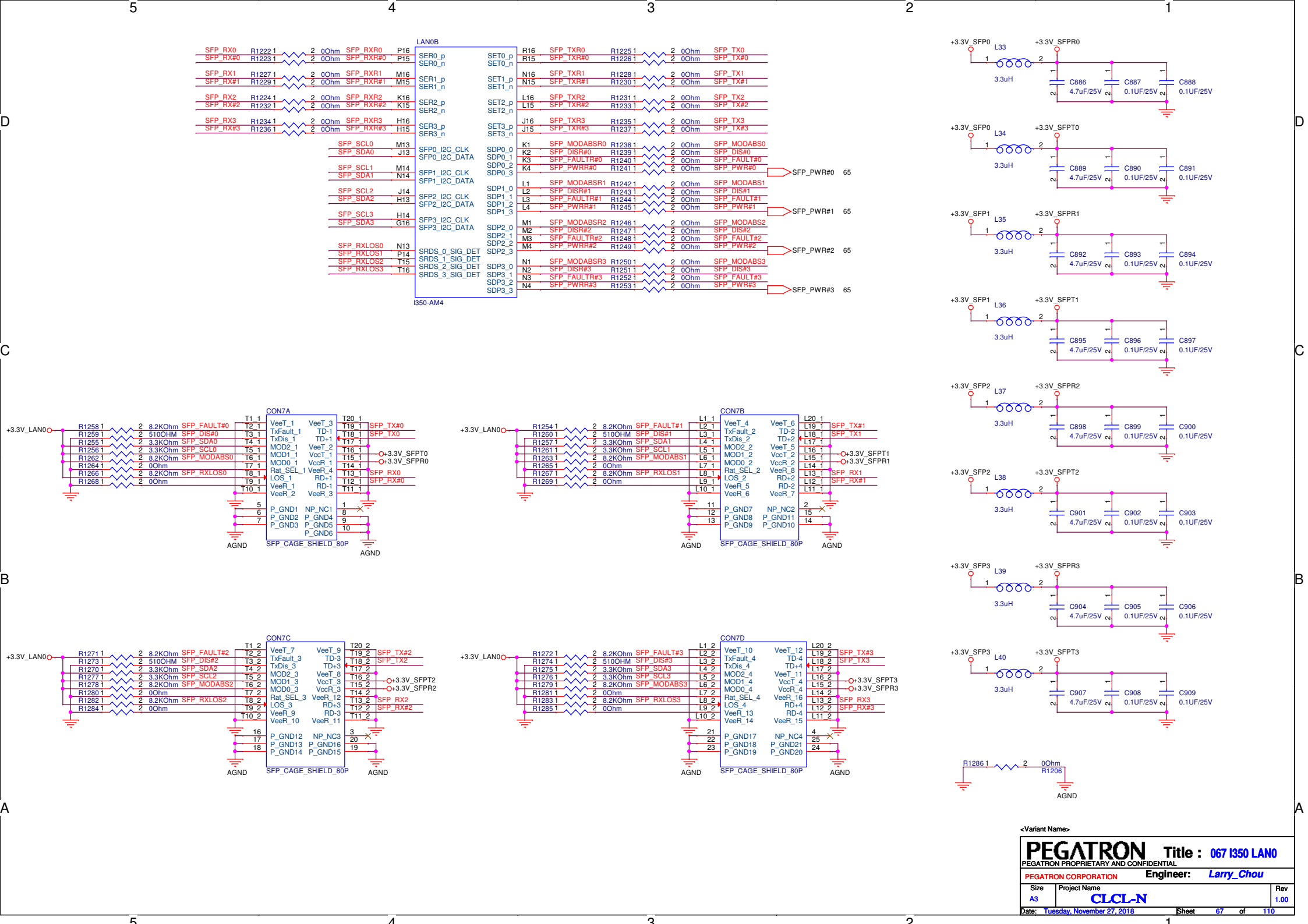
PEGATRON CORPORATION Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 64 of 110


LAN0F
LVR_1P8_CTRL
SVR_HDRV
SVR_SW
SVR_LDRV
SVR_COMP
VR_EN
SVR_FB
I350-AM4
R1758 3.3KOhm
+1V_LAN
+1V_LAN0
L41
60ohm/100Mhz
+1.8V_LAN
+1.8V_LAN0
L42
47Ohm/100Mhz
+3.3V_LAN0
+3.3V_SFP0
R1164
R1206
Q32
SI2365EDS-T1-GE3
R1166
R1168 3.3KOhm
C806 10UF/25V C0603
R1171
C808 0.1UF/25V
67 SFP_PWR#0
67 SFP_PWR#1
+3.3V_SFP1
R1165
Q33
R1167
R1169 3.3KOhm
C807 10UF/25V C0603
R1172
C809 0.1UF/25V
+3.3V_SFP2
R1173
Q36
R1178
R1181 3.3KOhm
C820 10UF/25V C0603
R1184
C825 0.1UF/25V
67 SFP_PWR#2
67 SFP_PWR#3
+3.3V_SFP3
R1174
Q37
R1179
R1182 3.3KOhm
C821 10UF/25V C0603
R1185
C826 0.1UF/25V
0Ohm
/X
LAN0E
I350-AM4
C831 47UF/16V C1210
C835 10UF/25V C0603
C836 1UF/25V C0603
C832 1UF/25V C0603
C837 1UF/25V C0603
C838 0.01uF/25V C0201
C839 0.01uF/25V C0201
C833 0.01uF/25V C0201
C834 1000PF/25V C0201
C840 1000PF/25V C0201
C841 1000PF/25V C0201
C842 1000PF/25V C0201
C843 1000PF/25V C0201
C844 47UF/6.3V C0603
C845 10UF/6.3V C0603
C846 1uF/6.3V C0201
C847 1uF/6.3V C0201
C848 0.01uF/25V C0201
C849 0.01uF/25V C0201
C850 1000PF/25V C0201
C851 1000PF/25V C0201
C852 1000PF/25V C0201
C853 1000PF/25V C0201
C854 47UF/6.3V C0603
C855 10UF/6.3V C0603
C1168 1uF/6.3V C0201
C1169 1uF/6.3V C0201
C1170 1uF/6.3V C0201
C1171 1uF/6.3V C0201
C1172 0.01uF/25V C0201
C1174 0.01uF/25V C0201
C1173 0.01uF/25V C0201
C1175 0.01uF/25V C0201
C864 1000PF/25V C0201
C865 1000PF/25V C0201
C866 1000PF/25V C0201
C867 1000PF/25V C0201
C868 1000PF/25V C0201
C869 1000PF/25V C0201
C870 1000PF/25V C0201
C871 1000PF/25V C0201
C872 1000PF/25V C0201
C873 1000PF/25V C0201
LAN0G
I350-AM4
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 065 I350 LAN0
PEGATRON CORPORATION
Engineer: Larry_Chou
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 65 of 110


LAN0A
LAN0C
LAN0D
LAN0H
I350-AM4
M95256-WMN6TP
U86
X7R/+/-10%
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 066 I350 LAN0
PEGATRON CORPORATION
Engineer: Larry_Chou
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 66 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

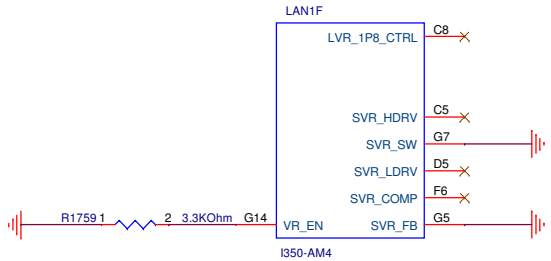
Title : 067 I350 LAN0

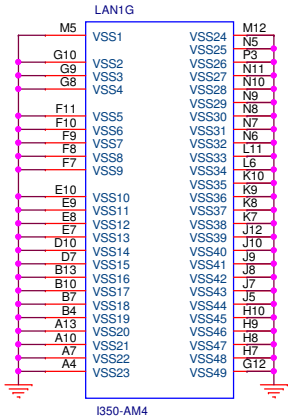
PEGATRON CORPORATION

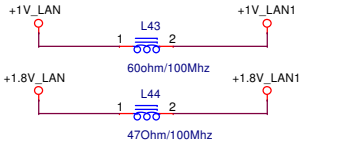
Engineer: Larry_Chou

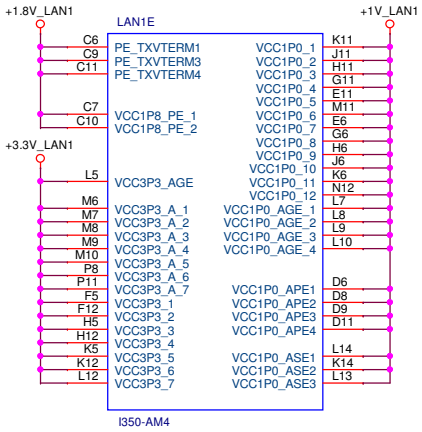
Size	Project Name	Rev
A3	CLCL-N	1.00

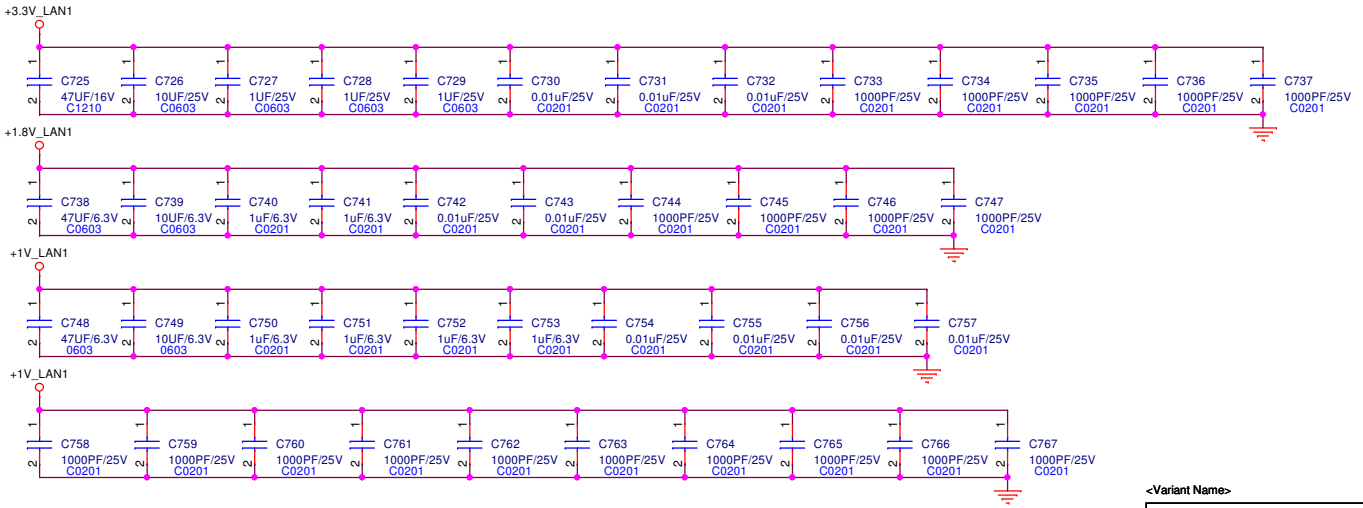
Date: Tuesday, November 27, 2018 Sheet 67 of 110











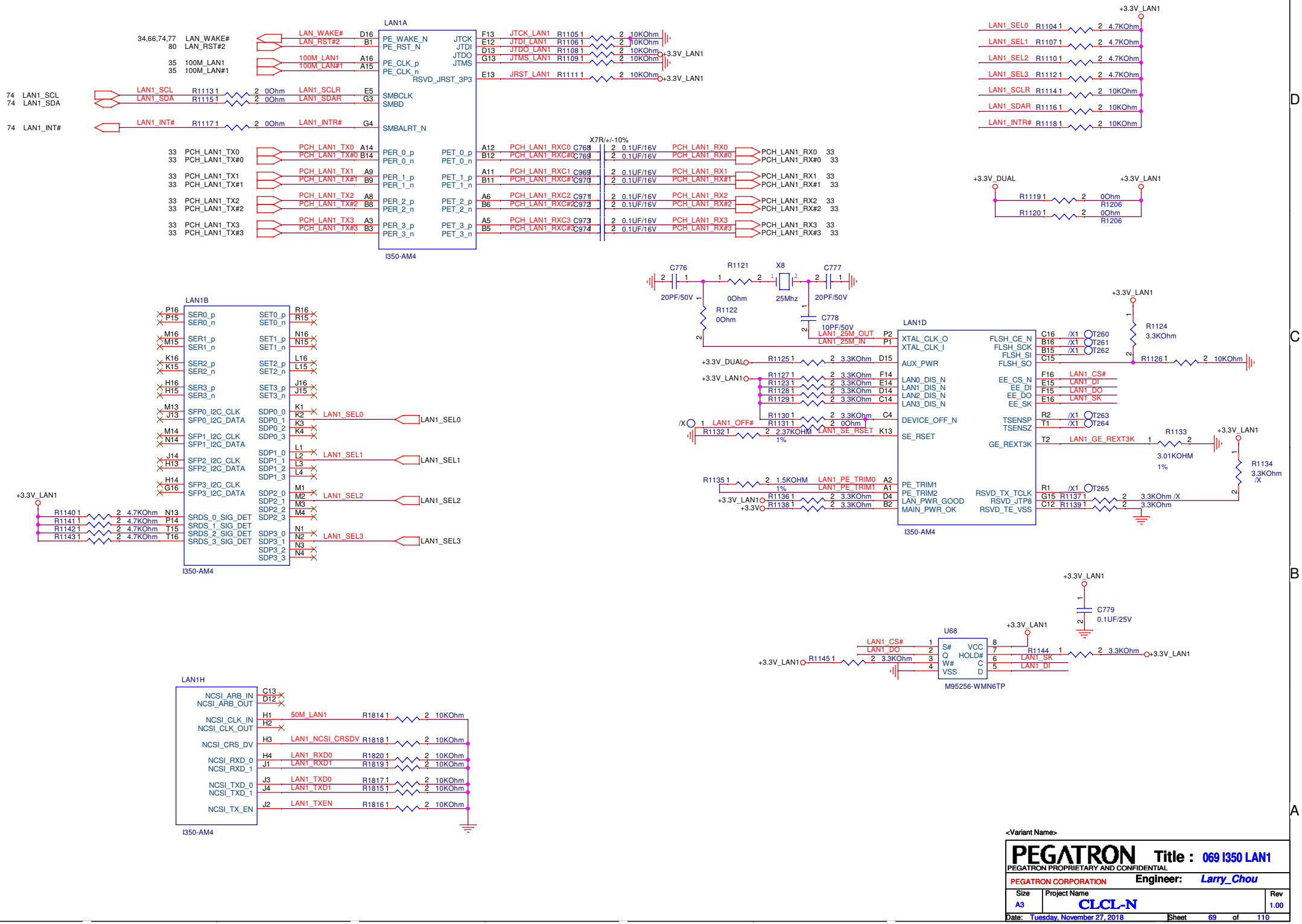
<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 068 I350 LAN1
Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 68 of 110



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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

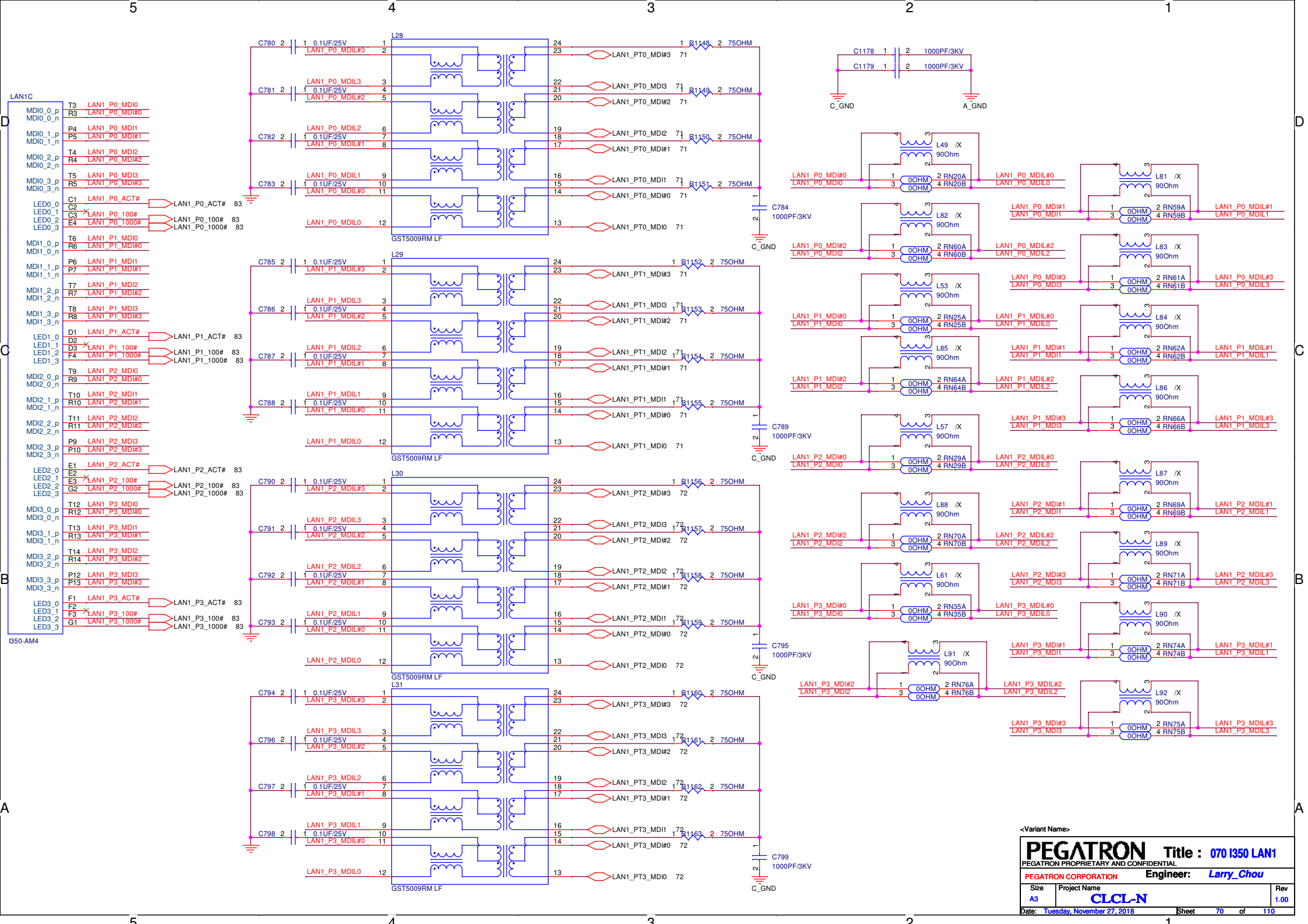
Title : 069 I350 LAN1

PEGATRON CORPORATION

Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 69 of 110



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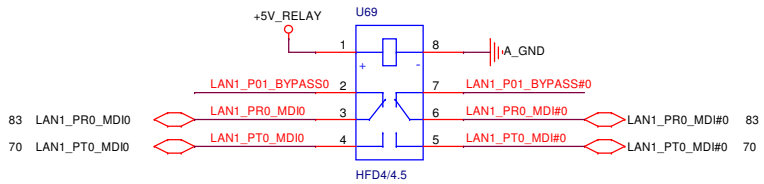
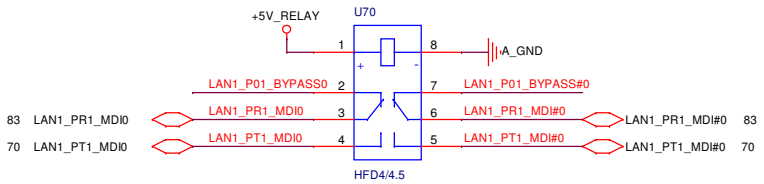
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

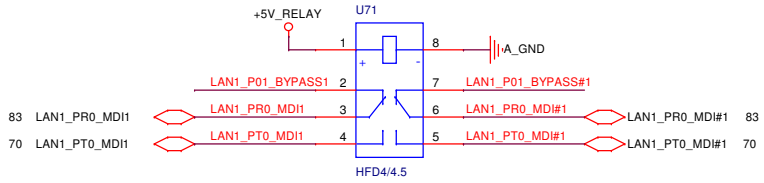
Title : 070 I350 LAN1
Engineer: Larry_Chou

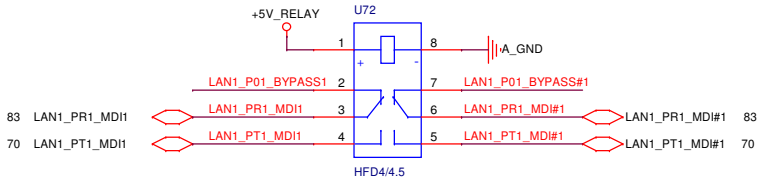
Size	Project Name	Rev
A3	CLCL-N	1.00

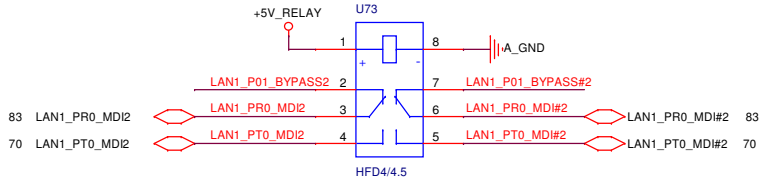
Date: Tuesday, November 27, 2018 Sheet 70 of 110

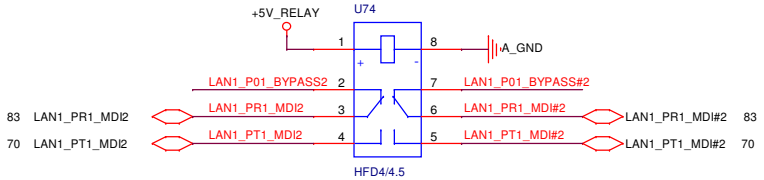


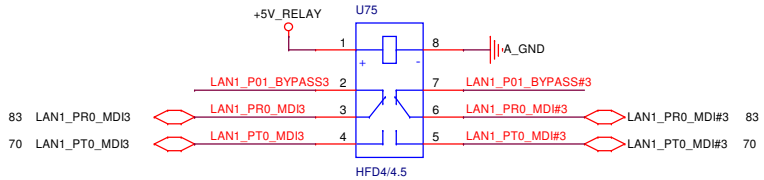


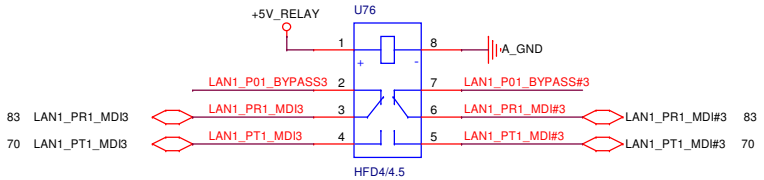












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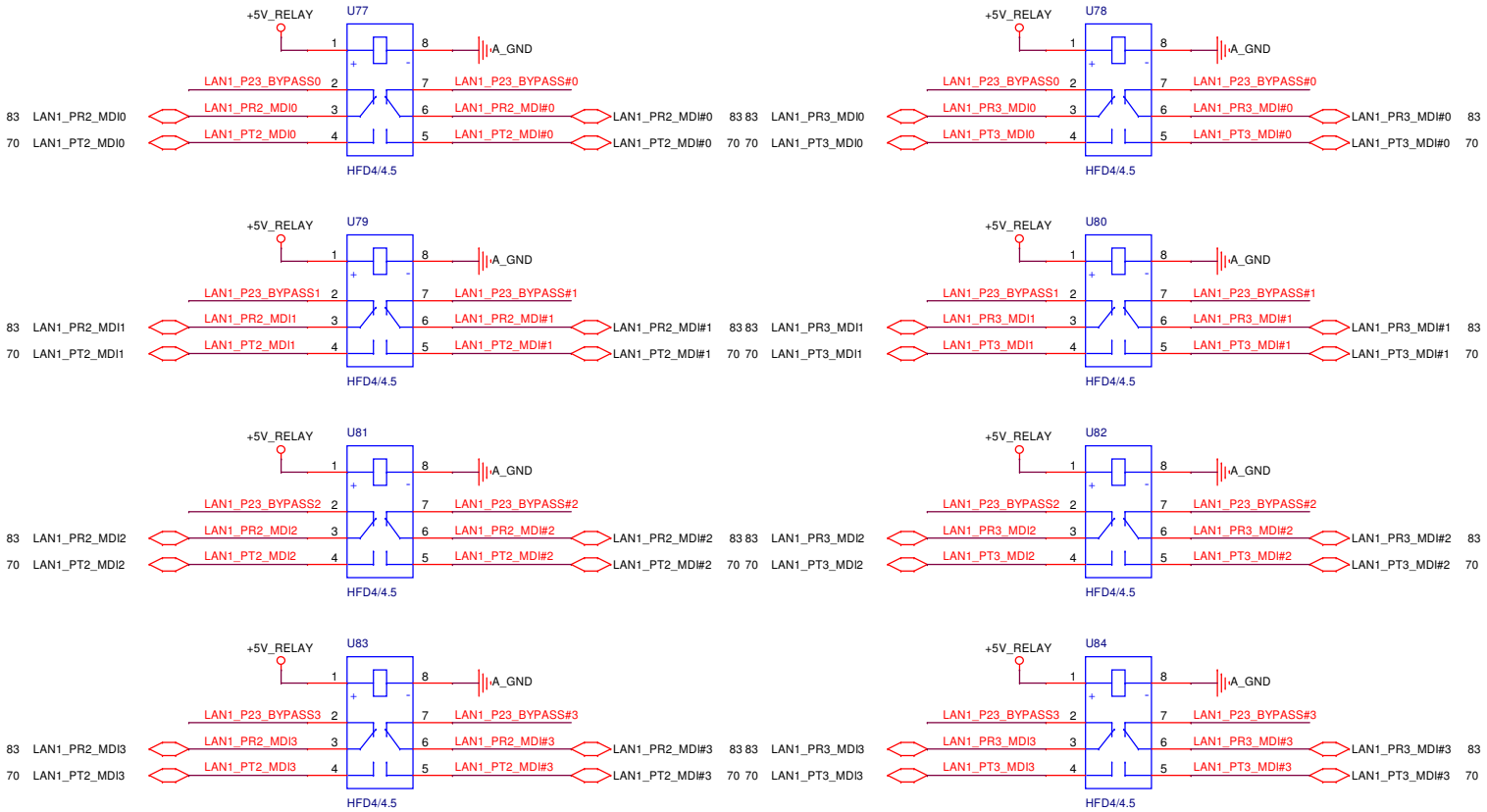
PEGATRON Title : 071 I350 LAN1 BYPAS

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON CORPORATION Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 71 of 110



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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

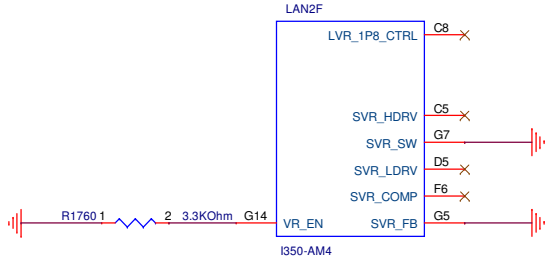
Title : 072.I350.LAN1.BYPAS

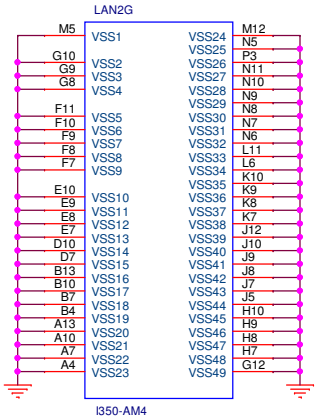
PEGATRON CORPORATION

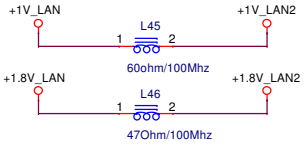
Engineer: Larry_Chou

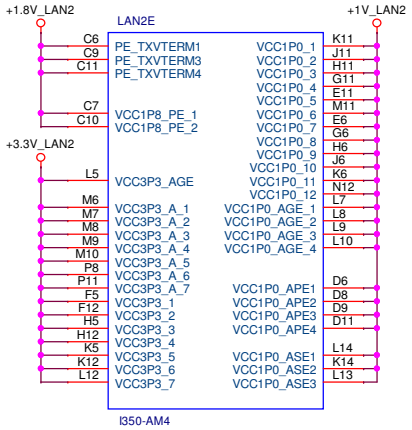
Size	Project Name	Rev
A3	CLCL-N	1.00

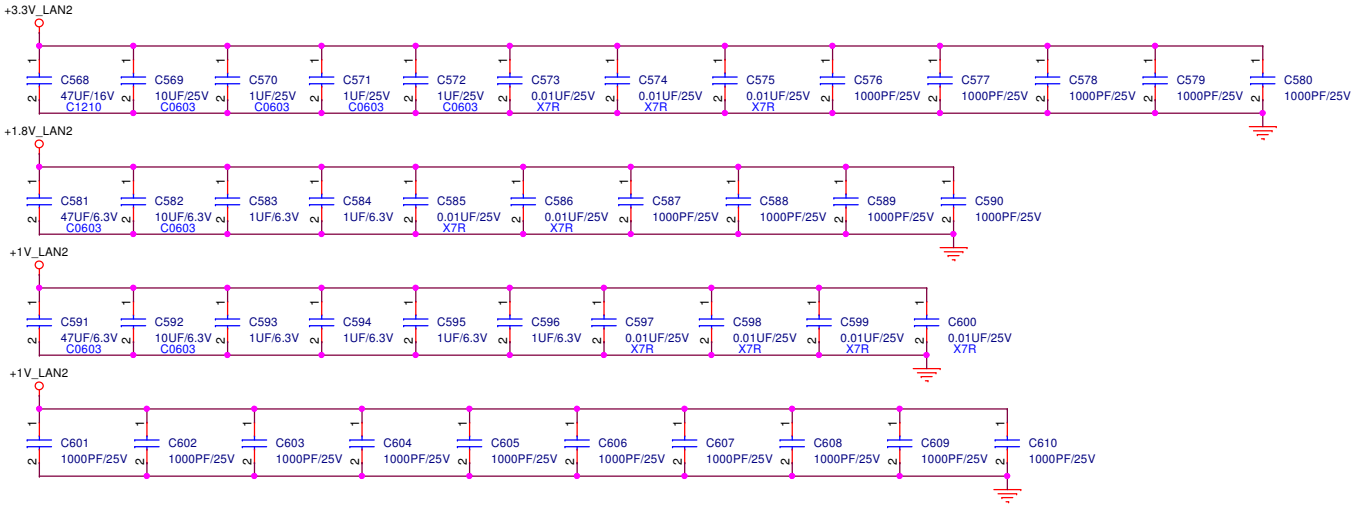
Date: Tuesday, November 27, 2018 Sheet 72 of 110











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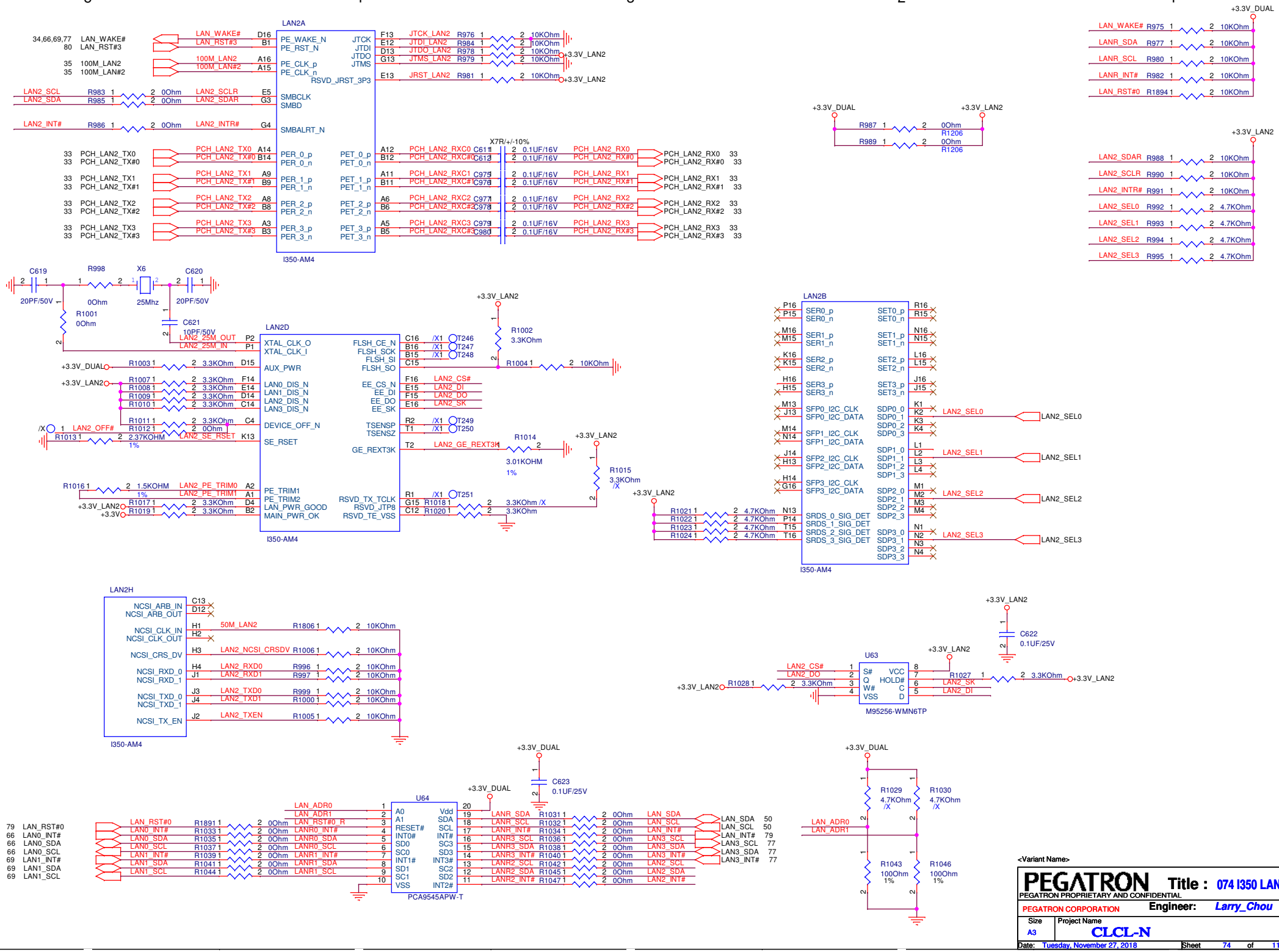
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 073 I350 LAN2
Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 73 of 110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I350-AM4
LAN2D
I350-AM4
LAN2B
I350-AM4
LAN2H
I350-AM4
U63
M95256-WMN6TP
U64
PCA9545APW-T
X7R/+/-10%
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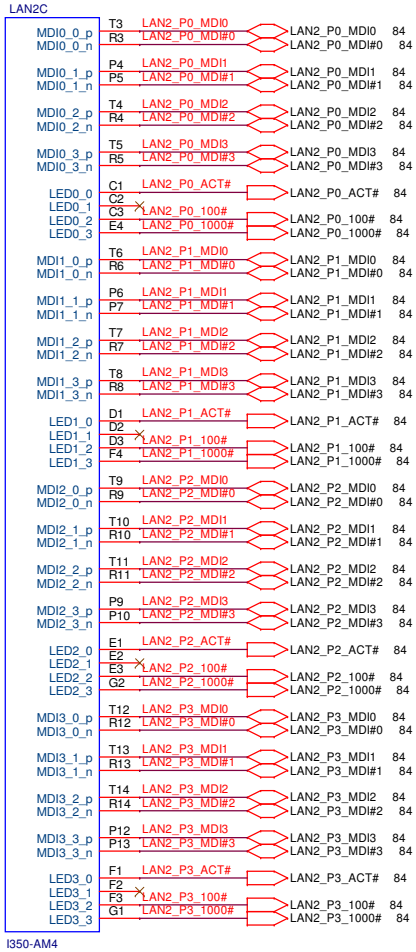
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 074 I350 LAN2
PEGATRON CORPORATION
Engineer: Larry_Chou
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 74 of 110



<Variant Name>

PEGATRON

Title : 075 I350 LAN2

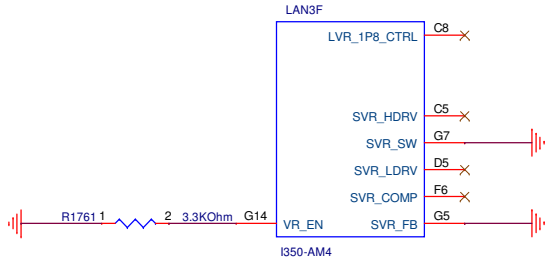
PEGATRON PROPRIETARY AND CONFIDENTIAL

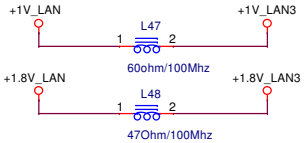
PEGATRON CORPORATION

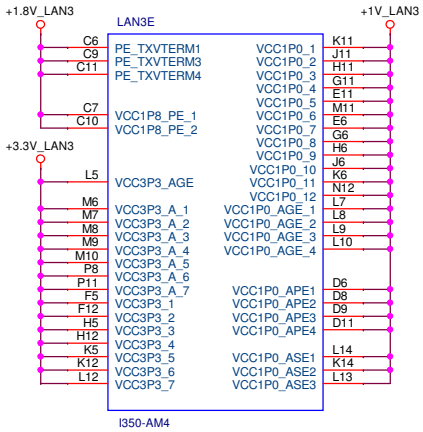
Engineer: Larry_Chou

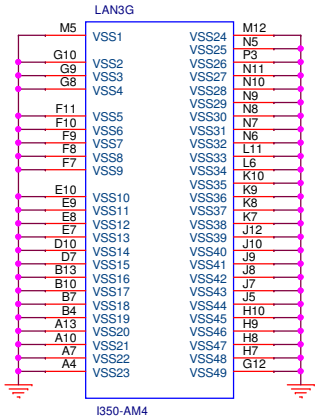
Size	Project Name	Rev
A3	CLCL-N	1.00

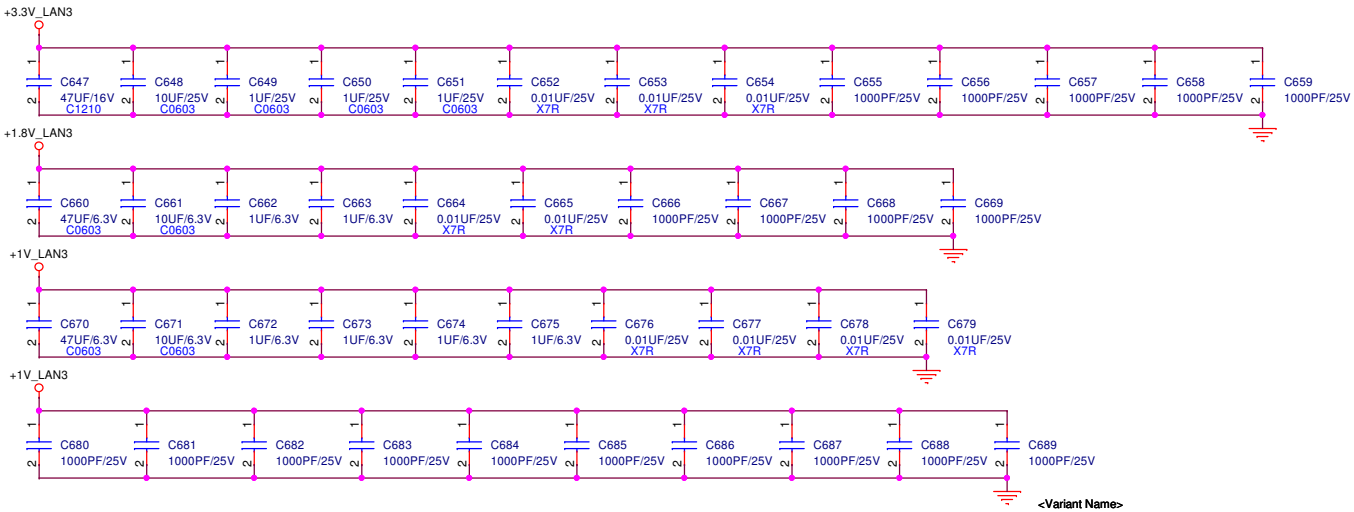
Date: Tuesday, November 27, 2018 Sheet 75 of 110











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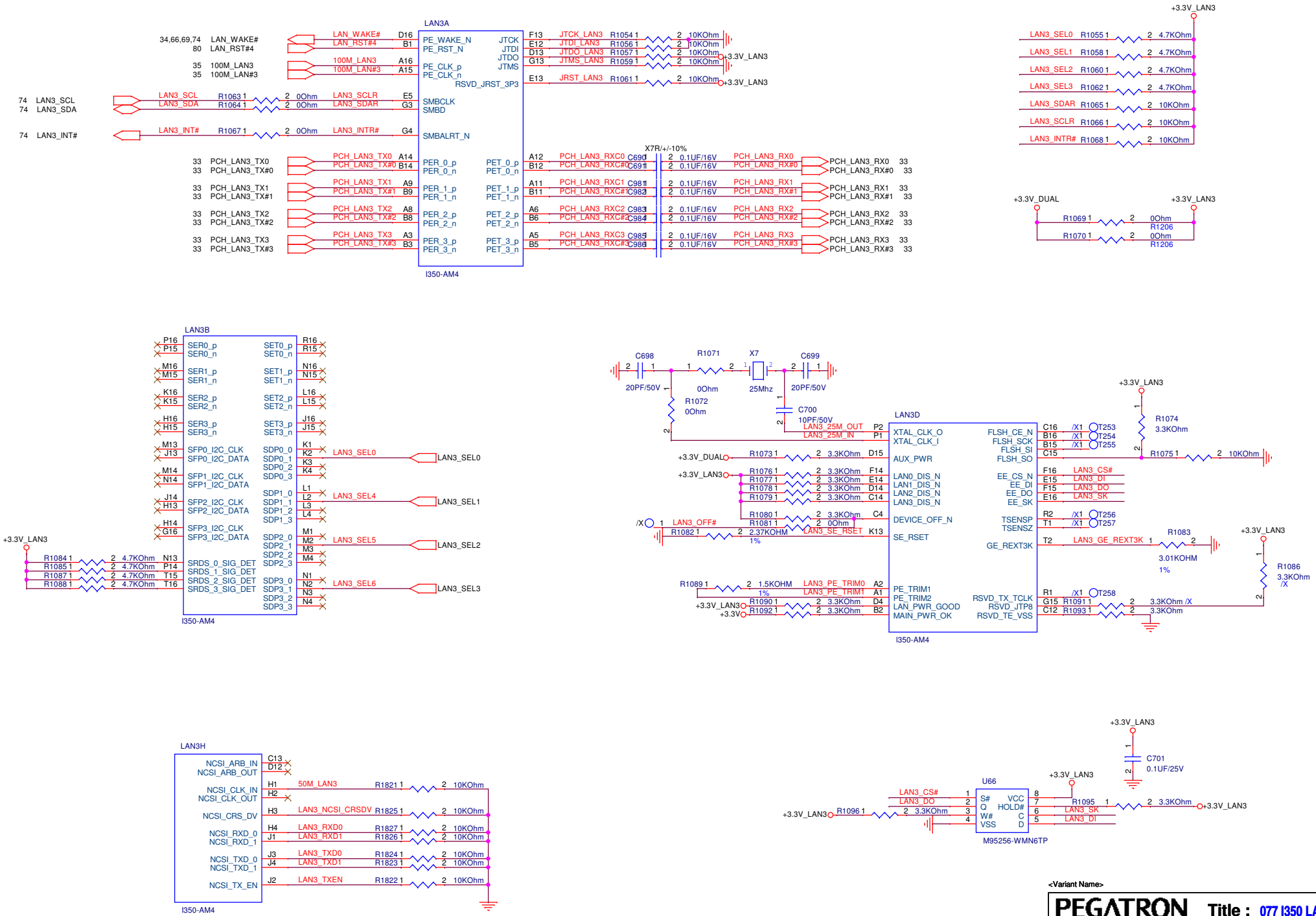
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 076 I350 LAN3
Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 76 of 110



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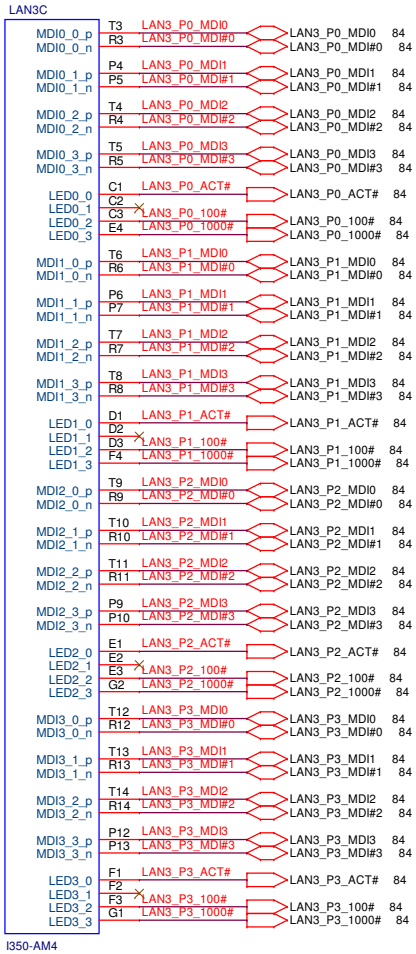
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION

Title : 077 I350 LAN3
Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 77 of 110



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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 078 I350 LAN3

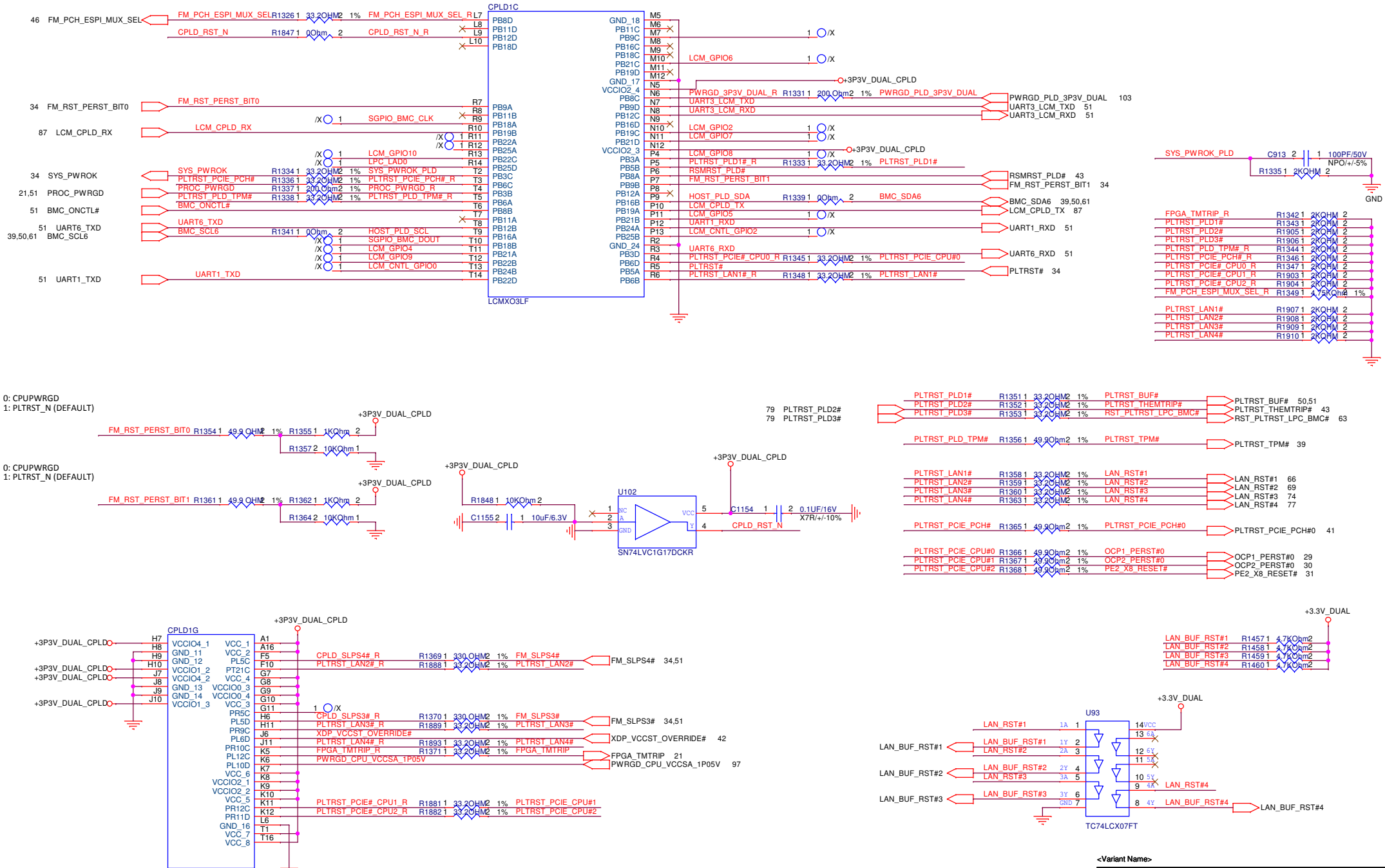
PEGATRON CORPORATION

Engineer: Larry_Chou

Size	Project Name	Rev
A3	CLCL-N	1.00

Date: Tuesday, November 27, 2018 Sheet 78 of 110

CPLD1B
LCMXO3LF
BMC_RDY
PWRGD_MEM_1P2V
CPU_1P05V_VCCSA_EN
MEM_1P2V_VDDQ_EN
PWRGD_CPU_VCCIO_1P0V
CPU_1P0V_VCCIO_EN
PWRGD_CPU_VCORE_R
CPU_VCORE_EN
TMTRIP#
FM_BMC_STRAP_SAMPLE
FM_PWRBRK_N
FM_THROTTLE_BMC_N
MEM_EVENT#
FM_THROTTLE_IN_N
FM_NM_THROTTLE#
FM_PMBUS_ALERT_EN
FM_CPLD_THERMTRIP#
+VRM_HOT_N
FPGA_PROCHOT
LAN_INT#
LAN_RST#0
+3P3V_DUAL_CPLD
PCH_1P05V_DUAL_EN
BMC_1P2V_DUAL_EN
PWRGD_PCH_1P05V_DUAL
PWRGD_PCH_GPPA_DUAL
PWRGD_BMC_1P2V_DUAL
PCH_GPPA_DUAL_EN
BMC_1P15V_DUAL_EN
BMC_2P5V_DUAL_EN
PWRGD_BMC_2P5V_DUAL
REAR_PWR_BTN#
PWRGD_BMC_1P15V_DUAL
RSMRST_PLD#_R
RSTI_SRST_PLD#
SLP_SUS#
P1_SKTOCC#_R
P1_SEL#
PSU_PWROK_R
FM_PSU_EN_R
FM_CPLD_PWRBTN#
VCCST_PWRGD#
MEM_2P5V_VPP_EN
PWROK_PCH_R
FM_VCCST_EN_R
PWRGD_MEM_2P5V
SMBUS_CPLD_REG_ALERT_N
FM_SMART_THROTTLE_R
PWRGD_CPU_VCORE_R
PWRGD_CPU_VCORE
PCH_GPPA_DUAL_EN
PCH_1P05V_DUAL_EN
BMC_2P5V_DUAL_EN
BMC_1P2V_DUAL_EN
BMC_1P15V_DUAL_EN
RSMRST_PLD#_R
FM_VCCST_EN_R
MEM_2P5V_VPP_EN
MEM_1P2V_VDDQ_EN
FM_SMART_THROTTLE_R
CPU_1P05V_VCCSA_EN
CPU_VCORE_EN
FM_PSU_EN_R
PLD_JTAG_TCK
PLD_JTAG_TDO_R
PLD_JTAG_TDI_R
PROGRAMN
PLD_JTAG_TMS_R
VCCST_PWRGD#
RST_SRST_PLD#
PWRGD_CPU_VCORE
C910
0.01UF/50V /X
FPGA_PROCHOT
PWROK_PCH_R
C911
C912
100PF/50V
NPO/+/-5%
R1318
R1319
2KOHM
CPLD1A
LCMXO3LF
OCP2_LD#
OCP2_DATA_IN
OCP2_DATA_OUT
PLD_JTAG_TDI
PLD_JTAG_TCK
OCP1_DATA_IN
BMC_SCL7
OCP1_SCAN_CLK
OCP1_LD#
OCP2_SCAN_CLK
OCP1_DATA_OUT
+1V_VCCST_VRGD
OCP1_PWRBRK#
OCP2_PWRBRK#
SW1_RSVD8
SW1_RSVD5
CPLD_ALL_VR_ENABLE
SW1_RSVD4
SW1_RSVD6
PROGRAMN
SW1_RSVD7
PLD_JTAG_TMS
FAN_TACH0
FAN_TACH1
FAN_TACH2
FAN_PWM0
FAN_PWM1
PLD_JTAG_TDO
FAN_PWM3
FAN_PWM2
BMC_SDA7
PLD_JTAG_JTAGEN
MEM_0P6V_VTT_EN
+3P3V_DUAL_CPLD_PG
+3P3V_DUAL_CPLD_EN
PWRGD_1V_LAN
+3P3V_DUAL_EN
+1P8V_LAN_PWRGD
+1P8V_LAN_CPLD_PWRGD
PLTRST_PLD2#_R
PLTRST_PLD3#_R
PLTRST_PLD2#
PLTRST_PLD3#
BMC_CPLD_SPARE0
BMC_CPLD_SPARE1
BMC_CPLD_SPARE2
BMC_CPLD_SPARE3
+5V_DUAL
R1317
22.1KOhm
1%
FM_PSU_ON#
Q38
NX7002BK
FM_PSU_EN
R1323
10KOhm
+3.3V_DUAL
HOST_BMC_UART_SEL
HOST_SOL_UART_SEL
SW1
SWITCH_16P
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON CORPORATION
Title : 079 CPLD-1
Engineer: Tom_Liao
Size A3
Project Name CLCL-N
Rev 1.00
Date: Tuesday, November 27, 2018
Sheet 79 of 110



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

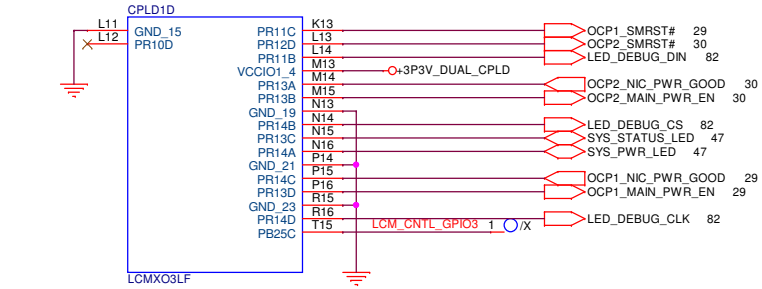
Title : 080 CPLD-2

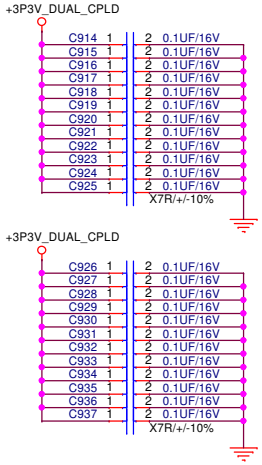
PEGATRON CORPORATION

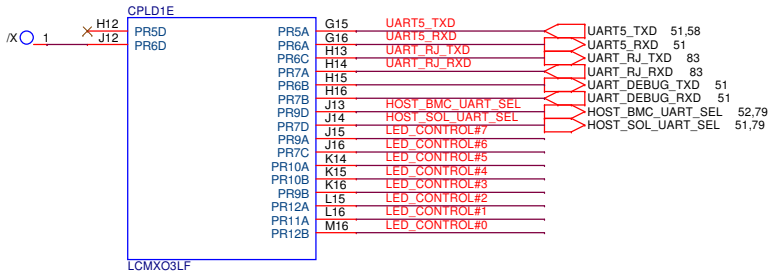
Engineer: Tom_Liao

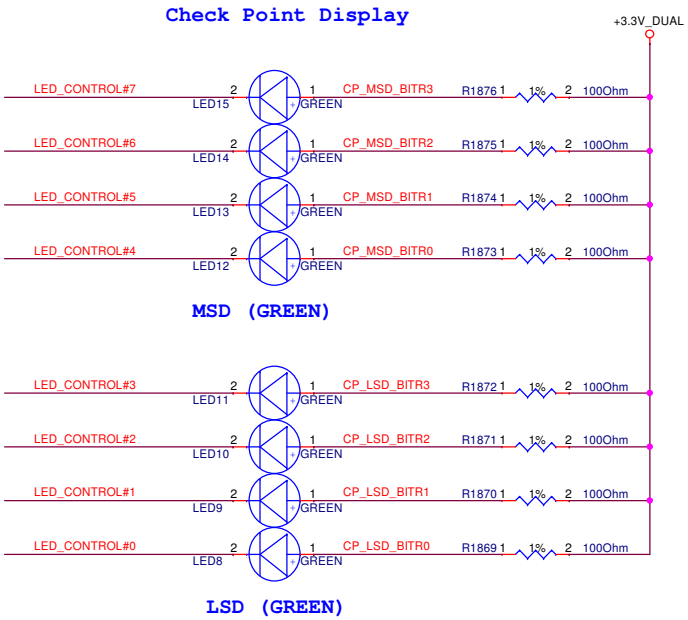
Size	Project Name	Rev
A3	CLCL-N	1.00

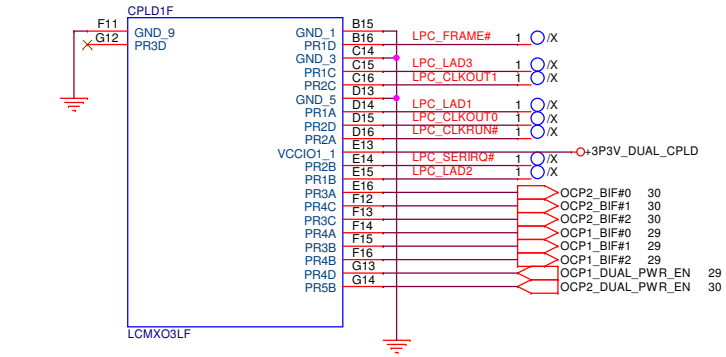
Date: Tuesday, November 27, 2018 Sheet 80 of 110











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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 081 CPLD-3
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	CLCL-N	1.00

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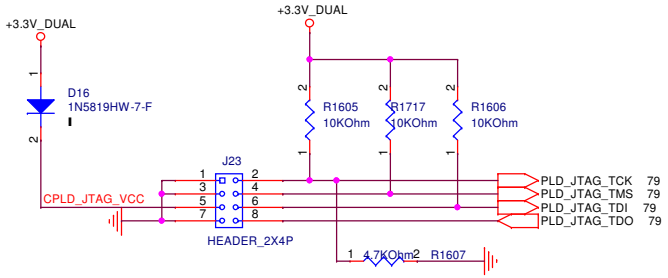
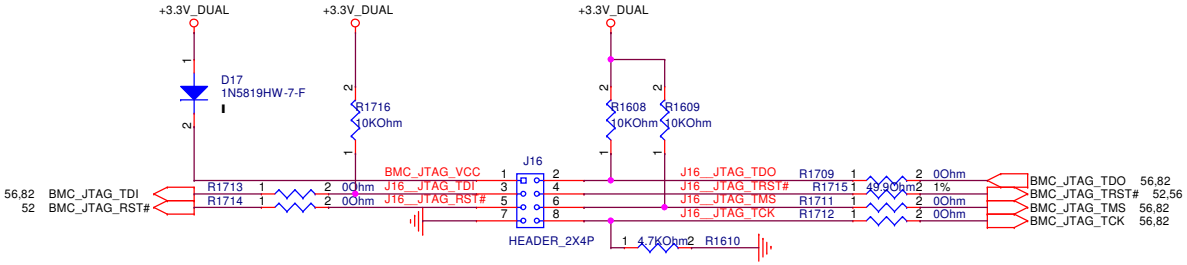
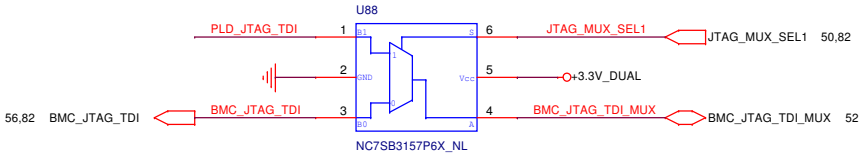
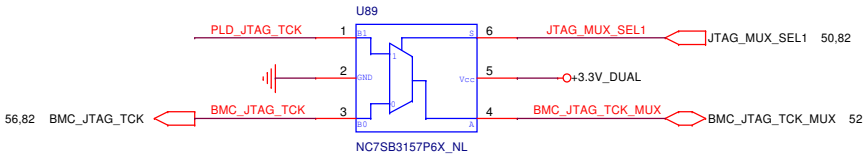
JTAG HEADER-CPLD

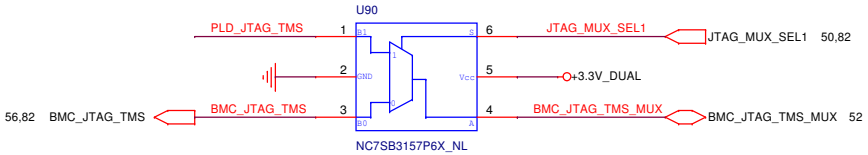


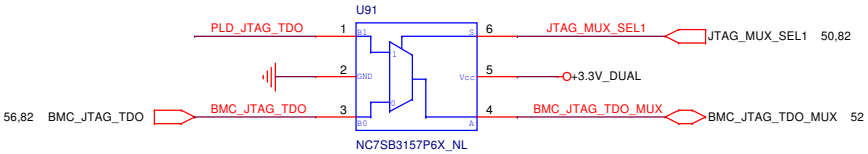
JTAG HEADER-BMC

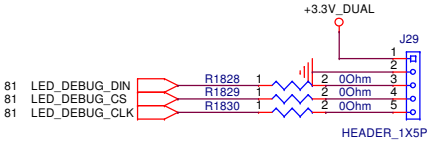


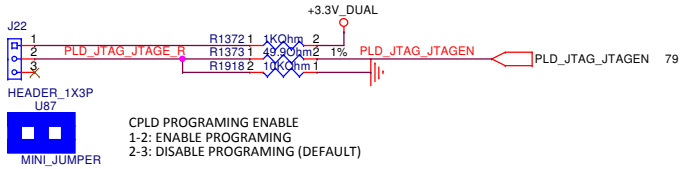












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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : 082 JTAG MUX
PEGATRON CORPORATION
Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

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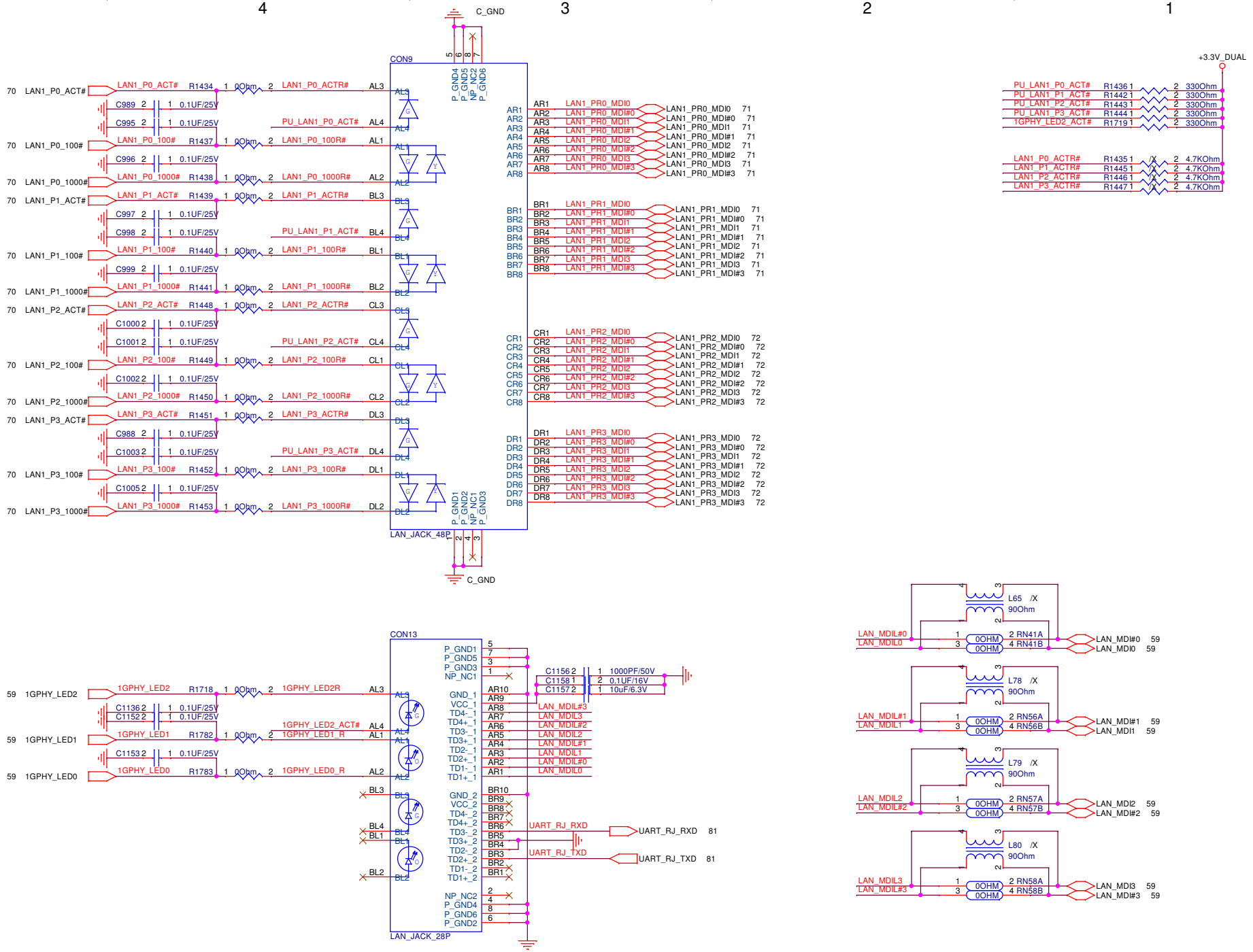

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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

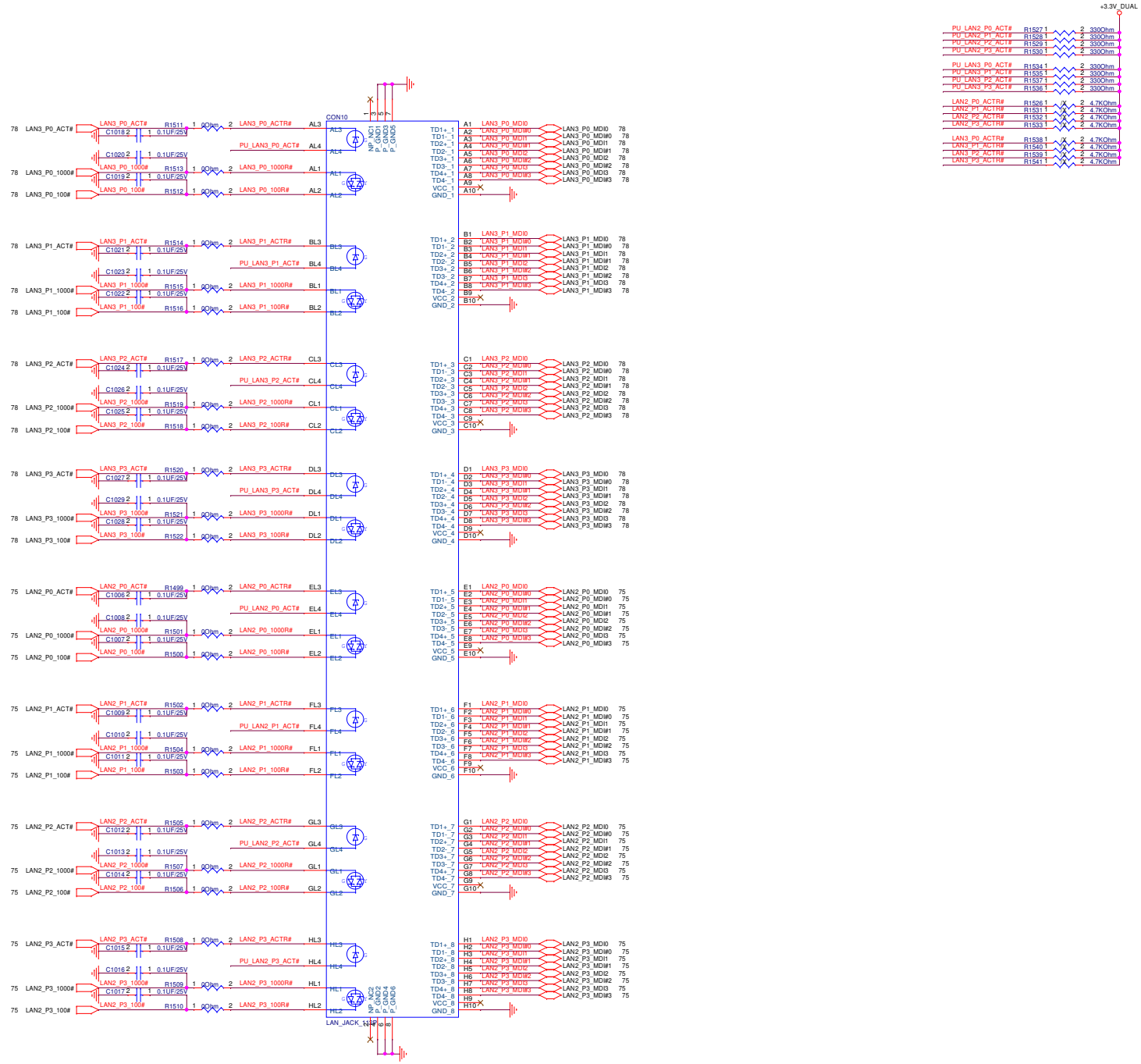
Title : 083 2x1,2x2 RJ45

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

Date: Tuesday, November 27, 2018 Sheet 83 of 110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CON10
LAN_JACK_16P
LAN3_P0_ACT#
LAN3_P0_1000#
LAN3_P0_100#
LAN3_P1_ACT#
LAN3_P1_1000#
LAN3_P1_100#
LAN3_P2_ACT#
LAN3_P2_1000#
LAN3_P2_100#
LAN3_P3_ACT#
LAN3_P3_1000#
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LAN2_P0_ACT#
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LAN2_P1_ACT#
LAN2_P1_1000#
LAN2_P1_100#
LAN2_P2_ACT#
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LAN2_P2_100#
LAN2_P3_ACT#
LAN2_P3_1000#
LAN2_P3_100#
PU_LAN3_P0_ACT#
PU_LAN3_P1_ACT#
PU_LAN3_P2_ACT#
PU_LAN3_P3_ACT#
PU_LAN2_P0_ACT#
PU_LAN2_P1_ACT#
PU_LAN2_P2_ACT#
PU_LAN2_P3_ACT#
LAN3_P0_MDI0
LAN3_P1_MDI0
LAN3_P2_MDI0
LAN3_P3_MDI0
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LAN2_P1_MDI0
LAN2_P2_MDI0
LAN2_P3_MDI0
330Ohm
4.7KOhm

<variant_name><Variant Name></variant_name>

PEGATRON

Title : <Title>

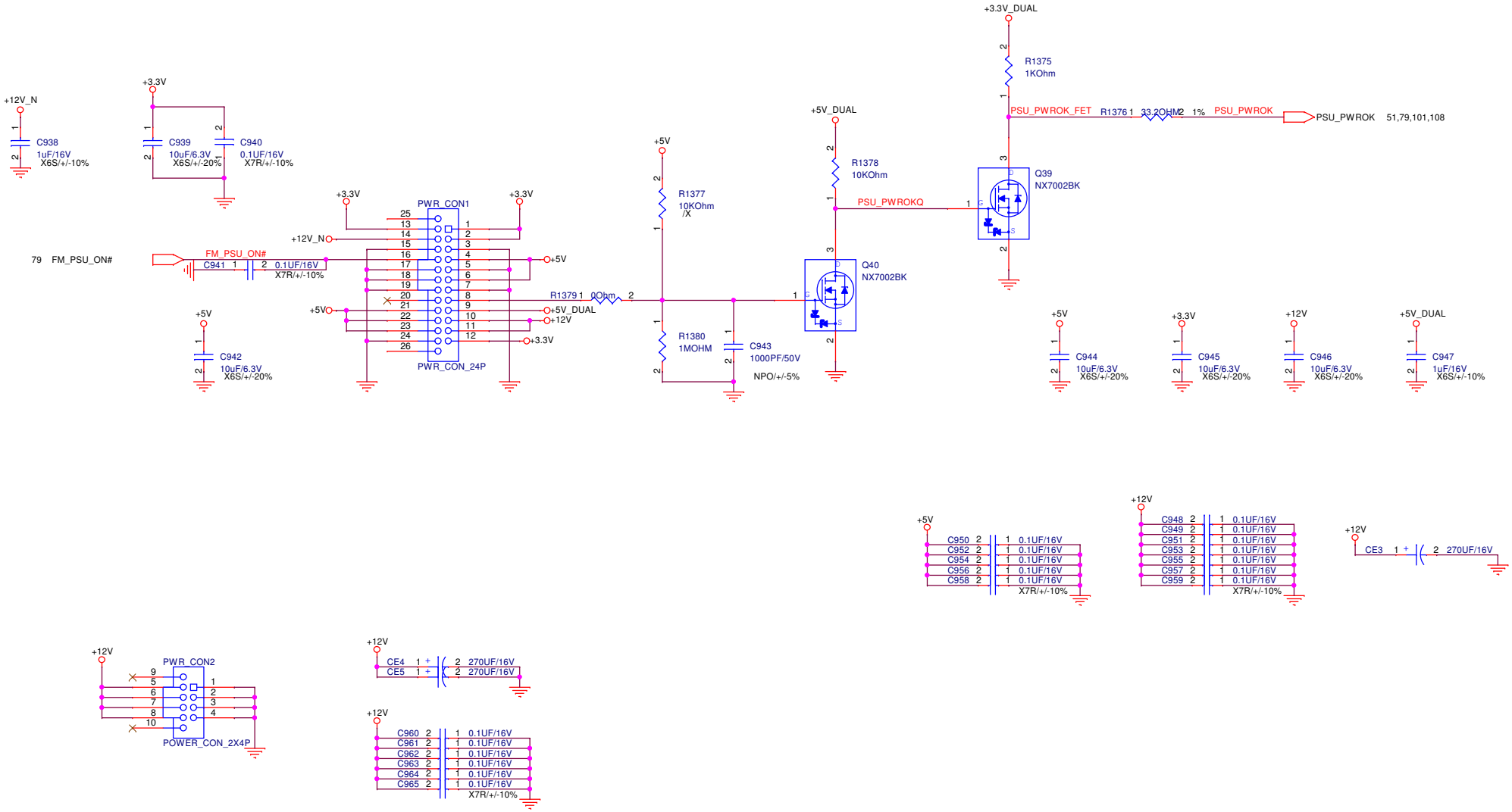
PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

Date: Tuesday, November 27, 2018 Sheet 85 of 110



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PEGATRON PROPRIETARY AND CONFIDENTIAL

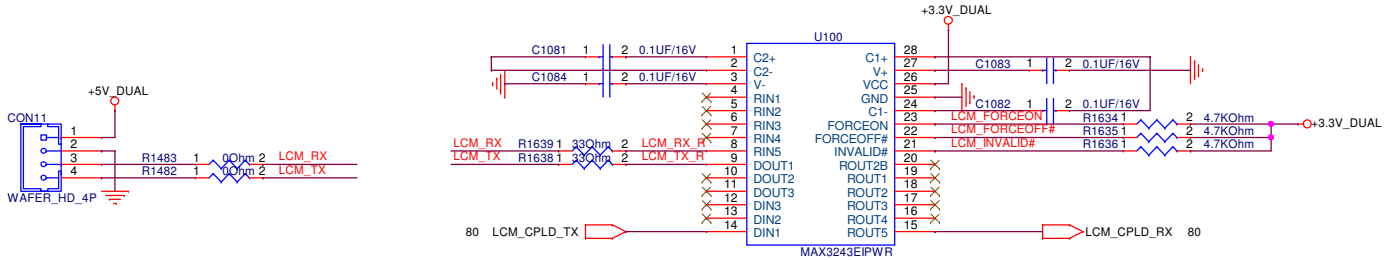
Title : 086 PWR CONN

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

Date: Tuesday, November 27, 2018 Sheet 86 of 110



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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 087 LCM OTHER

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

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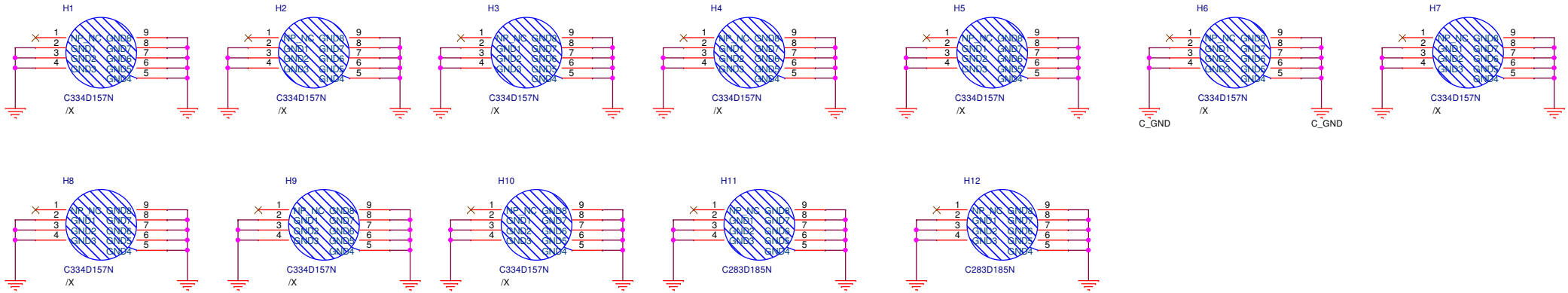
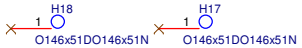


SSD Nut

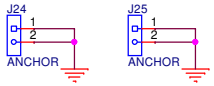
WIFI Nut

RF shielding Nut

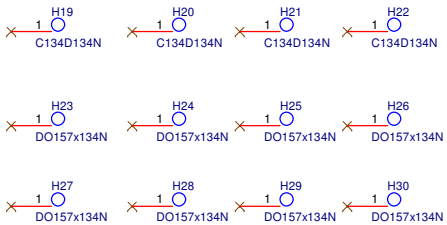
WIFI HOLE



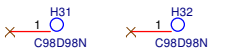
CLIP



TOOLING HOLE FOR GUIDE RAIL



VCORE HEAT SINK SCREWS



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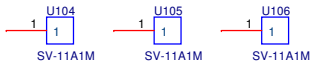
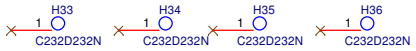
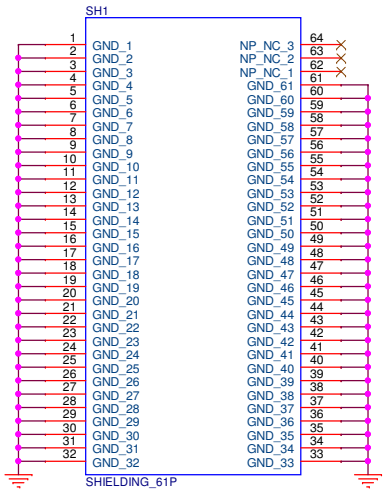


CPU HEATSINK SCREWS



SSD shielding



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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 088 MECH

PEGATRON CORPORATION

Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

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PEGATRON PROPRIETARY AND CONFIDENTIAL

<Variant Name>

PEGATRON Title : <Title>

PEGATRON CORPORATION Engineer: Ryan2_Wang

Size	Project Name	Rev
A3	<Doc>	1.00

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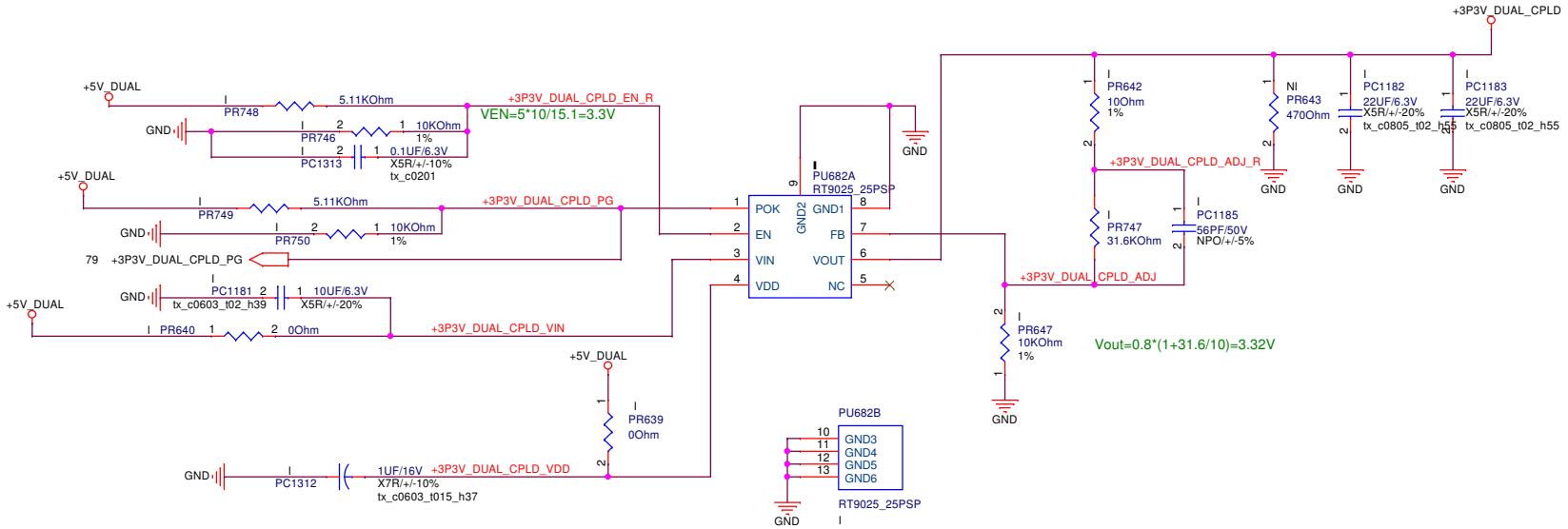
Power Rail : +3P3V_DUAL_CPLD
MAX = 0.2A
OCP = 3.5A
Max step = --
DI/DT = --
Pd = 0.34W
ThetaJA = 75°C/W
Tj = 0.4*75+40 = 65 °C < 125 °C



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : +3P3V_DUAL_CPLD

PEGATRON CORPORATION

Engineer: Gary_Chang

Size	Project Name	Rev
A3	<Doc>	1.00

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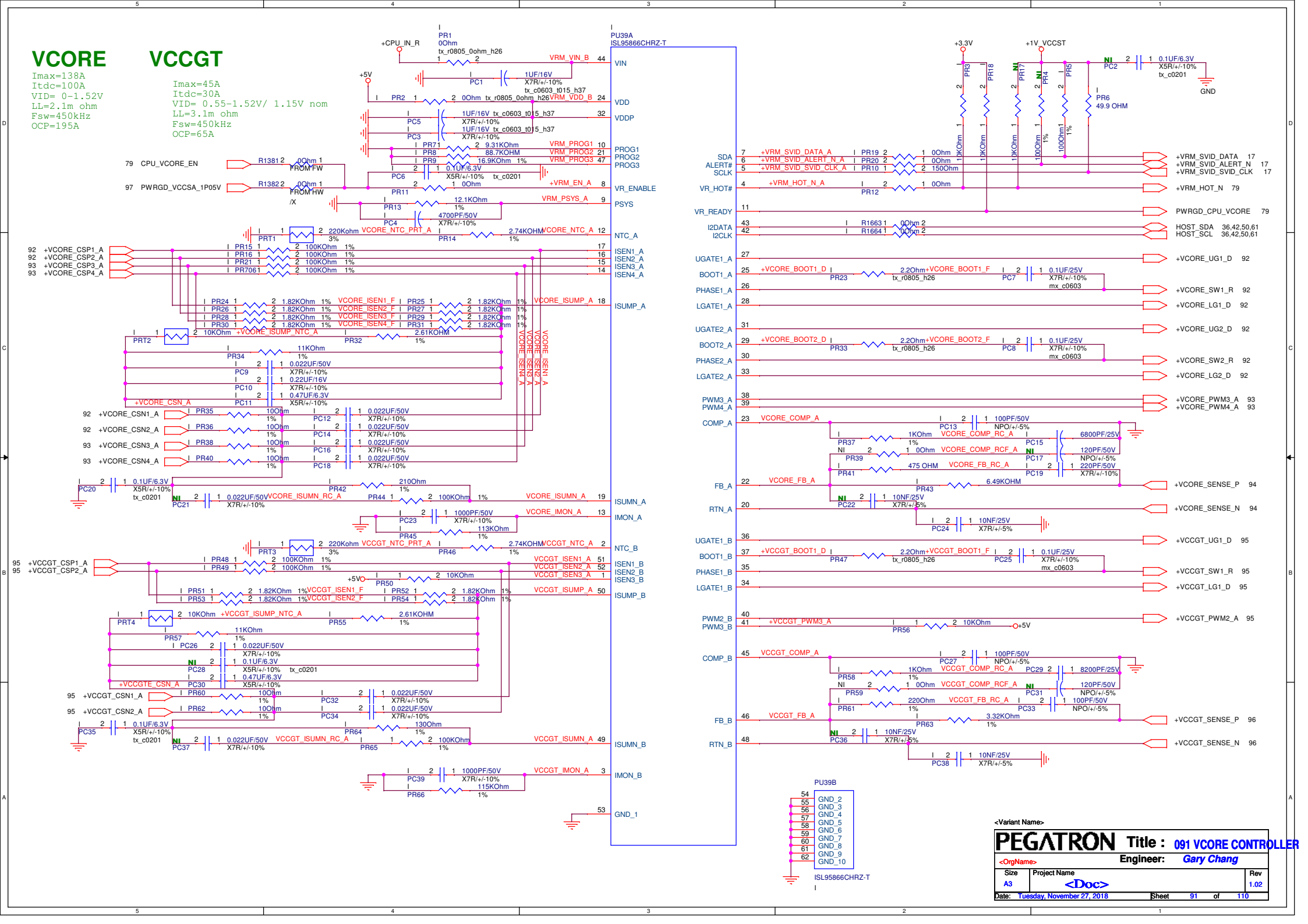
VCORE

Imax=138A
Itdc=100A
VID= 0-1.52V
LL=2.1m ohm
Fsw=450kHz
OCP=195A

VCCGT

Imax=45A
Itdc=30A
VID= 0.55-1.52V/ 1.15V nom
LL=3.1m ohm
Fsw=450kHz
OCP=65A



<Variant Name>
PEGATRON
Title : 091 VCORE CONTROLLER
<OrgName>
Engineer: Gary Chang
Size A3
Project Name <Doc>
Rev 1.02
Date: Tuesday, November 27, 2018
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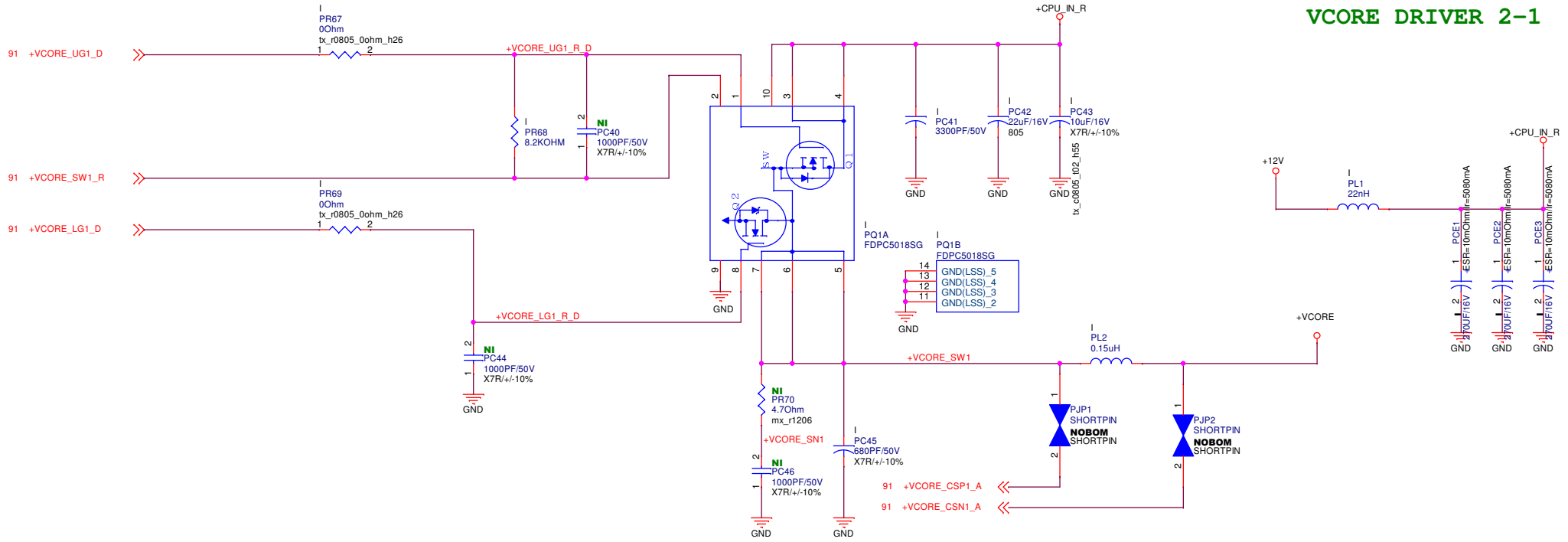
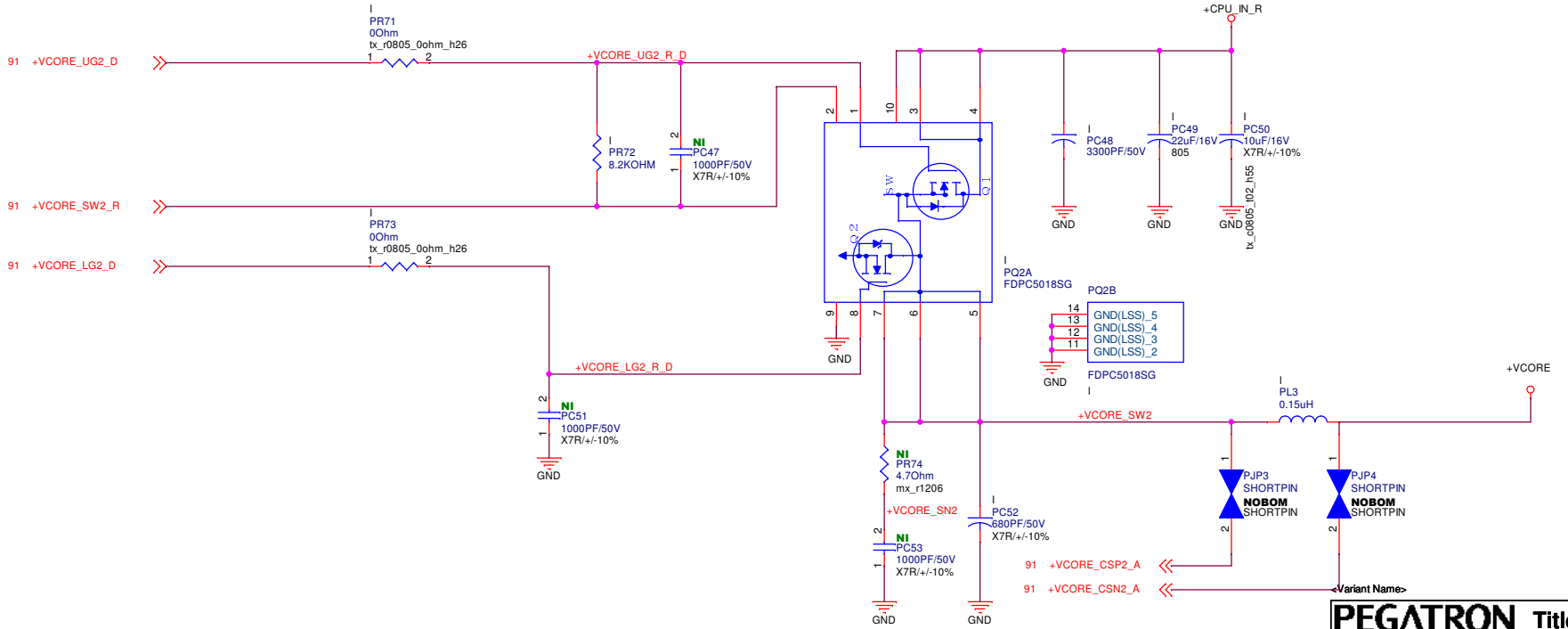
VCORE DRIVER 2-1





PEGATRON Title : 092 VCORE DRIVER 2-1

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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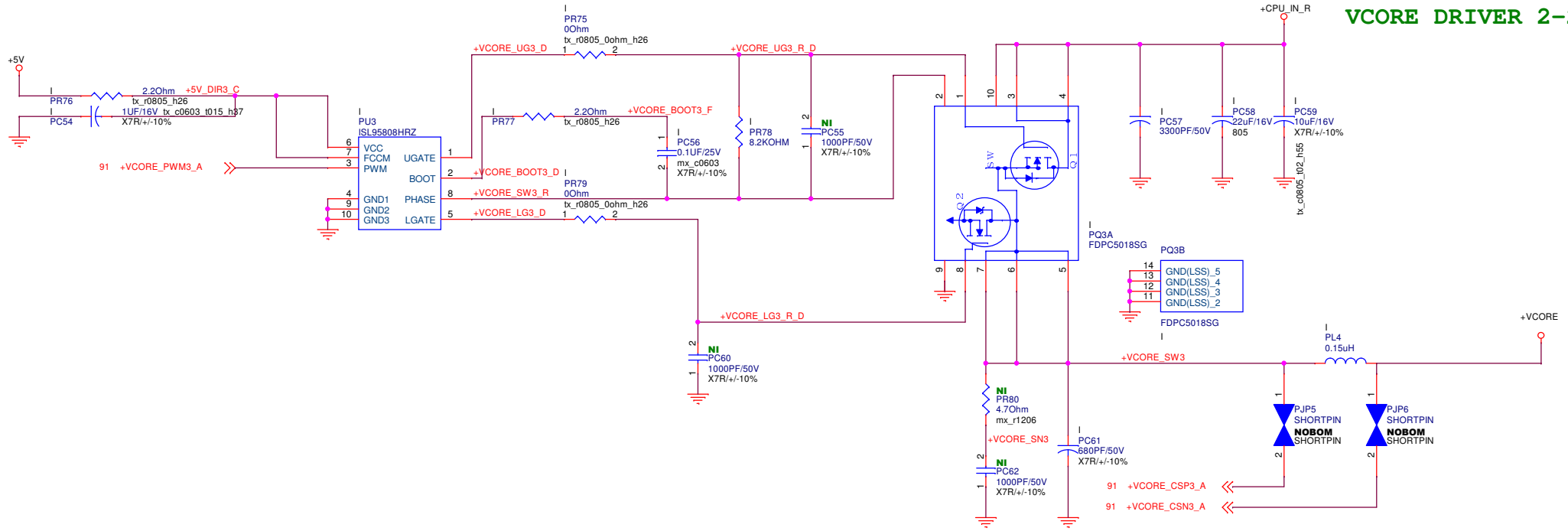
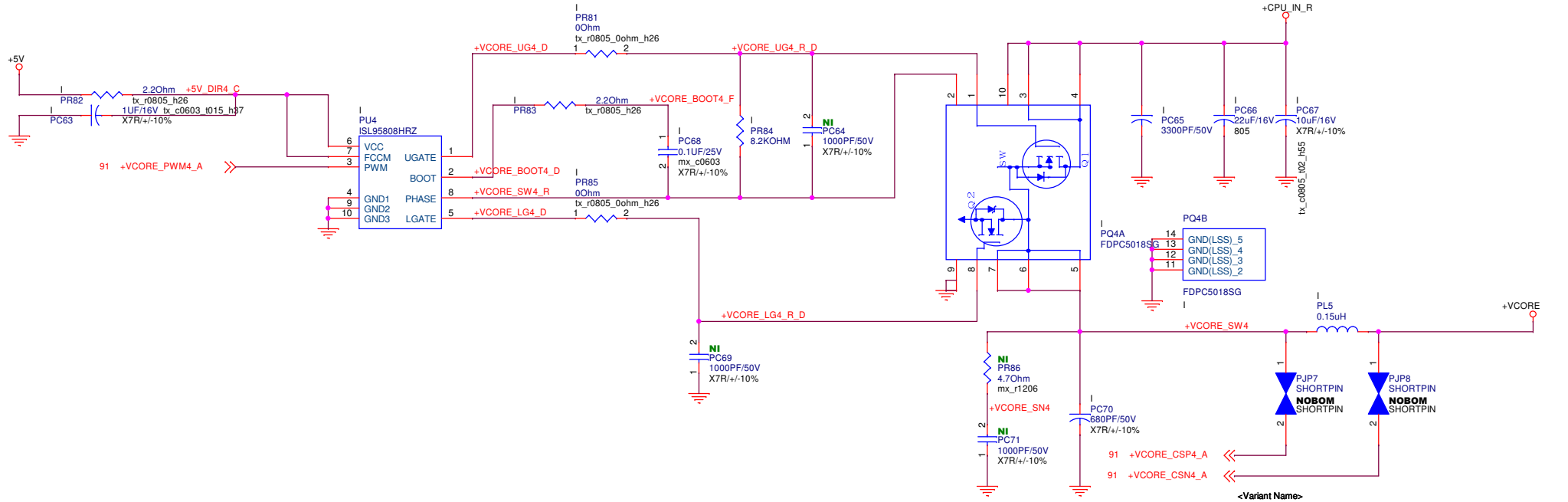
<Variant Name>

VCORE DRIVER 2-2





<Variant Name>

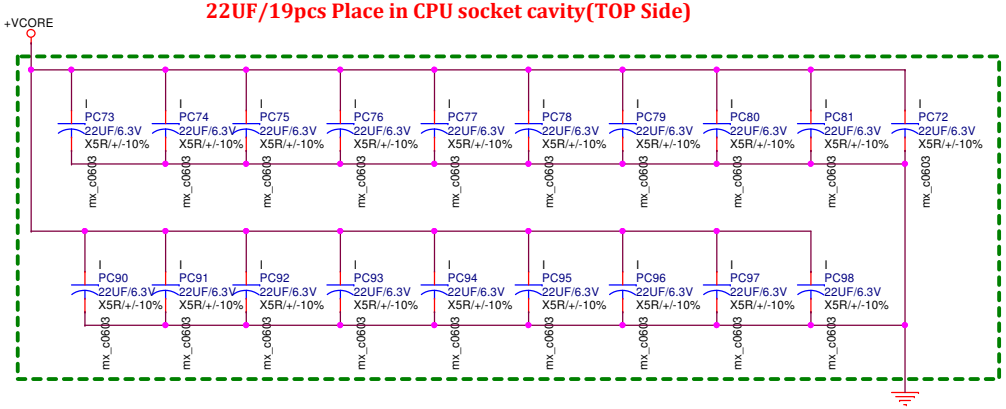
PEGATRON Title : 093 VCORE DRIVER 2-2

<OrgName> Engineer: Gary Chang

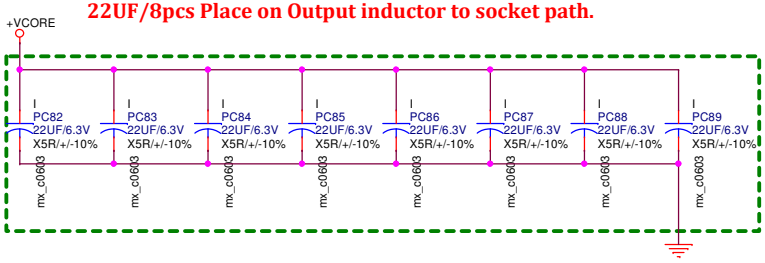
Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 93 of 110

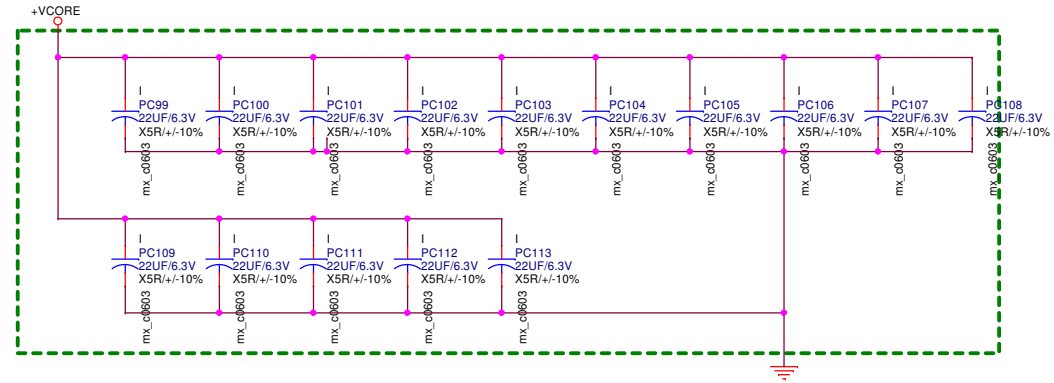
CAD NOTE:
22UF/19pcs Place in CPU socket cavity(TOP Side)

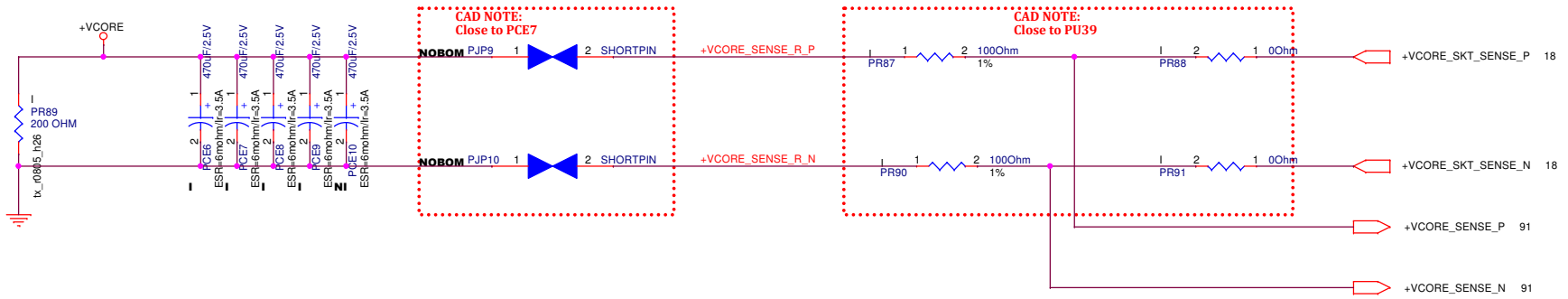


CAD NOTE:
22UF/8pcs Place on Output inductor to socket path.



CAD NOTE:
22UF/15pcs Place in CPU socket cavity(BOT Side)





<Variant Name>

PEGATRON Title : 094 VCORE CAP

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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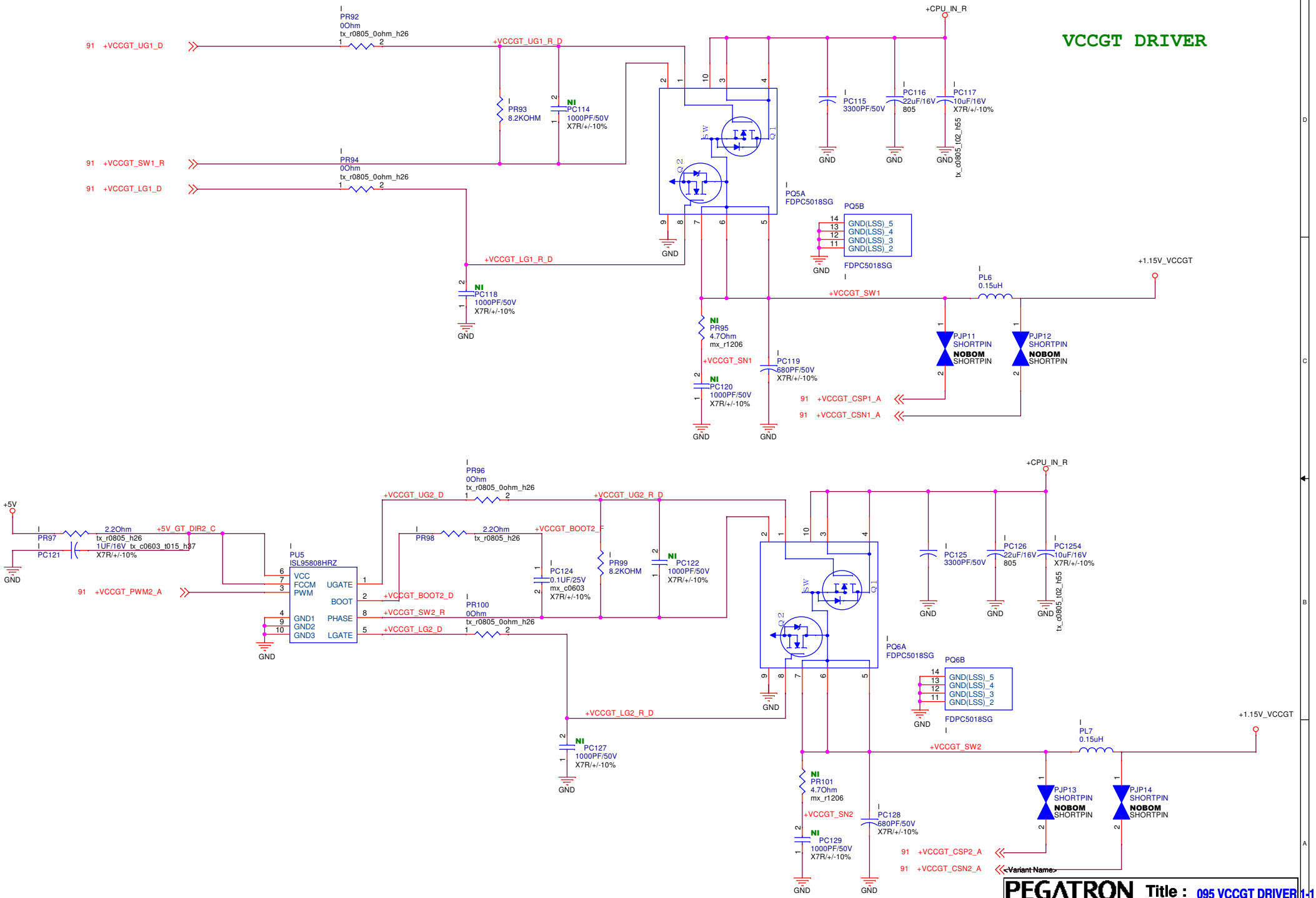
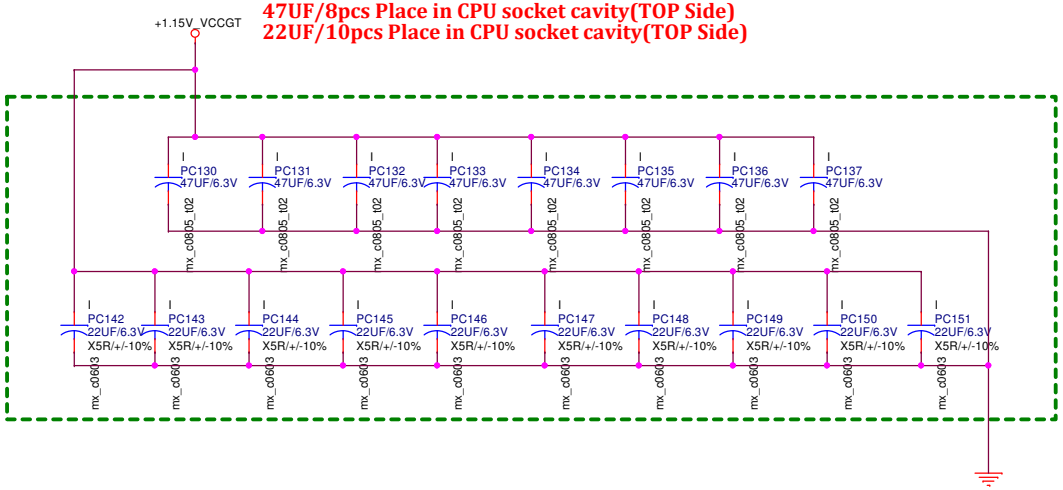
VCCGT DRIVER

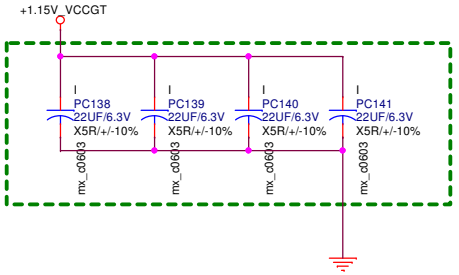


PEGATRON	Title : 095 VCCGT DRIVER	1-1
<OrgName>	Engineer: Gary Chang	
Size: A3	Project Name: <Doc>	Rev: 1.02
Date: Tuesday, November 27, 2018	Sheet 95 of 110	

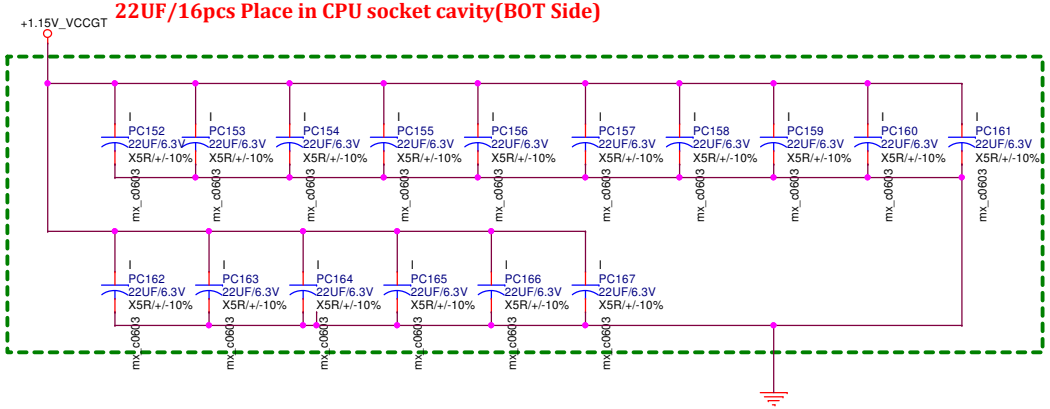
CAD NOTE:
47UF/8pcs Place in CPU socket cavity(TOP Side)
22UF/10pcs Place in CPU socket cavity(TOP Side)

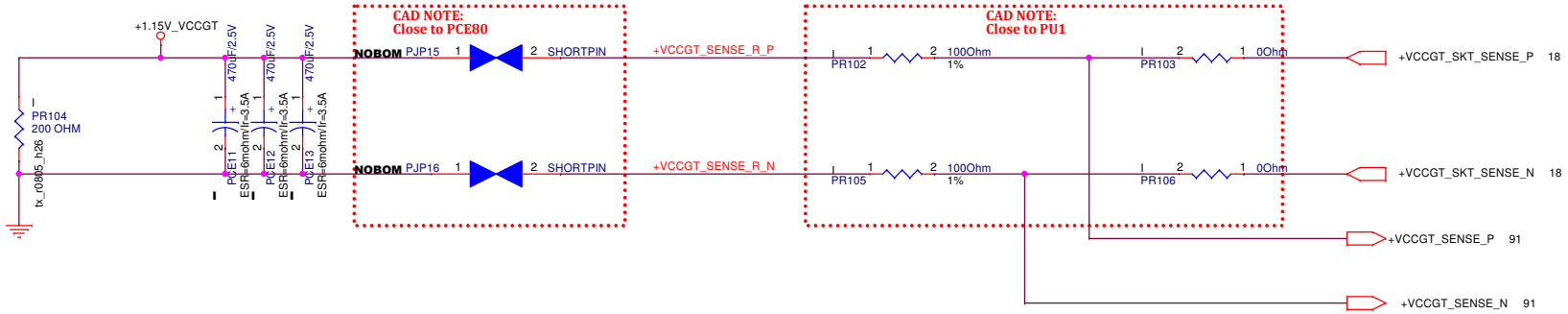


CAD NOTE:
22UF/8pcs Place on Output inductor to socket path.



CAD NOTE:
22UF/16pcs Place in CPU socket cavity(BOT Side)





<Variant Name>

PEGATRON Title : 096 VCCGT CAP

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 96 of 110

+VCCSA

Imax=11A
Itdc=10A
Irms=2.8A
LL=N/A
Fsw=500kHz
OCP=15A
Vripple=50mV

CAD NOTE:
22UF/2pcs Place in CPU socket cavity(TOP Side)

VEN=12*20/(51.1+20)=3.3V>1V

Vout=0.6*(1+7.32/10)+ripple 10mV=1.039V+0.01V=1.049V

$$I_{OCP} = \frac{R_{TRIP}}{12.3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

Table 1. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

<Variant Name>

PEGATRON Title : 097 VCCSA

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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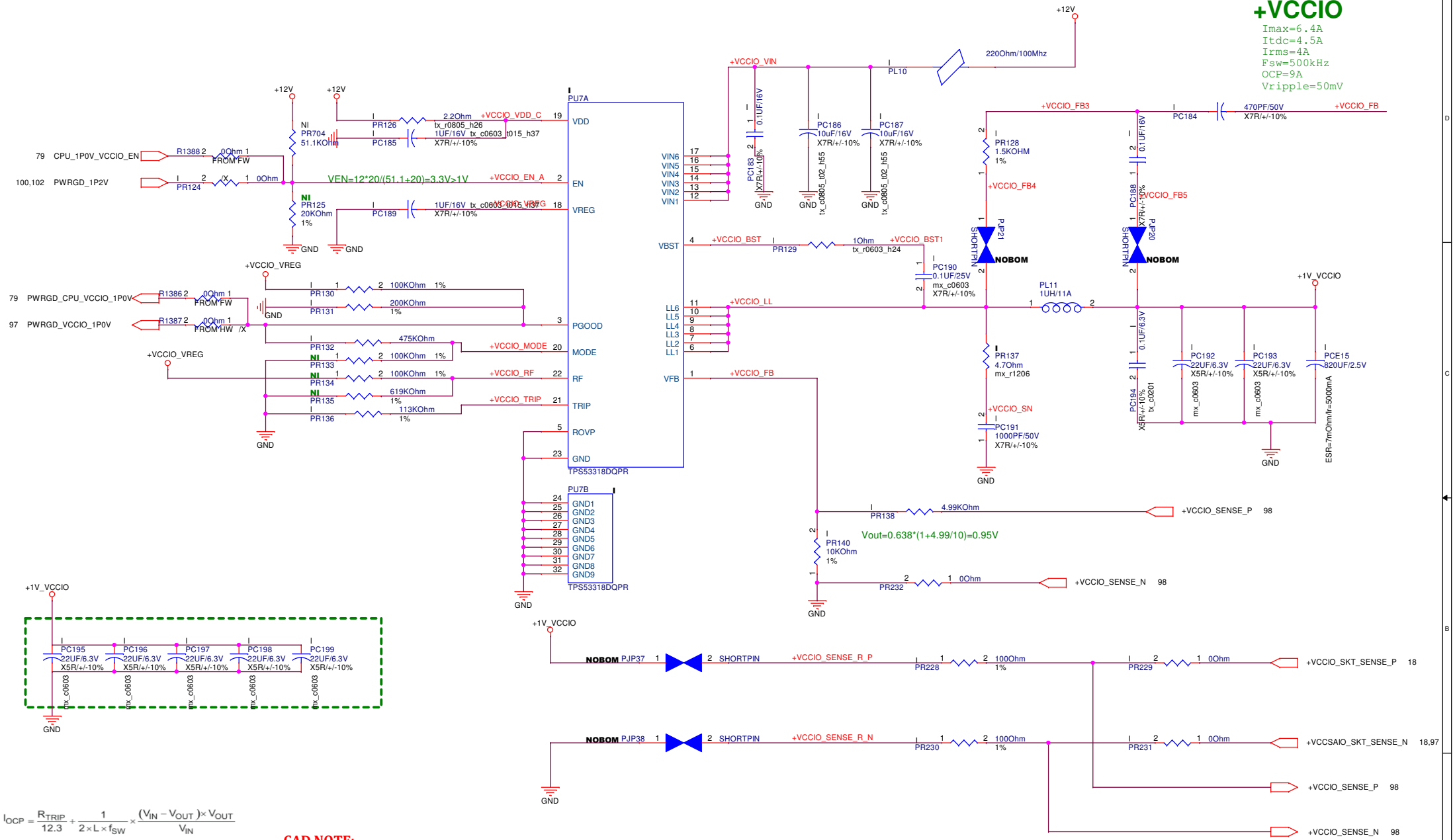
+VCCIO

Imax=6.4A
Itdc=4.5A
Irms=4A
Fsw=500kHz
OCP=9A
Vripple=50mV



$$I_{OCP} = \frac{R_{TRIP}}{12.3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

CAD NOTE:
22UF/2pcs Place in CPU socket cavity (TOP Side)

Table 1. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

<Variant Name>

PEGATRON Title : 098 VCCIO

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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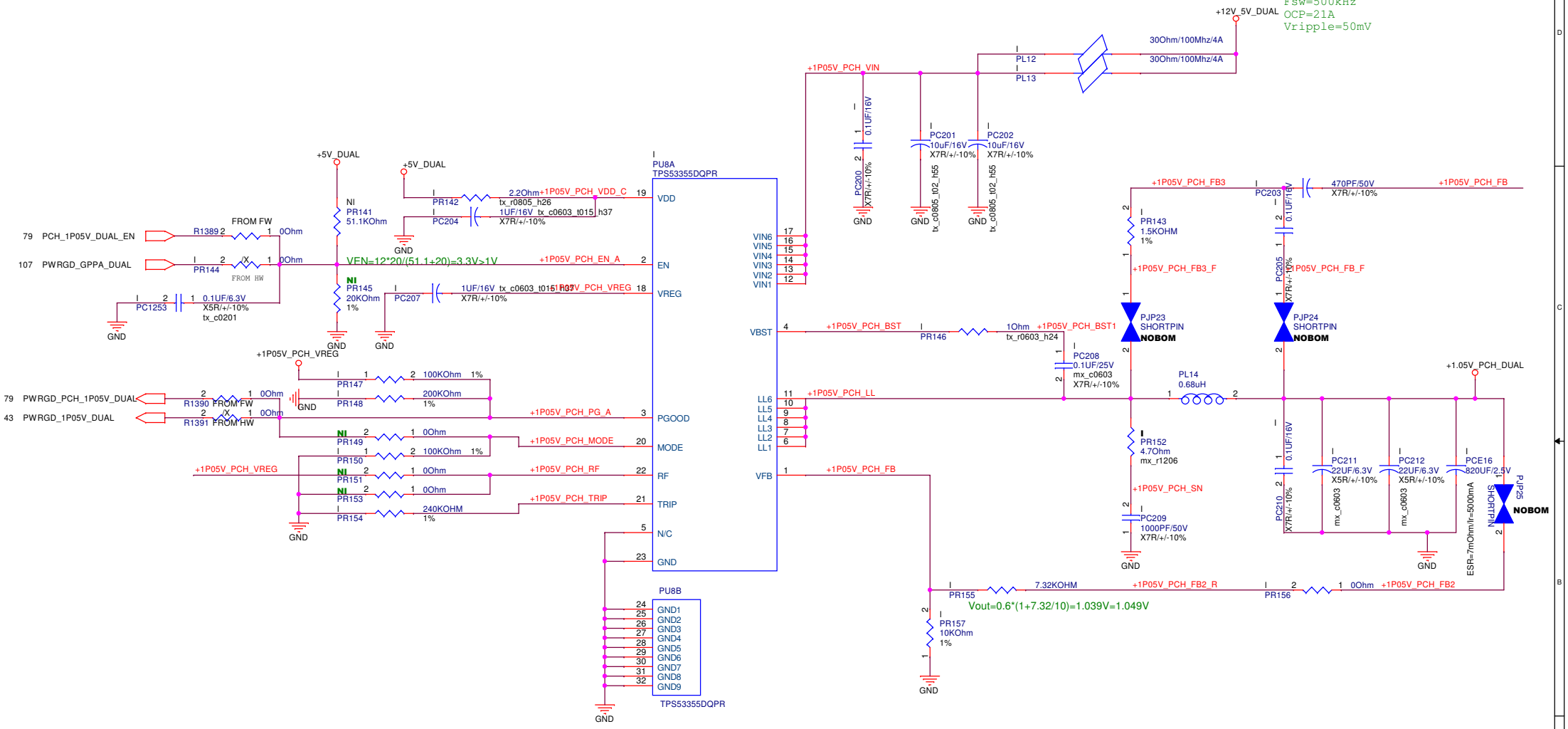
+1P05V_PCH_DUAL

Imax=14.8A
Itdc=11A
Irms=2.8A
Fsw=500kHz
OCP=21A
Vripple=50mV



$$I_{OCP} = \frac{R_{TRIP}}{12.3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

Table 1. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

<Variant Name>

PEGATRON Title : 099 1P05V_PCH_DUAL

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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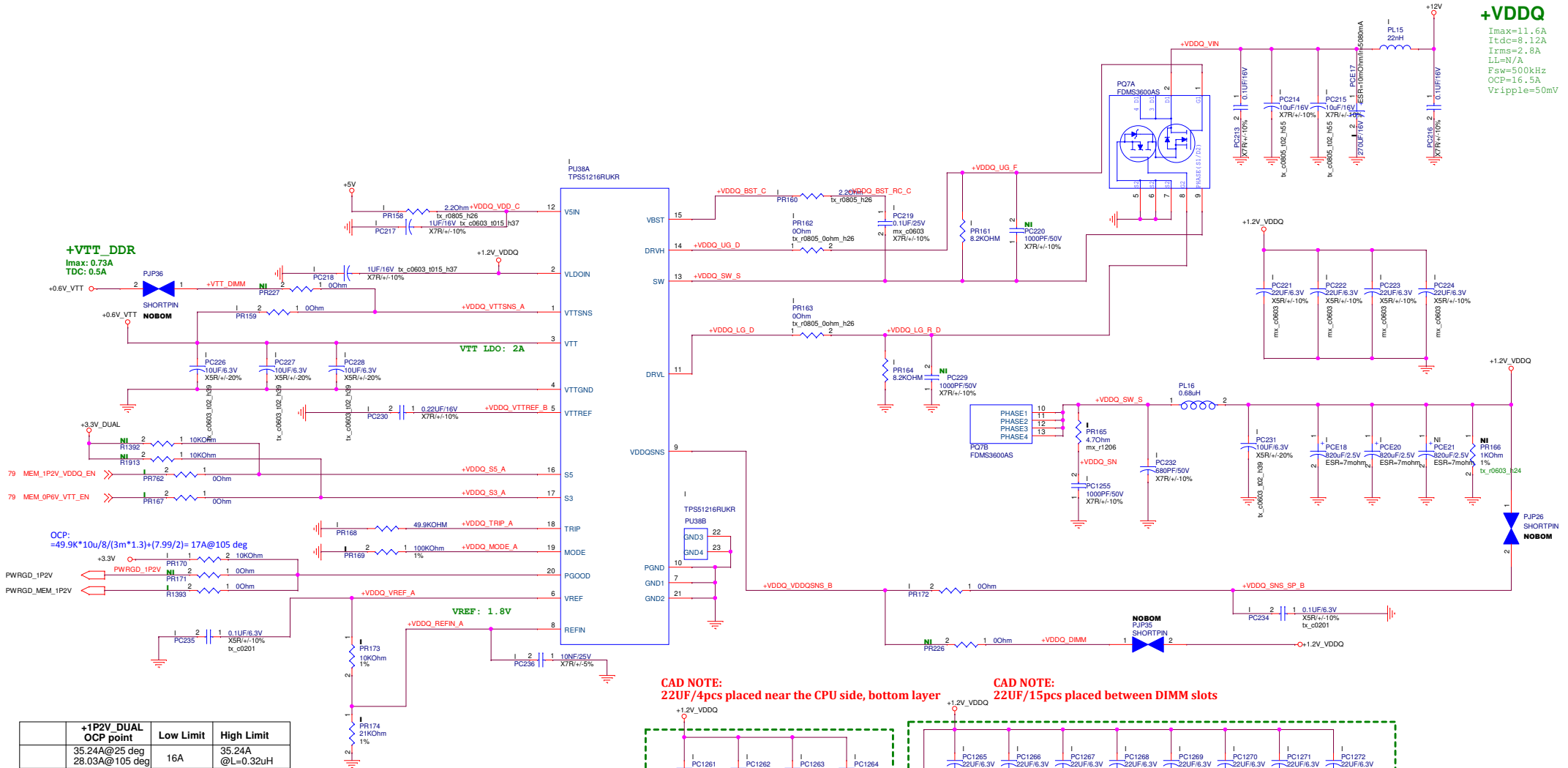


	+1P2V_DUAL OCP point	Low Limit	High Limit
	35.24A@25 deg 28.03A@105 deg	16A	35.24A @L=0.32uH
	35.24A@25 deg 28.03A@105 deg	16A	35.24A @L=0.32uH

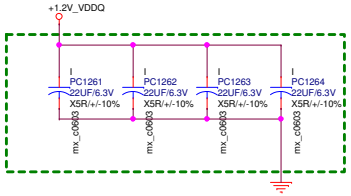
Table 2. MODE Selection

No.	Resistance between MODE and GND	Frequency	Discharge Mode
3	200kΩ	400kHz	Tracking Discharge
2	100kΩ	300kHz	
1	68kΩ	300kHz	Non-tracking Discharge
0	47kΩ	400kHz	

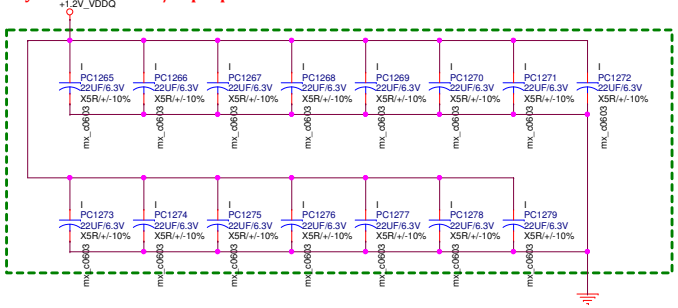
Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

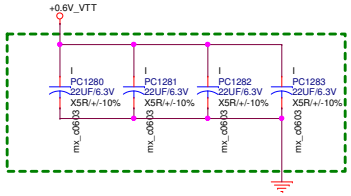
CAD NOTE:
22UF/4pcs placed near the CPU side, bottom layer



CAD NOTE:
22UF/15pcs placed between DIMM slots



CAD NOTE:
22UF/4pcs placed near the CPU side, bottom layer



<Variant Name>

PEGATRON Title : 100 VDDQ & VTT

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
Custom	<Doc>	1.02

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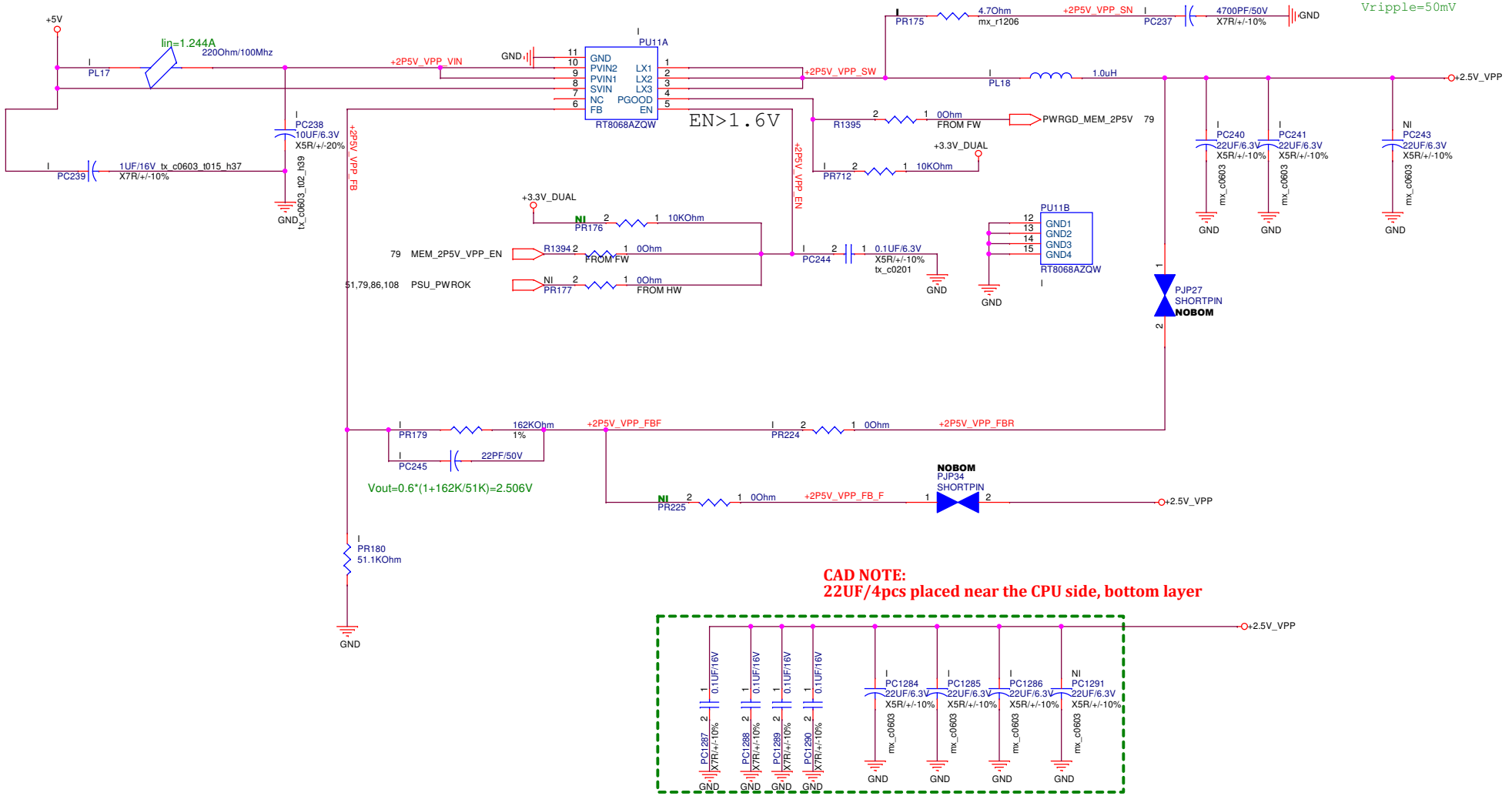
+2P5V_VPP

Iin=1.244A
Imax=2.24A
Irms=0.9A
Fsw=1MHz
OCP=4.5A
Vripple=50mV



<Variant Name>

PEGATRON Title : 101 VPP

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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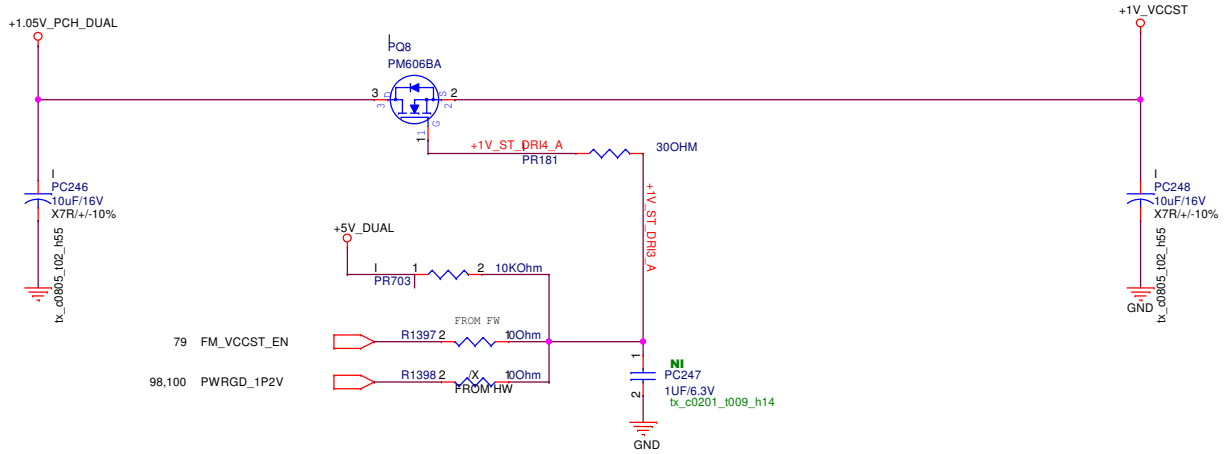
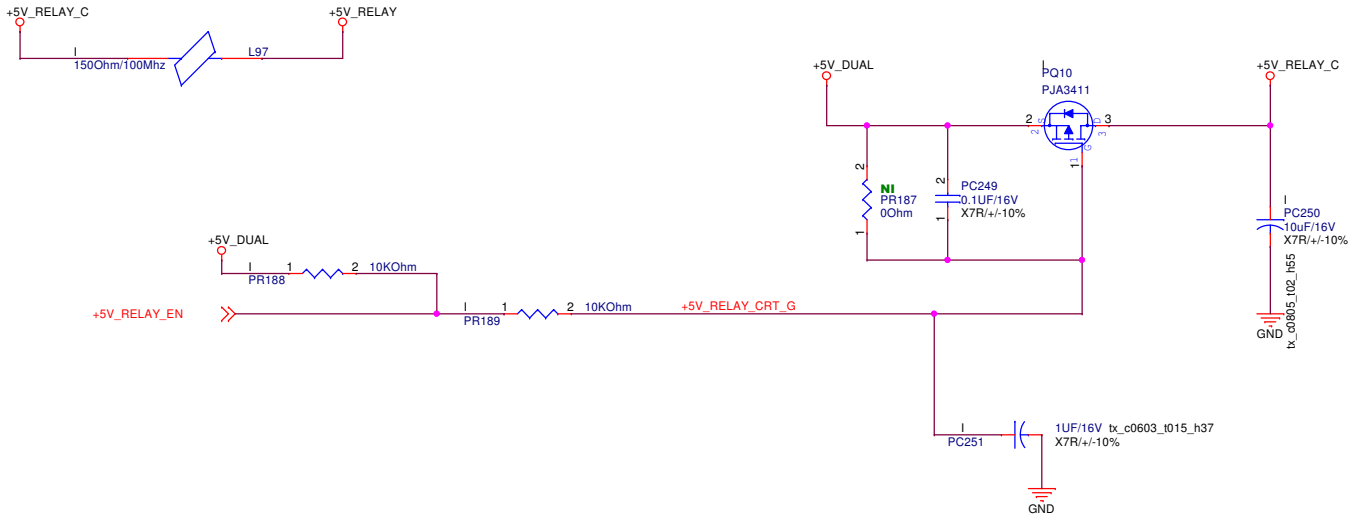


+VCCST

Imax=0.3A
Itdc=0.21A
Vdroop=31m*0.3A=09.5mV
Pd=0.3^2*31m=2.8mW



+5V_RELAY

Imax=1.03A
Itdc=0.7A
Vdroop=100m*1.03A=0.1V
Pd=1^2*100m=0.1W

<Variant Name>

PEGATRON Title : 102 VCCST & 5V_RELAY

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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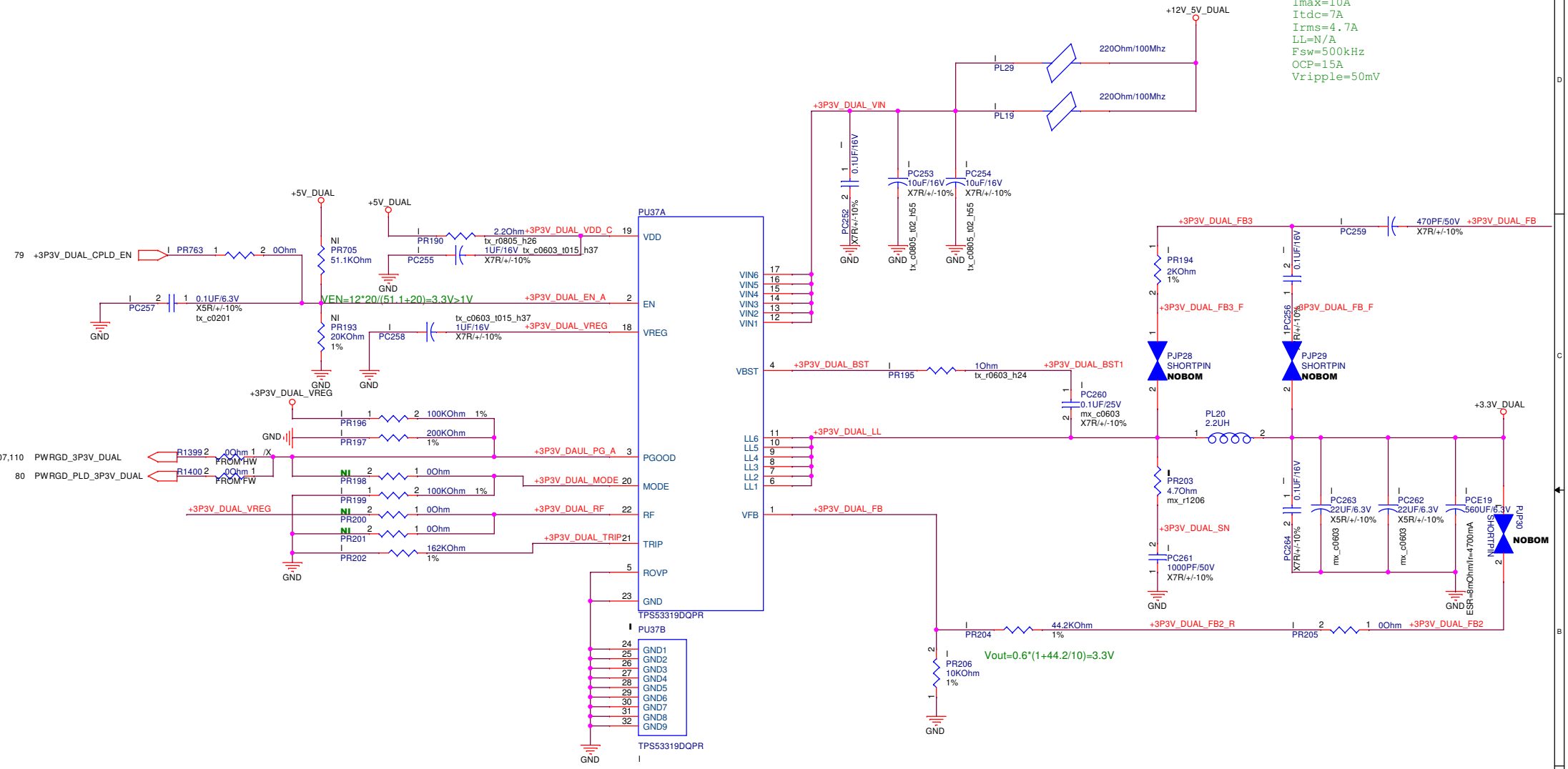
+3P3V_DAUL

Imax=10A
Itdc=7A
Irms=4.7A
LL=N/A
Fsw=500kHz
OCP=15A
Vripple=50mV



$$I_{OCP} = \frac{R_{TRIP}}{12.3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

Table 1. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

<Variant Name>

PEGATRON Title : 103 3P3V_DAUL

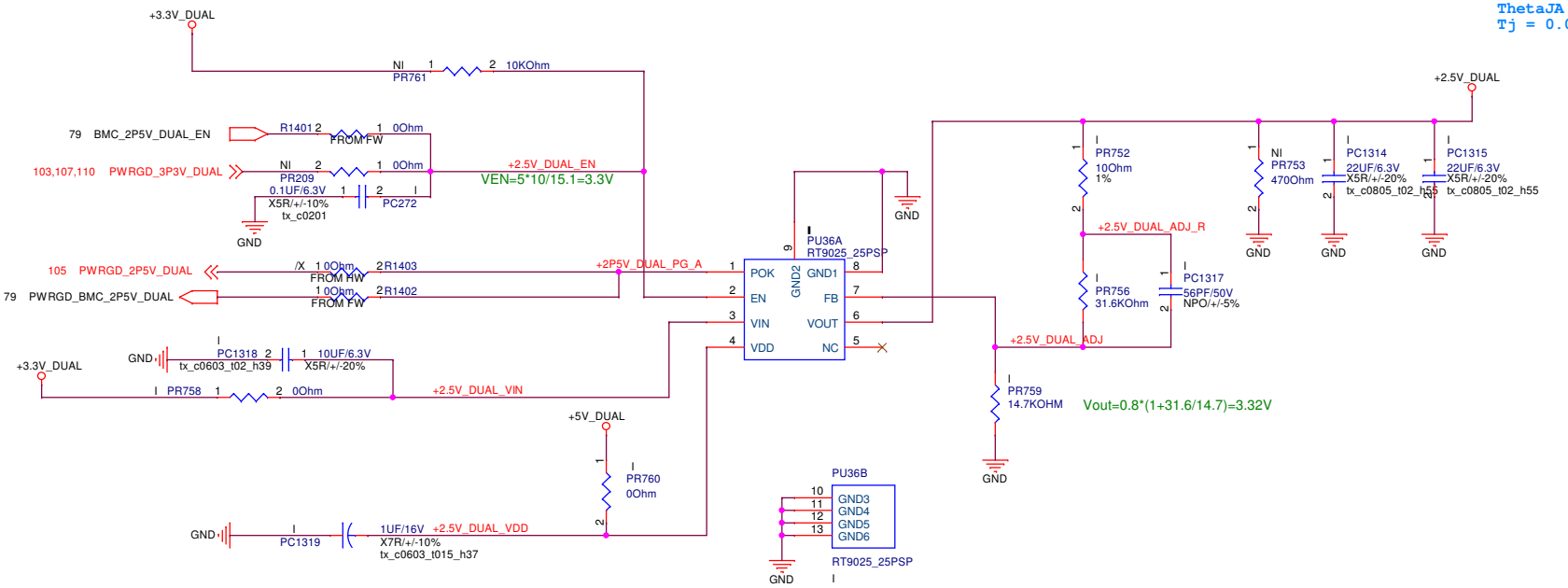
<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 103 of 110

+2P5V_DUAL

Power Rail : +2P5V_DUAL
MAX = 0.1A
OCP = 3.5A
Max step = --
DI/DT = --
Pd = 0.08W
ThetaJA = 75°C/W
Tj = 0.08*75+40 = 46 °C < 125 °C



<Variant Name>

PEGATRON Title 104 2P5V_DUAL

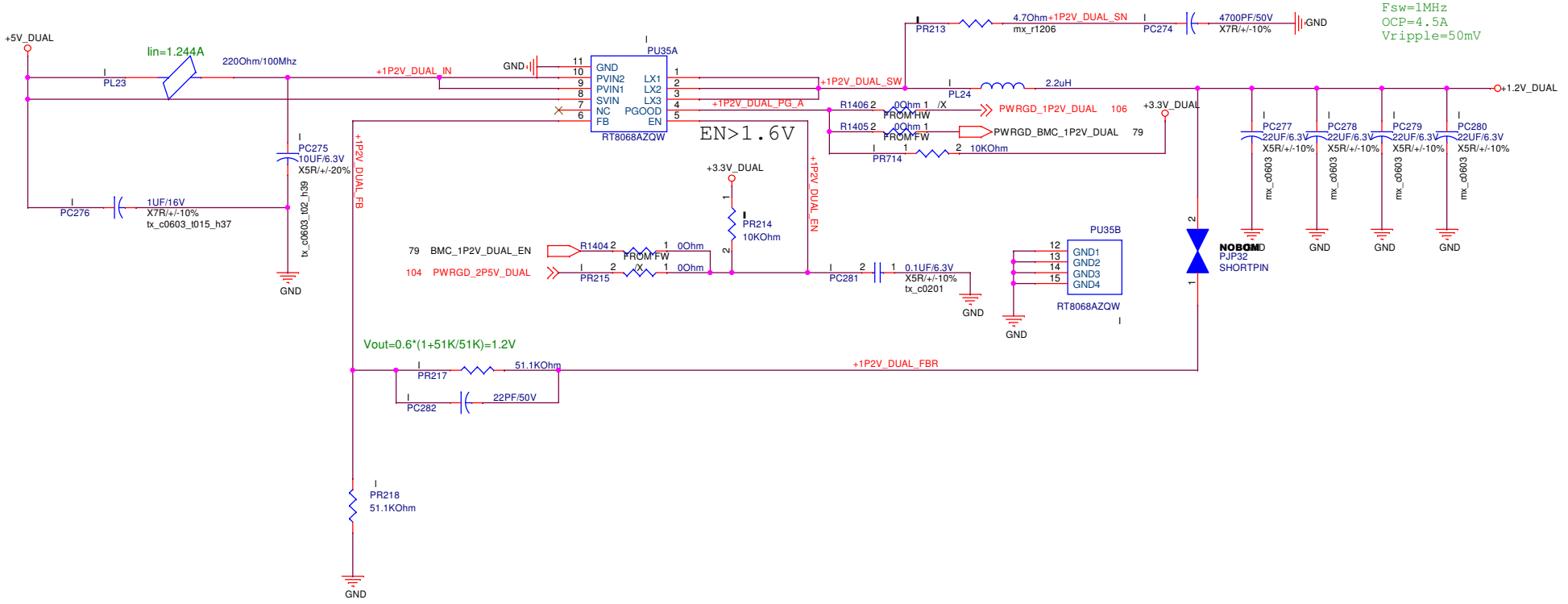
<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 104 of 110

+1P2V_DUAL

Imax=1.1A
Itdc=0.77A
Irms=0.83A
Fsw=1MHz
OCP=4.5A
Vripple=50mV



<Variant Name>

PEGATRON Title : 105 1P2V_DUAL

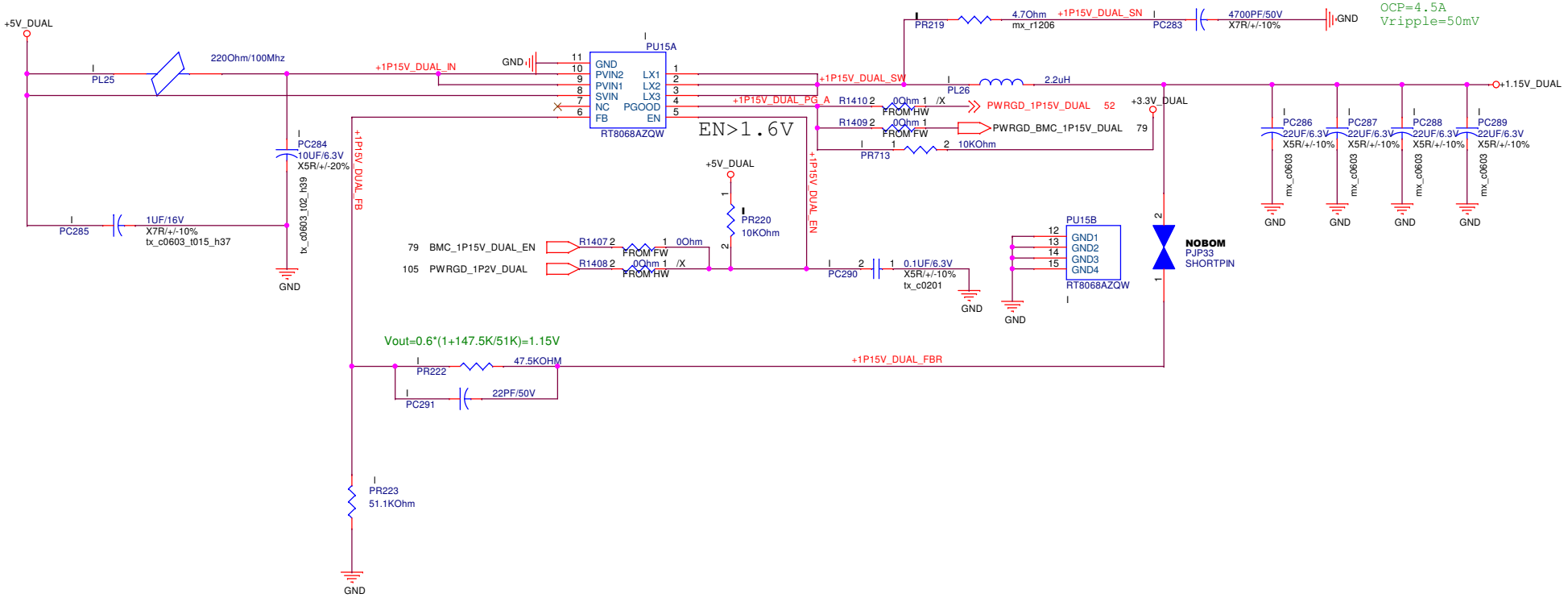
<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 105 of 110

+1P15V_DUAL

Imax=1A
Itdc=0.7A
Irms=0.81A
Fsw=1MHz
OCP=4.5A
Vripple=50mV



<Variant Name>

PEGATRON Title : 106 1P15V_DUAL

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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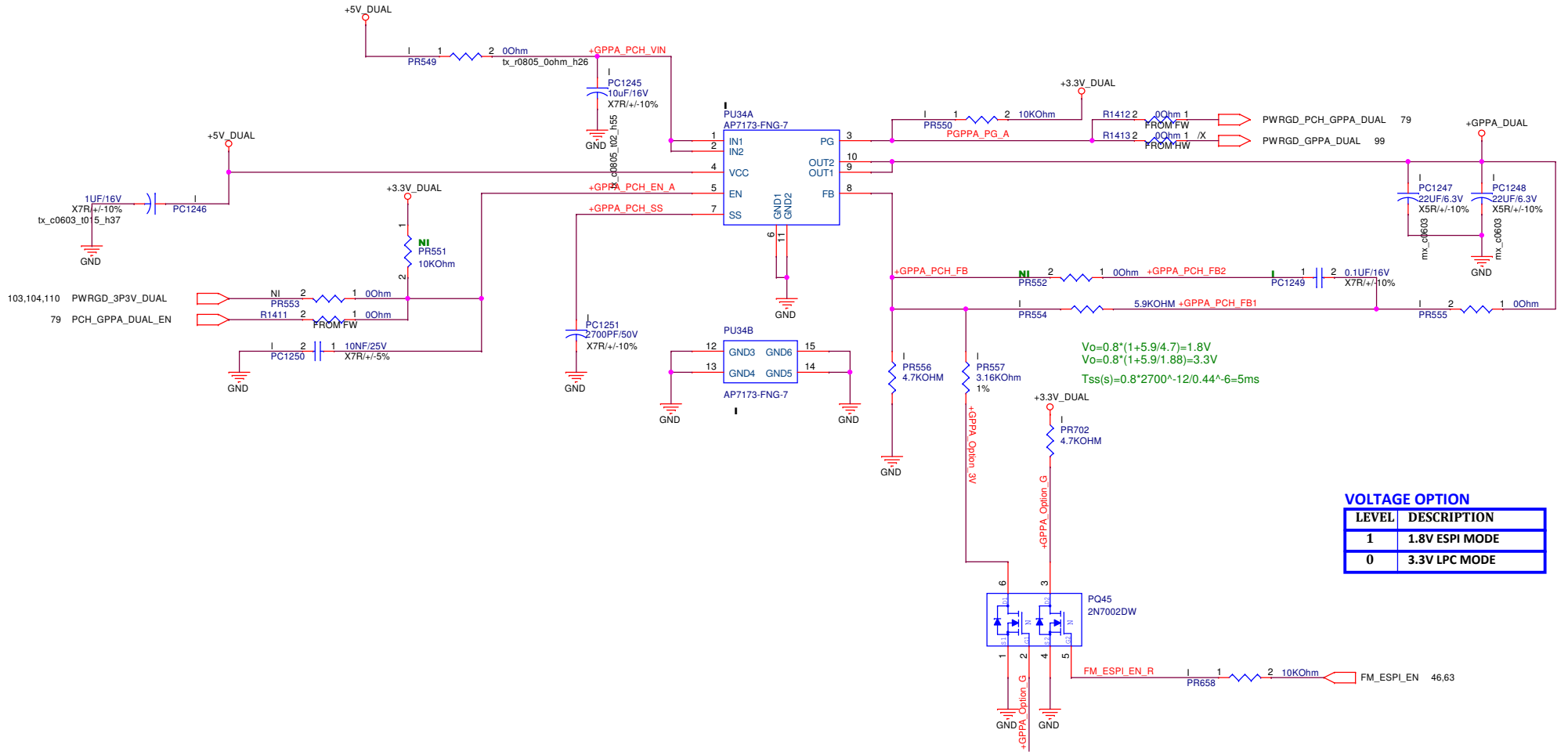
P1V8/3V3_PGPPA

Imax=0..22A
TDC=0.15A
Pd=(5-1.8)*0.22=0.704W
Current limit=3A



VOLTAGE OPTION

LEVEL	DESCRIPTION
1	1.8V ESPI MODE
0	3.3V LPC MODE

<Variant Name>

PEGATRON Title : P107 P1V8/3V3_PGPPA

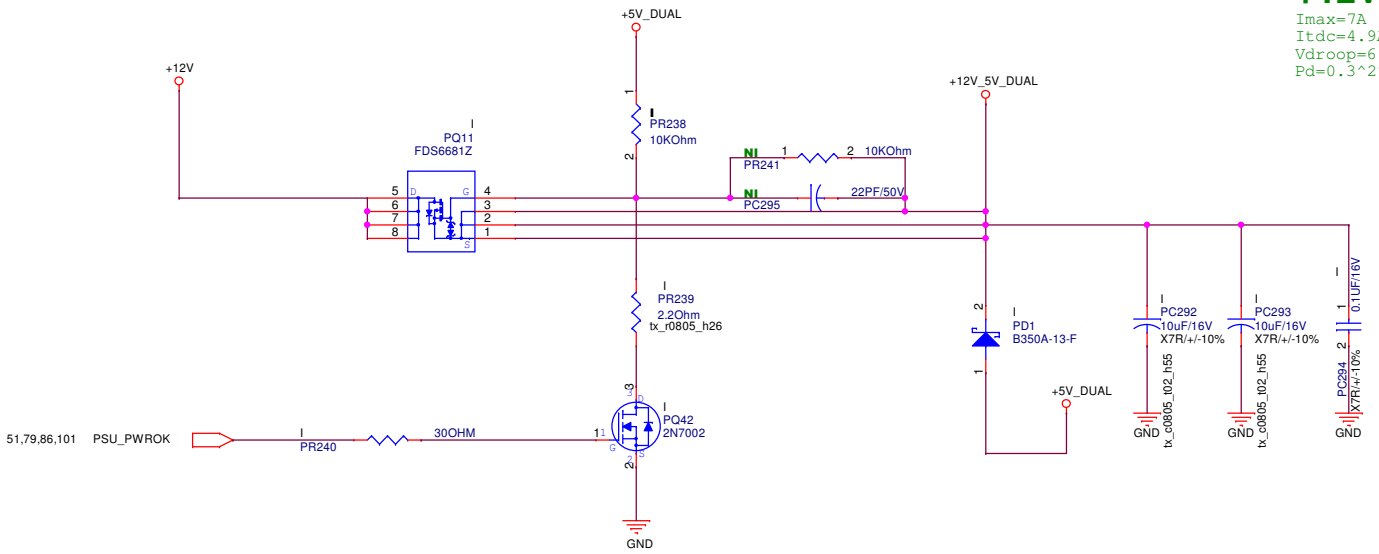
<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 107 of 110

+12V_5V_DUAL

Imax=7A
Itdc=4.9A
Vdroop=6.5m*7A=45mV
Pd=0.3^2*0.6m=0.3W



<Variant Name>

PEGATRON Title : 108 P12V_P5V_DUAL

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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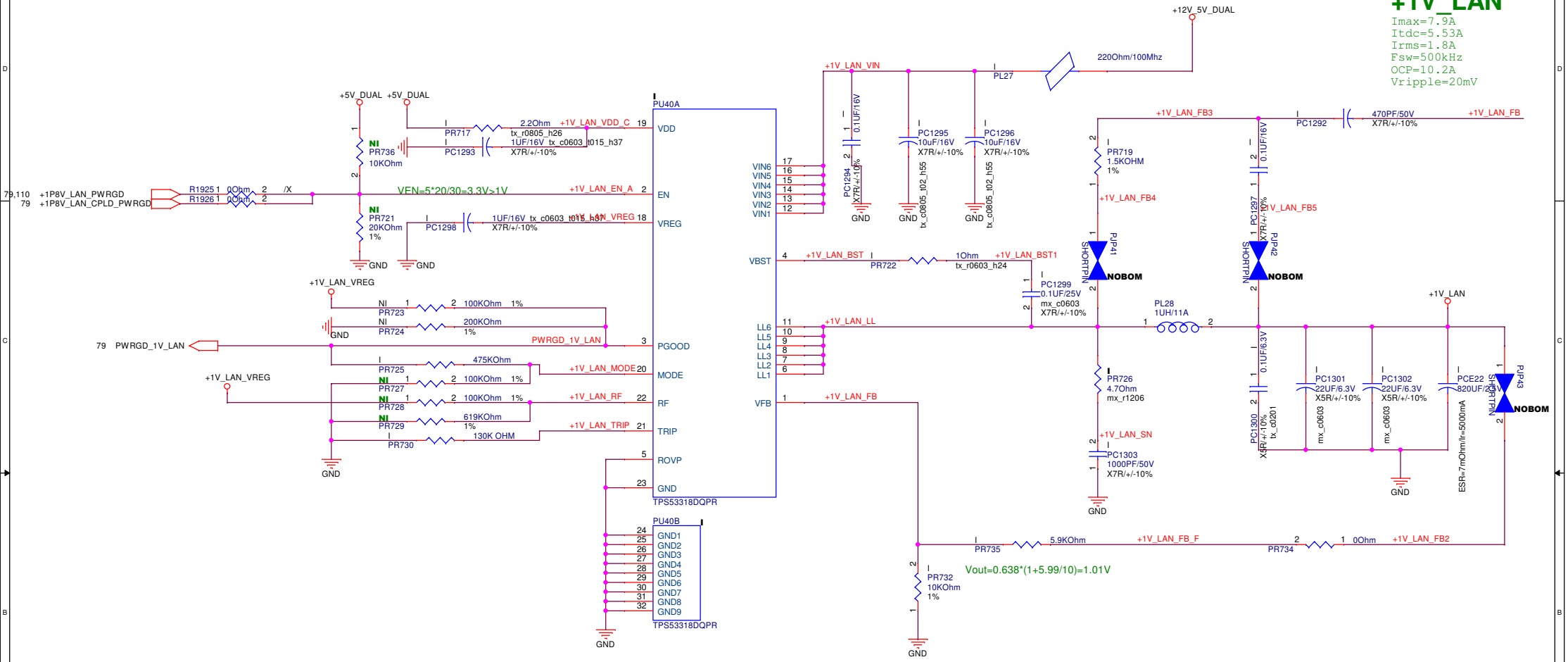
+1V_LAN

Imax=7.9A
Itdc=5.53A
Irms=1.8A
Fsw=500kHz
OCP=10.2A
Vripple=20mV



$$I_{OCP} = \frac{R_{TRIP}}{12.3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Table 1. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

<Variant Name>

PEGATRON Title : 109 +1V_LAN

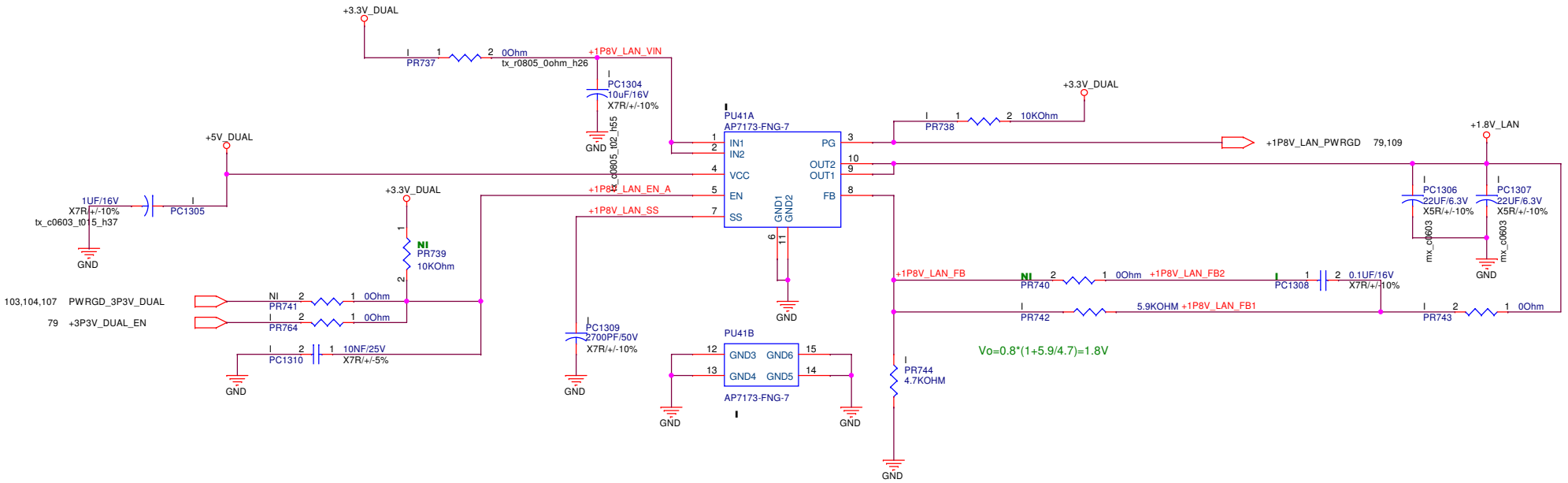
<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

Date: Tuesday, November 27, 2018 Sheet 109 of 110

+1P8V_LAN

Imax=0.6A
TDC=0.42A
Pd=(5-1.8)*0.6=1.9W
Current limit=3A



<Variant Name>

PEGATRON Title : +1P8V_LAN

<OrgName> Engineer: Gary Chang

Size	Project Name	Rev
A3	<Doc>	1.02

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