ODILO O I											
CPU Op Codes	<u></u>										
0b XXXX XXXX X1XX XXXX		Desumenia	Dite	Operation		Data Bits		luo no o die	ata Dita		Re
	0bX100 01XX	Pneumonic JMP	Bits 0b00	Operation	Dh	Ra		Immedia	ale Bils		Re
				PC <- Ra, Rb	Rb	Ra					
		JMP (with immediate)	0b00	PC <- k		_	k				
		CALL	0b01	[LR <- PC] : [PC <- Ra, Rb]	Rb	Ra					
		CALL (with immediate)	0b01	[LR <- PC] : [PC <- k]		_	k				
		RJMP	0b10	PC <- PC + Ra, Rb	Rb	Ra					
		RJMP (with immediate)	0b10	PC <- PC + k			k				
		RCALL	0b11	[LR <- PC] : [PC <- PC + Ra, Rb]	Rb	Ra					
		RCALL (with immediate)	0b11	[LR <- PC] : [PC <- PC + k]			k				
		Special Registers									
		The Most Significant bit te	lls if Read or Writ	е							
	0bX100 1XXX	Register	Value								
		Read	0b0XX								
		Write	0b1XX								
		The two least significant b	its determine whi	ch special register is being accessed							
		Register	Value								
		PC	0bX00								
		LR	0bX01								
		SP	0bX10								
		ADDR	0bX11								
				writing will use the second and third i		ombined as a 16 bit immediate					
						ombined as a 16 bit immediate					
		Otherwise, the second ins	truction byte sele	cts which general purpose registers a		ombined as a 16 bit immediate					
		Otherwise, the second ins Meaning Lower Byte Register	Bits 0b0000XXXX	cts which general purpose registers a Register a		ombined as a 16 bit immediate					
		Otherwise, the second inst Meaning	truction byte sele	cts which general purpose registers a Register a		ombined as a 16 bit immediate					
		Otherwise, the second ins Meaning Lower Byte Register	Bits 0b0000XXXX	cts which general purpose registers a Register a		ombined as a 16 bit immediate					
		Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register	Bits 0b0000XXXX	cts which general purpose registers a Register a		ombined as a 16 bit immediate					
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register	Bits 0b0000XXXX	cts which general purpose registers a Register a		ombined as a 16 bit immediate		Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops	Bits 0b0000XXXX 0bXXXX0000	cts which general purpose registers a Register a Register b				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic	Bits 0b0000XXX 0bXXXX0000	cts which general purpose registers a Register a Register b Operation				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET	Bits 0b0000XXX 0bXXXX0000 Bits 0b0000	cts which general purpose registers a Register a Register b Operation PC <- LR				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		
	0bX101 XXXX	Otherwise, the second ins Meaning Lower Byte Register Upper Byte Register General CPU Ops Pneumonic RET DNFG	Bits Ob0000 Bits Ob0000 Bits Ob0000 Ob0000 Ob0001	cts which general purpose registers a Register a Register b Operation PC <- LR - Disables changes to ALU Flags -				Immedia	ate Bits		

0bX11X XXXX	Pneumonic	Bits	Operation	Data	a Bits	Immediate Bits	
	JMP	0bX XX00	PC <- Ra, Rb	Rb	Ra		
	JMP (with immediate)	0bX XX00	PC <- k			k	
	CALL	0bX XX01	[LR <- PC] : [PC <- Ra, Rb]	Rb	Ra		
	CALL (with immediate)	0bX XX01	[LR <- PC] : [PC <- k]			k	
	RJMP	0bX XX10	PC <- PC + Ra, Rb	Rb	Ra		
	RJMP (with immediate)	0bX XX10	PC <- PC + k			k	
	RCALL	0bX XX11	[LR <- PC] : [PC <- PC + Ra, Rb]	Rb	Ra		
	RCALL (with immediate)	0bX XX11	[LR <- PC] : [PC <- PC + k]			k	
	The least significant 2 bits	of the Condition (Codes correspond to an ALU flag				
	IE: 0b1001XX would only b	e executed if the	flag 'C' (Carry) is set				
	The most significant bit of t	the Condition Cod	de can be set high to check if a ALU fl	ag is clear			
	IE: 0b1101XX would only b	e executed if the	flag 'C' (Carry) is NOT set				

Hello									
	ALU Op Codes	0b XXXX XXXX X01X XXXX							
Bits			Pneumonic	Bits	Operation	Sets Flags			
	4 Mod Bit		CLR	0b00000	b <- 0x00		reserved	Output is always stored into reg	ister B
	3		SER	0b10000	b <- 0xFF		broken		
	2 Instruction		NOT	0b00001	b <- !a				
			TWO	0b10001	b <- !(a + 1)				
C	0		AND	0b00010	b <- (a & b)				
			NND	0b10010	b <- !(a & b)				
	A		ORR	0b00011	b <- (a b)				
	ALU Flags		NOR	0b10011	b <- !(a b)				
Bits	Variable	Full Name	XOR	0b00100	b <- (a ^ b)				
7			XNR	0b10100	b <- !(a ^ b)				
	6		ADD	0b00101	b <- (a + b)				
	5		ADC	0b10101	b <- (a + b + C)				
	4		SUB	0b00110	b <- (a - b)				
	3		SBC	0b10110	b <- (a - (b + C))				
	2 T	Two's Compliment Overflow	INC	0b00111	b <- (a + 1)				
1		Carry Flag	DEC	0b10111	b <- (a - 1)				
C) Z	Zero Flag	MOV	0b01000	b <- a				
			MVN	0b11000	b <- !a				
			SET	0b01001	b <- b				
	Instruction Bits		STN	0b11001	b <- !b				
Bits	Description		CMP	0b01010	a - b				
b0:b4	ALU Op								
b5	Always High (ALU Flag)			0b01011					
b6	Always Low			0b11011					
b7	Use Immediate for B			0b01100					
b8:b11	Register A			0b11100					
b12:b15	Register B			0b01101					
(if b7 == High)				0b11101					
b16:b23	Immediate Value			0b01110					
				0b11110					
				0b01111					
				0b11111					

Always										
0bX001 XXXX										
There are only tw	vo operations that	can be performe	d directly on the m	nemory IO submo	dule		Instru	ction Bits		
							_		•	
						3	2	1	0	
Read						3 Enable Increment	0 = Pre, 1 = Post	0 = Inc, 1 = Dec	0 = Read, 1 = Write	
Read Write						Enable Increment	0 = Pre, 1 = Post	1 0 = Inc, 1 = Dec	0 0 = Read, 1 = Write	
						Enable Increment	0 = Pre, 1 = Post	1 0 = Inc, 1 = Dec	0 0 = Read, 1 = Write	
									0 = Read, 1 = Write	lue