Exam - Computer Architecture Unit I [06/02/2025] (A)

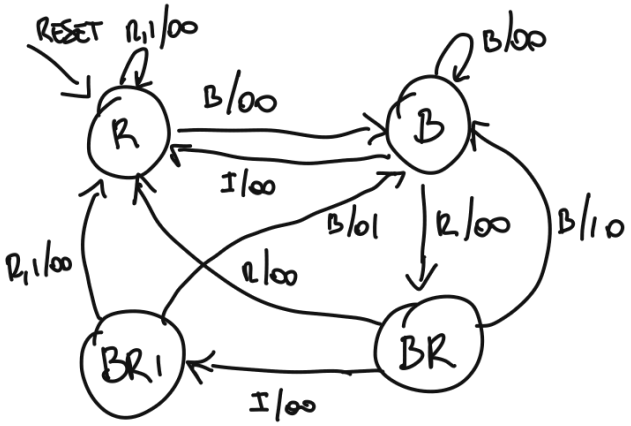
Surname: _____ **Name:** _____

Student ID Number (Matricola): _____

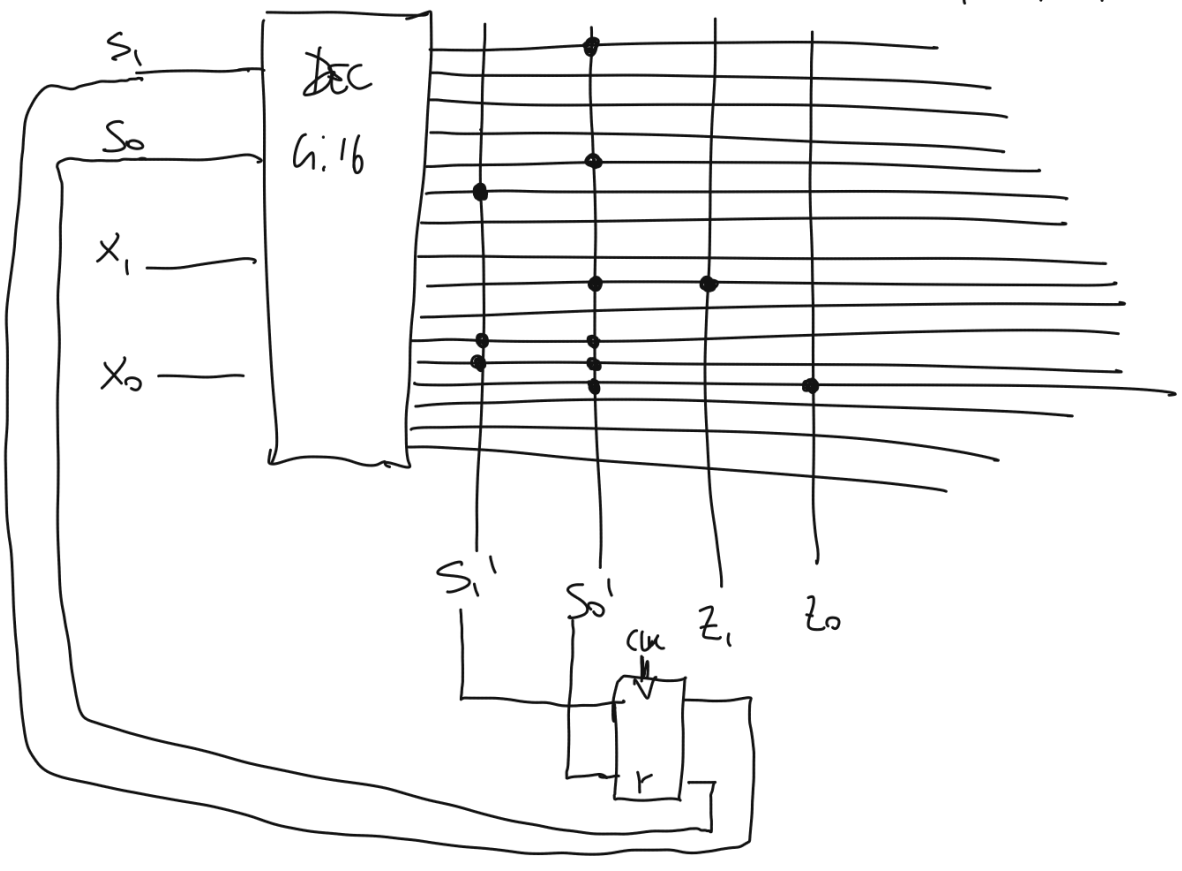
DSA Students should solve only the first 4 exercises (grade will be scaled accordingly)

Exercise 1 (7 points) Design a sequential circuit with two inputs x1, x0, that encode the characters B, R, I as shown on the table on the right. The circuit has 2 outputs z1 and z0. The circuit outputs z1=1 when it receives the sequence BRB, and z0=1 when it receives the sequence BRIB. Overlaps are allowed. Draw the FSM diagram, the state transition table, and the circuit.

x1, x0	character
00	B
01	R
1-	I



CS	S_1	S_0	INP.	X_1	X_0	NS	S_1'	S_0'	Z_1	Z_0
R	0	0	B	0	0	B	0	1	0	0
R	0	0	R	0	1	R	0	0	0	0
R	0	0	I	1	0	R	0	0	0	0
R	0	0	I	1	1	R	0	0	0	0
B	0	1	B	0	0	B	0	1	0	0
B	0	1	R	0	1	BR	1	0	0	0
B	0	1	I	1	0	R	0	0	0	0
B	0	1	I	1	1	R	0	0	0	0
BR	1	0	B	0	0	B	0	1	1	0
BR	1	0	R	0	1	R	0	0	0	0
BR	1	0	I	1	0	BRI	1	1	0	0
BR	1	0	I	1	1	BRI	1	1	0	0
BRI	1	1	B	0	0	B	0	1	0	1
BRI	1	1	R	0	1	R	0	0	0	0
BRI	1	1	I	1	0	R	0	0	0	0
BRI	1	1	I	1	1	R	0	0	0	0



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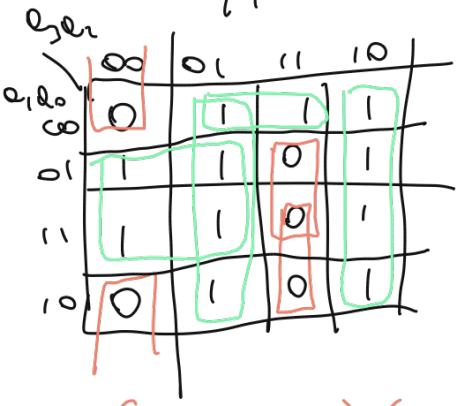
Exercise 2 (4 points) Design a circuit that computes how many days are in a given month. The month is specified by a 4-bit input $a_3a_2a_1a_0$. For example, if the inputs are (0001), the month is January, and if the inputs are (1100), the month is December. The output of the circuit Y_1 Y_0, must be equal to 11 only when the month specified on the input has 31 days, they must be equal to 10 when the input month has 30 days, and they must be equal to 01 when the input month has 28 days. The outputs must be equal to 00 in the remaining cases. Write down the truth table, and the minimal SOP and POS forms. Implement Y_0 using a 4-to-1 multiplexer.

DAYS	Q_3	Q_2	Q_1	Q_0	Y_1	Y_0
31	0	0	0	1	1	1
28	0	0	1	0	0	1
31	0	0	1	1	1	1
30	0	1	0	0	1	0
31	0	1	0	1	1	1
30	0	1	1	0	1	0
31	0	1	1	1	1	1
31	1	0	0	0	1	1
30	1	0	0	1	1	0
31	1	0	1	0	1	1
30	1	0	1	1	1	0
31	1	1	0	0	1	1
-	-	-	-	-	0	0

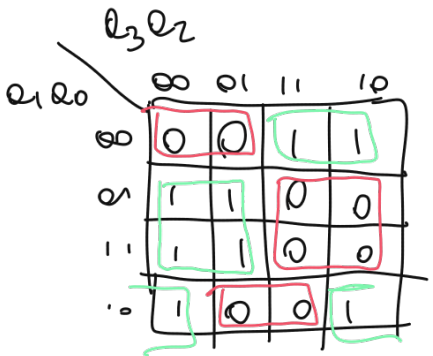
Y_1



$POS = (Q_3+Q_2+Q_0)(\overline{Q_3}+\overline{Q_2}+\overline{Q_0})(\overline{Q_3}+\overline{Q_2}+\overline{Q_1})$

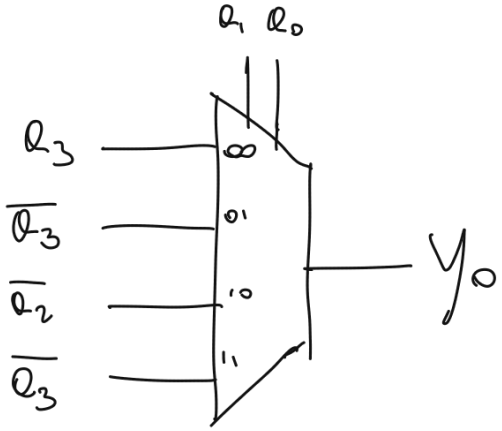
$SOP = Q_0\cdot\overline{Q_3} + \overline{Q_3}\cdot Q_2 + Q_3\cdot\overline{Q_2} + Q_2\overline{Q_1}\,\overline{Q_0}$

Y_0



$SOP = Q_3\overline{Q_1}\,\overline{Q_0} + \overline{Q_2}Q_1\overline{Q_0} + \overline{Q_3}Q_0$

$POS = (\overline{Q_3}+\overline{Q_0})(Q_3+Q_1+Q_0)(\overline{Q_2}+\overline{Q_1}+Q_0)$



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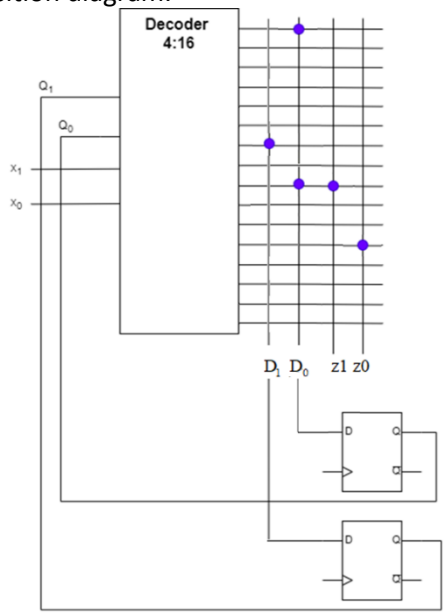
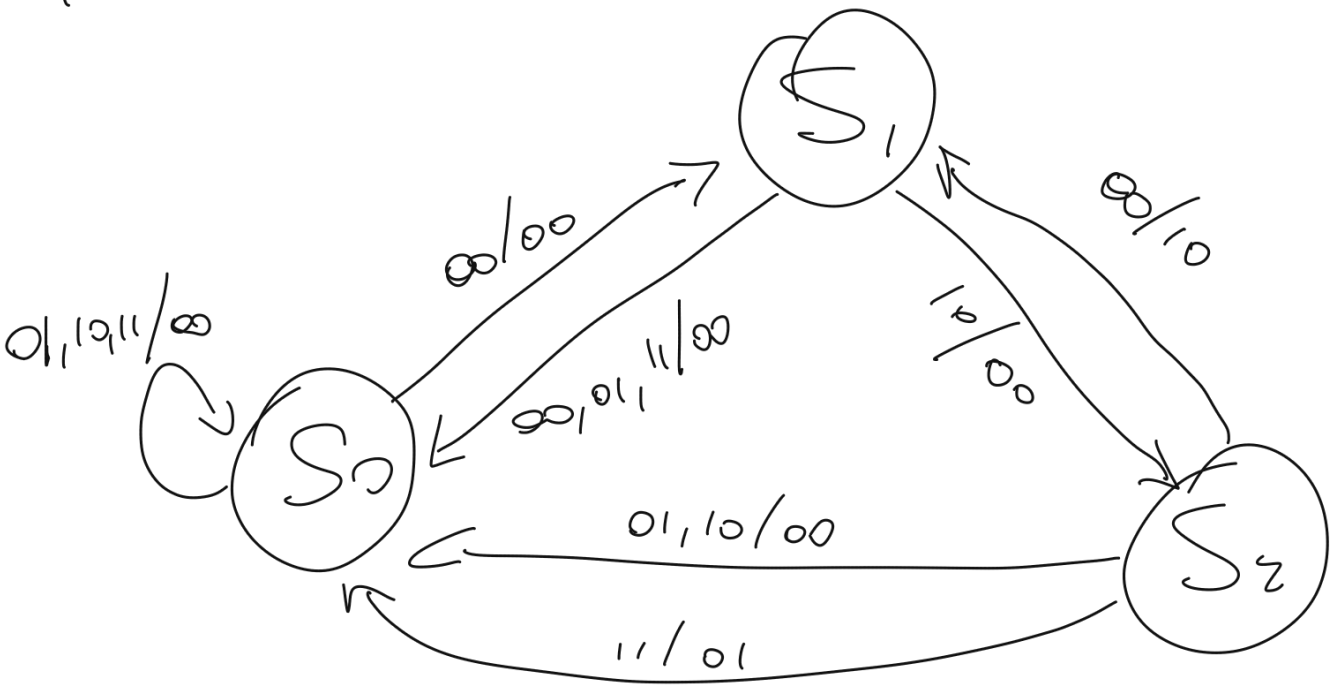
Exercise 3 (5 points) Analyze the sequential circuit in the figure below. Write down the next state table and the state transition diagram.



Q_1	Q_0	X_1	X_0	D_1	D_0	Z_1	Z_0
0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	1	1	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

$Q_1=1$ $Q_0=1$ IS UNREACHABLE

	Q_1	Q_0
S_0	0	0
S_1	0	1
S_2	1	0



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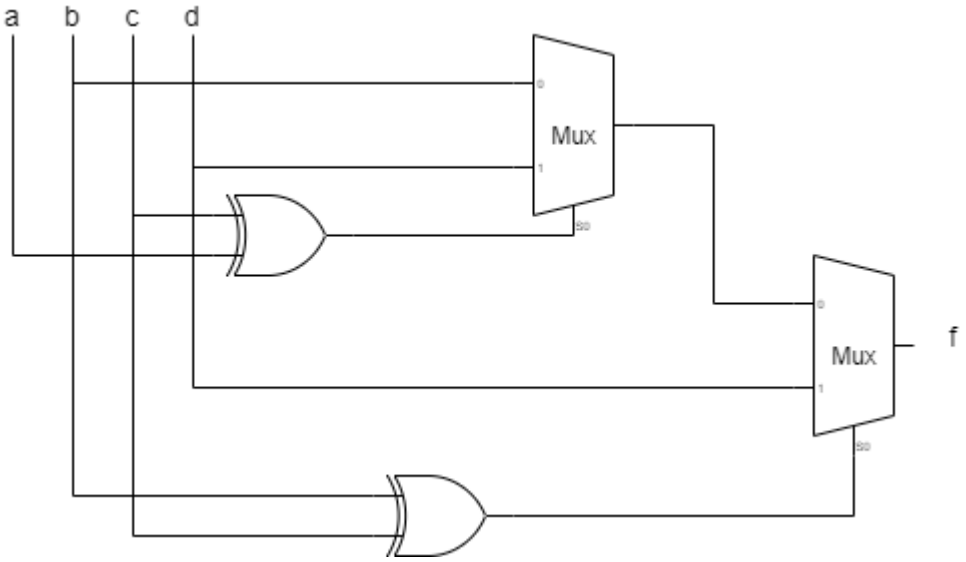
Exercise 4 (6 points)

- Consider the circuit depicted below and write down the boolean expression for the function *f*
- Transform the expression, using Boole's algebra axioms and theorems, to SOP form
- Write down the truth table for *f*
- Write down the minimal POS form for *f*



1) $f = \left[b(\overline{a \oplus c}) + d(a \oplus c)\right]\overline{b \oplus c} + d(b \oplus c) =$

2) $= b(bc + \bar{b}\bar{c})(ac + \bar{a}\bar{c}) + d(a\bar{c} + \bar{a}c)(bc + \bar{b}\bar{c}) + b\bar{c}d + \bar{b}cd =$

$= abc + d(a\bar{b}\bar{c} + \bar{a}bc) + b\bar{c}d + \bar{b}cd =$

$= abc + a\bar{b}\bar{c}d + \bar{a}bcd + b\bar{c}d + \bar{b}cd$

3)

abcd	f
0000	0
0001	0
0010	0
0011	1
0100	0
0101	1
0110	0
0111	1
1000	0
1001	1
1010	0
1011	1
1100	0
1101	1
1110	1
1111	1

4)

ab \ cd	00	01	11	10
00	0	0	1	0
01	0	1	1	0
11	0	1	1	1
10	0	1	1	0

$(b+d)(c+d)(a+d)(a+b+c)$

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Exercise 5 (4 points) Convert the base 10 number X = -320 in the IEEE 754 half-precision format and convert those 16 bits to a base-16 number. Then, convert the base-16 number Y = 5B00 to a binary string, and interpret that string as an IEEE 754 half-precision number. Compute X+Y in IEEE 754 half-precision, and convert the resulting 16 bits to a base-16 number.

$X = -320_{10}$ $\quad 320_{10} = 101000000 = 1.01 \times 2^8$

Sign = 1

biased exp. = 8+15 = 23 = 10111

mantissa = 0100000000

X = 1 10111 0100000000

D D 0 0

X = 0xDD00

Y = 0x5B00 = 0101 1011 0000 0000

sign b. exp. mantissa

b. exp = $1011_2 = 22_{10}$ -> exp = 22 - 15 = 7

$Y = +2^7 \cdot 1.11 = 0.111 \cdot 2^8 = 11100000_2 = 224_{10}$

$X = -1.01 \times 2^8$ $\xrightarrow{2s\ comp.}$ 01.01 -> 10.10 + 1 = 10.11

X+y = 10.110 + 00.111 = 11.101 $\xrightarrow{2s\ comp.}$ 00.010 + 1 = 00.011

$0.011 \times 2^8 =$

$= 01100000 =$

$= 96$

Thus, X+y = -96 =

$= -320 + 224$

$0.011 \times 2^8 = 1.1 \times 2^6$

X+y

Sign = 1

exp = 6 -> b. exp = 21 = 10101

mantissa = 1

X+y = 1 10101 1000000000

D 6 0 0

X+y = 0xD600

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Exercise 6 (4 points) Given the expression $f = \left(\bar{a} + \overline{b(b + \overline{cd})}\right) \oplus (\bar{a} + cd)$ simplify it and bring it to normal SOP form. Write the canonical form for f and implement f using NAND only.

$$f = \left(\overline{b(b + \overline{cd})} + \bar{a}\right) \oplus (\bar{a} + cd)$$

$$= \left(\overline{b + b\overline{cd}} + \bar{a}\right) \oplus (\bar{a} + cd)$$

$$= \left(\bar{a} + \bar{b}\right) \oplus (\bar{a} + cd)$$

$$= \overline{\left(\bar{a} + \bar{b}\right)}(\bar{a} + cd) + \left(\bar{a} + \bar{b}\right)\overline{(\bar{a} + cd)} =$$

$$= ab(\bar{a} + cd) + \left(\bar{a} + \bar{b}\right)a \cdot \overline{cd} = abcd + a\bar{b} \cdot \left(\bar{c} + \bar{d}\right) = abcd + a\bar{b}\bar{c} + a\bar{b}\bar{d}$$

$$a + a\overline{cde} = a \ (per\ assorbimento)$$

Forma Canonica

$$= abcd + a\bar{b}\bar{c}\bar{d} + a\bar{b}\bar{c}d + a\bar{b}c\bar{d}$$

Forma NAND:

$$NAND(NAND(a,b,c,d), NAND\left(a, NAND(b,b), NAND(c,c)\right), NAND\left(a, NAND(b,b), NAND(d,d)\right))$$

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