INTRODUCTION

The S6A0065 is a LCD driver IC which is fabricated by low power CMOS technology. Basically this IC consists of 20 x 2 bit bi-directional shift register, 20 x 2 bit data latch and 20 x 2 bit driver. (refer to Fig 1) This IC can be used as common or segment driver.

FUNCTION

- · Dot matrix LCD driver with 40 channel output.
- Selects function to use common/segment drivers simultaneously.
- Input / Output signal
 - Output: 20 x 2 channel waveform for LCD driving
 - Input: Serial display data and control signal from the controller LSI.
 Bias voltage (V₁-V₆)

FEATURES

Display driving bias: static - 1/5

Power supply voltage: 2.7- 5.5V

• Supply voltage for display: $3.0 - 13.0 \text{V} (V_{\text{LCD}} = V_{\text{DD}} - V_{\text{EE}})$

Interface

Driver (cascade connection)	Controller
Other S6A0065, S6A2067	S6A0069 S6A0070 S6A0073

- CMOS Process
- 64QFP or bare chip available



BLOCK DIAGRAM

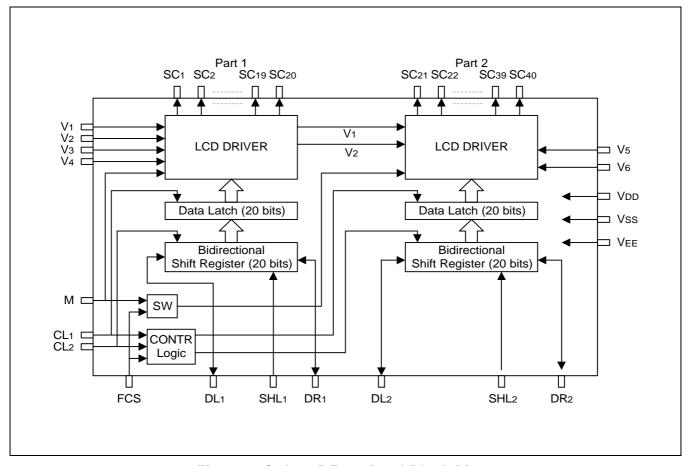


Figure 1. S6A0065 Functional Block Diagram



PIN CONFIGURATION

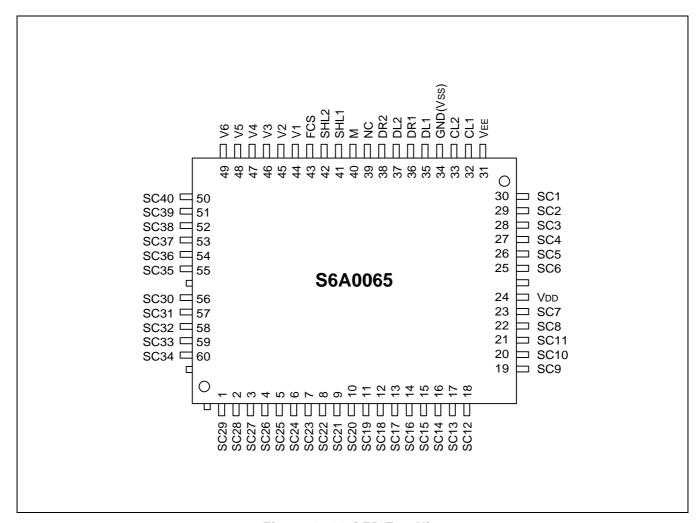
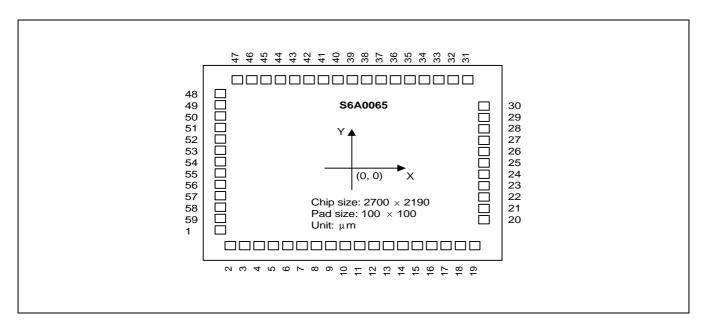


Figure 2. 60 QFP Top View



PAD DIAGRAM



NOTE: (0,0) is center in the chip.



PAD CENTER COORDINATES

Unit: um

PAD	PAD	COORDINATE		PAD	PAD	COORD	OINATE
NUMBER	NAME	Х	Υ	NUMBER	NAME	Х	Υ
1	VEE	-1120.2	-642.5	31	SC28	1117.5	865.2
2	CL1	-1062.5	-865.2	32	SC27	992.5	865.2
3	CL2	-937.5	-865.2	33	SC26	867.5	865.2
4	VSS	-812.5	-865.2	34	SC25	742.5	865.2
5	DL1	-687.5	-865.2	35	SC24	617.5	865.2
6	DR1	-562.5	-865.2	36	SC23	492.5	865.2
7	DL2	-437.5	-865.2	37	SC22	367.5	865.2
8	DR2	-312.5	-865.2	38	SC21	242.5	865.2
9	М	-187.5	-865.2	39	SC20	117.5	865.2
10	SHL1	-62.5	-865.2	40	SC19	-7.5	865.2
11	SHL2	62.5	-865.2	41	SC18	-132.5	865.2
12	FCS	187.5	-865.2	42	SC17	-257.5	865.2
13	V1	332.5	-865.2	43	SC16	-382.5	865.2
14	V2	457.5	-865.2	44	SC15	-507.5	865.2
15	V3	582.5	-865.2	45	SC14	-632.5	865.2
16	V4	707.5	-865.2	46	SC13	-757.5	865.2
17	V5	832.5	-865.2	47	SC12	-882.5	865.2
18	V6	957.5	-865.2	48	SC9	-1120.2	857.2
19	SC40	1082.5	-865.2	49	SC10	-1120.2	732.5
20	SC39	1120.2	-627.5	50	SC11	-1120.2	607.5
21	SC38	1120.2	-502.5	51	SC8	-1120.2	482.5
22	SC37	1120.2	-377.5	52	SC7	-1120.2	357.5
23	SC36	1120.2	-252.5	53	VDD	-1120.2	232.5
24	SC35	1120.2	-127.5	54	SC6	-1120.2	107.5
25	SC30	1120.2	-2.5	55	SC5	-1120.2	-17.5
26	SC31	1120.2	122.5	56	SC4	-1120.2	-142.5
27	SC32	1120.2	247.5	57	SC3	-1120.2	-267.5
28	SC33	1120.2	372.5	58	SC2	-1120.2	-392.5
29	SC34	1120.2	497.5	59	SC1	-1120.2	-517.5
30	SC29	1120.2	622.5				



PIN DESCRIPTION

Pin (No.)	I/O	Name		Description					Interface		
V _{DD} (24)		Operating Voltage For logical circuit (2.7 - 5.5V)						Power			
GND(34)	Power	0V (GND)								Supply	
V _{EE} (31)		Negative S	Negative Supply Voltage For LCD driver circuit								
V1, V2 (44,45)	I	Bias Volta	ge	Bi	Bias voltage level for LCD drive (select level)					Power	
SC ₁ - SC ₂₀	0		LCD driver	LCD driver output							LCD
V3, V4 (46, 47)	I	Part 1	Bias Voltage	Bia	Bias voltage level for LCD drive (non-select level)					Power	
SHL1(41)	I		Data interface		electio gister	n of the	shift direc	tion of Pa	rt 1 shift		V_{DD} or V_{SS}
						HL1	DL1		DR1		
						[/] DD	out		in		
					<u>`</u>	[/] ss	in		out		
DL1, DR1 (35, 36)	I/O			Da	Data input/output of Part 1 shift register				Controller or S6A0065		
SC ₂₁₋ SC ₄₀	0		LCD driver	LC	CD dri	ver outp	out				
V5, V6 (48, 49)	I	Part 2	Bias Voltage	Bias voltage level for LCD drive (non-select level)					Power		
SHL2(42)	I		Data interface	Selection of the shift direction of Part 2 shift register					V _{DD} or V _{SS}		
					SHL2 DL2 DR2						
						DD /oo	out		in		
DI O DDO	1/0	=		_	V _{SS} in out				0 (1)		
DL2,DR2 (37, 38)	I/O			Data input/output of Part 2 shift register				Controller or S6A0065			
M (40)	I		signal for LCD		PART	FCS	CL1	CL2	M polartty	,	Controller
014010		driver outp		ŀ		Vss	latch clock	shift clock	in polarity		
CL1,CL2 (32,33)	I	Data Shiit	/latch clock		1	VDD	│ →	→	М		
(= ,==,						Vss		_			
					2	VDD	latch clock	shift clock			
FCS(43)	I	Mode sele	ction	Shift/latch clock of display data and polarity of M signal are changed by FCS signal. By setting FCS to V _{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.							
NC(39)				No connection pin					NC		



MAXIMUM ABSOLUTE LIMT (Ta = 25° C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	- 0.3 to + 7.0	V
Driver Supply Voltage	V _{LCD}	V _{DD} - 15.0 to V _{DD} + 0.3	V
Input Voltage 1	V _{IN1}	- 0.3 to V _{DD} + 0.3	V
Input Voltage 2 (V ₁ - V ₆)	V _{IN2}	V _{DD} + 0.3 to V _{EE} - 0.3	V
Operating Temperature	T _{OPR}	- 30 to + 85	°C
Storage Temperature	T _{SRG}	- 55 to + 125	°C

^{*} Voltage greater than above may damage the circuit

ELECTRICAL CHARACTERSTICS

DC Characteristic \$ $V_{DD} = 2.7 - 5.5V$, $V_{DD} - V_{EE} = 3 - 13V$, $V_{SS} = 0V$, $V_{SS} = -30 - +85^{\circ}C$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	$f_{CL2} = 400kHz$	-	1	mA	-
Supply Current *	I _{EE}	f _{CL1} = 1kHz	-	10	μΑ	
Input High Voltage	V _{IH}	-	0.7V _{DD}	V _{DD}	V	CL1, CL2, DL1, DL2
Input Low Voltage	V _{IL}		0	0.3V _{DD}		DR1, DR2, SHL1, SHL2
Input Leakage Current	I _{LKG}	$V_{IN} = 0 - V_{DD}$	-5	5	μΑ	M, FCS
Output High Voltage	V _{OH}	I _{OH} = -0.4mA	V _{DD} -0.4	-		DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	$I_{OL} = +0.4$ mA	-	0.4	V	
Voltage Descending	V _{D1}	I _{ON} = 0.1mA for one of SC1-SC40	-	1.1		V(V1-V6)- SC(SC1-SC40)
	V _{D2}	I _{ON} = 0.05mA for each SC1-SC40	-	1.5		
Leakage Current	I _V	$V_{IN} = V_{DD} - V_{EE}$ (Output SC1-SC40 : floating)	-10	10	μΑ	V1-V6



^{*} V_{EE} : connect a protection resistor (220 Ω ± 5%)

AC Characteristic $V_{DD} = 2.7$ to 5.5V, $V_{DD} - V_{EE} = 3$ to 13V, $V_{SS} = 0$ V, Ta = -30 to +85 °C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f _{CL}	-	-	400	kHz	CL2
Clock High Level Width	t _{WCKH}	-	800	-		CL1, CL2
Clock Low Level Width	t _{WCKL}	-	800	-		CL2
Clock Set-up Time	t _{SL}	from CL2 to CL1	500	-	ns	
	t _{LS}	from CL1 to CL2	500	-		CL1, CL2
Clock Rise/Fall Time	t _R /t _F	-	-	200		
Data Set-up Time	t _{SU}	-	300	-		DL1, DL2, DR1, DR2, FLM
Data Hold Time	t _{DH}	-	300	-		
Data Delay Time	t _D	C _L = 15pF	-	500		DL1, DL2, DR1, DR2

^{*} Input/Output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at "H" or "L".



TIMING CHARACTERISTCS

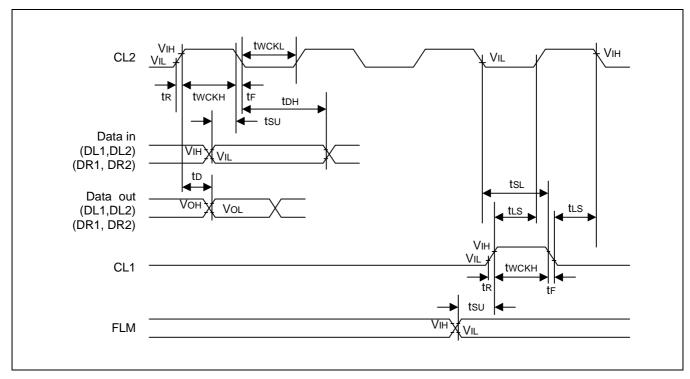


Figure 3. AC characteristics

FUNCTIONAL DESCRIPTON

1) To Drive Segment Type

When the FCS is connected to V_{SS} , S6A0065 (SC1-SC40) is operated as segment driver.(refer to Fig 4)

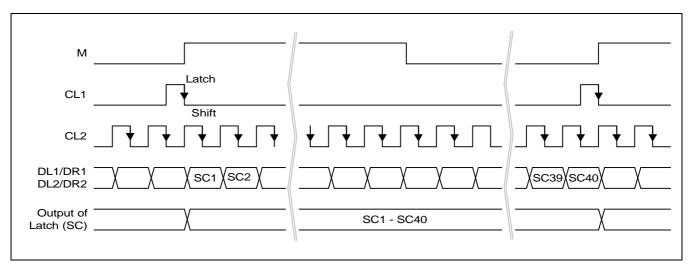


Figure 4. Segment Data Waveform



2) To Drive Common Type

When the FCS is connected to V_{DD} , only part2 (SC21-SC40) of S6A0065 is operated as common driver. (refer to Fig 5).

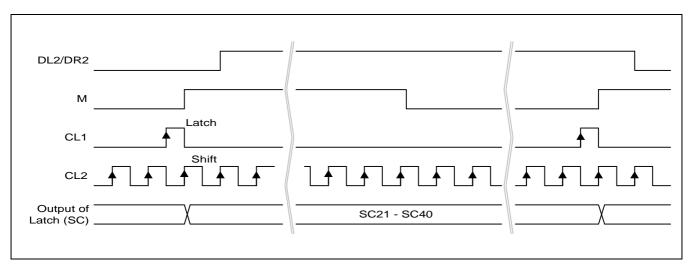


Figure 5. Common Data Waveforms

LCD OUTPUT WAVEFORMS

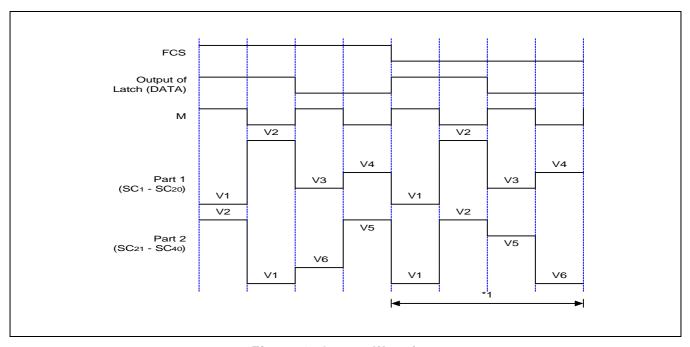


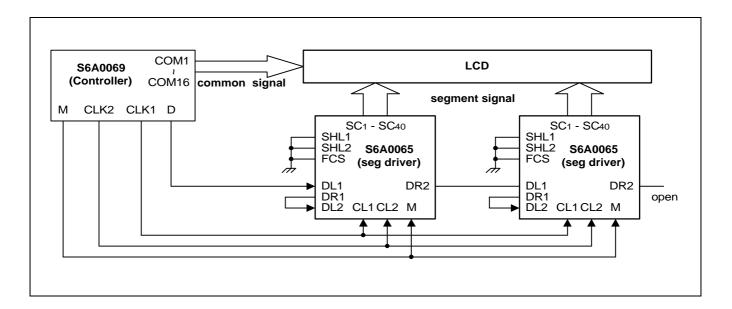
Figure 6. Output Waveforms

*1: To use for same function of part 1 and part 2, V3 and V5, V4 and V6 of power supply for LCD drive are short circuited respectively.

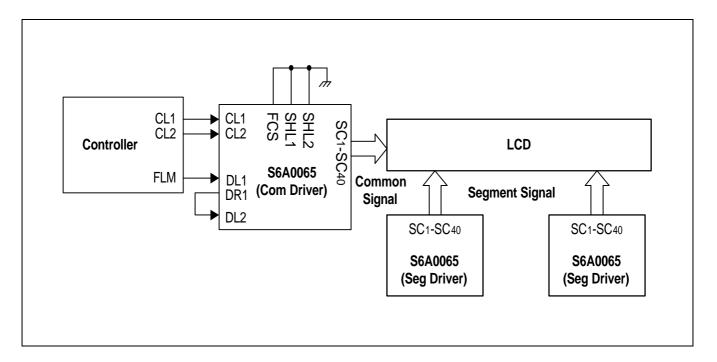


APPLICATION CIRCUIT

1) Segment Driver



2) Common Driver





3) Segment / Common Driver

