Laboratory Exercise 9

A Simple Processor

Figure 1 shows a digital system that contains a number of nine-bit registers, a multiplexer, an adder/subtractor unit, and a control unit (finite state machine). Data is input to this system via the nine-bit *DIN* input. This data can be loaded through the nine-bit wide multiplexer into the various registers, such as $R0, \ldots, R7$ and *A*. The multiplexer also allows data to be transferred from one register to another. The multiplexer's output wires are called a *bus* in the figure because this term is often used for wiring that allows data to be transferred from one location in a system to another.

Addition or subtraction of signed numbers is performed by using the multiplexer to first place one nine-bit number onto the bus wires and loading this number into register *A*. Once this is done, a second nine-bit number is placed onto the bus, the adder/subtractor unit performs the required operation, and the result is loaded into register *G*. The data in *G* can then be transferred to one of the other registers as required.

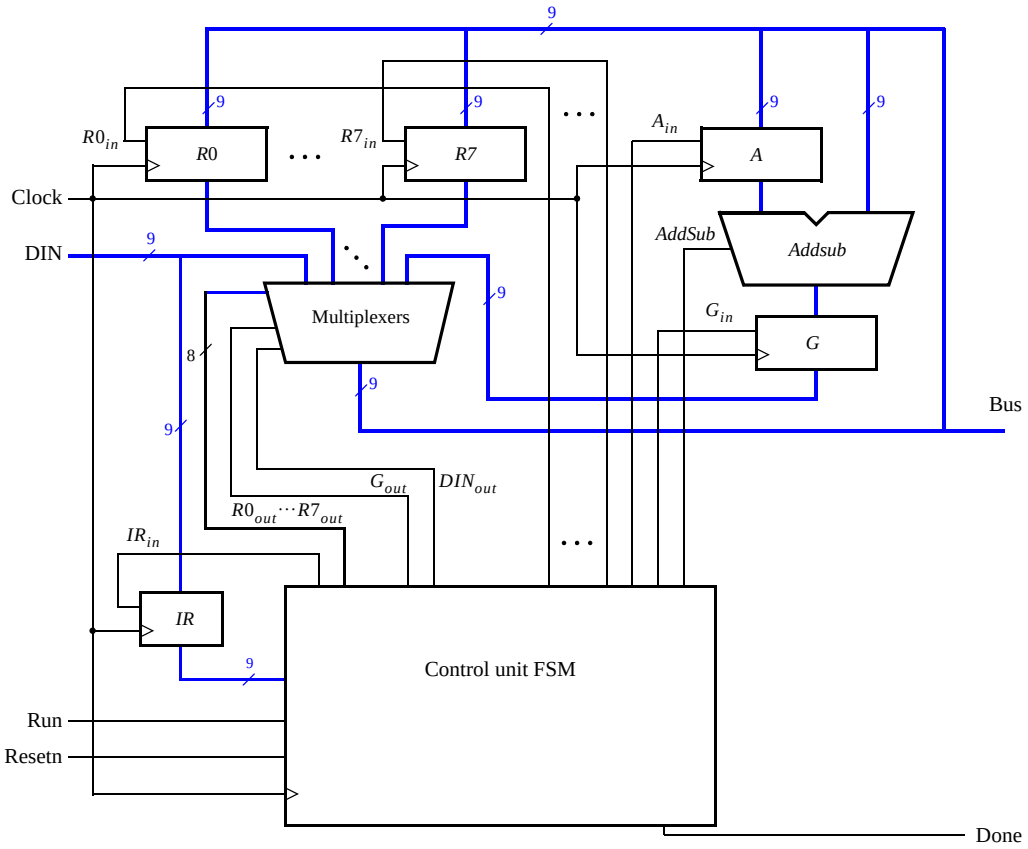

Figure 1: A digital system.

The system can perform different operations in each clock cycle, as governed by the *control unit*. This unit determines when particular data is placed onto the bus wires and it controls which of the registers is to be loaded with this data. For example, if the control unit asserts the signals $R0_{out}$ and A_{in}, then the multiplexer will place the contents of register $R0$ onto the bus and this data will be loaded on the next active clock edge into register *A*.

A system like the one in Figure 1 is often called a *processor*. It executes operations specified in the form of *instructions*. Table 1 lists the instructions that the processor has to support for this exercise. The left column shows the name of an instruction and its operands. The meaning of the syntax R$x \leftarrow$ [Ry] is that the contents of register Ry are loaded into register Rx. The **mv** (move) instruction allows data to be copied from one register to another. For the **mvi** (move immediate) instruction the expression R$x \leftarrow$ D indicates that the nine-bit constant D is loaded into register Rx.

Operation	Function performed
mv Rx,Ry	$Rx \leftarrow [Ry]$
mvi Rx,#D	$Rx \leftarrow D$
add Rx, Ry	$Rx \leftarrow [Rx] + [Ry]$
sub Rx, Ry	$Rx \leftarrow [Rx] - [Ry]$

Table 1: Instructions performed in the processor.

Each instruction can be encoded using the nine-bit format *IIIXXXYYY*, where *III* specifies the instruction, *XXX* gives the Rx register, and *YYY* gives the Ry register. Although only two bits are needed to encode our four instructions, we are using three bits because other instructions will be added to the processor in later parts of the exercise. Assume that *III* = 000 for the **mv** instruction, 001 for **movi**, 010 for **add**, and 011 for **sub**. Instructions are loaded from the the external input *DIN*, and stored into the *IR* register, using the connection indicated in Figure 1. For the **mvi** instruction the *YYY* field has no meaning, and the immediate data #*D* has to be supplied on the *DIN* input in the clock cycle after the **mvi** instruction word is stored into *IR*.

Some instructions, such as an addition or subtraction, take more than one clock cycle to complete, because multiple transfers have to be performed across the bus. The finite state machine in the control unit "steps through" such instructions, asserting the control signals needed in successive clock cycles until the instruction has completed. The processor starts executing the instruction on the *DIN* input when the *Run* signal is asserted and the processor asserts the *Done* output when the instruction is finished. Table 2 indicates the control signals that can be asserted in each time step to implement the instructions in Table 1. Note that the only control signal asserted in time step 0 is IR_{in}, so this time step is not shown in the table.

	T_1	T_2	T_3
(**mv**): I_0	RY_{out}, RX_{in}, *Done*		
(**mvi**): I_1	DIN_{out}, RX_{in}, *Done*		
(**add**): I_2	RX_{out}, A_{in}	RY_{out}, G_{in}	G_{out}, RX_{in}, *Done*
(**sub**): I_3	RX_{out}, A_{in}	RY_{out}, G_{in}, *AddSub*	G_{out}, RX_{in}, *Done*

Table 2: Control signals asserted in each instruction/time step.

Part I

Design and implement the processor shown in Figure 1 using VHDL code as follows:

1. Create a new Quartus project for this exercise.
2. Generate the required VHDL file, include it in your project, and compile the circuit. A suggested skeleton of the VHDL code is shown in parts a and b of Figure 2, and some subcircuit entities that can be used in this code appear in Figure 2c.
3. Use functional simulation to verify that your code is correct. An example of the output produced by a functional simulation for a correctly-designed circuit is given in Figure 3. It shows the value $(010)_8$ being loaded into *IR* from *DIN* at time 30 ns. This pattern represents the instruction **mvi** R0,#D, where the value $D = 5$ is loaded into $R0$ on the clock edge at 50 ns. The simulation then shows the instruction **mv** R1,R0 at 90 ns, **add** R0,R1 at 110 ns, and **sub** R0,R0 at 190 ns. Note that the simulation output shows *DIN* and *IR* in octal, and it shows the contents of other registers in hexadecimal.
4. Now, create another Quartus project which will be used for implementation of the circuit on your Intel FPGA DE-series board. This project should consist of a top-level module that contains the appropriate input and output ports for the DE-series board. Instantiate your processor in this top-level module. Use switches SW_{8-0} to drive the *DIN* input port of the processor and use switch SW_9 to drive the *Run* input. Also, use pushbutton KEY_0 for *Resetn* and KEY_1 for *Clock*. Connect the processor bus wires to $LEDR_{8-0}$ and connect the *Done* signal to $LEDR_9$.
5. Add to your project the necessary pin assignments for your board. Compile the circuit and download it into the FPGA chip.
6. Test the functionality of your circuit by toggling the switches and observing the LEDs. Since the processor's clock input is controlled by a pushbutton switch, it is possible to step through the execution of instructions and observe the behavior of the circuit.

```
LIBRARY ieee; USE ieee.std_logic_1164.all;
USE ieee.std_logic_signed.all;

ENTITY proc IS
   PORT ( DIN                  : IN     STD_LOGIC_VECTOR(8 DOWNTO 0);
          Resetn, Clock, Run   : IN     STD_LOGIC;
          Done                 : BUFFER STD_LOGIC;
          BusWires             : BUFFER STD_LOGIC_VECTOR(8 DOWNTO 0));
END proc;

ARCHITECTURE Behavior OF proc IS
   . . . declare components
   . . . declare signals
   TYPE State_type IS (T0, T1, T2, T3);
   SIGNAL Tstep_Q, Tstep_D: State_type;
   . . .
BEGIN
   High <= '1';
   I <= IR(1 TO 3);
   decX: dec3to8 PORT MAP (IR(4 TO 6), High, Xreg);
   decY: dec3to8 PORT MAP (IR(7 TO 9), High, Yreg);
```

Figure 2: Skeleton VHDL code for the processor. (Part a)

```
    statetable: PROCESS (Tstep_Q, Run, Done)
    BEGIN
        CASE Tstep_Q IS
            WHEN T0 => IF(Run = '0') THEN Tstep_D <= T0;
                       ELSE Tstep_D <= T1;
                       END IF; - - data is loaded into IR in this time step
            . . . other states
        END CASE;
    END PROCESS;

    controlsignals: PROCESS (Tstep_Q, I, Xreg, Yreg)
    BEGIN
        . . . specify initial values
        CASE Tstep_Q IS
            WHEN T0 => - - store DIN in IR as long as Tstep_Q = 0
                IRin <= '1';
            WHEN T1 => - - define signals in time step T1
                CASE I IS
                    . . .
                END CASE;
            WHEN T2 => - - define signals in time step T2
                CASE I IS
                    . . .
                END CASE;
            WHEN T3 => - - define signals in time step T3
                CASE I IS
                    . . .
                END CASE;
        END CASE;
    END PROCESS;

    fsmflipflops: PROCESS (Clock, Resetn, Tstep_D)
    BEGIN
        . . .
    END PROCESS;

    reg_0: regn PORT MAP (BusWires, Rin(0), Clock, R0);
    . . . instantiate other registers and the adder/subtractor unit
    . . . define the bus
END Behavior;
```

Figure 2: Skeleton VHDL code for the processor. (Part b)

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY dec3to8 IS
   PORT ( W     : IN     STD_LOGIC_VECTOR(2 DOWNTO 0);
          En    : IN     STD_LOGIC;
          Y     : OUT    STD_LOGIC_VECTOR(0 TO 7));
END dec3to8;

ARCHITECTURE Behavior OF dec3to8 IS
BEGIN
   PROCESS (W, En)
   BEGIN
      IF En = '1' THEN
         CASE W IS
            WHEN "000" => Y <= "10000000";
            WHEN "001" => Y <= "01000000";
            WHEN "010" => Y <= "00100000";
            WHEN "011" => Y <= "00010000";
            WHEN "100" => Y <= "00001000";
            WHEN "101" => Y <= "00000100";
            WHEN "110" => Y <= "00000010";
            WHEN "111" => Y <= "00000001";
         END CASE;
      ELSE
         Y <= "00000000";
      END IF;
   END PROCESS;
END Behavior;

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY regn IS
   GENERIC (n : INTEGER := 9);
   PORT ( R             : IN     STD_LOGIC_VECTOR(n-1 DOWNTO 0);
          Rin, Clock    : IN     STD_LOGIC;
          Q             : BUFFER STD_LOGIC_VECTOR(n-1 DOWNTO 0));
END regn;

ARCHITECTURE Behavior OF regn IS
BEGIN
   PROCESS (Clock)
   BEGIN
      IF Clock'EVENT AND Clock = '1' THEN
         IF Rin = '1' THEN
            Q <= R;
         END IF;
      END IF;
   END PROCESS;
END Behavior;
```

Figure 2: Subcircuit entities for use in the processor. (Part c)

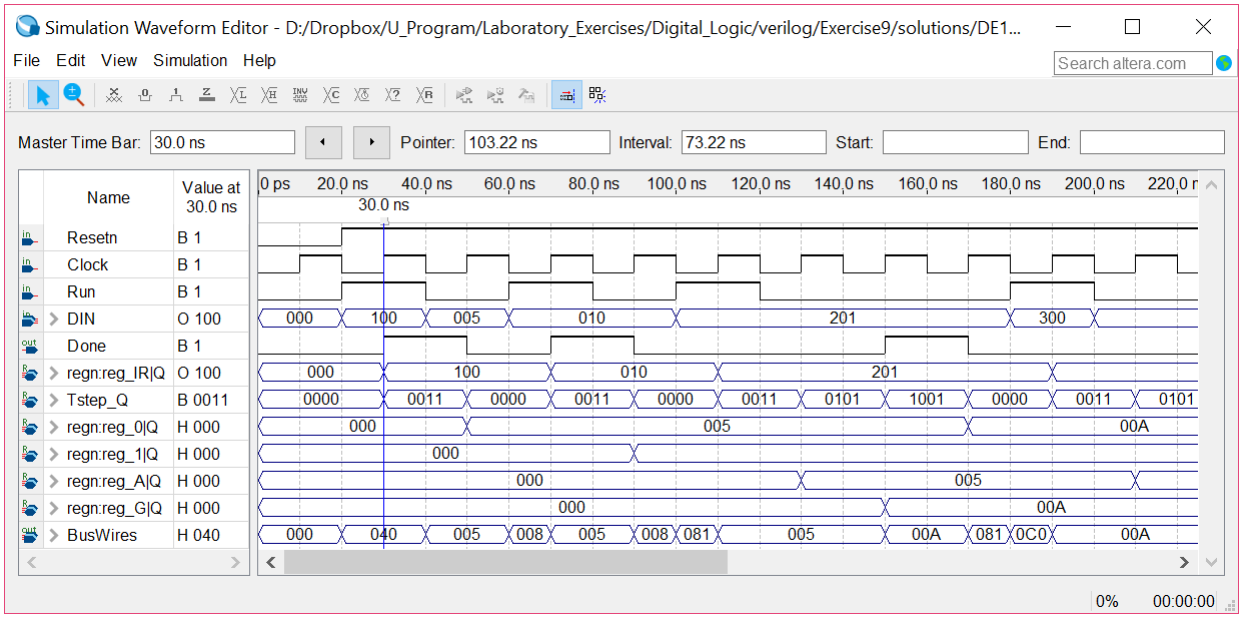

Figure 3: Simulation result for the processor.

Part II

In this part you are to design the circuit depicted in Figure 4, in which a memory module and counter are connected to the processor from Part I. The counter is used to read the contents of successive addresses in the memory, and this data is provided to the processor as a stream of instructions. To simplify the design and testing of this circuit we have used separate clock signals, *PClock* and *MClock*, for the processor and memory.

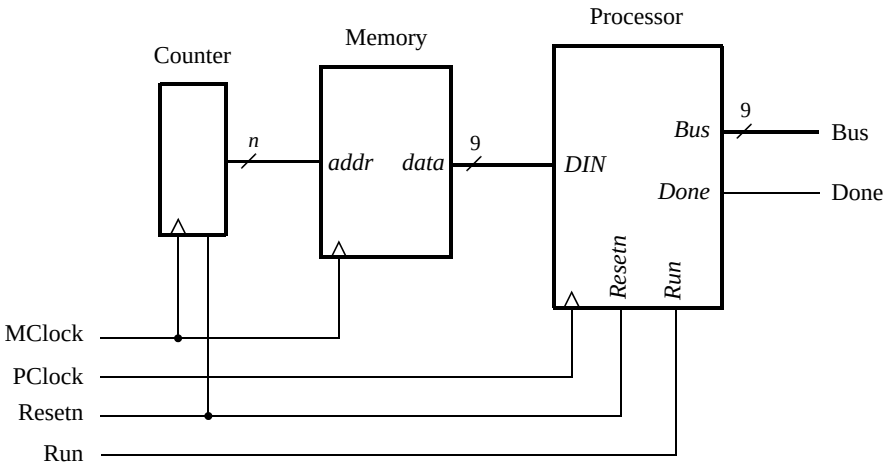

Figure 4: Connecting the processor to a memory and counter.

1. Create a new Quartus project which will be used to test your circuit.

2. Generate a top-level VHDL file that instantiates the processor, memory module, and counter.

   A diagram of the memory module that we need to create is depicted in Figure 5. Since this memory module has only a read port, and no write port, it is called a *synchronous read-only memory (synchronous ROM)*.

Note that the memory module includes a register for synchronously loading addresses. This register is required due to the design of the memory resources in the Intel FPGA chip. Use the Quartus IP Catalog tool to create the memory module, by clicking on Tools > IP Catalog. In the IP Catalog window choose the *ROM: 1-PORT* module, which is found under the Basic Functions > On Chip Memory category. Select VHDL as the type of output file to create, and give the file the name *inst_mem.vhd*.

Follow through the provided sequence of dialogs to create a memory that has one nine-bit wide read data port and is 32 words deep. Figures 6 and 7 show the relevant pages and how to properly configure the memory.

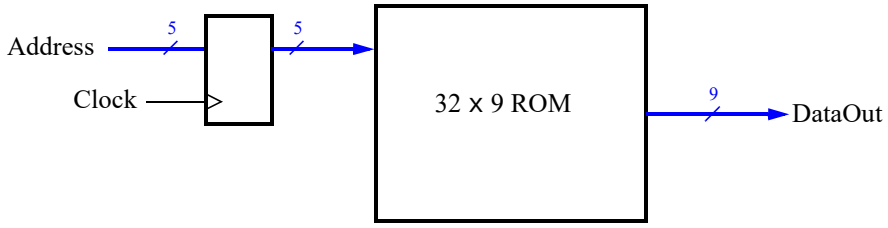

Figure 5: The 32 x 9 ROM with address register.

To place processor instructions into the memory, you need to specify *initial values* that should be stored in the memory once your circuit has been programmed into the FPGA chip. This can be done by initializing the memory using the contents of a *memory initialization file (MIF)*. The appropriate screen is illustrated in Figure 8. We have specified a file named *inst_mem.mif*, which then has to be created in the folder that contains the Quartus project. An example of a memory initialization file is given in Figure 9. Note that comments (% ... %) are included in this file as a way of documenting the meaning of the provided instructions. Set the contents of your *MIF* file such that it provides enough processor instructions to test your circuit.

3. Make sure your project includes the necessary port names and pin location assignments to implement the circuit on your DE-series board. Use switch SW_9 to drive the processor's *Run* input, use SW_0 for *Resetn*, use KEY_0 for *MClock*, and use KEY_1 for *PClock*. Connect the processor bus wires to $LEDR_{8-0}$ and connect the *Done* signal to $LEDR_9$.

4. Compile your VHDL code and use functional simulation to test the circuit. Ensure that instructions are read properly out of the ROM and executed by the processor. An example of functional simulation using the MIF file from Figure 9 is shown in Figure 10.

5. Once your simulation shows a properly-working circuit, download it into the FPGA chip. Test the functionality of your design on the DE-series board by toggling the switches and observing the LEDs. Since the circuit's clock inputs are controlled by pushbutton switches, it is possible to step through the execution of instructions and observe the behavior of the circuit.

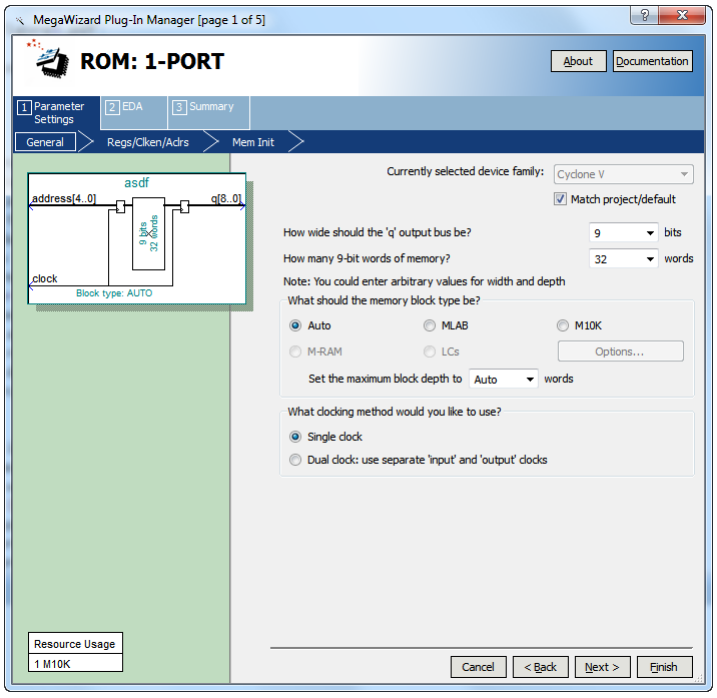

Figure 6: Specifying memory size.

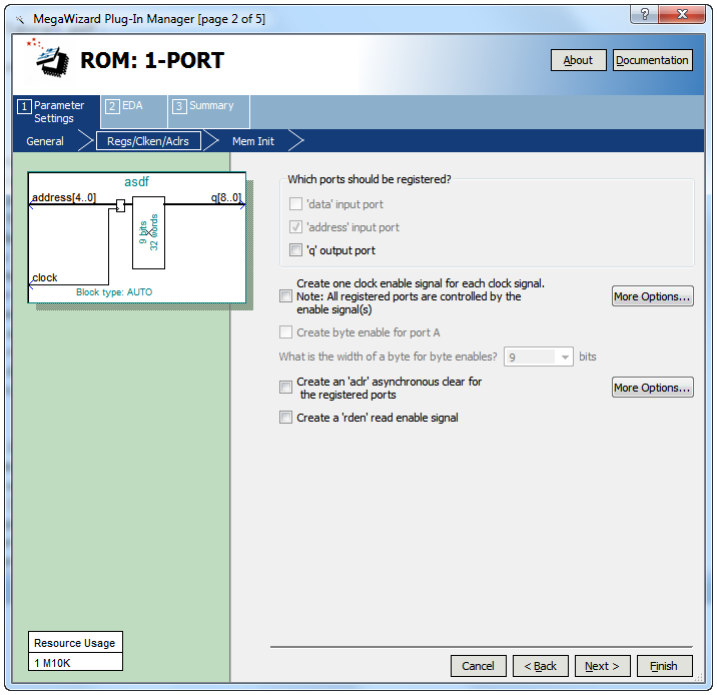

Figure 7: Specifying which memory ports are registered.

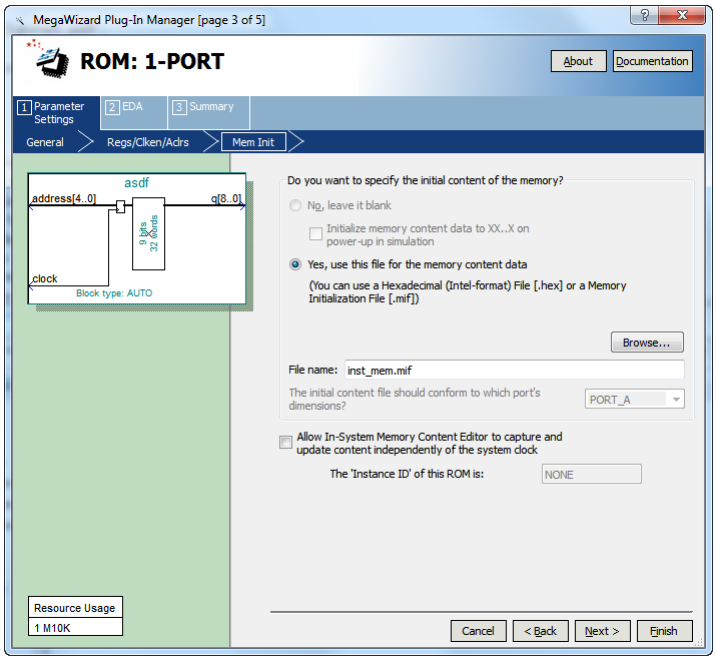

Figure 8: Specifying a memory initialization file (MIF).

```
DEPTH = 32;
WIDTH = 9;
ADDRESS_RADIX = HEX;
DATA_RADIX = BIN;
CONTENT
BEGIN

00 : 001000000;     % mvi r0,#5       %
01 : 000000101;
02 : 000001000;     % mv r1,r0        %
03 : 010000001;     % add r0, r1      %
04 : 011000000;     % sub r0, r0      %
05 : 000000000;
06 : 000000000;
. . . (some lines not shown)
1E : 000000000;
1F : 000000000;

END;
```

Figure 9: An example memory initialization file (MIF).

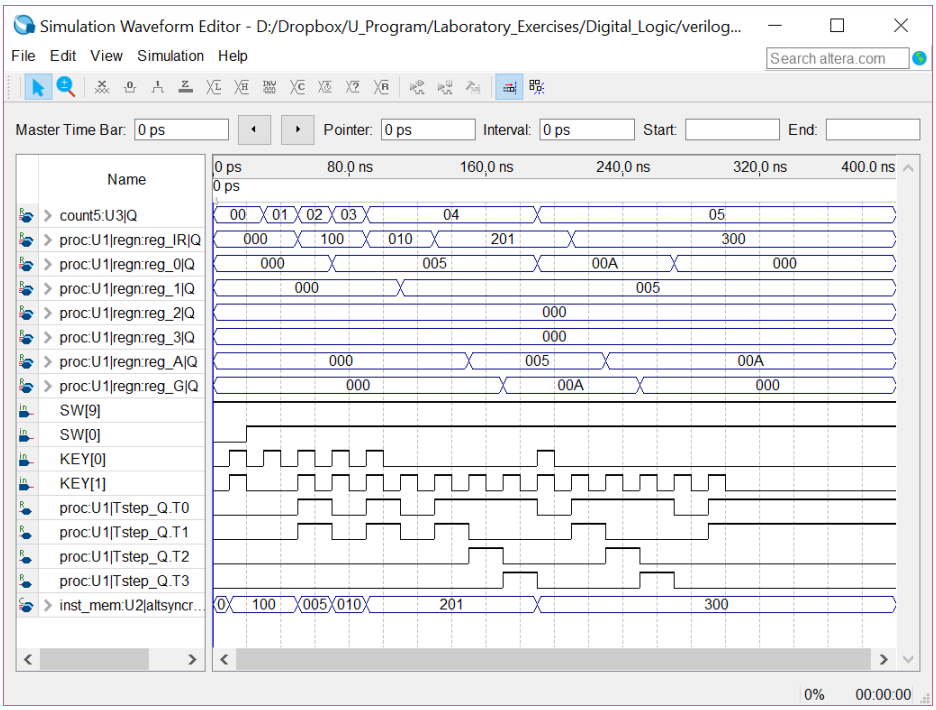

Figure 10: An example simulation output using the MIF in Figure 9.

Enhanced Processor

It is possible to enhance the capability of the processor so that the counter in Figure 4 is no longer needed, and so that the processor has the ability to perform read and write operations using memory or other devices. These enhancements involve adding new instructions to the processor and the programs that the processor executes are therefore more complex; they are described in Laboratory Exercise 10.