Cheng-En Tsai

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Website

EDUCATION

National Taiwan University — Taipei, Taiwan

B.S. in Electrical Engineering — Sep. 2021 – Dec. 2025

- **Overall GPA:** 4.16/4.3
- **Honors:** Dean's List Awards (2021 Fall, 2024 Spring)
- **Coursework:** Special Topics on Quantum Design Automation(A), Introduction to Electronic Design Automation(A+), Quantum Information and Computation(A+), Computer Architecture(A+), Machine Learning(A+)

PUBLICATIONS

[1] C.-T. Kuo, **C.-E. Tsai** and C.-Y. R. Huang, "A Novel Ultra-Low Logic Step Fault-Tolerant Quantum Circuit Synthesis via Lattice Surgery," accepted to *Design, Automation and Test in Europe (DATE 2026)*.

[2] **C.-E. Tsai** and H.-C. Cheng, "Resource-efficient and robust quantum federated learning via loss aggregation," submitted to *Proceedings of the National Academy of Sciences (PNAS)*.

[3] M.-T. Lau et al., including **C.-E. Tsai** and C.-Y. R. Huang, "Qsyn: A developer-friendly quantum circuit synthesis framework for NISQ era and beyond," in *2024 IEEE International Conference on Quantum Computing and Engineering (QCE)*, pp. 535–536, IEEE, Sept. 2024.

WORK EXPERIENCE

Google — New Taipei, Taiwan

Hardware Engineering Intern — Jun. 2025 – Sep. 2025

- Developed a Python-based automation tool for schematic and layout review, surpassing Cadence's Electrical Rule Checker (ERC) with customizable rule checks, signal integrity diagnostics, and an intuitive PyQt5-powered GUI.
- Implemented advanced features including In-Board Measuring Point analysis aligned with Intel AIBC standards, automated derating checks, and design comparison, significantly reducing manual review time.
- Enabled compatibility with Cadence Allegro PCB Editor via Extracta and Design Entry HDL, showcasing adaptability across industry-standard EDA tools for schematic and board-level design.

RESEARCH EXPERIENCE

Design Verification Lab, NTU — Jan. 2023 – Present

Undergraduate Researcher | Advisor: Prof. Chung-Yang (Ric) Huang

An Ultra-Low Logic Step Fault-Tolerant Quantum Circuit Synthesis via Lattice Surgery

- Developed FTQCS, a ZX-calculus–based synthesis framework that compiles quantum circuits into lattice-surgery schedules for surface-code execution.
- Reduced asymptotic space–time cost from $O(n^3)$ to $O(n^2)$ and demonstrated over 148× execution speedup and up to 8.4× lower overhead compared to prior compilers.

Qsyn: A Developer-Friendly Quantum Circuit Synthesis Framework [**Github**] [**arXiv**]

- Designed and implemented an end-to-end quantum circuit synthesis tool in C++ by integrating optimization algorithms to enhance efficiency and scalability.
- Applied Gray-code synthesis to translate tensor decompositions into quantum gates and enable structured optimization with given gate sets.

Quantum Information Lab, NTU — Feb. 2024 – Present

Undergraduate Researcher | Advisor: Prof. Hao-Chung Cheng

LossAgg-QFL: A resource-efficient and robust quantum federated learning via loss aggregation [**GitHub**]

- Proposed LossAgg-QFL, a communication-efficient, gradient-free quantum federated learning framework where clients transmit only scalar losses, enabling scalable training on non-IID data and compatibility with NISQ devices.
- Achieved up to 48.1% accuracy improvement over FedAdam on MNIST under non-IID settings, while reducing communication and circuit executions from parameter-dependent $\mathcal{O}(p)$ to constant $\mathcal{O}(1)$ per iteration.

Human Computer Interaction Lab, NTU Jan. 2023 – Jun. 2023

Undergraduate Researcher | Advisor: Prof. Mike Y. Chen

CrossHaptics: Real-time Haptic Feedback for VR Games via Vibration Pattern Analysis

- Designed a C# program to automatically capture VR controller vibration patterns from game developers, enabling support for additional haptic devices in all VR games.
- Conducted user studies and analyzed feedback to refine system performance and user experience iteratively.

SELECTED PROJECTS

T-Count Optimization Framework for Clifford+T Quantum Circuits [**Report**] Apr. 2024 – Jun. 2024

Quantum Information and Computation

- Designed a unified T-count optimization framework that integrates multiple reduction techniques including TMerge, Internal-H-OPT and advanced phase polynomial methods such as TODD for efficient circuit synthesis.
- Enhanced overall circuit efficiency by combining Gray synthesis (GraySyn) with T-parallelism (T-Par) strategies to exploit structural regularities and gate-level concurrency.

Reinforcement Logic Optimization for a General Cost Function [**Github**] [**Report**] Apr. 2024 – Jun. 2024

Electronic Design Automation

- Developed a program to optimize digital circuits based on a black-box cost estimator, addressing complex objectives beyond traditional PPA metrics.
- Implemented the A2C reinforcement learning algorithm and Simulated Annealing on Yosys-ABC, achieving up to 55.3% improvement in loss compared to the Greedy algorithm.

Quantum Circuit Enumeration with Unitary Matrix [**Report**] Nov. 2023 – Jan. 2024

Quantum Design Automation

- Implemented a synthesis framework that generates quantum circuits directly from arbitrary unitary matrices through two-level matrix decomposition and Gray-code synthesis for efficient multi-qubit control realization.
- Implemented analytical phase reconstruction and decomposition into native gate sets, achieving compact, functionally equivalent circuits with minimized depth and gate count.

TEACHING EXPERIENCE

Quantum Information and Computation (COMME5061) Feb. 2025 – Jun. 2025

Teaching Assistant | Instructor: Prof. Hao-Chung Cheng

- Supported graduate-level quantum computing coursework by designing exams, grading assignments, answering student inquiries on quantum information theory, and guiding final project development.

Cornerstone EECS Design and Implementation (EE1006) Feb. 2025 – Jun. 2025

Teaching Assistant | Instructor: Prof. Ho-Lin Chen and Prof. Chia-Yi Yeh

- Guided first-year EE students in building line-tracing autonomous vehicles and self-proposed projects, developing maker skills in both hardware and software.

LEADERSHIP

NTUEE Summer Camp Oct. 2023 – Jul. 2024

Coordinator

- Led a team of 100+ electrical engineering students to organize a 7-day educational camp for 120 high school students across Taiwan, introducing core EE concepts through hands-on activities and lectures.

NTUEE × DFLL Orientation Camp Jan. 2023 – Aug. 2023

Vice Coordinator

- Led 80+ EE and DFLL students to host a 3-day orientation camp for incoming freshmen, designing interactive activities to foster cross-department engagement and community building.

TECHNICAL SKILLS

Languages: Mandarin (Native), English (Fluent, TOEFL iBT 108: R29/L30/S23/W26, GRE 321: V151/Q170/W3.5)

Programming Languages: C/C++/Arduino, Python, Verilog, JavaScript/CSS/HTML, Go

Developer Tools: RPi, git, MBed OS, STM32CubeIDE, vim