EEE 5320
Cadence Assignment #1

Objective:

1. Introduce the Cadence simulation environment
2. Become familiar with DC and parametric analysis in Cadence
3. Gain understanding about MOS device characteristics

Background:

Cadence's Analog Design Environment (ADE) is the tool you will use to simulate your design. It allows you to run many types of simulations (DC, AC, transient, etc.) with full control over design variables, temperature, process variations, and more. The ADE has multiple simulators within the environment that are SPICE-based.

Procedure:

1. In Cadence, create a schematic and draw the circuit shown in Fig. 1.

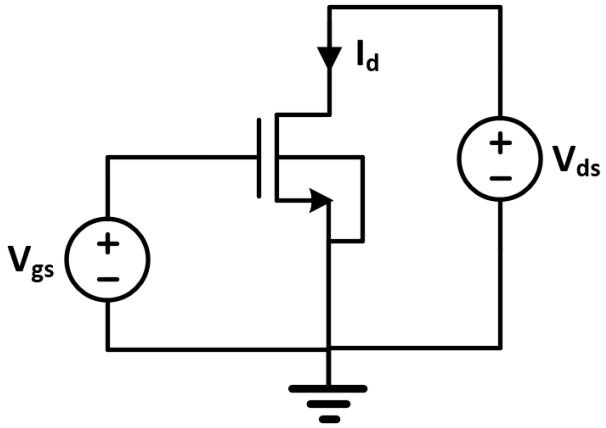

Figure 1: NMOS Circuit for DC Simulation

2. Use DC voltage sources for V_{gs} and V_{ds}. Set the NMOS aspect ratio to $\frac{W}{L} = \frac{3\mu m}{0.24\mu m}$
    a. To instantiate a DC voltage source, in the 'Add Instance' dialog box set:
        i. 'Library' -> analogLib
        ii. 'Cell' -> vdc
        iii. 'View' -> symbol
    b. To instantiate the ground symbol, in the 'Add Instance' dialog box set:
        i. 'Library' -> analogLib
        ii. 'Cell' -> gnd
        iii. 'View' -> symbol

    c. To instantiate a 4-terminal NMOS transistor, in the 'Add Instance' dialog box set:

i. ‘Library’ -> gpdk180
ii. ‘Cell’ -> nmos
iii. ‘View’ -> symbol

3. Instead of setting the DC voltage of each source to a fixed value, you can assign a variable to the DC voltage parameter. Here you can set the V_{gs} and V_{ds} DC voltages to vgs and vds, respectively.
4. On the toolbar of the schematic window, click on Launch > ADE L. It will open a simulation window that looks like the one shown in Fig. 2 below.

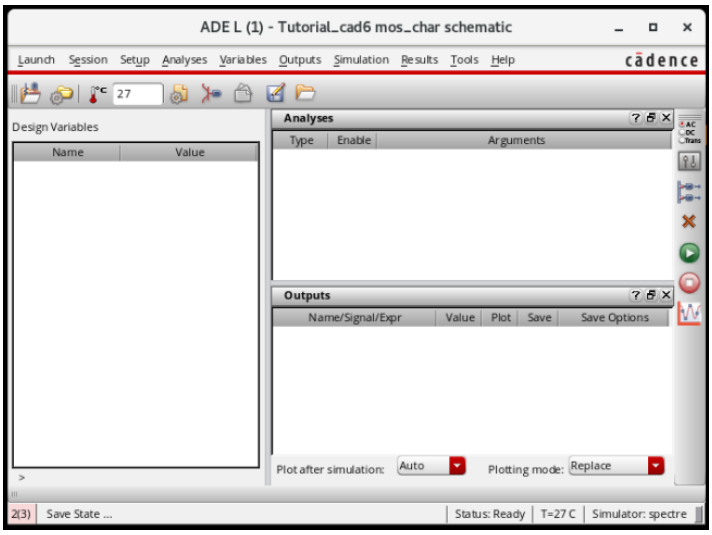

Figure 2: ADE L Simulation Window

5. You can copy the variables from your schematic into the simulation window by selecting Variables > Copy from Cellview on the ADE toolbar. You should see the ‘Design Variables’ area populated by your DC voltage source variables, as shown in Fig. 3. If you do not set a value for each variable, the simulation will not run.

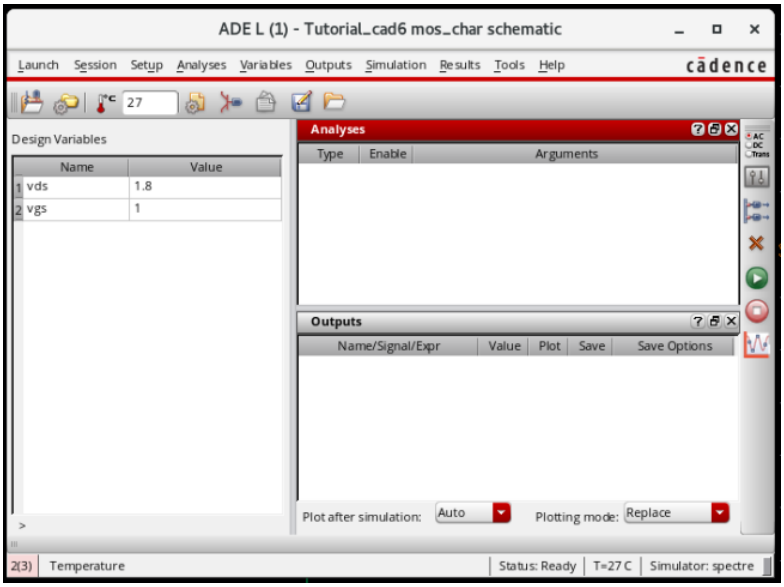

Figure 3: ADE L Window with Design Variables Populated

6. Next, you will need to set what type of analysis will be done in this simulation. On the ADE toolbar, select Analyses > Choose…, and set the options as shown in Fig. 4 for a DC analysis. Be sure that the Variable Name in the 'Sweep Variable' section is the same as one of the design variables copied from your schematic.

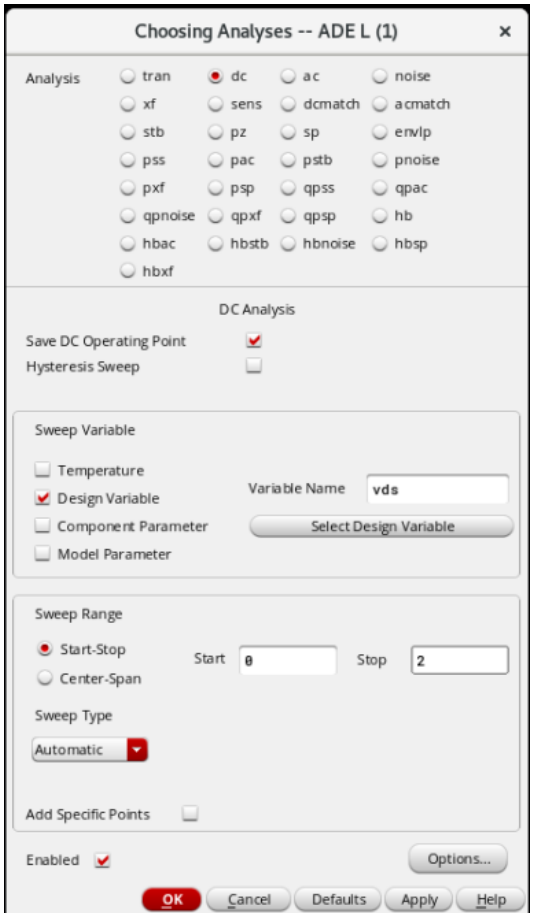

Figure 4: DC Analyses Settings for ADE Simulation

7. By default, the voltage values of all nets in the schematic will be saved when running a simulation in ADE, but the currents in each node will not be saved. Because we will want to observe the effects on the drain current of the transistor, we must manually select this current to be saved.

   In the ADE toolbar select Outputs > To Be Plotted > Select On Design. This should bring you back to your schematic view, where you can select any nets (wires) to save voltages or nodes (red squares) to save currents. To save the drain current, select the node at the NMOS drain in your schematic and it will become highlighted. You can select any other nets/nodes and then press Esc on your keyboard to end the selection. Your ADE window should now look like the one shown in Fig. 5 with the Analyses and Outputs sections populated.

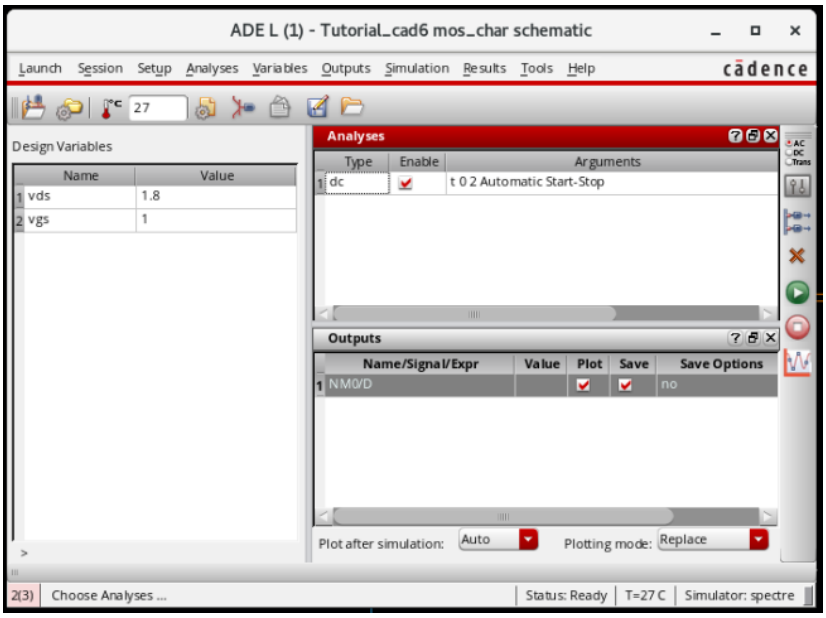

Figure 5: ADE Simulation Window with Analyses and Outputs Populated

8. To run the simulation, you can select Simulation > Netlist and Run, or click the green play button on the right side of the ADE window.
9. Perform the necessary simulations and explain your findings as described in Questions 1, 2, and 3 below.

Question 1:

Using the circuit in Fig. 1, Plot I_d vs. V_{gs} (sweep V_{gs} from 0V to 2V) for V_{ds} = 0.5V, 1V, 1.5V, and 2V. Explain your findings. (Note: please include the plots for the different V_{ds} values in one graph by using parametric analysis as described below)

Question 2:

a) For the same circuit, plot I_d vs. V_{ds} (sweep V_{ds} from 0V to 2V) for V_{gs} = 0.5V, 1V, 1.5V, and 2V. Explain your findings. (Note: please include the plots for different V_{gs} values in one graph by using parametric analysis as described below)

b) Find the approximate value of the output resistance of the transistor based on your simulation. Justify/explain your answer.

c) Double the width AND length of the transistor, and repeat questions 2a and 2b. Explain your results

Question 3:

Note: To find V_{eff} you can use the DC operating point characteristics of the transistor. After running a DC simulation, select Results > Print > DC Operating Points from the ADE toolbar. Then select the transistor in your circuit.

a) Using the same transistor aspect ratio (W/L) as in question 2c, find the approximate voltage to be applied to the gate (V_g) to get a drain current (I_d) of 1mA ± 100µA when V_{ds} is 1.5V. Also, find the value of the effective voltage (V_{eff1}).

b) Double only the width of the transistor, and once again find the approximate V_g necessary to get a drain current of 1mA ± 100µA when V_{ds} is 1.5V. Find the value of the effective voltage (V_{eff2}).
c) Discuss your observations of the relationship between V_{eff1} and V_{eff2}.

Parametric Analysis:

1. The parametric analysis tool allows a user to run the same simulation multiple times while varying a design variable or temperature.
2. To access the parametric analysis tool, select Tools > Parametric Analysis from the ADE toolbar. A new window will open allowing you to set the sweep options for a specific variable. To sweep the gate voltage from 0V to 2V, you may set the parametric analysis options as shown in Fig. 6 below and then press the green play button to run the simulation.

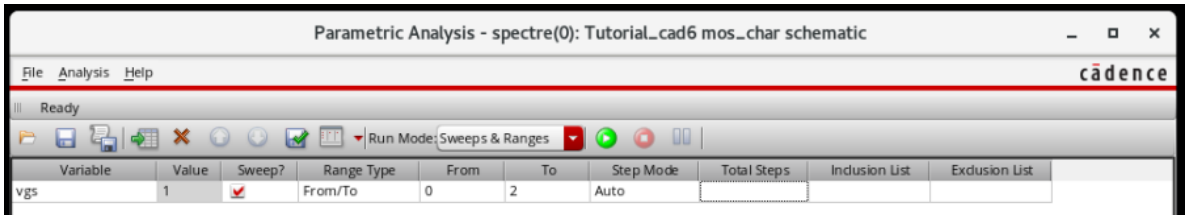

Figure 6: Parametric Analysis Settings to Sweep V_{gs} from 0V to 2V

3. This will run your DC analysis at multiple values of V_{gs}. You can use the step mode to define what type of sweep you want to perform on the variable (linear, linear steps, decade, etc.)

   Note: Parametric analysis can be used for other types of simulations (AC, transient, etc.) whereas the DC sweep variable set in the DC analyses options (Fig. 4) can only be used in DC simulations.

Your Report Should Include:

1. Show a screenshot of your schematic from Cadence. Include the DC annotations in the figure by doing the following. On the ADE toolbar, select Results > Annotate > DC Node Voltages, and select Results > Annotate > DC Operating Points.
2. Include all plots in a single graph for questions that sweep multiple variables (1, 2a, and 2c). In other words, for question 1 you would show a screenshot of a single graph with 4 lines that represent I_d vs. V_{gs}.

   Note: To make your graph easier to view, it is possible to change the color or width of the lines on a graph by right clicking that line.

3. Under each plot, you should have an explanation about the plot (e.g. you can write about the transistor region of operation at different voltages, approximate value of the threshold voltage, behavior of the current in different regions, etc.)
4. Your work must be submitted through Canvas as a **single PDF** document. Please review your PDF file before submitting it to ensure that all graphs are clear and no formatting issues have occurred.

Common Mistakes:

- Please make sure you have ‘check and saved’ your schematic before running the simulations. If you alter your schematic and do not check and save, the simulation will not run. You can look at the Virtuoso log window (also referred to as the CIW window) to get a better understanding of what has gone wrong when something is behaving unexpectedly.
- Be sure to assign values to your variable sin the ADE window, otherwise the simulation will not run
- By default, you must manually select currents in the schematic to be plotted or saved before running a simulation, otherwise they will not be viewable.