EEE 5320

Cadence Assignment 2

Due 10/6 11:59 pm

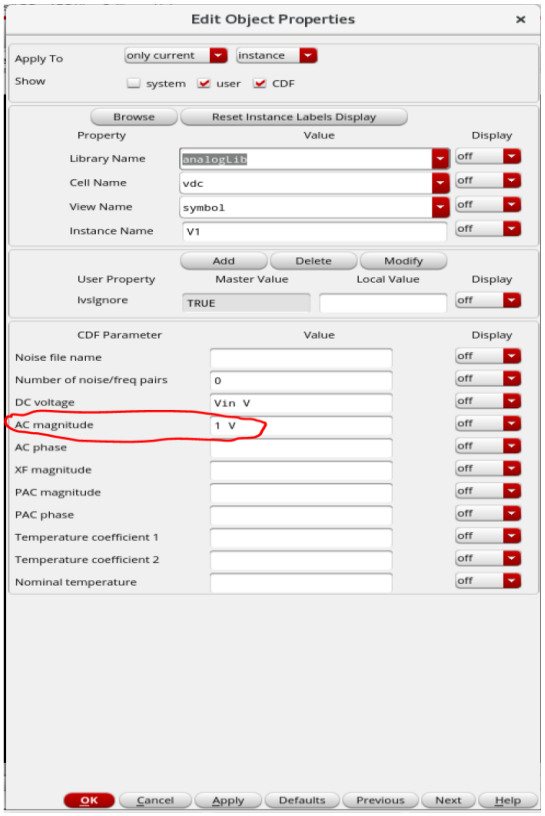
Format: Report

Objectives:

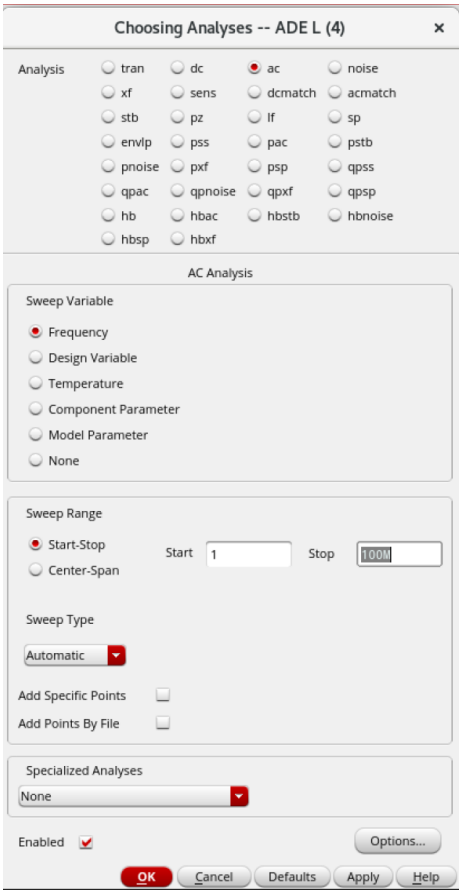
1. Getting used to DC/AC simulation in Cadence
2. Getting familiar with single stage amplifier operation principle
3. Introduce the concept of output swing

AC Simulation Guideline

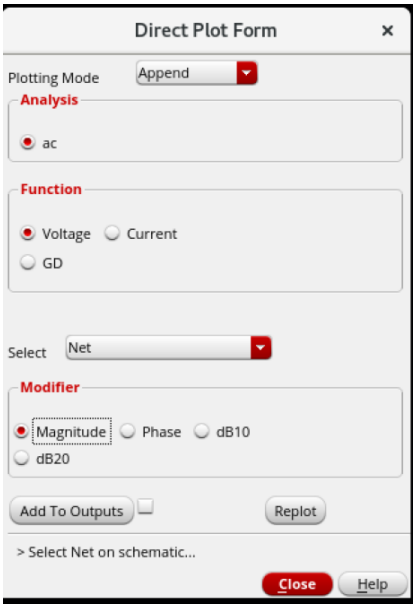
For AC simulation, first you need to give the AC magnitude as the stimuli in the schematic. Find your input, for instance, ideal voltage source (idc), and set the AC magnitude to be 1V

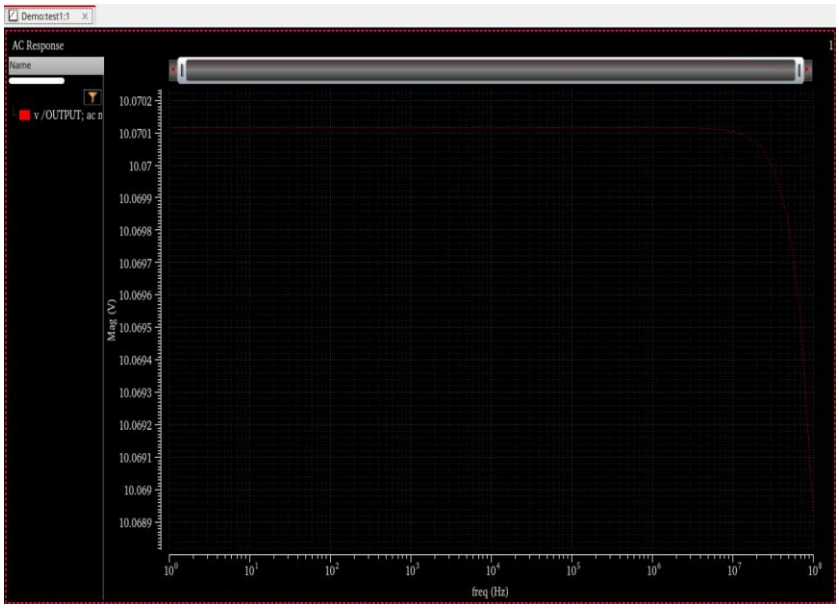


After check & save your schematic, in ADE, go to Analysis and create a new AC analysis and then run the simulation



After successfully run the simulation, go to Results -> Direct Plot -> Main Form. Leave this window open and go back to the schematic. Choose the wire (output) that you want to plot and press Esc. The AC simulation result will pop out. For Y axis unit, you can choose either V/V by selecting Magnitude as the modifier or dB by selecting dB20 (10V/V = 20dB). The expected AC simulation result of part A is shown below





Part A

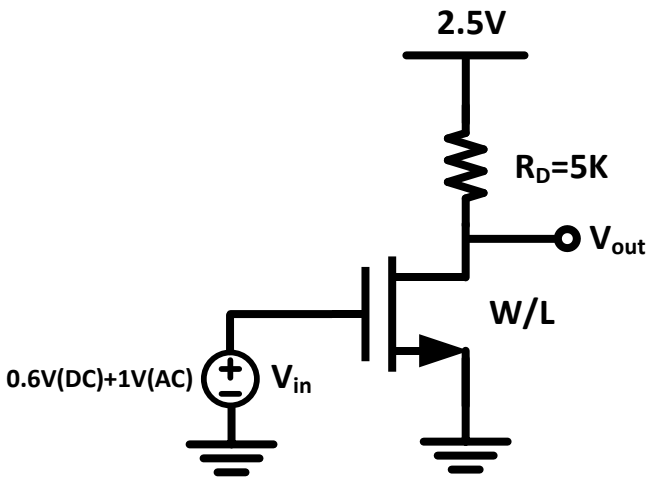


Figure 1. CS Amplifier

1) With given components value, find the W & L value that set the NMOS in saturation and the AC gain of the amplifier to be or larger than 10V/V. Include screenshot of schematic under DC simulation with annotations on and the AC magnitude result. What is the DC current of this amplifier? What is the output swing of this amplifier? Explain what limits the swing, V_{ds} or VDD? (Output swing means the maximum output range ($\pm V_{sw}$ from the output DC operating point) allowed while all transistors can be in saturation, i.e., $V_{out\_DC} \pm V_{sw}$ make all transistors in SAT & within the supply boundary)
   (Hint1: you can find the DC parameters by going to Results -> Print -> DC operating point and select the NMOS. There should be a list pops out and you can find Vth / Vdsat (Veff))
   (Hint2: If you use 45nm process to complete this assignment, the largest allowed W is 10um. If you want to further increase the W, you can set the multiplier)
2) If the input DC value varies by ±10mV, what is the DC current and output swing under these cases?

Part B

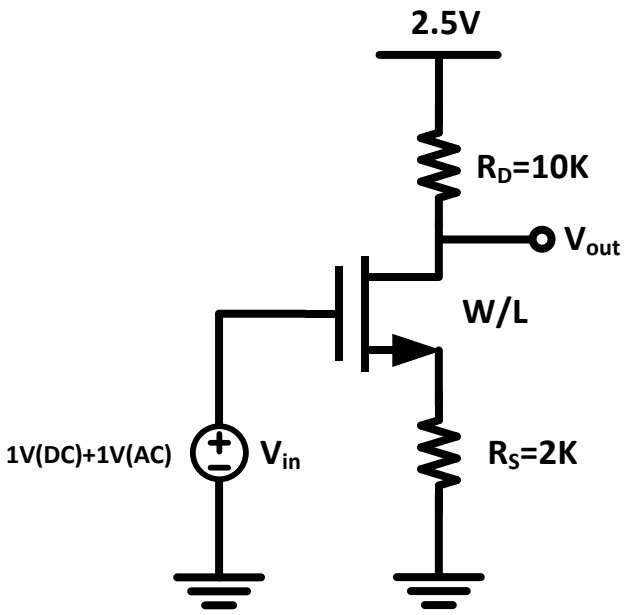


Figure 2. CS Amplifier with source degeneration

1) With given components value, find the W & L value that set the NMOS in saturation and the AC gain of the amplifier to be or larger than 2.5V/V. Include screenshot of schematic under DC simulation with annotations on and the AC magnitude result. What is the DC current of this amplifier? What is the output swing of this amplifier? Explain what limits the swing, V_{ds} or VDD?
2) If the input DC value varies by ±10mV, what is the DC current and output swing under these cases?