EEE 5320

Cadence Assignment

3 Format: Report

Objectives:

1. Getting familiar with simulation in Cadence
2. Getting familiar with different current mirror structures
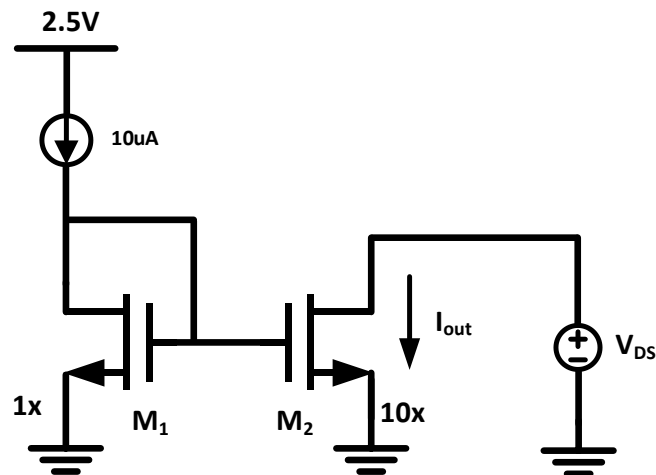
Part A. Basic Current Mirror

Figure 1. Basic Current Mirror

1) Build the circuit in Cadence as shown in Figure 1. Assume 1x = 0.5u/0.18u and V_{DS} = 1.5V. What is the value of I_{out}? Use screenshot of DC simulation to prove your result.
2) If V_{DS} = 1V and 2V, what will be the value of I_{out} under these two cases? Use screenshot of DC simulation to prove your result.
3) If 1x = 1u/1u and V_{DS} = 1.5V. What is the value of I_{out}? Use screenshot of DC simulation to prove your result.
4) If 1x = 1u/1u and V_{DS} = 1V and 2V, what will be the value of I_{out} under these two cases? Use screenshot of DC simulation to prove your result.
5) Compare the results from 2) and 4). What is the difference and what can be the cause of that?
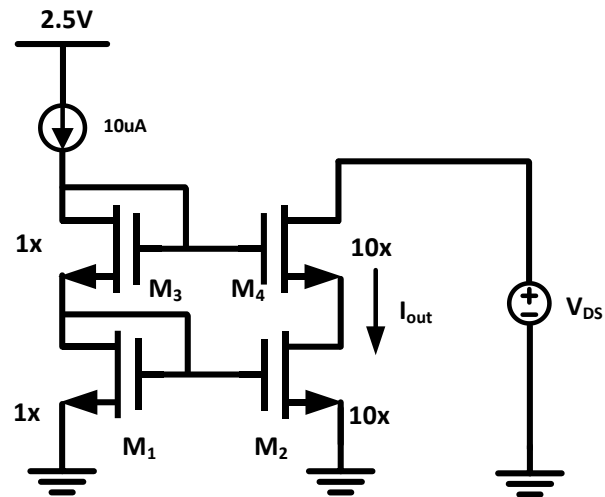
Part B. Cascode Current Mirror

Figure 2. Cascode Current Mirror

1) Build the current mirror as shown in Figure 2. Repeat question 1) to 4) from Part A.
2) Compare with the results from 2) & 4) in Part A. What is the benefit of this cascode current mirror and what can be the cause?
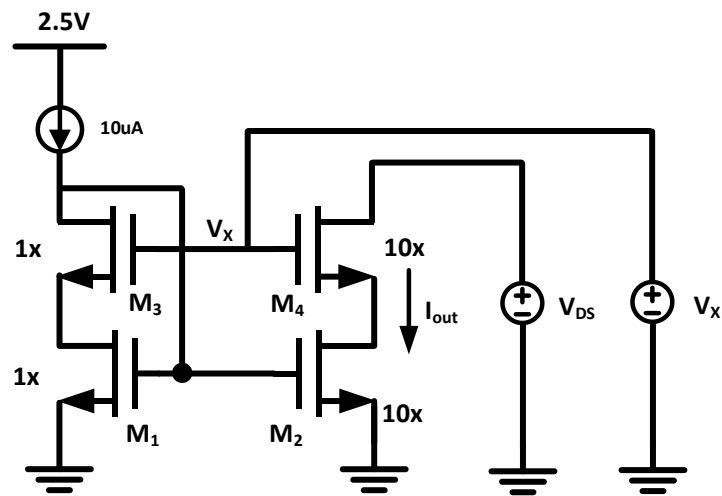
Part C. Wide-Swing Current Mirror

Figure 3. Wide-swing Current Mirror

1) Build the current mirror as shown in Figure 3. Assume 1x = 1u/1u, V_{DS} = 1.5V and V_X = 1V. What is the value of I_{out}? Use screenshot of DC simulation to prove your result.

2) If V_{DS} = 1V and 2V, what will be the value of I_{out} under these two cases? Use screenshot of DC simulation to prove your result.

3) What is the minimum V_X that can set all transistors in saturation? Compare with V_X = 1V, how does the I_{out} change with different V_{DS}?

4) Compare with the results from 1) in Part B. What is the difference? What is the biggest advantage of this wide-swing structure?