IMPORTANT:

Every problem or question must be handed in separately. Do not answer different problems or questions in the same piece of paper. The student name and group must be written in all the pages. Calculators are not allowed in any case.

Exam time: 3 hours

Problem 1 (2 points)

We are asked to design a 4-bit adder-subtractor in order to create a functional block. Several blocks of them will be used later to build a system that makes the operation (|D|*2)-3, where D is represented in 2s-complement.

Solve the next questions:

a) Design a complete 1-bit full-adder. Draw the resulting gates diagram for that.

b) Using 4 full-adders, as the ones designed in the first question (a), and additional logic gates, build a 4-bit adder-subtractor. Give appropriate names to their inputs, using numerical subindexes to represent their magnitude order. Draw blocks to represent the full-adders (It is not necessary to draw their internal gates).

*For the following questions: Draw adder-subtractors **as blocks** (it is not necessary to draw the internal gates) with the appropiate input/output names and make the necessary connections. Consider that N is an input represented in 2s-complement.*

c) Using a single 4-bit adder-subtractor, as the one designed in the second question (b) and a 4-bit input N, connect appropriately the adder so that the output is the absolute value of N. Hint: if N is positive, the block must do the operation 0+N, but if N is negative, the block must do the operation 0-N

d) Using a single 4-bit adder-subtractor and a 4-bit input N, connect appropriately the adder so that the output is 2*N.

e) Using a single 5-bit adder-subtractor and a 5-bit input N, connect appropriately the adder so that the output is N-3.

f) Using the previous designed functional blocks in (c), (d) and (e), draw the block diagram of a digital system that performs the operation (|A|*2)-3. Every adder-subtractor must be a single block.

Problem 2 (3 points)

A RAM module of 16K x 8 must be located in the memory map of a system, whose address bus has 16 lines and whose data bus has 8 bits.

The memory positions between the 2000_H and the $5FFF_H$ are used by a ROM memory. The memory positions between the $A000_H$ and the $FFFF_{H.}$ are used by a EPROM memory as well. The other positions are absolutely free.

a) How much ROM memory does the system have?
b) How much EPROM memory does the system have?
c) Indicate the possible location for the RAM module. Write the start and the final addresses for this module in hexadecimal.
d) If the RAM module is implemented with 2 chips (8K x 8), calculate the chip select expressions for both of them (CSRAM-1 y CSRAM-2).
e) Draw the chip select circuit for every module in the system. Use a decoder with the necessary inputs and with active-high outputs for that, using the minimum possible number of logic gates.

NOTE: Consider that the chip selects CSROM, CSEPROM, CSRAM-1 y CSRAM-2 are active-high.

Problem 3 (3 points)

A) You must design the control system for a dryer. This control system has the following 3 inputs: Start, SR (Fast dry) and Finish. The input "Finish" comes from a timer that calculates the time for every dry step. The input "Finish" will be active during a clock edge when the programmed time has elapsed. The input "Start" is active during a clock cycle when the user wants to start the dry process. Once a dry process is started, the selected program will be finished completely. The input "SR" selects the fast dry program.

The dryer has 2 dry steps:

- First dry step: low temperature and engine on.
- Second dry step: high temperature and engine on.

The temperature and the engine are controlled by the T and M outputs respectively, which are active-high. T is activated when the temperature is high. If any program is activated, both outputs are non-active.

The second step for the dry can have 2 different durations depending on the value of the input "SR". If SR is active, the dry process will be fast and therefore the duration of the second dry step will be the same as in the first step (the time indicated by the timer in the input "Finish"). If SR is not active, the second dry step will last double time than the first step, therefore it must wait until the timer executes the programmed time twice.

Draw the state transition graph for a finite state machine that implements this system. Is the machine Mealy's or Moore's type and why?

B) In the figure 3 you can see the state transition graph of a different circuit. This circuit has the following inputs and outputs:

Inputs:
- Clk: system clock.
- Reset: active-high signal to initialize the machine, being S0 the initial state.
- A: 2 bits

Output:
- S: 1 bit

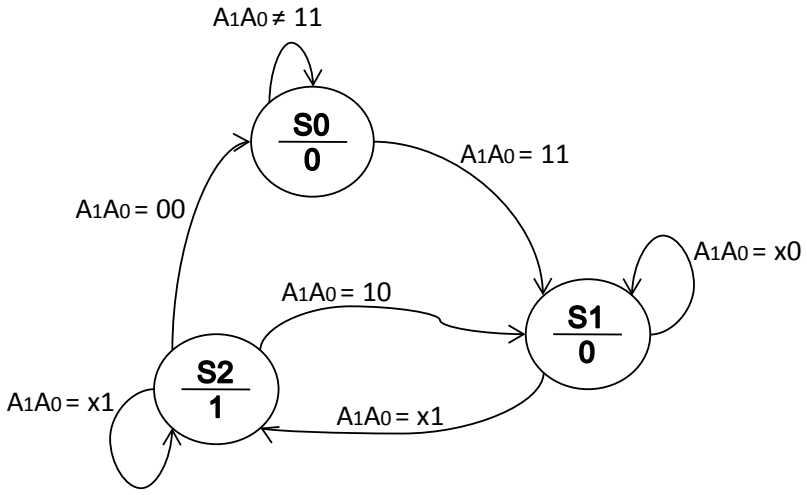


Figure 3

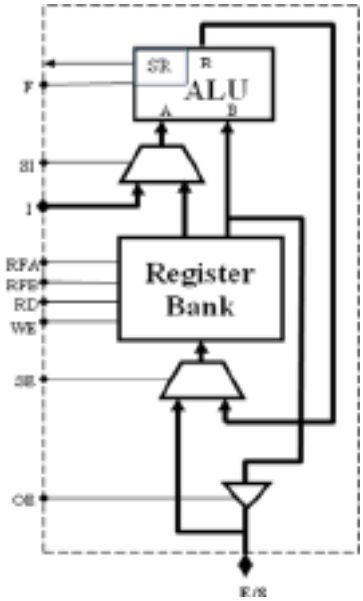
Design the finite state machine that implements this system. Use synchronous D flip-flops, which are rising-edge triggered. Answer the next questions justifying them:

a) ¿Is it a Mealy's or a Moore's machine and why?
b) Indicate the flip-flop number and the encoding assigned to the states.
c) Obtain the transition table and the output table.
d) Obtain the simplified boolean expressions for the state function and the output function.
e) Draw the complete block diagram of the designed machine (it is not necessary to draw the logic gates).

NAME: **GROUP:**

Problem 4 (2 points)

In the next figure you can see the datapath of a microprocessor.



a) What is the utility of the RFA and RFB signals?

b) What is the utility of the F signal?

c) What is the utility of the SI signal?

d) Consider that the register bank has 8 registers addressed with bits.

The content of the register bank is showed in the next table:

Register	Content
0	24'H
1	02'H
2	13'H
3	07'H
4	11'H
5	00'H
6	0A'H
7	0F'H

Consider that the ALU works using the operation descripction showed in the next table:

F	Operation
000	NOT B
001	A+B (ARITHMÉTICAL)
010	A XOR B
011	A AND B
100	A+B (LÓGICAL)
101	A-B
110	A*B
111	NOT A

Fill in the next table:

RFA	RFB	F	A	B	R
110	001	001			
000	110	111			
111	000	100			
010	011	011			