PROBLEMA 1

The basic memory of the martian exploration vehicle Rober Curiosity has a total addressable size of 1M x 32 bits. The low part of the memory is configured using 512K x 32 bits ROM memory chips. The following section has been reserved for fure extensions and has a size of 256K. The rest o the memory will be completed using RAM memory it the 1M total capacity.

Rover "Curiosity"

The memory chips in stock in NASA headquarters are: RAM chips with size 256K x 32 bits and ROM chips with size 512K x 16 bits.

We are asked to answer the following questions:
1) How many chips will we need of each time? Indicate the initial and final address of each of the integrated circuits in binary and hexadecimal.
2) Draw the decoder you will need to use to address all the memory chips that are part of the total memory. Clearly indicate all the lines and buses.

PROBLEM 2:

We have a memory card with an architecture as the one shown in figure 1, where B1, B2 and B3 are different memory banks, made with different integrated circuits.

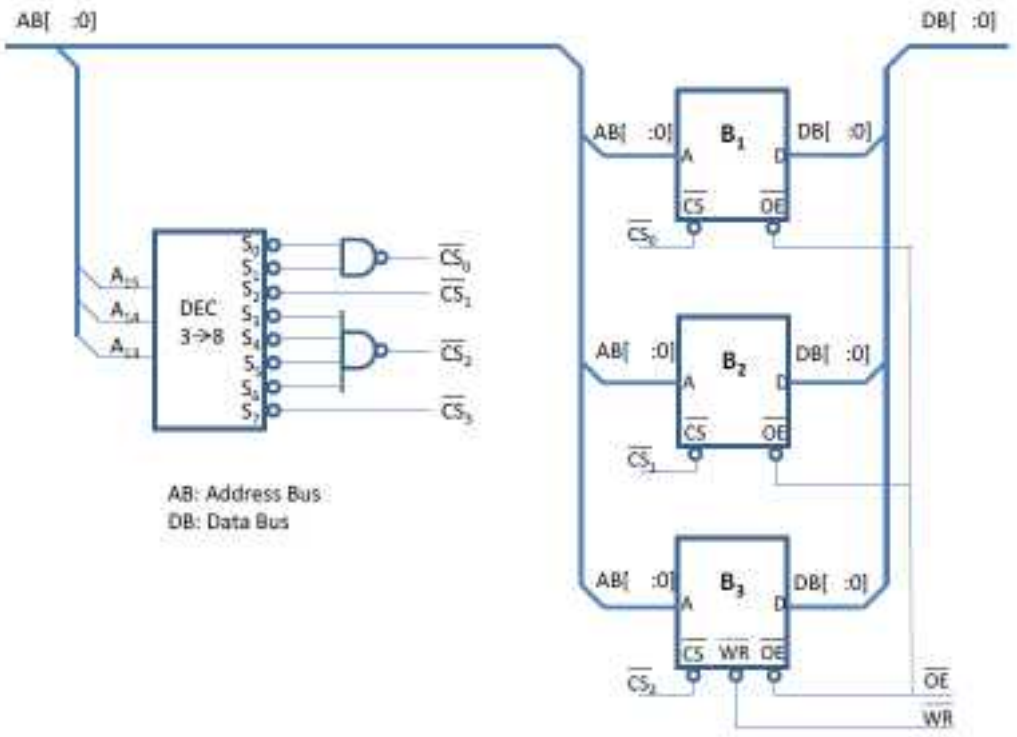

Figure 1

Please, answer the following questions:

1. Indicate the number of data lines, address lines and the size of the memory banks B1, B2 y B3. Elaborate your answer
2. How many data and address lines must a microprocessor have to be able to handle the complete memory card we have?
3. Calculate the maximum memory size installed in the card and the maximum achievable size, after future memory extensions.
4. To construct the memory banks B1, B2 y B3 the memory modules that were uses are listed below:

   4 SRAM chips with 32K x 4 bits
   1 EEPROM chip with 8K x 16 bits
   2 ROM chips with 16K x 8 bits

   Bases on this list of modules and the signals connected to the banks, indicate the type of memory within each bank and draw the memory map, indicating the initial an final addresses (in hex) of each of the memory modules.
5. Draw the scheme of each of the memory Banks, using the indicated memory modules and connect the data, address and control signal buses. All the memory modules have the following active low control signals: CS (chip select), OE (Output Enable) y WR (Write).

PROBLEM 3:

A RAM memory module of 16K x 8bits must be placed in the memory map of a system that has an address bus of 16 lines and a data bus of 8 bits.

The memory positions between 2000H and 5FFFH are occupied by ROM memory. The positions from A000H to FFFFH are occupied by EPROM memory. The rest, are free.

a) Which is the ROM memory capacity of the system?
b) Which is the EPROM memory capacity of the system?
c) Where can we place our new RAM module? Indicate the initial and final addresses in hex
d) If the new RAM module is made by two chips (8k x 8 each), obtain the activation function for each one of them (chip select for RAM1 is CSRAM-1 and chip select for RAM2 is CSRAM-2).
e) Draw the selection circuit for all the memories of the system, using a decoder with all the inputs you may need. Consider the outputs to be active high an use the minimum number of logic gates.

NOTA: All the chip select control signals are active high: CSROM, CSEPROM, CSRAM-1 y CSRAM-2