IMPORTANT:

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Time: 3h

Problem 1 (2.5 points)

The circuit shown in the Figure.1 corresponds to the arithmetic unit of a data path. This unit performs an operation on two numbers A and B having two bits each.

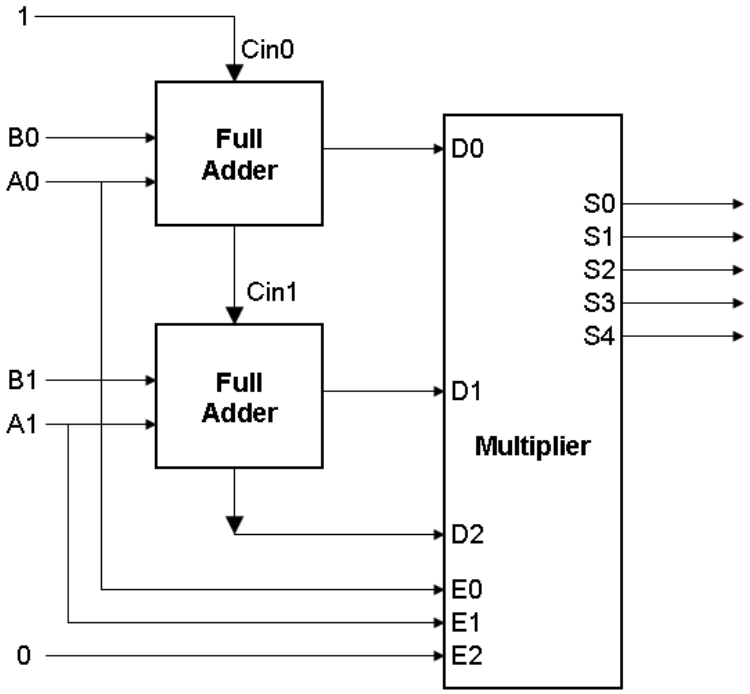

Figure.1

We want to resynthesize this control unit, taking into account that the data A never reaches 3.

a) Identify the arithmetic operation performed by the unit.
b) Provide in 'Decimal' the table for the possible input values of A and B along with the outputs D and S.
c) Provide the 'Binary' truth table of the whole unit, taken as inputs the possible values of A and B and output S. Consider the restriction of data A.
d) Synthesize the function S0 with the minimum number of NAND gates.
e) Synthesize the function S1 with a 'Decoder' with low active outputs and minimum possible number of additional logic gates.
f) Synthesize the function S2 with a 'Multiplexer' having 2-selection inputs and minimum possible number of additional logic gates.
g) Synthesize the function S3 with the minimum possible number of NOR gates.

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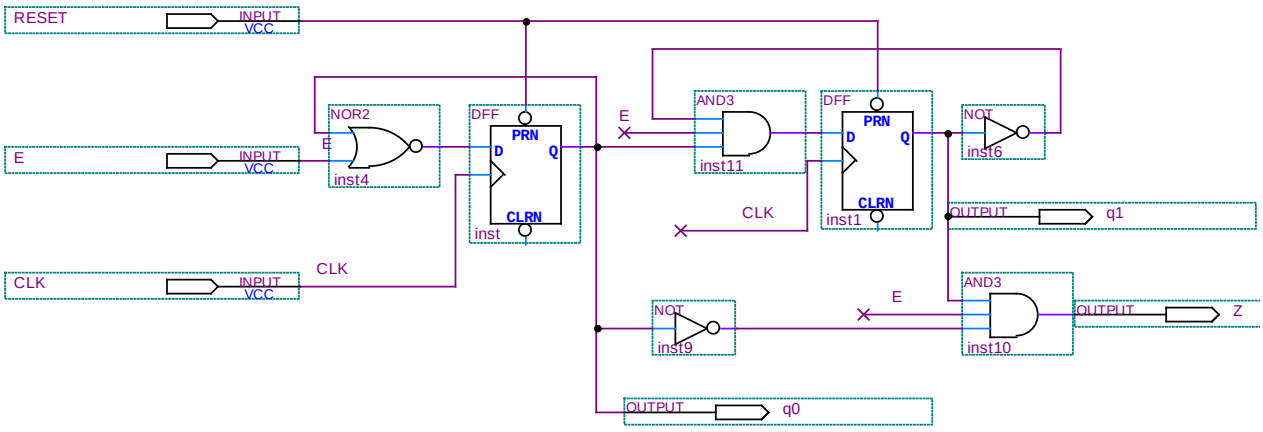
Problem 2 (2,5 points)

For the circuit of the figure:



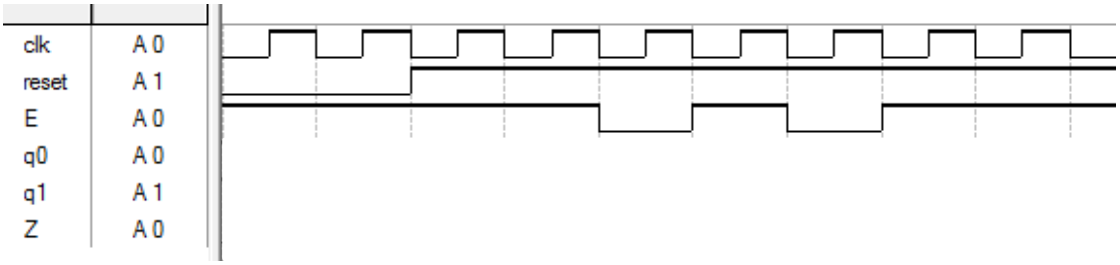
1. Write the logic expressions of the inputs of the flip-flops and the outputs.

2. Fill the following table and draw the state transition graph, considering the provided state encoding.

Q1	Q0	
0	0	E0
0	1	E1
1	0	E2
1	1	E3

Q1	Q0	E	D1	D0	Z	$Q1^+$	$Q0^+$

3. Fill the following chronogram, considering that the flip-flops are rising edge triggered:



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Problem 3 (2 points)

Answer to the following questions, circling the correct answer. If you make a mistake, correct it so that the answer is clear and not ambiguous, or it will be considered as not correct.

The score in this question will be proportional to:

Number of correct answers – (Number of wrong answers)/3

(Not answered questions are not considered wrong)

1. Tri-state buffers allow:
   a) Increasing the number of inputs that can be connected to an output.
   b) Connecting several outputs without short circuits.
   c) Storing a bit while the buffer is powered.
   d) None of the above.

2. The noise margin is:
   a) Intervals of voltages associated to the different logic levels.
   b) The difference between the power supply voltage and the admissible input voltage in a logic gate.
   c) The difference between the noise voltage in the output and the noise voltaje in the input of a logic gate.
   d) None of the above.

3. ASICs are:
   a) Integrated circuits that can be programmed just once.
   b) Re-programmable Integrated Circuits.
   c) Application Specific Integrated Circuits.
   d) None of the above.

4. The Status Register of a microprocessor contains:
   a) The result of the last operation.
   b) An operand of the operation to be performed.
   c) Next instruction to execute.
   d) None of the above.

5. The Program Counter of a Microprocessor contains:
   a) The number of executed instructions.
   b) The size of the program being executed.
   c) The memory address of the next instruction to execute.
   d) None of the above.

6. The Von Neumann Architecture is characterized by:
   a) It can access program memory and data memory at the same time.
   b) It uses the same address BUS to access data and program addresses.
   c) It has an independent register bank for input/output operations.
   d) None of the above.

7. If an ALU performs the AND operation with the operands 0x63 and 0x45 the result will be:
   a) 0x12
   b) 0x41
   c) 0xA8.
   d) None of the above.
   NOTE: "0x" means HEXADECIMAL

8. The size of the instructions in a microprocessor:
   a) It is the same for all of them.
   b) It is the same as the size of the memory word.
   c) It is a multiple of the size of the memory word.
   d) None of the above.

9. To program in assembly language:
   a) It is necessary to know the microprocessor architecture.
   b) It is necessary to know the operation codes of the instructions.
   c) It is necessary to know high level programming languages.
   d) None of the above.

10. The controller circuit of a microprocessor:
   a) is a combinational circuit.
   b) is a synchronous sequential circuit.
   c) is an asynchronous sequential circuit.
   d) None of the above.

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Problem 4 (3 points)

A microprocessor system has a data memory of 256M x 16 bits. In this memory the lowest part is read-only and the highest part is RAM memory. There are 64M addresses of ROM and 192M addresses of RAM.

To implement this memory the following chips are available:

2 chips de ROM de 32M x 16 bits	IC1, IC2
2 chips de RAM de 64M x 8 bits	IC3, IC4
1 chip de RAM de 128M x 16 bits	IC5

a) Draw the memory map of the system, indicating the first and last addresses of each module, both in binary and hexadecimal.

b) Draw the circuit with all the modules and connections, using a 2:4 decoder with active-low outputs for the addresses decoding.
Note: All the control inputs of the memories are active-low.