Sesión 3: LFSR

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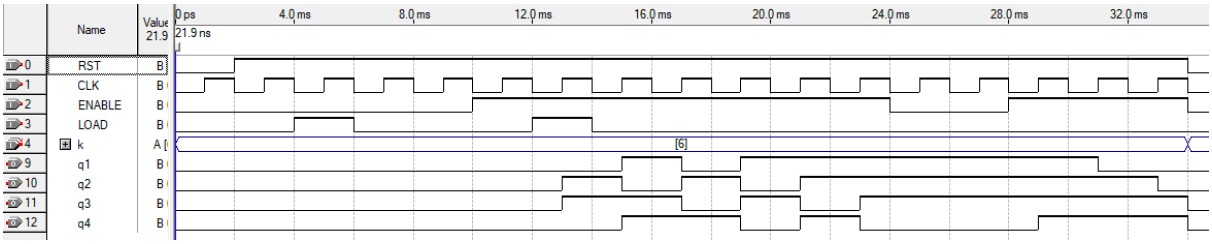
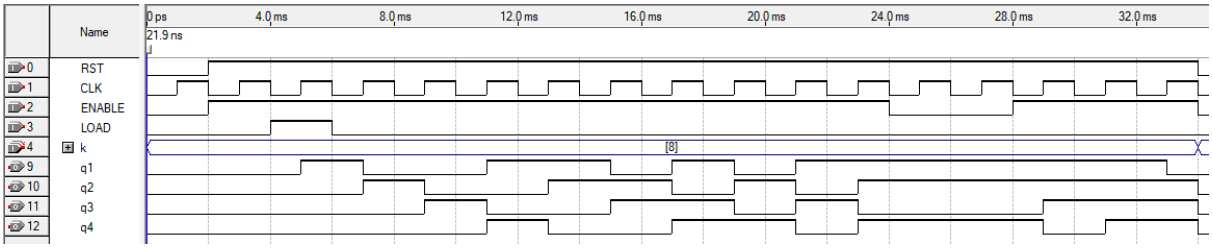
Pregunta 1:

El cronograma obtenido al simular el circuito es el siguiente:



Pregunta 2:

La simulación del LFSR con la carga del valor 8:



BCD(1000)=LSB DNI

Pregunta 3:

El periodo de nuestro reloj son 2ms, por lo que la frecuencia al ser la inversa de este, sería 0,5kHz=500Hz.

Pregunta 4:

ENABLE Pin 16

LOAD Pin 41

RST Pin 1

Claves

- k4 Pin 37
- k3 Pin 17
- k2 Pin 40
- k1 Pin 18

CLK Pin 43

Todos los pines.

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O Bank	User Assignment
RST	1	input	TTL			N
GND+	2					
VCC	3	power				
RESERVED	4					
RESERVED	5					
RESERVED	6					
TDI	7	input	TTL			N
q1	8	output	TTL			N
q4	9	output	TTL			N
GND	10	gnd				
q3	11	output	TTL			N
q2	12	output	TTL			N
TMS	13	input	TTL			N
RESERVED	14					
VCC	15	power				
ENABLE	16	input	TTL			N
k3	17	input	TTL			N
k1	18	input	TTL			N
RESERVED	19					
RESERVED	20					
RESERVED	21					
GND	22	gnd				
VCC	23	power				
RESERVED	24					
RESERVED	25					
RESERVED	26					
RESERVED	27					
RESERVED	28					
RESERVED	29					
GND	30	gnd				
RESERVED	31					
TCK	32	input	TTL			N
RESERVED	33					
RESERVED	34					
VCC	35	power				
RESERVED	36					
k4	37	input	TTL			N
TDO	38	output	TTL			N
RESERVED	39					
k2	40	input	TTL			N
LOAD	41	input	TTL			N
GND	42	gnd				
CLK	43	input	TTL			N
GND+	44					

Esquemático del circuito