PROBLEMA 1

The basic memory of the martian exploration vehicle Rober Curiosity has a total addressable size of 1M x 32 bits. The low part of the memory is configured using 512K x 32 bits ROM memory chips. The following section has been reserved for fure extensions and has a size of 256K. The rest o the memory will be completed using RAM memory it the 1M total capacity.

Rover "Curiosity"

The memory chips in stock in NASA headquarters are: RAM chips with size 256K x 32 bits and ROM chips with size 512K x 16 bits.

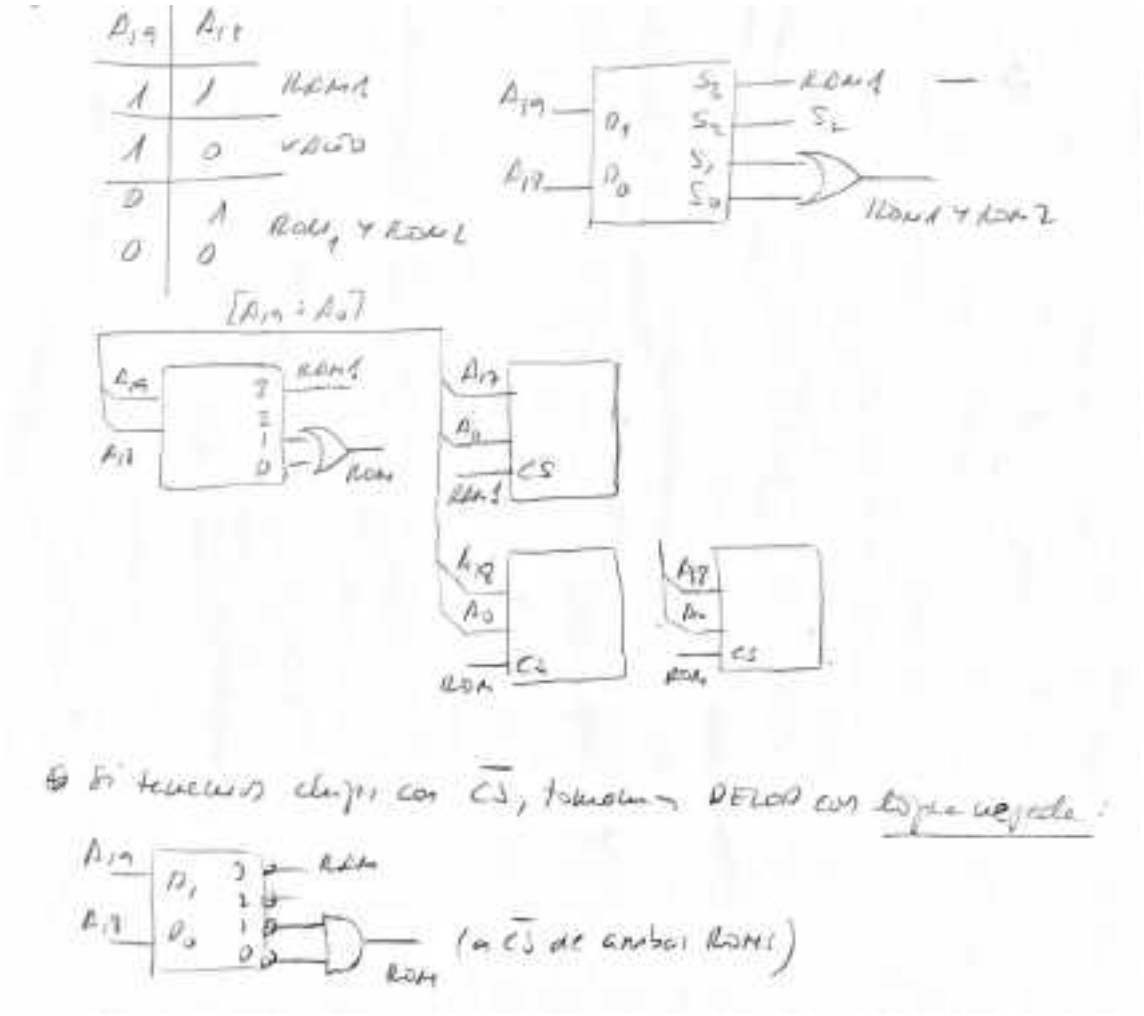
We are asked to answer the following questions:
1) How many chips will we need of each time? Indicate the initial and final address of each of the integrated circuits in binary and hexadecimal.
2) Draw the decoder you will need to use to address all the memory chips that are part of the total memory. Clearly indicate all the lines and buses.

SOLUTION

1)

Bank	**Memory map**		**Adresses (binary)**	**Adresses (hex)**
B1	RAM1		(1111)(1111)(1111)(1111)(1111) (1100)(0000)(0000)(0000)(0000)	Inicio: 0xFFFFF Fin: 0xC0000
Vacío	X		(1011)(1111)(1111)(1111)(1111) (1000)(0000)(0000)(0000)(0000)	Inicio: 0xBFFFF Fin: 0x80000
B2	ROM 1	ROM2	(0111)(1111)(1111)(1111)(1111) (0000)(0000)(0000)(0000)(0000)	Inicio: 0x7FFFF Fin: 0x00000

2)



Exercise from: Ejercicio propuesto FIE GIE curso 2016/2017

PROBLEM 2:

We have a memory card with an architecture as the one shown in figure 1, where B1, B2 and B3 are different memory banks, made with different integrated circuits.

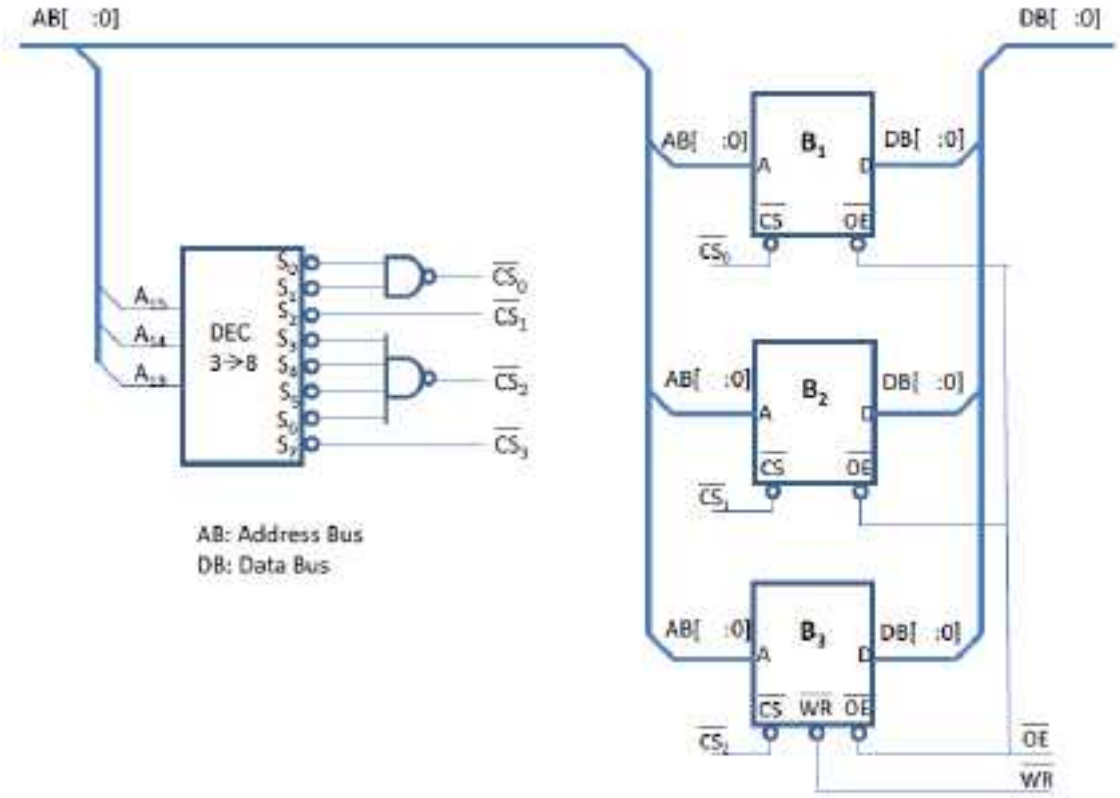


Figure 1

Please, answer the following questions:

1. Indicate the number of data lines, address lines and the size of the memory banks B1, B2 y B3. Elaborate your answer
2. How many data and address lines must a microprocessor have to be able to handle the complete memory card we have?
3. Calculate the maximum memory size installed in the card and the maximum achievable size, after future memory extensions.
4. To construct the memory banks B1, B2 y B3 the memory modules that were uses are listed below:

   4 SRAM chips with 32K x 4 bits
   1 EEPROM chip with 8K x 16 bits
   2 ROM chips with 16K x 8 bits

   Bases on this list of modules and the signals connected to the banks, indicate the type of memory within each bank and draw the memory map, indicating the initial an final addresses (in hex) of each of the memory modules.
5. Draw the scheme of each of the memory Banks, using the indicated memory modules and connect the data, address and control signal buses. All the memory modules have the following active low control signals: CS (chip select), OE (Output Enable) y WR (Write).

SOLUCIÓN

1.

	Direcciones	Datos	Tamaño (#palabras x tamaño palabra)
B1	14 bits	16 bits	16k x 16 bits
B2	13 bits	16 bits	8k x 16 bits
B3	15 bits	16 bits	32k x 16 bits

Block size = $2^{(\text{max lines in address bus})}$/number output in dec = $2^{16}/8$ = 64k / 8 = 8k
(memory size addressable per decoder output)

CS0 = S0 + S1 → **B1** = 2 x 8k = **16k** = 2^{14}
CS1 = S2 → **B2** = 1 x 8k = **8k** = 2^{13}
CS2 = S3 + S4 + S5 + S6 → **B3** = 4 x 8k = **32k** = 2^{15}

Considering the chips from 4), the data bus will be equal to the máximum data bus of those chips: E2PROM with 16 data bits

2.

µP data bus: 16 bits
µP address bus: 16 bits

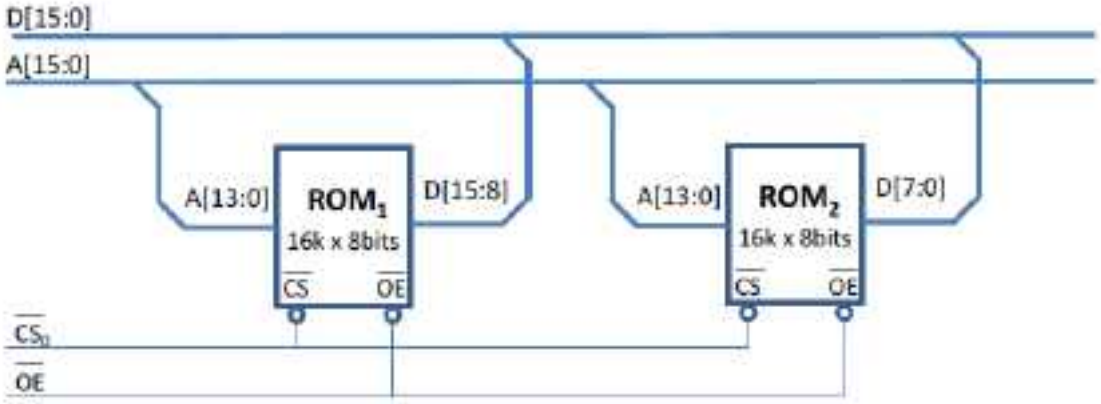
3.

Memory installed: 56k x 16 bits
Maximum expansion: 8k x 16bits

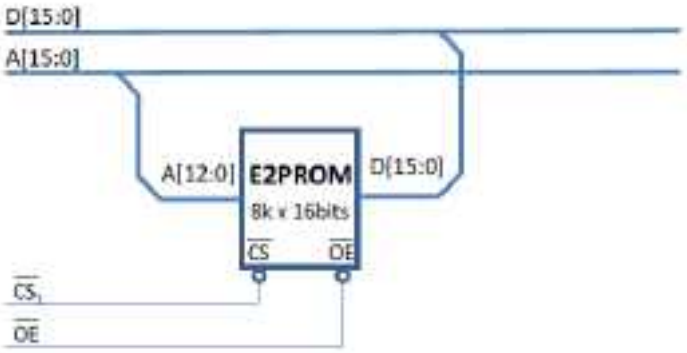
4.

Bank	**Memory map**				**Addresses (hex)**
B1	ROM 1		ROM2		Inicio: 0x0000 Fin: 0x3FFF
B2	E2PROM				Inicio: 0x4000 Fin: 0x5FFF
B3	SRAM 1	SRAM 2	SRAM 3	SRAM 4	Inicio: 0x6000 Fin: 0xDFFF
Exp	Expansión				Inicio: 0xE000 Fin: 0xFFFF

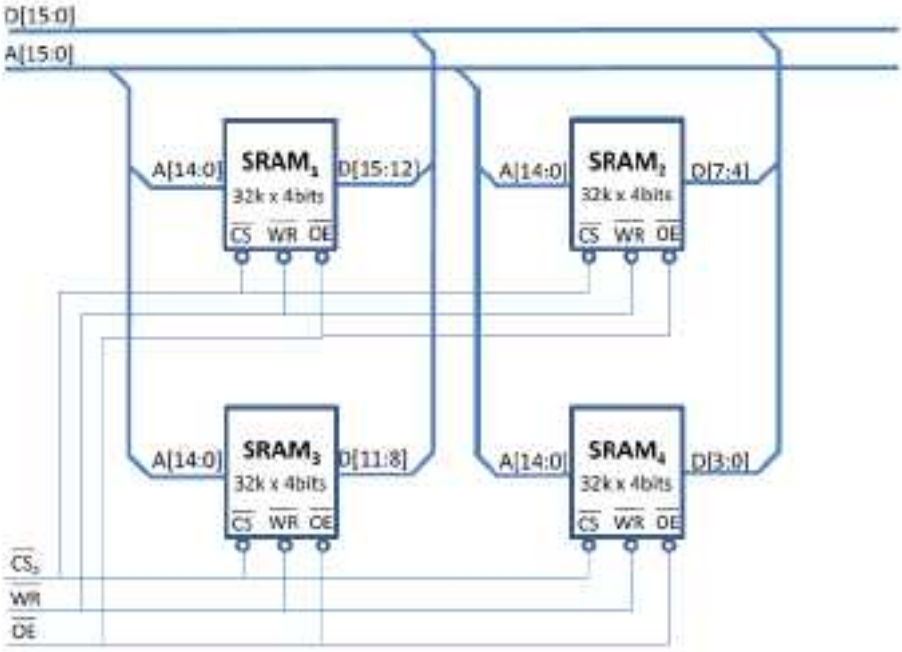
5.
Bank 1


D[15:0]
A[15:0]
A[13:0]
ROM1
16k x 8bits
D[15:8]
A[13:0]
ROM2
16k x 8bits
D[7:0]
CS
OE
CS0
OE

Bank 2


D[15:0]
A[15:0]
A[12:0]
E2PROM
8k x 16bits
D[15:0]
CS
OE
CS1
OE

Bank 3


D[15:0]
A[15:0]
A[14:0]
SRAM1
32k x 4bits
D[15:12]
A[14:0]
SRAM2
32k x 4bits
D[7:4]
CS WR OE
A[14:0]
SRAM3
32k x 4bits
D[11:8]
A[14:0]
SRAM4
32k x 4bits
D[3:0]
CS2
WR
OE

Problem from FINAL EXTRAORDINARIO TC JUNIO 2016, EJERCICIO 3

PROBLEM 3:

A RAM memory module of 16K x 8bits must be placed in the memory map of a system that has an address bus of 16 lines and a data bus of 8 bits.

The memory positions between 2000H and 5FFFH are occupied by ROM memory. The positions from A000H to FFFFH are occupied by EPROM memory. The rest, are free.

a) Which is the ROM memory capacity of the system?
b) Which is the EPROM memory capacity of the system?
c) Where can we place our new RAM module? Indicate the initial and final addresses in hex
d) If the new RAM module is made by two chips (8k x 8 each), obtain the activation function for each one of them (chip select for RAM1 is CSRAM-1 and chip select for RAM2 is CSRAM-2).
e) Draw the selection circuit for all the memories of the system, using a decoder with all the inputs you may need. Consider the outputs to be active high an use the minimum number of logic gates.

NOTA: All the chip select control signals are active high: CSROM, CSEPROM, CSRAM-1 y CSRAM-2

SOLUCIÓN

a) ROM?

5FFF-2000 +1 = 3FFF +1 = 4000h = 16K

A15(32K	A14(16K)	A13(8k)	A12(4k)	A11(2k)	...	...	...	...	A0(1)
0	1	0	0	0	0	0			0

b) EPROM?

FFFF-A000 +1 = 5FFF +1 = 6000h = 24K

A15(32K	A14(16K)	A13(8k)	A12(4k)	A11(2k)	...	...	...	...	A0(1)
0	1	1	0	0	0	0			0

c) RAM module placement

Areas available:
0000h -1FFFh => (1FFFh+1= 2000h = 8K) => Does not fit (we need 16K)
6000h- 9FFFh =>(3FFFh +1= 4000 = **16K**) => RAM fits (16K!)

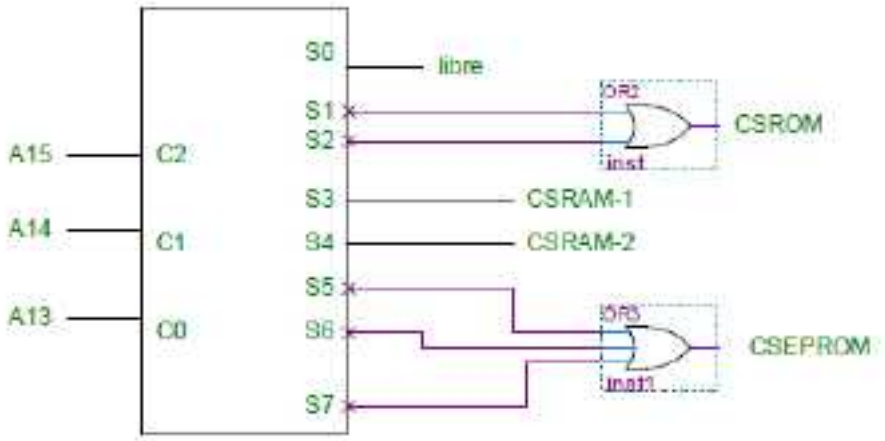
d) Activation of the modules

RAM-1 from 6000h to 7FFFh
RAM-2 from 8000h to 9FFFh

A15 (32K)	A14 (16K)	A13 (8k)	A12 (4k)	A11 (2k)	...	...	...	...	A0 (1)	CSRAM-1	CSRAM-2
0	1	1	X	X	X	X			X	1	0
1	0	0	X	X	X	X			X	0	1

CSRAM-1= A15'·A14·A13
CSRAM-2= A15·A14'·A13'

e) Selection circuit



Problem from: Electrónica Digital 2014/15