Sesión 4: Juego de dados

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Tabla de verdad del bloque COMPARADOR.

Tabla de									C4	-	
Enable	X1	X2	X3	X4	Y1	Y2	Y3	Y4	G1	G2	Empate
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	0	1	0
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1	0	0	0	1	0	0	0	1	0	0	1
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						1					
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	0						0		0		
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L	•										

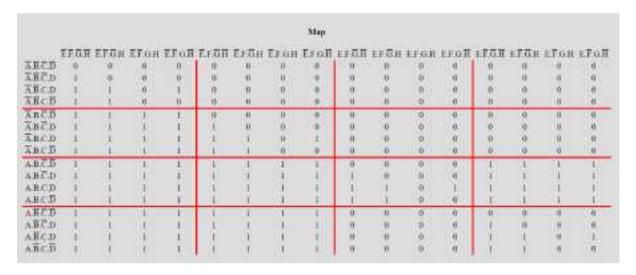
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	1			1	1	1				1	
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					0	0		0			
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1	1	1	1	1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1	0	1	0	0
1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	0	0	0	0	X	Χ	X

Cuando el Enable tenga valor cero, el circuito no calcula un ganador.

Y1=E Y2=F Y3=G Y4=H

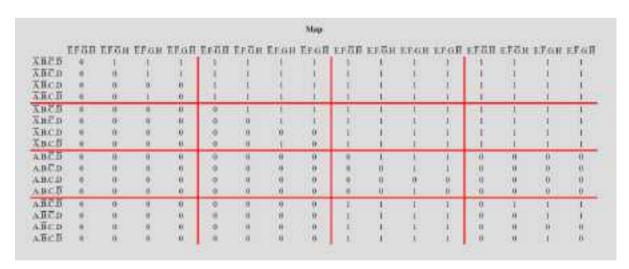
Karnaugh G1:



Ecuación de mintérminos: (El apóstrofe es negación)

 $y = \mathsf{AE}' + \mathsf{BEF}' + \mathsf{AHF} + \mathsf{CEFG}' + \mathsf{BCEG'} + \mathsf{ACFG}' + \mathsf{ABCG'} + \mathsf{DEFGH'} + \mathsf{CDEFH'} + \mathsf{BDEGH'} + \mathsf{BCDEH'} + \mathsf{ADFGH'} + \mathsf{ACDFH'} + \mathsf{ABCGH'} + \mathsf{ABCDH'} +$

Karnaugh G2:



Ecuación de mintérminos: (El apóstrofe es negación)

3 - A/E - A/BT - B/EF - A/B/CG - A/CFG - B/CEG - C/EFG - A/B/CD/H - A/D/D/H - A/CD/H - A/D/E/H - B/CE/H - B/D/E/H - B/D/E/H - D/EF/H - D/EF/H

Empate: Hemos utilizado una puerta lógica NOR, ya que si no gana ninguno será empate. Si las salidas de G1 y G2 son ambas cero, entonces la salida de Empate será un uno.

Desarrollos para el bloque FSM:

Tabla de estados:

	Q1	Q0
Reposo	0	0
Juega 1	0	1
Juega 2	1	0
Ganador	1	1

Tabla de verdad del bloque FSM.

Start	Q1	Q0	Q'1	Q'0	D1	D0	Load1	Load2	Enable
0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0
0	1	1	1	1	1	1	0	0	1
1	0	0	0	1	0	1	0	0	0
1	0	1	1	0	1	0	1	0	0
1	1	0	1	1	1	1	0	1	0
1	1	1	0	0	0	0	0	0	1

D1 D0

Start\Q1Q0	00	01	11	10
0	0	0	1	1
1	0	1	0	1

Start\Q1Q0	00	01	11	10
0	0	1	1	0
1	1	0	0	1

L1 L2

Start\Q1Q0	00	01	11	10
0	0	1	0	0
1	0	1	0	0

Start\Q1Q0	00	01	11	10
0	0	0	0	1
1	0	0	0	1

Enable

Start\Q1Q0	00	01	11	10
0	0	0	1	0
1	0	0	1	0

(El apóstrofe es negación)

L1=Q1'Q0 L2=Q1Q0' Enable=Q1Q0

D1=Q1Q0'+Start'Q1+StartQ1'Q0

D0= Start'Q0+ StartQ0'

1.Tamaño del diseño:

	Resource	Usage
1	Logic cells	24 / 64 (38 %)
2	Registers	16 / 64 (25%)
3	Number of pterms used	63
4	User inserted logic elements	0
5	☐ 1/0 pins	19 / 36 (53 %)
6	Clock pins	1/2(50%)
7	- Dedicated input pins	1/2(50%)
8	Global signals	2
9	Shareable expanders	0/64(0%)
10	Parallel expanders	5/60(8%)
11	Cells using turbo bit	24 / 64 (38 %)
12	Maximum fan-out node	fsm:inst3linst
13	Maximum fan-out	17
14	Highest non-global fan-out signal	fsm:inst3linst
15	Highest non-global fan-out	17
16	Total fan-out	159
17	Average fan-out	3.70

2.Entradas y salida, con su número pin:

	Name	Pin #
1	D11	19
2	D12	21
3	D13	5
4	D14	20
5	D21	16
6	D22	18
7	D23	4
8	D24	14
9	Empate	8
10	Gana1	6
11	Gana2	11

	Name	Pin #
1	CLK	43
2	LOAD	41
3	RST	1
4	Start	40

3. Hemos tomado como posibles valores de los dados los números del 0 al 15, teniendo en cuenta que son 8 entradas y todas sus posibilidades.