Universidad Carlos III de Madrid

Digital Electronics. 1st midterm exam. March, 2015

Groups 65-69-79-95

Surname, Name:

Time: 1h. 20'

Question 1.1 (write your answer on this question paper)

a) Obtain the representation of +3FAh and –3BBh in the following systems/codes: (8/10)

Hexadecimal	+3FA	-3BB
Decimal system	+1018 1/10	-955 1/10
Binary system	+ 1111111010 1/10	- 1110111011 1/10
BCD code	0001000000011000 1/10	----------
Gray's code	1000000111 1/10	----------
2s-complement code	0111111111010 1/10	1000100010101 1/10

b) Perform the following operation in 2s-complement using the minimum necessary number of bits to represent the addends so that there is no overflow in the operation: (2/10)

+3FAh – (–3BBh)

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  0011111111010   →  +1018
+ 0011101110111   →  + 955
  0111110111101   →  1973
                     check
```

Necessary number of bits:	Sum result (in 2s-C)
12 1/10	0111101110101 1/10

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Question 1.2 (write your answer on this question paper)

We want to design a combinational circuit for a manufacturing plant of ceramic tiles. This circuit will be used to classify and select tiles. The criteria used to select and classify them come from 4 inputs (S, C, W, T):

- First sight examination: S (0 good, 1 wrong)
- Defect detection using a camera connected to a computer: C (0 good, 1 wrong)
- Correct weight detection: W (0 good, 1 wrong)
- Separation by color tone: T (0 light, 1 dark)

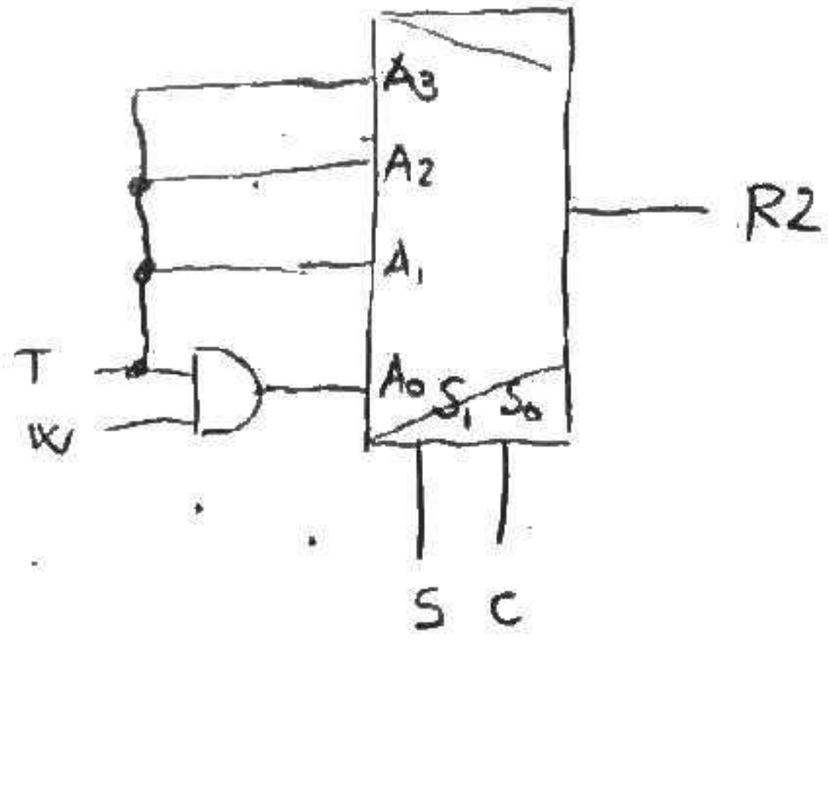
The circuit should have two outputs, to indicate the two following situations:

- R1: rejected tile (any of the tests were wrong)
- R2: rejected dark tile (dark tile and any of the tests were wrong)

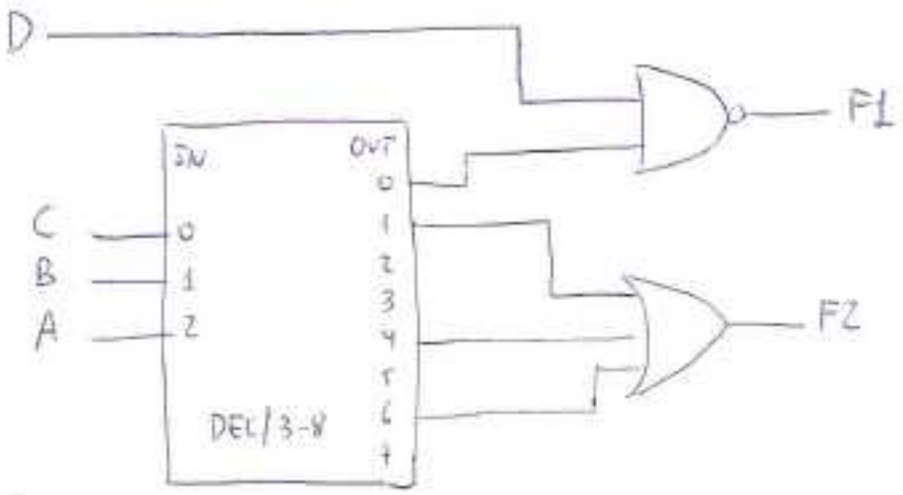
a) Get the truth table of the circuit: 4/10

S	C	W	T	R1 (2/10)	R2 (2/10)	
0	0	0	0	0	0	
0	0	0	1	0	0	W·T
0	0	1	0	1	0	
0	0	1	1	1	1	
0	1	0	0	1	0	
0	1	0	1	1	1	T
0	1	1	0	1	0	
0	1	1	1	1	1	
1	0	0	0	1	0	
1	0	0	1	1	1	T
1	0	1	0	1	0	
1	0	1	1	1	1	
1	1	0	0	1	0	
1	1	0	1	1	1	T
1	1	1	0	1	0	
1	1	1	1	1	1	

b) Implement R2 using a 4:1 multiplexer (4 data inputs) and additional logic gates if necessary 6/10



* Question 1.3



a)

→ $\overline{F1} = \overline{D \cdot out_0}$ → F1 is only "0" if D=1 and $out_0 = 1$, that means D=1, C=0, B=0 and A=0. Otherwise F1=1

→ $F2 = out_3 + out_4 + out_6$ → F2 is "1" if $out_3 = 1$ (A=0, B=0, C=1) or $out_4 = 1$ (A=1, B=0, C=0) or $out_6 = 1$ (A=1, B=1, C=0)

→ Therefore, the truth table is the next one:

A	B	C	D	F1	F2
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	0

b)

AB \ CD	00	01	11	10
00			1	1
01				
11	1	1		
10	1	1		

→ $\bar{a}.\bar{b}.c$

→ $a.\bar{c}$

=> $FZ = \bar{A}.\bar{B}.C + A.\bar{C} =$

NOT (complemented with NOR)

$= \overline{(A+B+\bar{C})} + \overline{\bar{A}+C}$

NOR

NOR

→ $FZ = \overline{A+B+\bar{C}} + \overline{\bar{A}+C}$

* Question 1.4

$F1 = \sum(2,3,6,7,8,9,11,12,13,15) = F1(D,C,B,A)$

$FZ = \sum(0,2,4,8,10,12) = FZ(D,C,B,A)$

4)

DC \ BA	00	01	11	10
00			1	1
01			1	1
11	1	1	1	
10	1	1	1	

→ $\bar{D}.B$

→ $A.B$

→ $D.\bar{B}$

$F1 = \bar{B}.D + A.B + B.\bar{D}$

b)

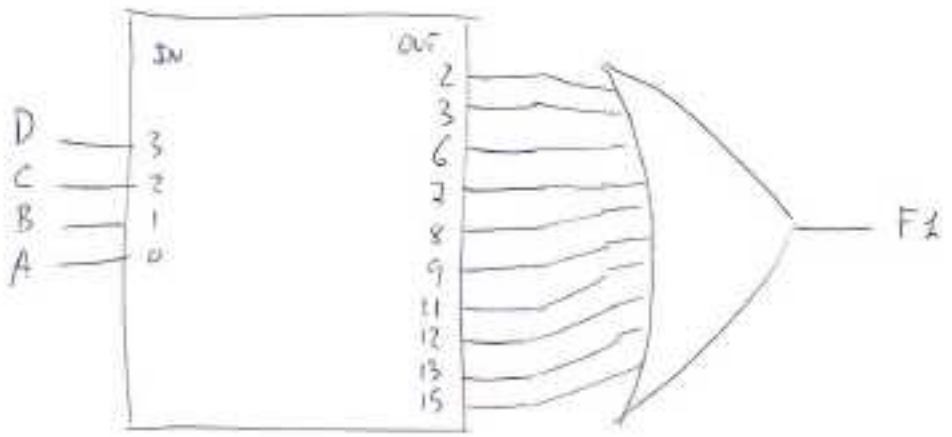
DC \ BA	00	01	11	10
00	1			1
01	1			
11	1			
10	1			1

→ $\bar{C} + \bar{B}$

→ $\bar{A}$

$$F2 = \bar{A} \cdot (\bar{C} + \bar{B})$$

c) 1st solution with OR gates.



2nd solution with NOR gates