PROBLEMA 1

We must design the memory of a digital system. Below, the requirements are detailed:

- Word length (data): 16 bits
- 16K of PROM at the bottom of the memory (smaller directions)
- After the PROM part, we must place 16K of SRAM memory
- 32K of EEPROM memory at top of the memory

The available chips are: 16Kx8 PROM, 16Kx16 SRAM and 32Kx16 EEPROM. All the memory chips modules have active high control signals.

To finish the design, we must answer the following questions:

1. Determine the number of address lines of the system
2. Find the number of memory modules we need of each type.
3. Draw the memory map and indicate the initial al final addresses (in hex) of each of the modules.
4. Obtain the logic functions to decode the memory (CS input of each of the chip modules we will include)
5. Implement the logic functions to decode the memory using a programable logic device as the one shown in figure 1. Use the minimum amount of logic gates.
6. Design the final circuit. Tag all the signals needed to interconnect the memory chips (control signals, data bus and address bus). You do not need to repeat the decoding logic but connect the generated control inputs where necessary.

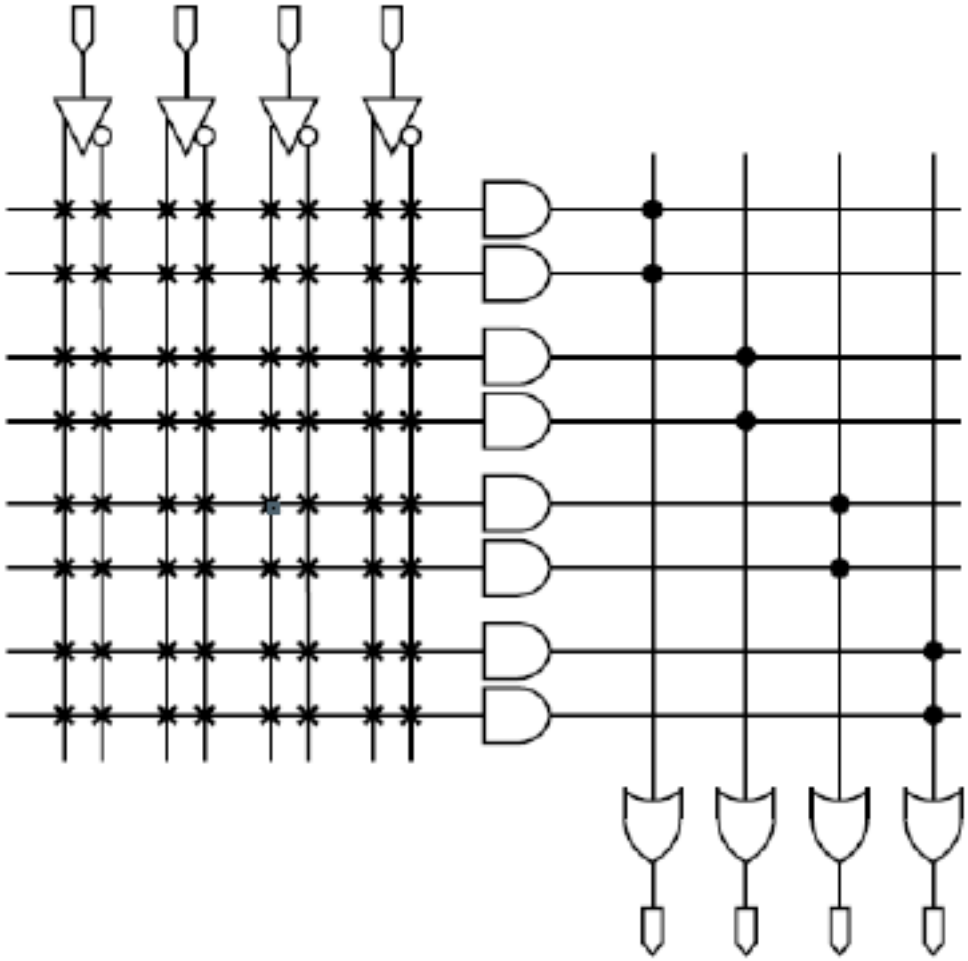


Figure 1

Solution:

1) (1 point)

Memory size = (16K+16K+32K)×16 bits = 64K×16 bits

We need 16 address lines: $64K = 26 \cdot 2^{10} = 2^{16}$

2) (1 point)

PROM (16K×16) → 2 chips of 16K×8 to extend the word size

(PROM1 and PROM2)

SRAM (16K×16) → 1 chip of 16K×16

EEPROM (32K×16) → 1 chip of 32K×16

3) (2 points)

To code 64K = 2^{16} different addresses (16 address lines in the address bus) we need 4 hexadecimal digits. The address bus lines are A15, A14, A13, …, A0, where A15 corresponds to the most significant bit and A0 to the least significant bit

Bank/block	**Memory map**		**Addresses (hex)**
B1	PROM 1 (16Kx8)	ROM2 (16Kx8)	Inicio: 0x0000 Fin: 0x3FFF
B2	SRAM1 (16Kx16)		Inicio: 0x4000 Fin: 0x7FFF
B3	EEPROM (32Kx16)		Inicio: 0x8000 Fin: 0xFFFF

4) (2 points)

The memory block with the smallest size has 16K

64K/16K = 4 → the memory must be divided in 4 blocks de 16K.

To select each of the blocks, we need two lines of the address bus (4=2^2). These lines correspond to the most significant bits of the address bus (A15, A14)

The following table indicates the values of those bits for each of the five memory chip modules we will use:

	A15	A14
PROM1 y 2	0	0
SRAM	0	1
EEPROM	1	X

From the table above, we can deduce the Chip Select control inputs for each one of the memory chips (CS) as functions of A_{15} and A_{14}:

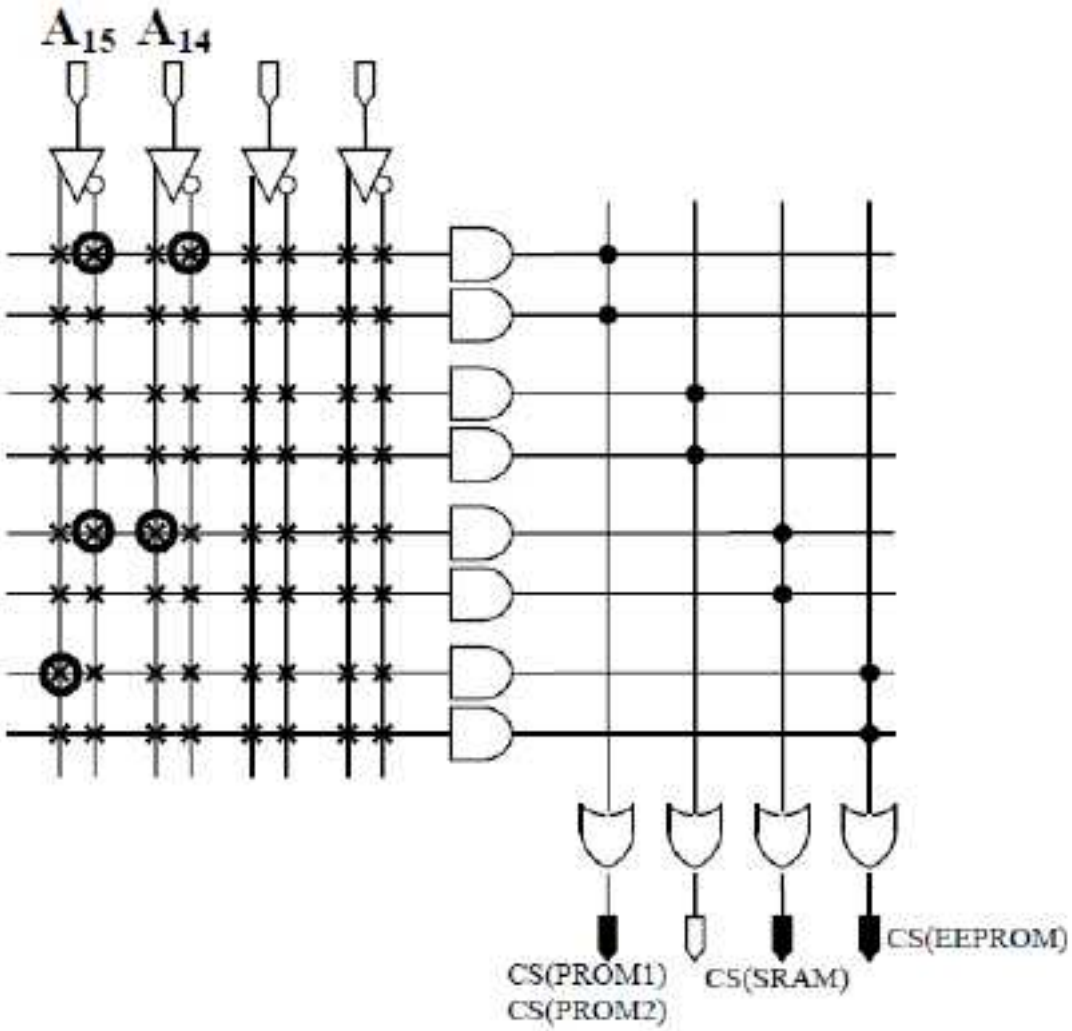
CS(PROM1) = CS(PROM2) = $\overline{A_{15}} \cdot \overline{A_{14}}$

CS(SRAM) = $\overline{A_{15}} \cdot A_{14}$

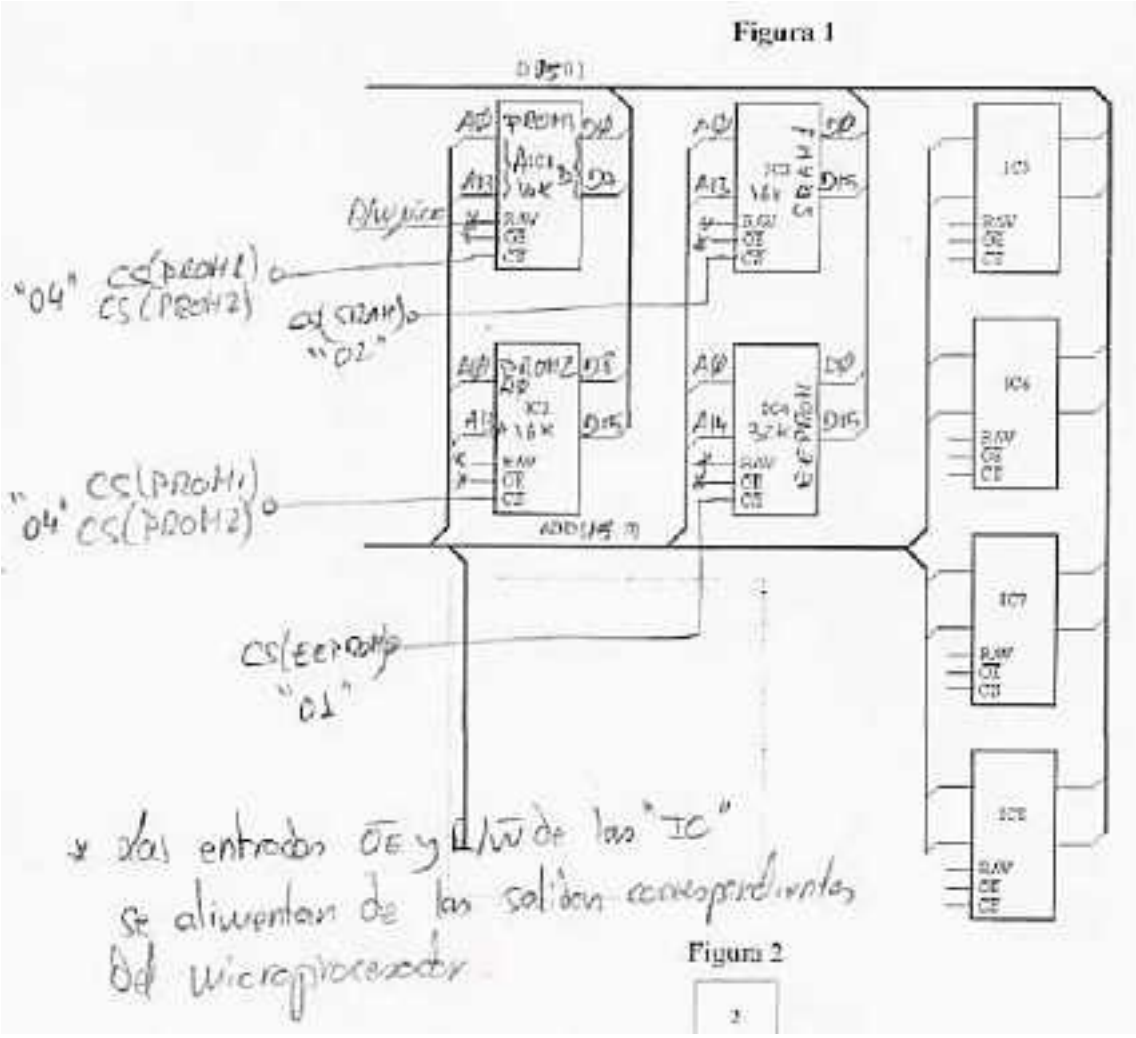
CS(EEPROM) = A_{15}

5) (2 points)

To use the PAL as decoding system we need to connect the A15 and A14 of the address bus as inputs. The decoding system must implement the functions from 4):



5)



Problem from: examen extraordinario curso 2013/14

PROBLEMA 2

We have a memory whose architecture includes 4 RAM 4Kx8 bits modules and 3 ROM Nx8 bits modules. All the ROM memory modules are placed consecutively at the bottom of the memory (smaller addresses). The initial and final addresses of these three ROM modules are 0000 and 3FFF, respectively. Right on top of this ROM block, the four RAM modules are placed.

Considering that the data bus of the system is made with 8 bits, we must answer the following questions:

1. Draw the complete memory map. Indicate the initial and final address of each module in hexadecimal and binary.
2. Indicate the number of address lines necessary to Access all the memory positions of the 7 chips. Elaborate you answer.

3. Indicate the total size of the ROM part of the memory.
4. Indicate the total size of the RAM part of the memory.
5. Which is the size of the total (ROM+RAM) memory, made by 7 modules (4 RAM and 3 ROM)? Elaborate your answer.
6. When operating the memory, we have received the following message on screen: "MEMORY ERROR: ADDRESS HEX 7102". We need to replace the damaged memory module. Which module is that, according to the solution of 1)?
7. A program coded in a low-level language tries to write new data in the memory address 5072_H. We have received the error message: "MEMORY WRITE ERROR: ADDRESS HEX 5072". According to 1), is this possible?
8. If we want to extend the total memory of the system to 253Kx8 bits, maintaining the same ratio between ROM and RAM from 1), how many RAMS de 4Kx8 bits modules do we need?

SOLUCIÓN

1.

Memoria	Dirección	A15	A14	A13	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1RAM 4	FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4K	F000	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
RAM 3	EFFF	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4K	E000	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
RAM 2	DFFF	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
4K	D000	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
RAM1	CFFF	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4K	C000	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ROM3	BFFF	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16k	8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ROM2	7FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16K	4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ROM1	3FFF	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16K	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2. 16 address lines: A0 hasta A15
3. Total ROM = 3x(16Kx8bits) = 48Kx8bits
4. Total RAM = 4x(4Kx8bits) = 16Kx8bits
5. Total memory = RAM + ROM = 62Kx8bits

6. Replace ROM2
7. The error is possible. Address 5072H corresponds to a ROM position, that is a Read Only Memory.
8. Multiply by x4 the solution of 1): 4x(64Kx8bits) = 256Kx8bits. Hence:
   4x4 = 18 RAM modules of 4Kx8bits each.