PROBLEMA 1

We must design the memory of a digital system. Below, the requirements are detailed:

- Word length (data): 16 bits
- 16K of PROM at the bottom of the memory (smaller directions)
- After the PROM part, we must place 16K of SRAM memory
- 32K of EEPROM memory at top of the memory

The available chips are: 16Kx8 PROM, 16Kx16 SRAM and 32Kx16 EEPROM. All the memory chips modules have active high control signals.

To finish the design, we must answer the following questions:

1. Determine the number of address lines of the system
2. Find the number of memory modules we need of each type.
3. Draw the memory map and indicate the initial al final addresses (in hex) of each of the modules.
4. Obtain the logic functions to decode the memory (CS input of each of the chip modules we will include)
5. Implement the logic functions to decode the memory using a programable logic device as the one shown in figure 1. Use the minimum amount of logic gates.
6. Design the final circuit. Tag all the signals needed to interconnect the memory chips (control signals, data bus and address bus). You do not need to repeat the decoding logic but connect the generated control inputs where necessary.

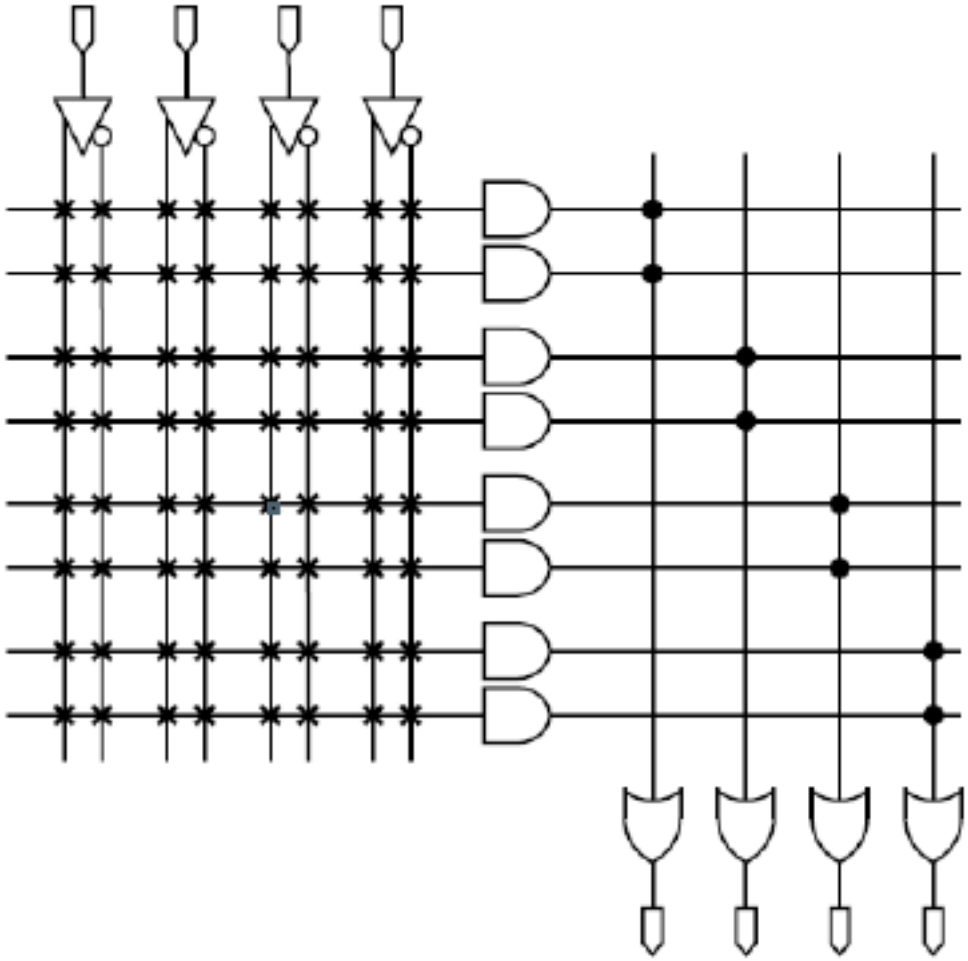

Figure 1

PROBLEMA 2

We have a memory whose architecture includes 4 RAM 4Kx8 bits modules and 3 ROM Nx8 bits modules. All the ROM memory modules are placed consecutively at the bottom of the memory (smaller addresses). The initial and final addresses of these three ROM modules are 0000 and 3FFF, respectively. Right on top of this ROM block, the four RAM modules are placed.

Considering that the data bus of the system is made with 8 bits, we must answer the following questions:

1. Draw the complete memory map. Indicate the initial and final address of each module in hexadecimal and binary.
2. Indicate the number of address lines necessary to Access all the memory positions of the 7 chips. Elaborate you answer.
3. Indicate the total size of the ROM part of the memory.
4. Indicate the total size of the RAM part of the memory.

5. Which is the size of the total (ROM+RAM) memory, made by 7 modules (4 RAM and 3 ROM)? Elaborate your answer.
6. When operating the memory, we have received the following message on screen: “MEMORY ERROR: ADDRESS HEX 7102”. We need to replace the damaged memory module. Which module is that, according to the solution of 1)?
7. A program coded in a low-level language tries to write new data in the memory address 5072_H. We have received the error message: “MEMORY WRITE ERROR: ADDRESS HEX 5072”. According to 1), is this possible?
8. If we want to extend the total memory of the system to 253Kx8 bits, maintaining the same ratio between ROM and RAM from 1), how many RAMS de 4Kx8 bits modules do we need?