Universidad Carlos III de Madrid
Digital Electronics. 2nd midterm exam. April, 2015
Groups 65-69-79-95

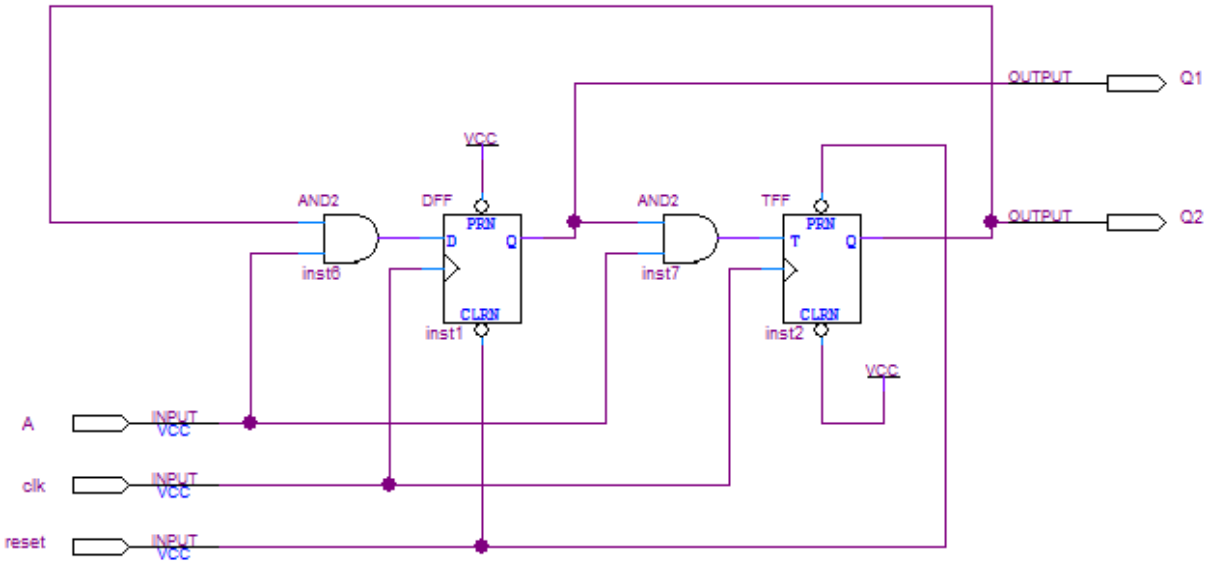
Surname, Name:

Time: 1h. 40’

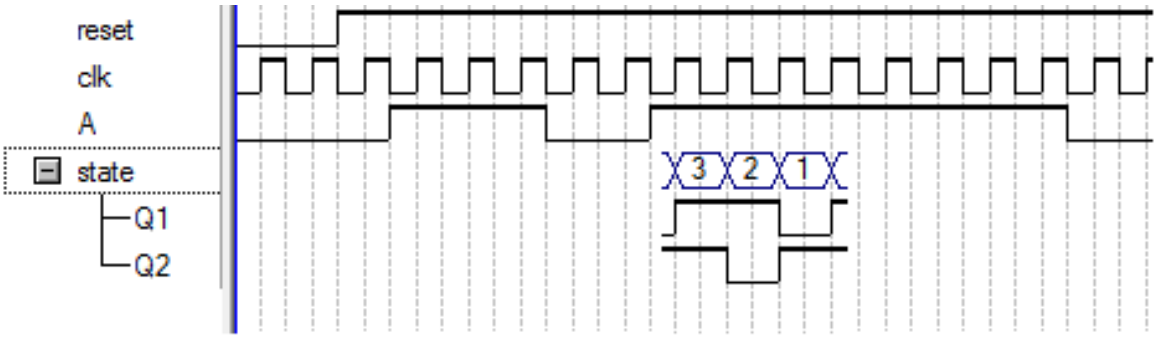
Question 1 *(recommended time: 25’)*

Note: you can hand over the chronogram in this same sheet (remember to write your name)

Given the following circuit:



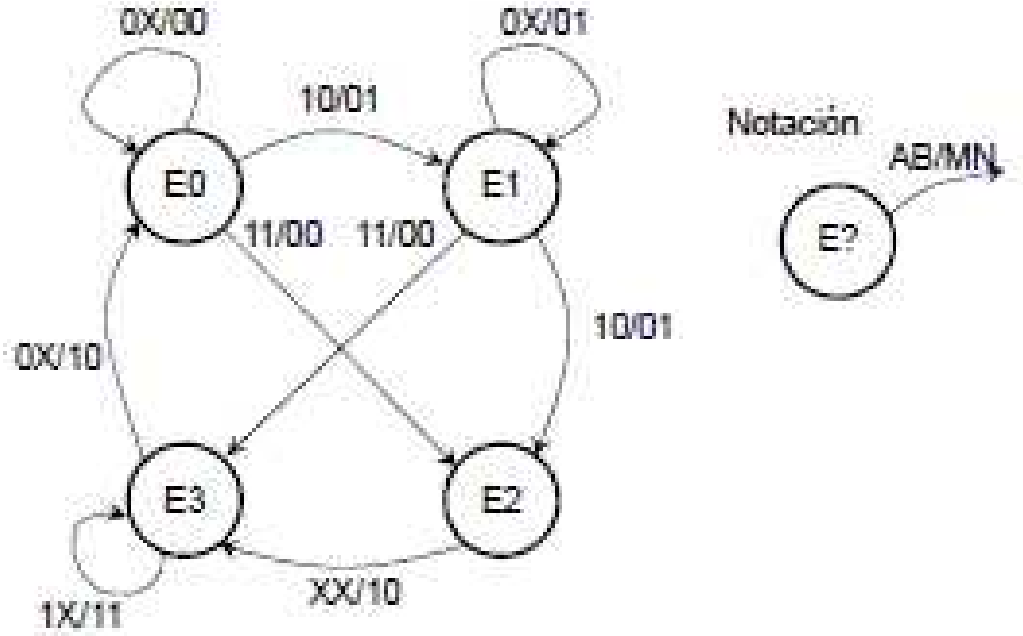
a) Get the expressions of the state functions D and T.
b) Get the transition table of the circuit (use Q1 as MSB and Q2 as LSB).
c) Draw the state transition graph (STG) of the circuit
d) Complete the following chronogram (the state value is represented as unsigned integer, with Q1 as the MSB and Q2 as the LSB).



Question 2 *(recommended time: 25')*

Given the next state transition graph (with the next state assignment: E0 = 00, E1 = 01, E2 = 10, E3 = 11), answer the next points to get the corresponding synchronous sequential circuit using D flip-flops and logic gates (E2 is the initial state). The circuit inputs are A and B, and the circuit outputs are called M and N (see graph legend at the right):

1) Is it a Mealy's or a Moore's circuit?
2) How many flip-flops do you need to solve the problem?
3) Get the transition table
4) Get the state functions
5) Get the output functions
6) Implement (draw) the final circuit



Question 3 *(recommended time: 25')*

a) Draw the State Transition Graph of a **Moore's model** finite state machine for a **sequence generator**. Depending on the value of an input S, the circuit generates one of the two following sequences:

S	Sequence:
0	2-bit Binary counter: 00, 01, 10, 11, 00, 01, 10, …
1	2-bit Gray's code counter: 00, 01, 11, 10, 00, 01, 11, …

When S changes, it is not necessary to complete the current sequence to its end, and it is not necessary either to start the new sequence from 00. Taking these conditions into consideration, try to design the circuit with the minimum possible number of states.

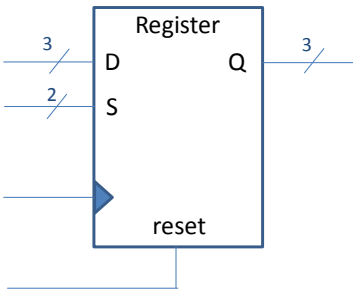
The circuit has only a 1-bit output, the bits are sent in series one after another.

b) Draw the State Transition Graph of a **Moore's model** finite state machine for a **sequence detector**, used to detect any of two the previous sequences, with the following characteristics:

- It receives bits in serial (one bit in each clock rising edge). Note: It has a 1-bit input S.
- It has two 1-bit outputs B and G.
  - B should be activated when a complete binary count from 00 to 11 is detected.
  - G should be activated when a complete Gray's count from 00 to 10 is detected.

Question 4 *(recommended time: 15')*

Design a Universal serial register with the following characteristics:



- It is a 3-bit register, with outputs Q2, Q1, Q0 (Q2 is the most significant bit, and it should be drawn at the left).
- It is synchronous, with a clock input
- It has to be implemented with D flip-flops that have Clear and Preset asynchronous inputs
- It has an asynchronous reset. It is active-low and initializes to (Q2,Q1,Q0) = (1,0,0).
- It has 2-bit selection input S1, S0, that allows to select among the following modes:

S0	S1	Mode
0	0	Hold (keep state)
0	1	Shift Left
1	0	Shift Right
1	1	Load from inputs D2, D1, D0

Question 1 : (2,5 points)

a) State fonctions → (0,25 points)

$$D = A \cdot Q_2$$
$$T = A \cdot Q_1$$

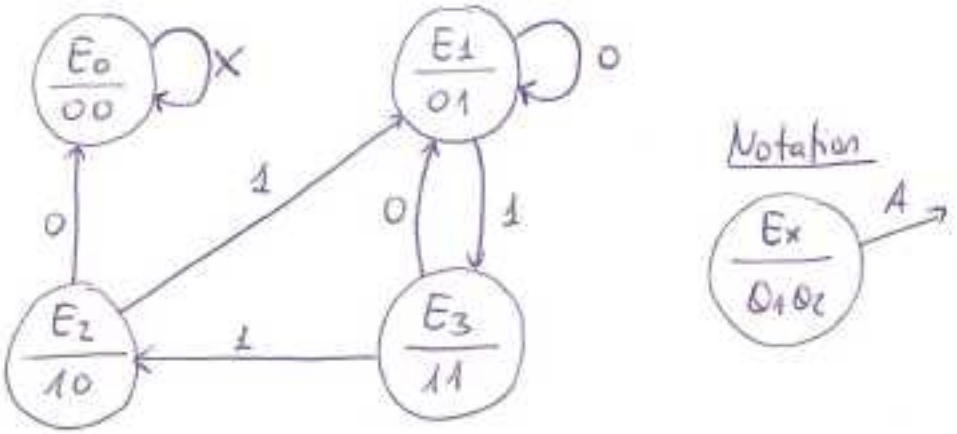
b) Transition table → Looking at the state fonctions and knowing the flip-flop behaviours (0,75 points)

A	Q_1	Q_2	Q_1'	Q_2'	D	T
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	1	1	1	0
1	1	0	0	1	0	1
1	1	1	1	0	1	1

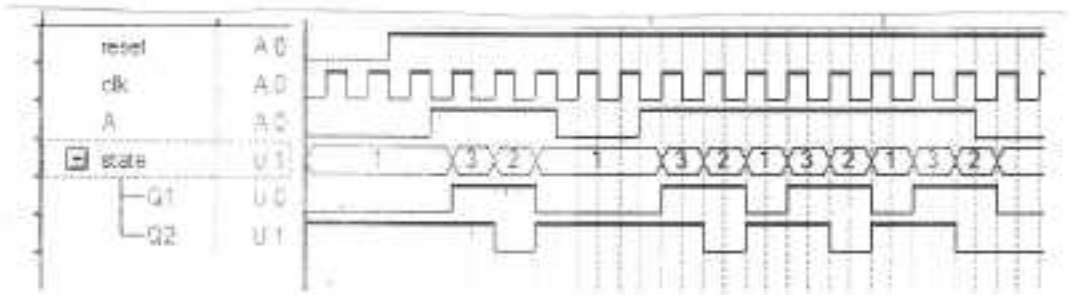
or

Q_1	Q_2	A	Q_1'	Q_2'	D	T
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	1
1	1	0	0	1	0	0
1	1	1	1	0	1	1

c) STG → Looking at the transition table (0,75 points)



d) Chronogram → From the transition table (0,75 points)



Question 2: (2,5 points)

a) It is Mealy because the outputs depends on the states and the inputs (A, B)
(0,1 points)

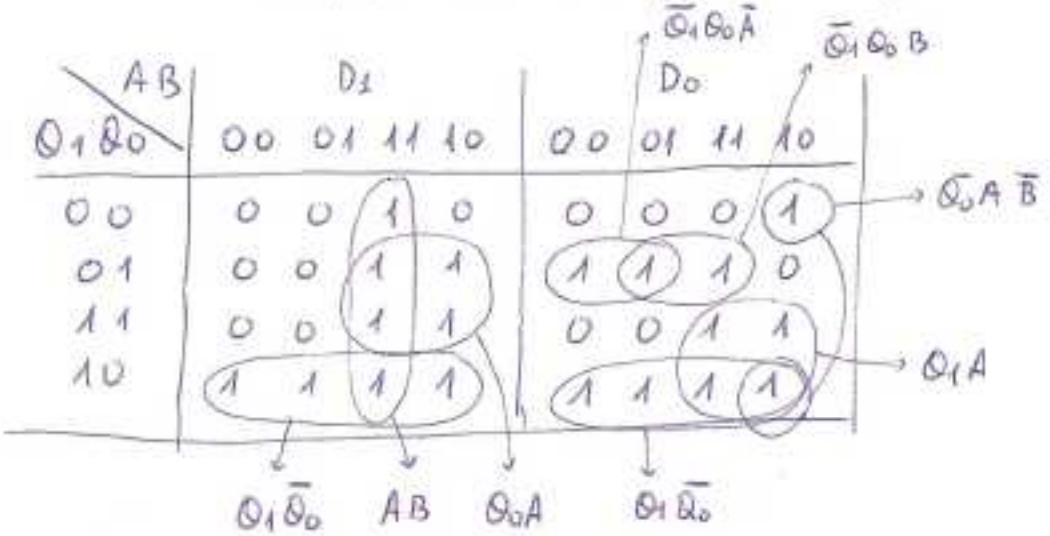
b) $2^n \geq N$ | n = number of flip-flops, N = number of states | $\Rightarrow 2^n \geq 4 \Rightarrow$ **$n = 2$ flip-flops**
(0,15 points)

c) Transition table → looking at the STG (0,5 points)

Q_1	Q_0	A	B	Q_1'	Q_0'	M	N	D_1	D_0
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0	1
0	0	1	1	1	0	0	0	1	0
0	1	0	0	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0	1
0	1	1	0	1	0	0	1	1	0
0	1	1	1	1	1	0	0	1	1
1	0	0	0	1	1	1	0	1	1
1	0	0	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	1	0	1	1
1	1	0	0	0	0	1	0	0	0
1	1	0	1	0	0	1	0	0	0
1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

States & Inputs | States in the next cycle | Outputs | flip-flop inputs

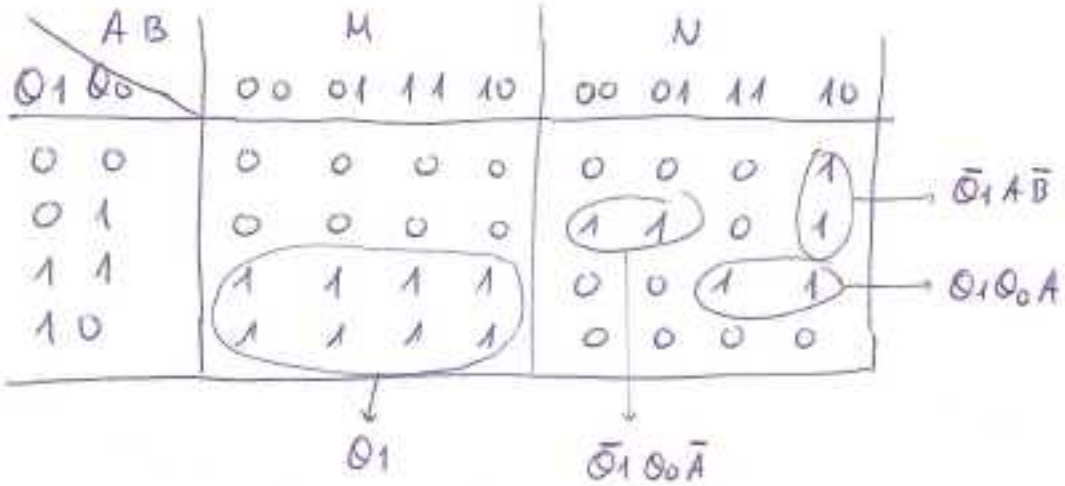
d) State functions → Karnaugh simplification of D_1 and D_0 with Q_1, Q_0, A and B (0,5 points), looking at the transition table



$$D_1 = Q_1 \bar{Q}_0 + AB + Q_0 A$$

$$D_0 = Q_1 \bar{Q}_0 + Q_1 A + \bar{Q}_1 Q_0 \bar{A} + \bar{Q}_1 Q_0 B + \bar{Q}_0 A \bar{B}$$

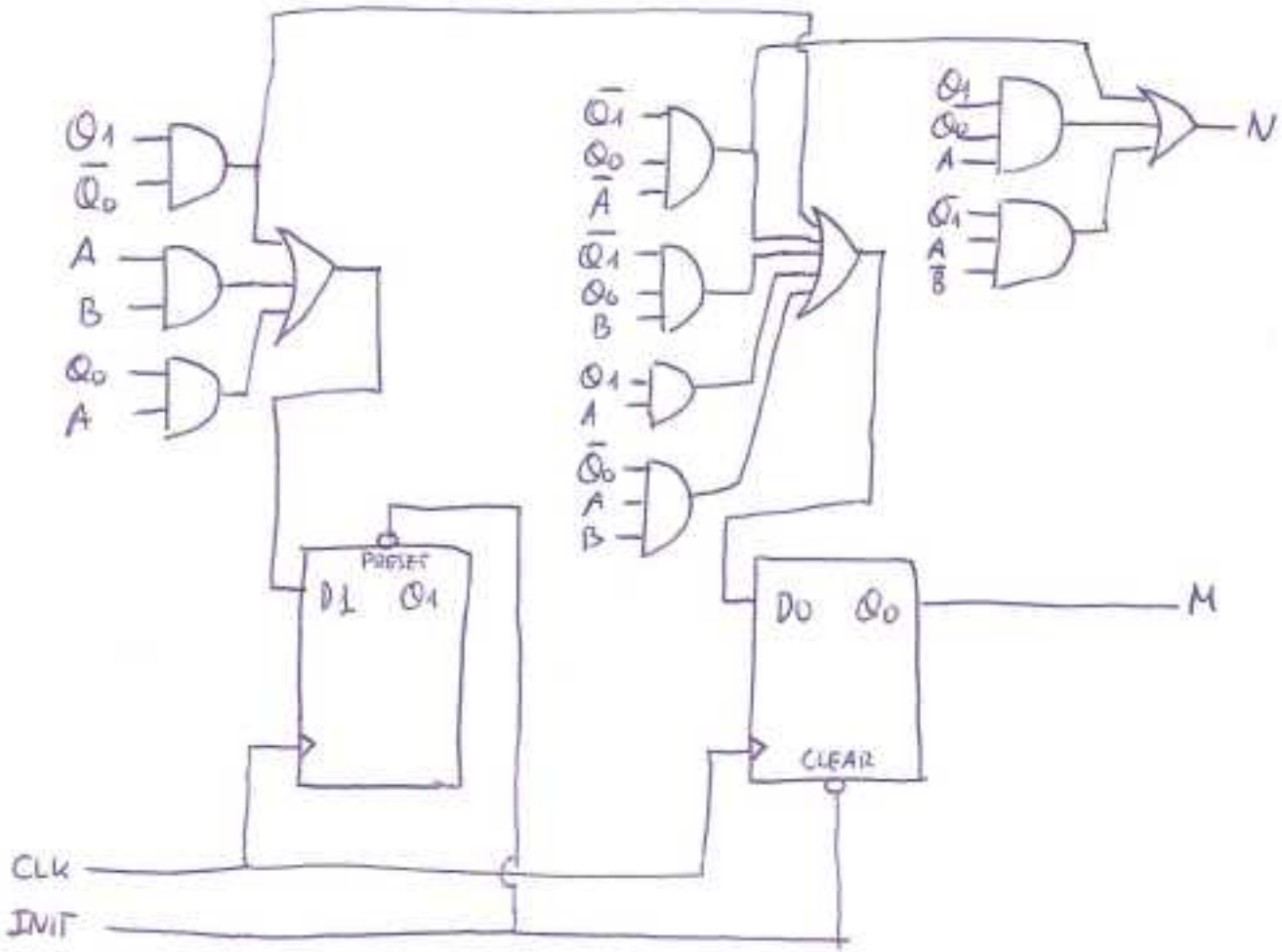
e) Output functions → Karnaugh simplification of M and N with Q_1, Q_0, A and B (0,5 points), looking at the transition table



$$M = Q_1$$

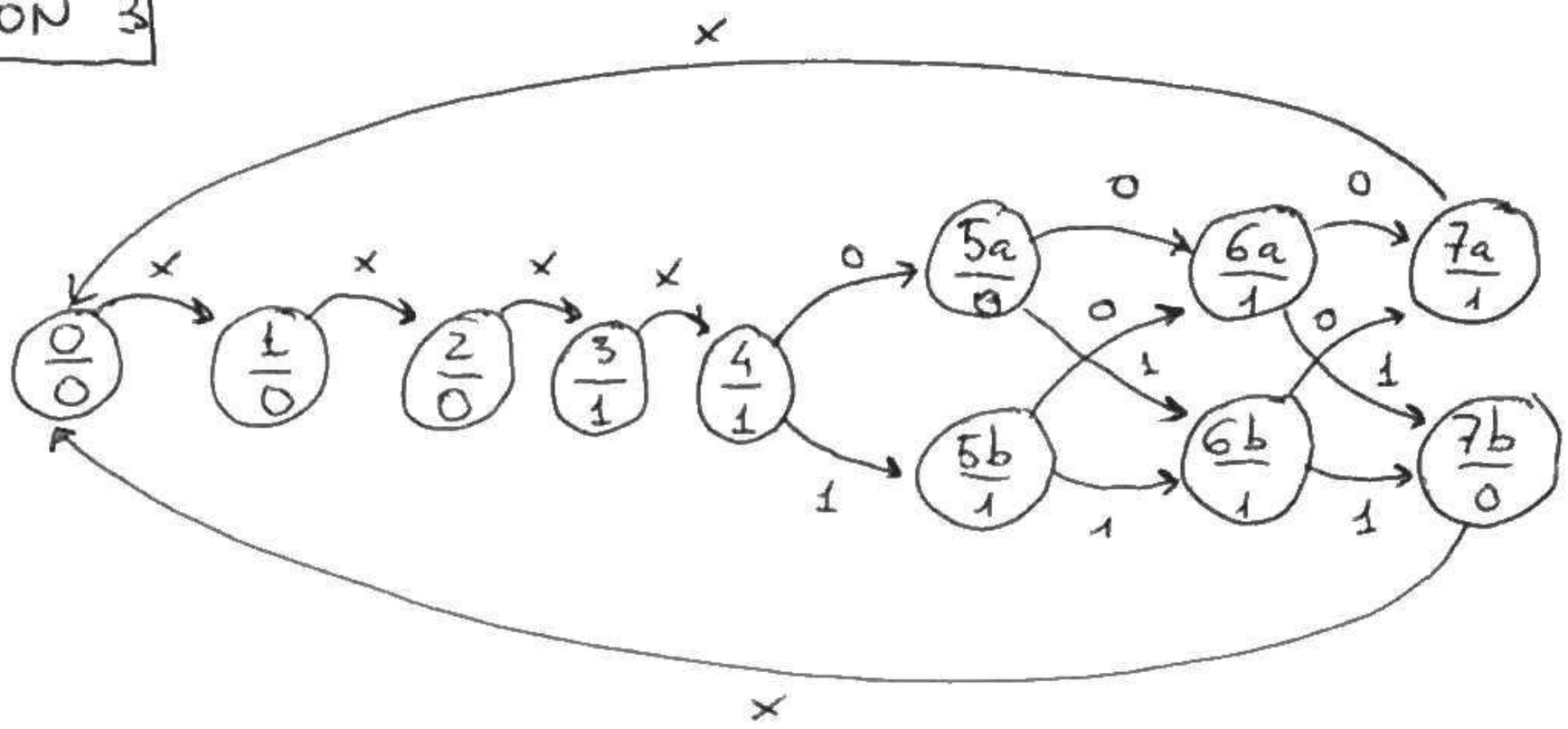
$$N = \bar{Q}_1 Q_0 \bar{A} + \bar{Q}_1 A \bar{B} + Q_1 Q_0 A$$

g) Consider that N, D_1 and D_0 have common components and the initial state is E2 = 10, so that Q_1 must have the init line connected to PRESET and Q_2 must have the init line connected to CLEAR. (0,5 points)

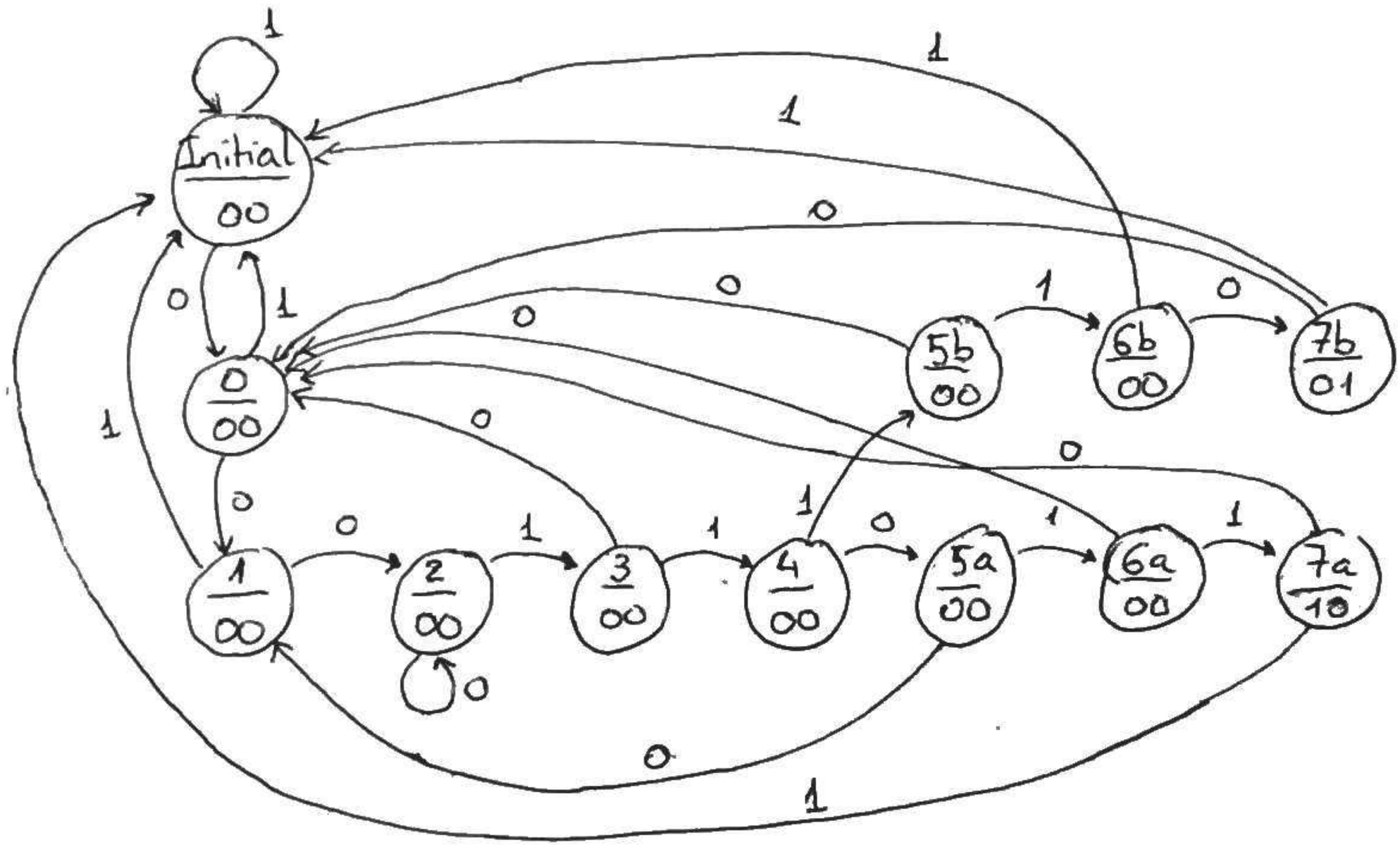


QUESTION 3

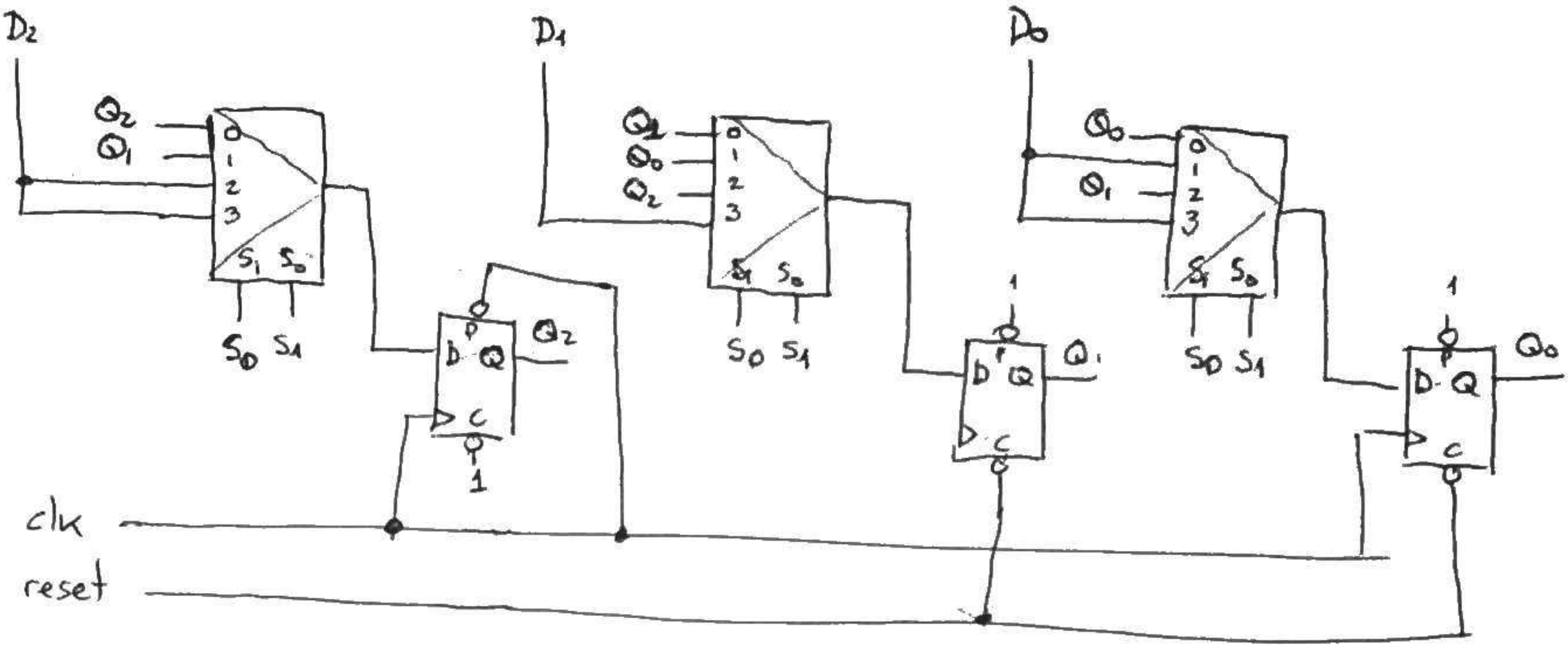
a)



b)



QUESTION 4



Note: it has designed so that D_2 is the serial input when shifting right and D_0 is the serial input when shifting left. There are other possible solutions.