Universidad Carlos III de Madrid

Grados en Ingeniería: Tecnología de Telecomunicaciones, Sistemas de Comunicaciones, Telemática, Sistemas Audiovisuales

ELECTRÓNICA DIGITAL.

Final exam – 26th May 2015

NAME:	**GROUP:**

IMPORTANT:

- **Every problem/question must be handed over separately in a different sheet. Do not mix the solutions of several problems or questions in the same sheet.**
- **Every sheet must include the name and group of the student.**
- **Calculators are not allowed.**

Time: 3 hours

Problem 1 (2.5 points)

A diamond size classification system has 3 light sensors located at 3 different levels: High (SA), Medium (SM) and Low (SB). If a diamond is big, the system activates the 3 light signals. If the diamond is medium-size, the system only activates 2 light signals (SM and SB). If the diamond is small, the system activates one signal (SB). Finally if the diamond is tiny, the system doesn't activate any signal. The system has also a weight sensor calibrated in kilts (SP). This sensor sets to "1" if there are more than 3 kilts and resets to "0" in return. The classification conditions are the next ones:

- A big diamond (G) or a medium-size one (M) must weight 3 kilts at least, otherwise the diamond is rejected (R).
- If the diamond is small, it can't never weight more than 3 kilts, in that case the diamond is rejected (R).
- The tiny diamonds are always rejected (R).
- The unreal conditions must be considered as impossible.

You must solve:

a) Obtain the truth table of the system and show it in the table shown below.
b) Obtain the simplified logic expression of the function R as product of sums
c) Obtain the simplified logic expression of the function R as sum of products
d) Implement the function R using NAND gates.
e) Implement the function R using a multiplexer with 2 selection inputs and the minimal number of extra logic gates.
f) Implement the function R using a decoder with 4 inputs and low-level active outputs, and the minimal number of extra logic gates.

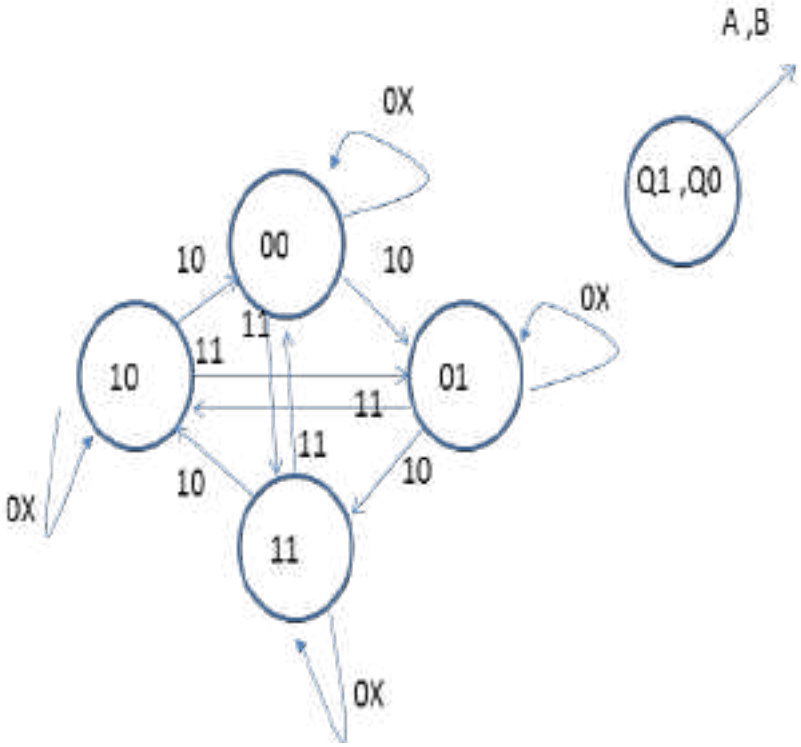
SA	SM	SB	SP	G	M	P	R
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

Problem 2 (2.5 points)

Part 1:
Draw the state transition graph (MOORE) of a sequential system that controls the filling of a vehicle fuel tank.
The filling hose has a valve to control the fuel output. A signal (V) works on this valve, so that if V = ”1”, the valve opens and the fuel flows out, but if the V = ”0”, the valve closes and the fuel can’t flow out.
The fuel hose has a sensor (L) that has the value “1” if the tank is full.
There is a pushbutton (P) that signals a “1” if it is pressed and “0” otherwise.

The operating conditions are as follows:
If the pushbutton is pressed and released immediately (a clock period) and the tank is not full, the fuel flows out until the pushbutton is pressed again or the tank is full (In case of stopping the fuel output pressing the pushbutton, it is necessary to release and press again to let the fuel flow out).
If the pushbutton is pressed and kept pressed (and the tank is not full) the fuel flows out until the pushbutton is released or the tank is filled up.

Part 2:
Given the next state graph, where Q1 and Q0 are the outputs of the flip-flops and A and B are the inputs of the system,



a) Obtain the transition table.
b) Obtain the state functions (the flip-flops are type D).

NAME:	**GROUP:**

Problem 3 (2.5 points)

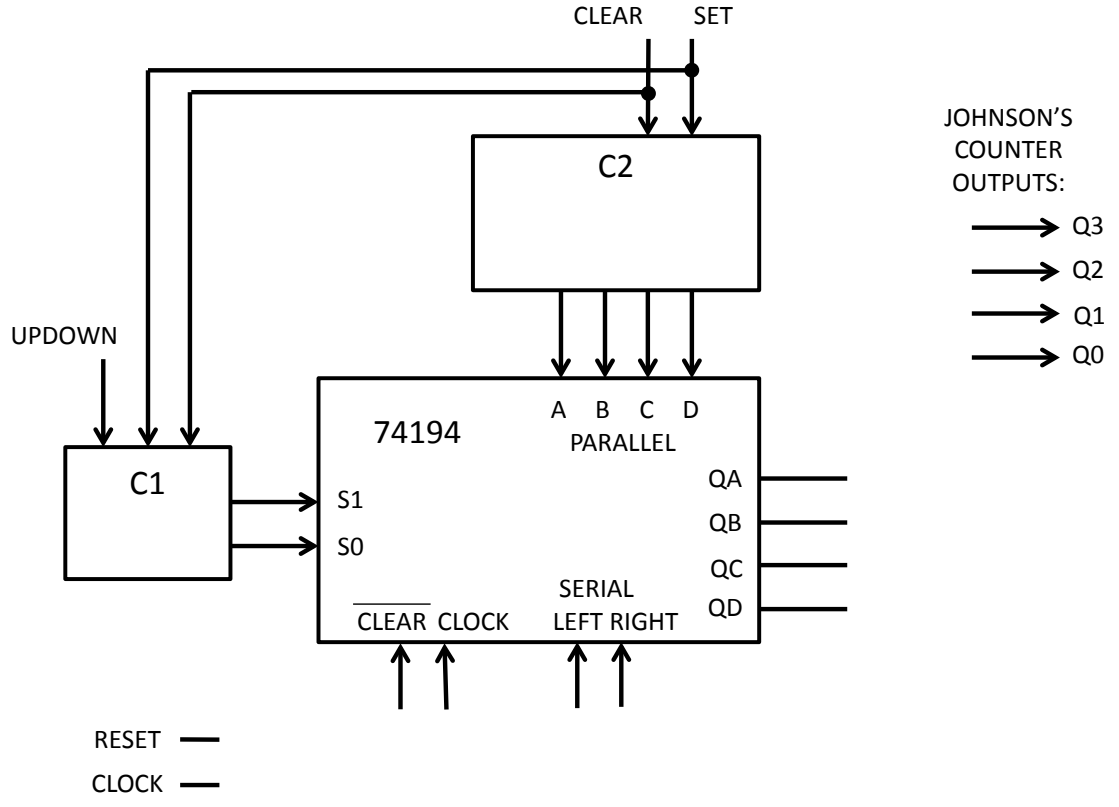
Given the universal shift register 74194, the same register used in the practical session 4, with the next truth table:

TRUTH TABLE

INPUTS										OUTPUS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	⊓	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	⊓	X	X	a	b	c	d	a	b	c	d
H	L	H	⊓	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⊓	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⊓	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⊓	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

X: Don't Care : Don't Care
a ~ d : The level of steady state input voltage at input A ~ D respectively
QA0 ~ QD0 : No change
QAn ~ QDn : The level of QA, QB, QC, respectively, before the mst recent positive transition of the clock.

We want to design a Johnson counter using this chip. In order to accomplish it, the following data path has been designed, where some connections must still be done, and where C1 and C2 are combinational blocks:



The Johnson counter must have these features:

- The system has an UPDOWN input to select the counter as up-counter or down-counter ("0" for up and "1" for down).
- The system has a SET input to preload the counter in a synchronous way with the value "1111"
- The system has a CLEAR input to preload the counter in a synchronous way with the value "0000"
- If SET and CLEAR are active at the same time, the counter will be in a "hold" state (the current count value will not change).

Answer the next theoretical questions:

a) Write the table for the 4-bit Johnson code.
b) Design a 4-bit Johnson counter using a 4-bit shift register (D flip-flops).

Answer the next question about the design of the counter in this problem:

c) Write the truth table of the necessary circuit for the block C2 (use the below table)
d) Write the truth table of the necessary circuit for the block C1 (use the below table).

UPDOWN	CLEAR	SET	S1	S0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table for the block C1

CLEAR	SET	A	B	C	D
0	0				
0	1				
1	0				
1	1				

Table for the block C2

e) Complete the missing connections in the circuit (do it in the data path of the exam sheet and hand it over with the rest of the problem).

Problem 4 (2.5 points)

We want to design the memory of a 16 bits microprocessor with a maximal addressing capacity of 64K, so that it includes the next memory types and sizes:

- 8K of EEPROM, using chips of 4K x 16b
- 16K of SRAM, using chips of 16KB
- 32K of FLASH, using chips of 8K x 16b or 16KB

Note: 1B = 8 bits, 1b = 1 bit

The low positions of the memory map must be used by the FLASH, the high positions of the memory map must be used by the EEPROM and the free gap of the memory must be located between the SRAM y and the EEPROM. You must:

a) Obtain the memory map, with the start and the final addresses of every block in hexadecimal
b) Obtain the decoding system for the memory (CS signals)
c) Draw all the chips of the memory with the data and address buses and the CS signals