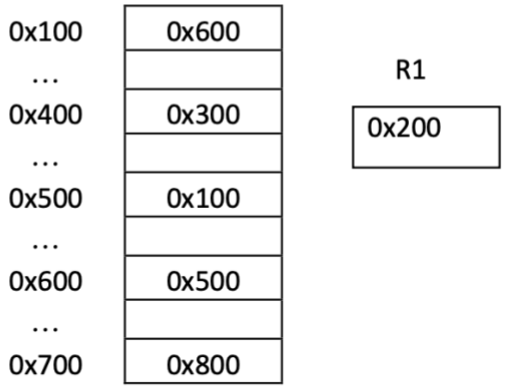
1. Suppose we have the instruction Load 500. Given memory and register R1 contain the values below:



and assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

Ans.

Mode	Value
Immediate	500
Direct	100
Indirect	600
Indexed	800

2. A nonpipelined system takes 200ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 40ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit?

Ans.

SpeedUp = (200ns x 200)/((5+200-1)(40ns)) = 40000/8160 = 4.9019

Max SpeedUp = 5

3. Assume the pipelining of 4 stages, explain the potential pipeline hazards (if any) in each of the code segments in a) and b).

Suppose we have a four-stage pipeline, where:

- S1 = fetch instruction
- S2 = decode and calculate effective address
- S3 = fetch operand
- S4 = execute instruction and store results

a) X=R2+Y
R4= R2+X

b) R1=R2+X
X =R3+Y
Z =R1+X

Ans.

a) The problem is a resource conflict at time 4, as both instructions need to access memory.

Time Period →	1	2	3	4	5
X=R2+Y	fetch instruction	decode	fetch Y	Add & store in X	
R4=R2+X		fetch instruction	decode	fetch X*	

b) The problem is a resource conflict at time 3 and a data dependency at time 5.

Time Period →	1	2	3	4	5	6
R1 = R2 + X	fetch inst	decode	fetch X	Add & store in R1		
X = R3 + Y		fetch instr	decode	fetch Y	Add and store in X	
Z = R1 + X			fetch instr*	decode	fetch X*	