

1.)

22. Suppose we have the instruction Load 500. Given memory and register R1 contain the values below:

0x100	0x600	
...		
0x400	0x300	
...		
0x500	0x100	
...		
0x600	0x500	
...		
0x700	0x800	

R1

0x200

and assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

Ans

Immediate: 0x500

Direct: 0x100

Indirect: 0x600

Indexed: 0x800

2.) A nonpipelined system takes 200ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 40ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit?

Ans

$$\begin{aligned}
 S &= nt_n / (k + n - 1)t_p \\
 &= (200 * 200) / (5 + 200 - 1) * 40 \\
 &= 1000 / 204 \\
 &= 4.901
 \end{aligned}$$

Maximum Speedup (k) = 5

3.) Assume the pipelining of 4 stages, explain the potential pipeline hazards (if any) in each of the code segments in a) and b).

Suppose we have a four-stage pipeline, where:

- S1 = fetch instruction
- S2 = decode and calculate effective address
- S3 = fetch operand
- S4 = execute instruction and store results

a) $X = R2 + Y$
 $R4 = R2 + X$

Ans

The first instruction, $X = R2 + Y$, can be executed in stages S1, S2, S3 and S4. The second instruction, $R4 = R2 + X$, can be fetched in stage S1 while the first instruction is being executed in stage S2, S3, and S4. Therefore, there are no potential pipeline hazards in the instructions.

b) $R1 = R2 + X$
 $X = R3 + Y$
 $Z = R1 + X$

Ans

The first instruction, $R1 = R2 + X$, requires the value of X, which is calculated in the second instruction, $X = R3 + Y$. However, the second instruction has not yet completed when the first instruction is being executed, so there is a data dependency between the two instructions. The third instruction, $Z = R1 + X$, requires the value of R1, which is calculated in the first instruction. However, the first instruction is not complete when the third instruction is being executed, so there is a data dependency between the two instructions. Therefore, to avoid these pipeline hazards, two pipeline stalls are required, one after the first instruction and one after the second instruction.

$R1 = R2 + x$
STALL
 $X = R3 + Y$
STALL
 $Z = R1 + X$

Using two stalls will ensure the instructions are executed in the correct order however, it will also reduce the performance and efficiency of the pipeline.

Group 2 (8 people)

1. 65130500201 Kampol Suwannatam
2. 65130500204 Jirawat Rongsupan
3. 65130500207 Chewin Grerasitsirt
4. 65130500209 Natthanon Somroop
5. 65130500210 Nontakorn Chatkoonsathien
6. 65130500212 Nithit Lertcharoensombat
7. 65130500227 Issadaorn Kulsantao
8. 65130500237 Chayapol Mahatthanachai