1. Description

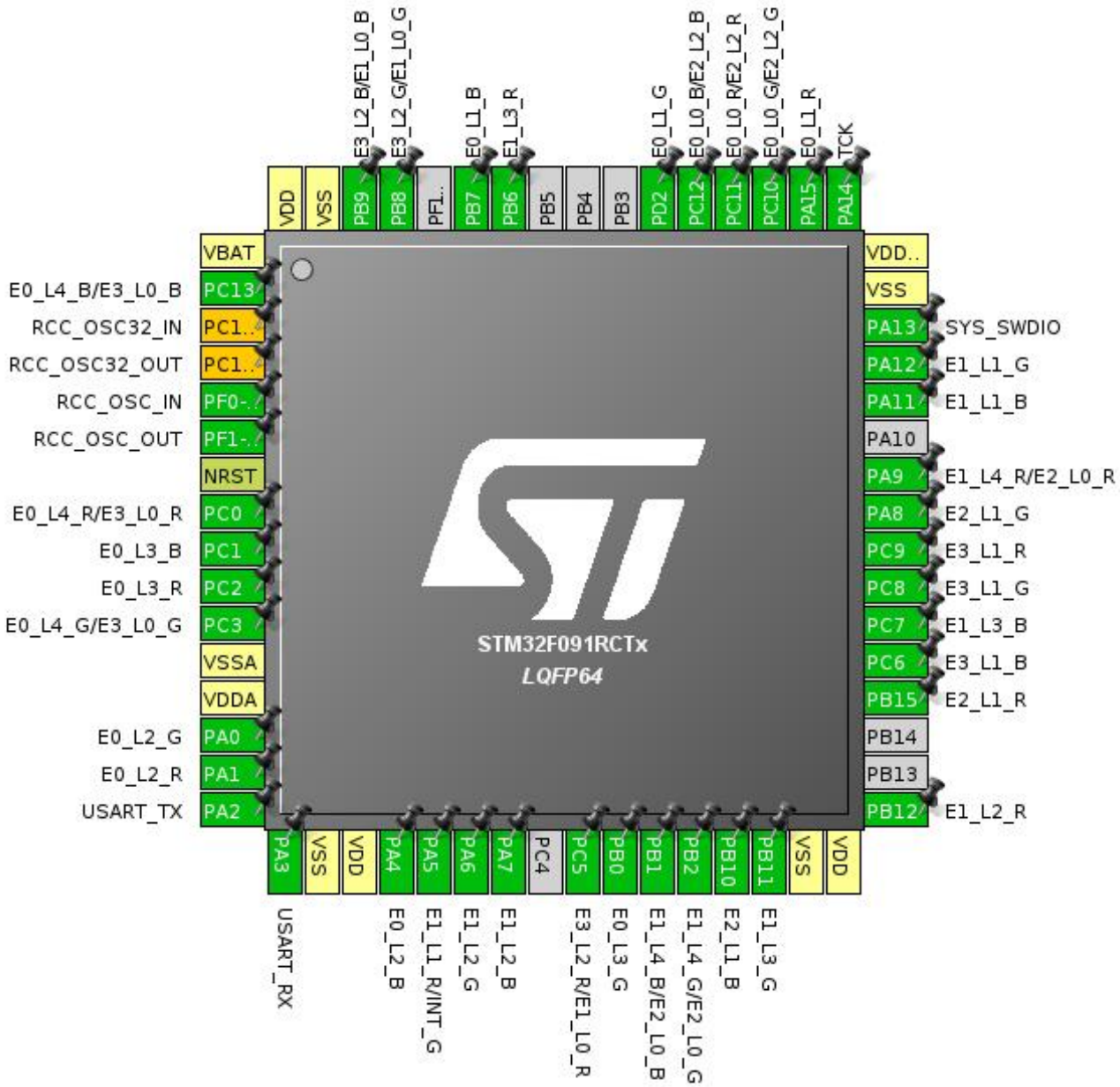
1.1. Project

Project Name	backlight-controller
Board Name	NUCLEO-F091RC
Generated with:	STM32CubeMX 4.13.0
Date	02/27/2016

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x1
MCU name	STM32F091RCTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

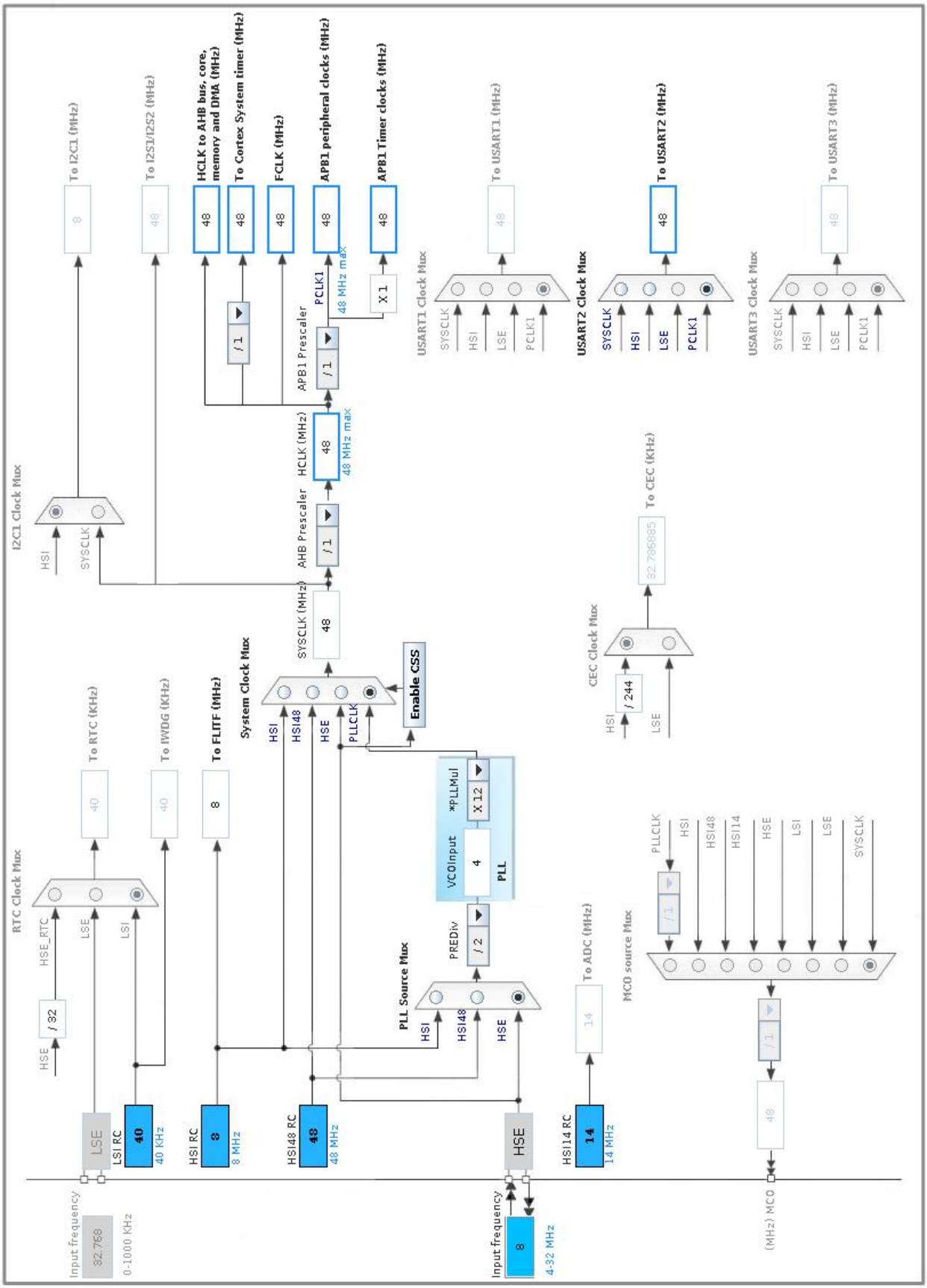
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	E0_L4_B/E3_L0_B
3	PC14OSC32_IN **	I/O	RCC_OSC32_IN	
4	PC15OSC32_OUT **	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	E0_L4_R/E3_L0_R
9	PC1 *	I/O	GPIO_Output	E0_L3_B
10	PC2 *	I/O	GPIO_Output	E0_L3_R
11	PC3 *	I/O	GPIO_Output	E0_L4_G/E3_L0_G
12	VSSA	Power		
13	VDDA	Power		
14	PA0 *	I/O	GPIO_Output	E0_L2_G
15	PA1 *	I/O	GPIO_Output	E0_L2_R
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	E0_L2_B
21	PA5 *	I/O	GPIO_Output	E1_L1_R/INT_G
22	PA6 *	I/O	GPIO_Output	E1_L2_G
23	PA7 *	I/O	GPIO_Output	E1_L2_B
25	PC5 *	I/O	GPIO_Output	E3_L2_R/E1_L0_R
26	PB0 *	I/O	GPIO_Output	E0_L3_G
27	PB1 *	I/O	GPIO_Output	E1_L4_B/E2_L0_B
28	PB2 *	I/O	GPIO_Output	E1_L4_G/E2_L0_G
29	PB10 *	I/O	GPIO_Output	E2_L1_B
30	PB11 *	I/O	GPIO_Output	E1_L3_G
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	E1_L2_R
36	PB15 *	I/O	GPIO_Output	E2_L1_R
37	PC6 *	I/O	GPIO_Output	E3_L1_B
38	PC7 *	I/O	GPIO_Output	E1_L3_B
39	PC8 *	I/O	GPIO_Output	E3_L1_G

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PC9 *	I/O	GPIO_Output	E3_L1_R
41	PA8 *	I/O	GPIO_Output	E2_L1_G
42	PA9 *	I/O	GPIO_Output	E1_L4_R/E2_L0_R
44	PA11 *	I/O	GPIO_Output	E1_L1_B
45	PA12 *	I/O	GPIO_Output	E1_L1_G
46	PA13	I/O	SYS_SWDIO	
47	VSS	Power		
48	VDDIO2	Power		
49	PA14	I/O	SYS_SWCLK	TCK
50	PA15 *	I/O	GPIO_Output	E0_L1_R
51	PC10 *	I/O	GPIO_Output	E0_L0_G/E2_L2_G
52	PC11 *	I/O	GPIO_Output	E0_L0_R/E2_L2_R
53	PC12 *	I/O	GPIO_Output	E0_L0_B/E2_L2_B
54	PD2 *	I/O	GPIO_Output	E0_L1_G
58	PB6 *	I/O	GPIO_Output	E1_L3_R
59	PB7 *	I/O	GPIO_Output	E0_L1_B
61	PB8 *	I/O	GPIO_Output	E3_L2_G/E1_L0_G
62	PB9 *	I/O	GPIO_Output	E3_L2_B/E1_L0_B
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Disabled
Prefetch Buffer	Enabled
Data Cache	Disabled
Flash Latency(WS)	1 WS (2 CPU cycle)

5.2. SYS

mode: Serial-WireDebug

Timebase Source: SysTick

5.3. TIM6

mode: Activated

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.4. USART2

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	*	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	*	Low	USART_RX
Single Mapped Signals	PC14OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L4_B/E3_L0_B
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L4_R/E3_L0_R
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L3_B
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L3_R
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L4_G/E3_L0_G
	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L2_G
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L2_R
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L2_B
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L1_R/INT_G
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L2_G
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L2_B
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3_L2_R/E1_L0_R
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L3_G
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L4_B/E2_L0_B
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L4_G/E2_L0_G
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E2_L1_B
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L3_G
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L2_R
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E2_L1_R
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3_L1_B
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L3_B
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3_L1_G
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3_L1_R

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E2_L1_G
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L4_R/E2_L0_R
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L1_B
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L1_G
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L1_R
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L0_G/E2_L2_G
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L0_R/E2_L2_R
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L0_B/E2_L2_B
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L1_G
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1_L3_R
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0_L1_B
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3_L2_G/E1_L0_G
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E3_L2_B/E1_L0_B

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
Non maskable interrupt	unused		
Hard fault interrupt	unused		
PVD and VDDIO2 supply comparator interrupts through EXTI lines 16 and 31	unused		
Flash global interrupt	unused		
RCC and CRS global interrupts	unused		
TIM6 global and DAC channel underrun error interrupts	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x1
MCU	STM32F091RCTx
Datasheet	026284_Rev2

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	backlight-controller
Project Folder	/mnt/noname-1gbe/xambientbacklight/hardware/nucleo-f091rc/backlight-controller
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F0 V1.5.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No