زانکۆی گەشەپێدانی مرۆیی

UNIVERSITY OF HUMAN DEVELOPMENT

DIGITAL ELECTRONICS LABORATORY

Experiment No.1
Part (I)
Logic gates (AND, OR, NOT, Exclusive-OR)

Object:
To understand digital logic circuits and their functions.

Theory:
In digital logic circuits there are only two voltage levels. Whereas in analog circuits many different voltages may exist at the same time, in digital circuits there are only two.

These two voltages are referred to as logic 1 and logic 0 states. As true and false or by some other similar name. Because of the se of only two states, digital logic is said to be binary in nature.

In digital logic there are three basic elements: the AND gate, the OR gate, and inverter NOT gate. What they do is very simple but it is essential that you under stand them by inter connecting a number of these gates into circuits, thy can perform various increasingly complex functions such as addition of two numbers. Counting multiplication or division of any two numbers. Keeping the time of day, and even running a whole computer.

To learn their characteristics and the simple short and methods by which their functions can be described, the two gates and the inverter will be studied separately.

AND gate:
The AND gate is advice whose output is a logic 1 if both of it's inputs are logic 1.
If only one input is a 1 with the other logic 0, the output will be a 0.

This gate is shown by symbol in Fig (1-a). Where the two inputs are on the left, marked

A and B, and the out put is on the right, marked C. and it's truth table shown in Fig (1-b) , and the logic equation is **C=A.B**

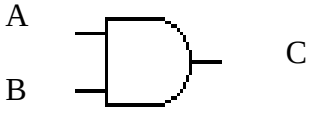


Fig. (1-a) the AND logic gate symbol.

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Fig. (1-b) truth table of AND gate.

OR gate:

The OR gate is a device whose the output is a logic 1 if either or both its inputs are Logic 1. The OR gate is shown by symbol in Fig. (2-a) with two inputs A and B again on the left and output C on the right. And the truth table for OR gate is shown in Fig. (2-b) and the logic equation is **C=A+B**

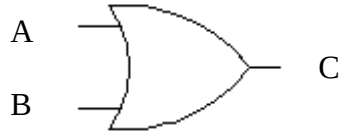


Fig. (2-a) OR logic gate symbol.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Fig. (2-b) truth table of OR gate.

NOT (inverter):

The third and most simple element of digital logic is the inverter. It is also known as the NOT function. The inverter is different from the AND and OR gates, in that it has only a single input. The inverter simply converts logic 1 at its input to logic 0 at its output and conversely, logic 0 to a 1. The inverter can be represented by either of the symbols shown in Fig. (3-a).

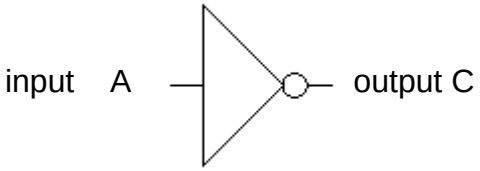


Fig. (3-a) the inverter logic symbol.

A	C
0	1
1	0

Fig. (3-b) truth table of inverter.

NAND gate:

The NAND gate function is the complement of the AND function. As indicated by a graphic symbol which consists of an AND graphic symbol followed by a small circle which represents the NOT gate that is shown in Fig. (4-a) and the truth table shown in Fig. (4-b).

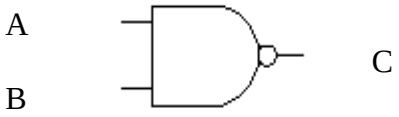


Fig. (4-a)Logic symbol for NAND gate.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Fig (4-b) Truth table for NAND gate.

NOR gate:

The NOR function is the complement of the OR function and uses an OR graphic symbol followed b a small circle which represents NOT gate. That is shown in Fig. (5-a), and the truth table shown in Fig. (5-b).

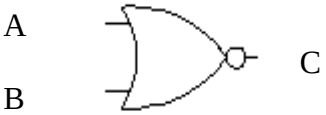


Fig. (5-a) Logic symbol for NOR gate.

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Fig. (5-b) Truth table for NOR gate

Exclusive OR gate:

There is one more gate that needs to be considered- the Exclusive OR gate (EX-OR), shown in Fig. (6-a).the EX-OR gate has a logic high output when either of its input is high, but not when both are high. Notice that in the logic equation we have introduced a new symbol **Θ** called-EX-OR.

The EX-OR gate is quite useful, since its output is high only when the inputs are different, its truth table shown in Fig. (6-b). The logic equation is:-

$C=\bar{A}B+A\bar{B}$

$C=A \oplus B$

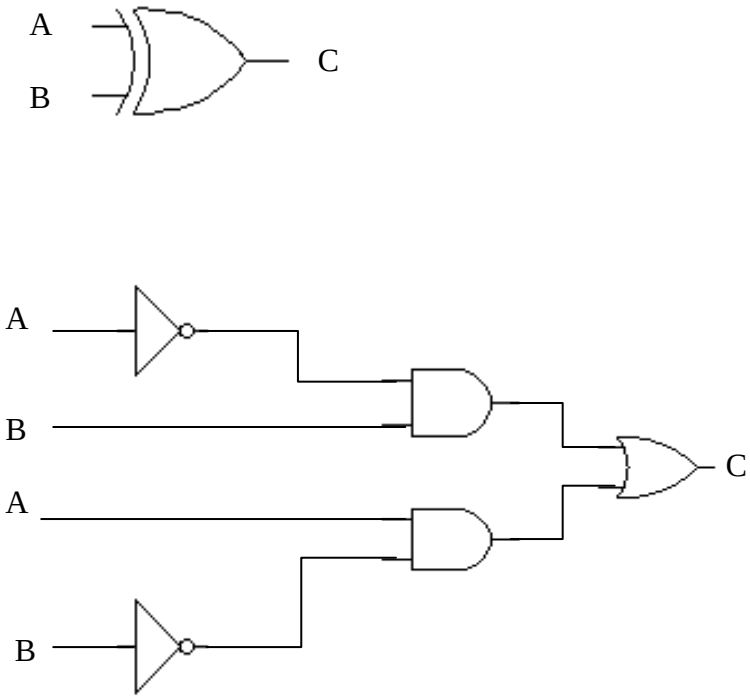


Fig. (6-a) EX-OR logic symbol and equivalent circuit.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Fig. (6-b) Truth table 0f EX-OR.

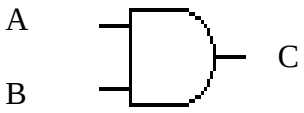
Timing Diagrams:

When a logic gate is performing a useful function in a circuit. Its inputs can change and its output will react to these changes according to the truth tables for that gate. It's quite useful to have a symbolic representation for these logic states, as they change time. A convenient method for doing this is to draw a timing diagram.

In Fig. (7) the operation of AND gate is shown in timing diagram for an arbitrary sequence of high and low logic signals applied to the A and B inputs. Input A, input B and output C of the AND gate are each represented by a continuous line.

Corresponding to whether the particular input or output is logic 1 (high) or logic 0 (low) at particular time.

The main purpose of a timing diagram is to show what the conditions in a logic circuit are at any one particular time. By using timing lines, it is possible to over see an inputs and outputs simultaneously. If any in put or output line is displayed on an oscilloscope screen.



Procedure:

1. Connect the circuit shown in Fig. (1-a).
2. Apply a signal to (A) input from the first pulse generator of amplitude. 4V (P.P), f=1KHz. Draw the wave form of input A.
3. Apply a signal to (B) input from the second pulse generator of amplitude. 4V (P.P), f= 500Hz. Draw the wave form of input B.
4. Draw the output wave form of the AND logic gate.
5. Repeat step (2), (3) and (4) for Fig. (2-a),(4-a),(5-a),(6-a) and draw the output wave forms for each figure.

Discussion:

1. Make a complete truth table for a four input NOR gate.
2. Design the logic circuit for the following conditions and draw the output wave form, X is a 0 if any two of the three variable A. B and C are 1, X is 1 for all other conditions.
3. improve:

   a) AB+A(B+C)+B(B+C)=B+AC

   b) [AB(C+BD)+AB]C=BC

4. Use NAND gate, NOR gate or combinations of both to implement the following expression:

   a) X=A[B+C(D+E)]

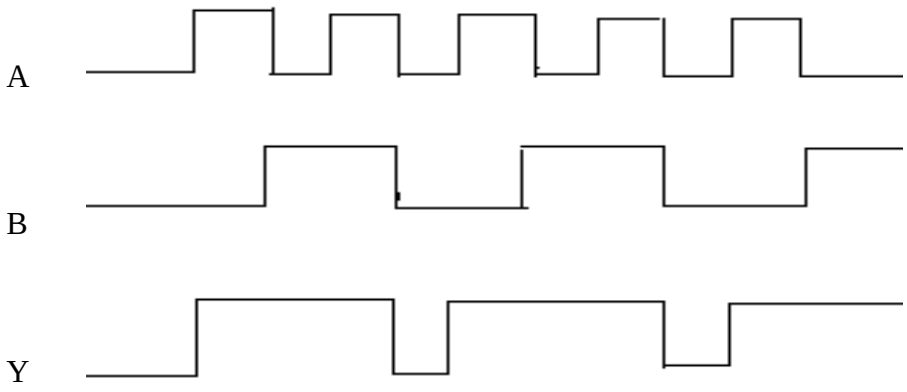
   b) X=B(CDE+EFG)(AB+C)

5. 1) What is the applications of AND gate and OR gate?

   2) In OR gate why 1+1=1?

   3) The Fig. (9-a) shows the A&B inputs plus the Y output, for the OR gate given the A and B inputs of Fig. (9-a) draw the Y output for each of the following

   a) The AND gate.
   b) The NAND gate.
   c) The NOR gate.
   d) The negative AND gate.
   e) The negative OR gate.



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