Pic 16 F 12 176 - 1/P

Note	RB7	RB6		RB5	RB4	RB3	RB2	RB1	RBO	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RAO	I/O ⁽²⁾ 40-Pin PDIP
2: 1:	40	39	3	38	37	36	35	34	33	13	14	7	o	5	4	w	2	40-Pin PDIP
This is a PPS remappable input signal. The input function may be moved from the default location shown to one or several other PORTx pins. All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.		74	-	13	12	=	10	9	8	28	29	22	21	20	19	18	17	40-Pin UQFN
	17	16	10	15	14	=	10	9	00	30	31	24	23	22	21	20	19	44-Pin TQFP
1	17	16	Ď	15	14	12	=======================================	10	9	32	33	24	23	22	21	20	19	44-Pin QFN
VIND	AND7	ANBo	AND 0	ANB5	ANB4 ADCACT(1)	ANB3	ANB2	. ANB1	ANBO	ANA7	ANA6	1	ANA4	ANA3	ANA2	ANA1	ANAO	ADC
01	l,	1		1	1	1	1	1	1	1	1	1	1	VREF+	1	Н	1	Reference
	1	1		1	L	C1IN2- C2IN2-	1	C1IN3- C2IN3-	C2IN1+	ı	1	1	1	C1IN1+	C1IN0+ C2IN0+	C1IN1- C2IN1-	C1INO- C2INO-	Comparator
in	1-	1		1	1	1	1	1	ZCD	1	1	1	ı F	1	1	1	1	Zero-Cross Detect
	DAC10UT2		ı	1	1	1	1	1	1	L	1	1	1	DAC1REF+	DAC10UT1	11	1	44-Pin TQFP 44-Pin QFN ADC Reference Comparator Zero-Cross Detect DAC Timers/SMT
	-1		ı	T1G(1)	1	1	1	-1	1	11	1	1	TOCKI(1)	1	J	T	1	Timers/SMT
-	1		1	1	1	1	1	1	1	1	1	1	1	1	1	П	1	ССР
	1		1	1	1	1	1	1	1	1	1	1	ı	1	1	1	1	PWM
	31		1	1	11	11	1	1	CWG1IN(1)	11-	1	1	1	1	1	ı	1	CWG
			1	1	1	ıf	SDA(1, 3, 4, 5, 6)	SDA(1, 3, 4, 5, 6)	1	E	1	SS(1)	1	1	1	l	1	MSSP
	DT2(1)	CN2(1)	TX2(1)	1	1	11	1	1	L	1	1	1	1	1	1	1	1	EUSART
	CLCIN3(1)		CLCIN2(1)	11	1	1	-1	1	1	1	1	1	1	1	1	CLCIN1(1)	CLCINO(1)	CLC
	74		1	11	1	1	1	1	1	1	1	1	1	1	-1	1.	1	RTCC
	SEG15		SEG14	SEG13 COM1	сомо	SEG11 CFLY2	SEG10 CFLY1	SEG9	SEG8	SEG7	SEG6	1	SEG4 COM3	SEG3	SEG2	SEG1	SEGO	LCD
	IOCB7	-	10СВ6	IOCB5	IOCB4	10СВ3	10СВ2	IOCB1	ЮСВО	IOCA7	IOCA6	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCAO	Interrupt-on-Change
	1		1	1	1	1	1	HB1	1	1	1	1	11	1	1	1	1	High Current
	~		~	~	~	~	~	~	~	~	~	1	~	~	· ~	~	~	Pull-up
	ICSPDAT	ICDDAT/	ICSPCLK/	R. I	-1	1	1	1	INTPPS	OSC1	OSC2	VBAT	1	1	1	1	1	Basic

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Basic	SOSCO	SOSCI	1	1	1	1	ĩ			1	1	1	1	1	1	1	L	1	MCLR
dn-IIn4	>	>	>	>	>	>	>	>	>	-	>	>	>	>	>	>	>	>	>
High Current	1	1	-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1
egnsd-no-tqurrefnl	locco	10001	IOCC2	locc3	IOCC4	locce	10CC7	1	1	1	i	1	1	1	1	1	1	1	IOCE3
гср	1	1	COM2 SEG18	SEG19	SEG20	SEG22 VLCD2	SEG23	SEG24	SEG25	COM5 SEG26	COM4 SEG27	SEG28	SEG29	SEG30	SEG31	SEG32	COM6 SEG33	COM7 SEG34	1
ээтя	T	1	1	1	1	ı	1	ı	1	1	1	1	1	1	1	1	1	1	1
сгс	1	ı	1	-1	ı	ı	1	ı	1	1	1	1	1	1	1	1	1	1	1
TAASUB	1	ı	11	1	1	TX1(1)	RX1(1) DT1(1)	ı	1	242	RXZ	1	ı	1	1	1	1	sope	1
ASSM	1	1	ħ	SCK ⁽¹⁾ SCL ^(1,3,4)	SDI ⁽¹⁾ SDA ^(1,3,4)	1	П	1	1	1	1	1	1	1	1	1	1	el e	1
CMG	1	1	1	L	1	1	1		1	ı	1	1	1	1	1	ı	1	1	1
MWq	1	1	1	Ĩ	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4 00	1	CCP2(1)	CCP1(1)	1	1	1	1		1	Į:	1	1	1	1	1	1	1	1	1
TM&\s19miT	T1CKI ⁽¹⁾ SMTWIN1 ⁽¹⁾	SMTSIG1 ⁽¹⁾ T4IN ⁽¹⁾	1	T2IN(1)	Е	1	1	1	1	I,	1	1	1	1	1	1		1	1
DAC	1	I	1	1	1	1	1	-	1	1	1	1	1	ı	1	1	1.	1	-
Zero-Cross Detect	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		1
Comparator	1	1	1	1	1	1	1	ı	1	1	i	1	1	ı	1	1	1		1
eonere1e7	1	I	Į.	1	1	1	1	ı	1	1	1	1	1	1	1	1	1	1	1
ADC	1	1	ANC2	ANC3	ANC4	ANC6	ANC7	ANDO	AND1	AND2	AND3	AND4	ANDS	AND6	AND7	ANEO	ANE1	ANE2	1
44-Pin QFN	34	35	36	37	42	4	-	38	39	40	4	2	m .	4	2	52	56	27	18
44-Pin TQFP	32	35	36	37	45	4	+	- 1	39	40		-	-	-	-	72	26 2	_	18
40-Pin UQFN	30	31	32	33	38	40	-	-	35	36		-		-	_	73	24 2	_	16
4IQ4 niq-04	15	16	17	00	23	25	26	-	20	21	-	-				0	9		-
I/O(5)	RCO	RC1	RC2	RC3	RC4	RC6		-	RD1	RD2	Barrie B					אבח	RE1		KES

Note	OUT ⁽²⁾	Vss	Voo	VLCD3	I/O ⁽²⁾
5 4 3 2 2		31	32	24	40-Pin PDIP
T S T T A T	-1	6 27	7 26	39	40-Pin UQFN
digital digital sis is a sis a	1	6 29	7 28	43	44-Pin TQFP
a PP(al out a bidi inpu inpu	1	30	7 28	43	44-Pin QFN
This is a PPS remappable input signal. The input function may be moved from the de All digital output signals shown in this row are PPS remappable. These signals may this is a bidirectional signal. For normal module operation, the firmware should map These pins are configured for I ² C logic levels. PPS assignments to the other pins will SMBUS input buffer thresholds. These are alternative I ² C logic levels pins.	ADGRDA ADGRDB	1	1	1	44-Pin TQFP 44-Pin QFN ADC Reference Comparator Zero-Cross Detect DAC Timers/SMT CCP PWM
input signown in the al. For no for I ² C I nolds.	1	1	1	1	Reference
gnal. The in this row are ormal mod ogic levels els pins.	C10UT C20UT	1	1	1	Comparator
nput fur e PPS r lule ope	1	1	1	1	Zero-Cross Detect
nction may be emappable. T eration, the fir assignments t		1	I	1	DAC
moved from these signals in these signals in the mware should the other pire.	TMR0	1	1	_	Timers/SMT
he default nay be ma map this s is will oper	CCP1 CCP2	1	1	1	ССР
location sapped to o signal to the ate, but in	PWM3	1	1	1	PWM
nown to one output onto on e same pin in put logic leve	CWG1A CWG1B CWG1C CWG1D	1	1	1	cwg
This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS These pins are configured for I ² C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as SMBUS input buffer thresholds. SMBUS input buffer thresholds.	SDO SCK SCL SDA	1	1	1	MSSP
PORTx pilex pin opt put and I	822823	1	1	1	EUSART
ins. PPS output registers. T as selected by INLCVL register, instead of the I ² C specific or	CLC10UT RTCC	1	1	I	CLC
egisters.	RTCC	ı	1	1	RTCC
;VL registe	1	ı	1	VLCD3	LCD
r, instead	1	1	1	1	Interrupt-on-Change
of the	1	1	1	1	High Current
I ² C s	- 1	1	1	1	Pull-up
pecific o	1	VSS	VDD	1	Basic
7	SAME TO SECURE A PROPERTY OF THE SECURE AS A SECURE AS	238	122/1/2	0000	II

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Note:

See Table 4 for the pin allocation tables.

Pichelu President

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	Total 4									Capteur I (ADC)	Capteur U (ADC)	Capteur °C (ADC)	DTMF4	DTMF3	DTMF2	DTMF1	I/O in	
	Total 1															DTMF Enable	I/O interrupt	
Total IO: 19	Total 13			AUX-3	AUX-2	AUX	SD	TX DATV	TX 10G - 2	TX 10G - 1	TX 2G4	TX 1G2	FAN	Watchdog	PTTUHF	PTT VHF	I/O Out	THE RESIDENCE OF THE PARTY OF T
	Total 1															BIP	PWM Out	
															COM Accessoire	COM Matrice HDMI	UART	
															Ecran LCD Facade	Matrice video 2	12c	
																	SPI	
																	Timer 8	
																1	Timer 16.	

BIP : generation BIP 1Khz ou autre tone I/O Out : Sortie pour commande ULN 2003

 $Watchdog: Compteur\ externe\ RAZ\ (\ voir\ si\ interne\ OK\)$ $COM\ Acc: Bootloader\ ou\ IHM\ lors\ du\ boot\ sinon\ communication\ vers\ PC\ ou\ interface\ Moxa$