PIC16(L)F19155/56/75/76/85/86 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F19155/56/75/76/85/86 family devices that you have received conform functionally to the current Device Data Sheet (DS40001923**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F19155/56/75/76/85/86 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F19155/56/75/76/85/86 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A1	A3	A4
PIC16F19155	3096h	2001h	2003h	2004h
PIC16LF19155	3097h	2001h	2003h	2004h
PIC16F19156	3098h	2001h	2003h	2004h
PIC16LF19156	3099h	2001h	2003h	2004h
PIC16F19175	309Ah	2001h	2003h	2004h
PIC16LF19175	309Bh	2001h	2003h	2004h
PIC16F19176	309Ch	2001h	2003h	2004h
PIC16LF19176	309Dh	2001h	2003h	2004h
PIC16F19185	30BAh	2001h	2003h	2004h
PIC16LF19185	30BBh	2001h	2003h	2004h
PIC16F19186	30BCh	2001h	2003h	2004h
PIC16LF19186	30BDh	2001h	2003h	2004h

Note 1: The Device and Revision IDs is located at the respective addresses 8006h and 8005h of configuration memory space.

2: Refer to the *"PIC16(L)F191XX Memory Programming Specification"* (DS40001880) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Summary	Affected Revisions		
				A1	A3	A4
Analog-to-Digital Converter with Computation (ADC^2)	ADC^2 with Fixed Voltage Reference (FVR)	1.1	Using the FVR as the ADC positive voltage reference can cause missing codes.	X		
	ADC^2 with Guard Ring Outputs	1.2	The Guard Ring Output feature is not implemented.	X		
	ADC^2 FRC Clock Sleep Mode	1.3	If in Sleep and ADRC is used, the oscillator continues to run after conversion.	X		
	ADC^2 FRC Clock ADGO Delay	1.4	When using FRC as clock source, there is a delay of 1 instruction cycle.	X		
	ADC^2 Conversion	1.5	At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground.	X		
Reset and VBAT	VBAT with ULPBOR	2.1	Higher current with ULPBOR active.	X		
Liquid Crystal Display (LCD) Controller	Internal VLCD3 Measurement	3.1	Non-stable readings.	X		
	1/2 MUX, 1/2 Bias with External Resistor Ladder	3.2	1/2 MUX, 1/2 Bias with External Resistor Ladder is not operational.	X		
Comparator (CMP)	C2 Low-Power Clocked Comparator	4.1	Unstable output.	X	X	X
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	5.1	WWDT only operates from the LFINTOSC clock source.	X		
Real-Time Clock and Calendar (RTCC)	RTCC Alarm	6.1	An alarm will not occur if the lower nibble of ALRMLSEC <3:0> is configured to 0x0.	X		
Electrical Specifications	SMBus VIL Level	7.1	The maximum VIL level changes when VDD is below 4.0V.	X		
	Fixed Voltage Reference (FVR) Accuracy	7.2	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	X	X
	Nonvolatile Memory (NVM) for LF Devices	7.3	Performing a row erase through the NVMREG access may not execute as expected when VDD is lowered.	X	X	X
	Min VDD Specification	7.4	VDD Min. specifications are changed for LF devices only.	X	X	X
Device Information Area (DIA)	Fixed Voltage Reference Data	8.1	FVR Reference Data may be missing	X		

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Analog-to-Digital Converter with Computation (ADC^2)

1.1 ADC^2 with Fixed Voltage Reference (FVR)

Using the FVR as the positive voltage reference (V_{REF+}) for the ADC, can cause an increase in missing codes.

Work around

Method 1: Increase the bit conversion time, known as TAD, to 8 µs or higher.

Method 2: Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A3	A4					
X							

1.2 ADC^2 with Guard Ring Outputs

The two guard ring drive outputs ADGRDA and ADGRDB are not implemented on these devices.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

1.3 ADC^2 FRC Clock Sleep Mode

If the part is in Sleep and the ADCRC oscillator is used as the clock source to the ADC, the oscillator continues to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

1.4 ADC^2 FRC Clock ADGO Delay

When using the FRC as the clock source for ADC^2, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test (`BTFSC`) instruction on the ADGO bit, immediately after setting the ADGO bit. See Code Example below.

```
BSF     ADCON0,ADGO ;Start conversion
BTFSC   ADCON0,ADGO ;Is conversion done?
GOTO    $-1           ;No, test again
```

The `BTFSC` will pass the very first time in this situation.

Work around

Add a `NOP` instruction after setting the ADGO bit and before testing the bit for completion of conversion. See Code Example below:

```
BSF     ADCON0,ADGO ;Start conversion
NOP
BTFSC   ADCON0,ADGO ;Is conversion done?
GOTO    $-1         ;No, test again
```

Affected Silicon Revisions

A1	A3	A4					
X							

1.5 ADC^2 Conversion

At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground, which in turn may take some charge out of the internal sample and hold capacitor. The problem is more pronounced on inputs with an impedance greater than 1 kΩ.

This issue will be seen when sampling the following internal channel inputs: FVR, DAC, and Temperature Indicator and when sampling external sources on an analog pin, including the CVD.

Work around

When sampling the internal channel inputs, FVR, DAC, and Temperature Indicator, increase the minimum T_{AD} time to 4 µs to increase accuracy.

When sampling an external source through an analog pin, keep the input impedance below 1 kΩ.

When using the ADC as an internal reference for the CVD module, there is no work around.

Affected Silicon Revisions

A1	A3	A4					
X							

2. Module: Reset and VBAT

2.1 VBAT with ULPBOR

In order to avoid high IBAT currents of 10 µA or greater, when utilizing VBAT to provide battery backup the ULPBOR should not be activated. When the part is used in this fashion, VDD should also be either off (0 volts) or >1.5V.

Work around

Do not use VBAT along with ULPBOR.

Affected Silicon Revisions

A1	A3	A4					
X							

3. Module: Liquid Crystal Display (LCD) Controller

3.1 Internal VLCD3 Measurement

The ¼ scale tap point provided on the LP Resistor Ladder for use together with the ADC does not provide stable readings to support monitoring of the LCD pump output level.

Work around

Measure the VLCD3 via an external ADC.

Affected Silicon Revisions

A1	A3	A4					
X							

3.2 1/2 MUX, 1/2 Bias with External Resistor Ladder

The 1/2 MUX, 1/2 bias with External Resistor Ladder mode of operation is non-functional.

Work around

For 1/2 MUX, 1/2 Bias mode operation use the internal LP, MP or HP ladder.

Affected Silicon Revisions

A1	A3	A4					
X							

4. Module: Comparator (CMP)

4.1 C2 Low-Power Clocked Comparator

The output of the Low-Power Clocked Comparator (CMP2) is unstable and is not recommended for use.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

5. Module: Windowed Watchdog Timer (WWDT)

5.1 Watchdog Timer Clock Source

When the WDTCS <2:0> bits of the WDTCON1 register are set to either the MFINTOSC (b'001') or the SOSC ('b010') clock source, the WWDT does not operate.

Work around

Use the LFINTOSC (b'000') as the clock source for the WWDT.

Affected Silicon Revisions

A1	A3	A4					
X							

6. Module: Real-Time Clock and Calendar (RTCC)

6.1 Real-Time Clock and Calendar (RTCC) Alarm

When using the RTCC alarm function in any mode other than AMASK<3:0> = 0b0000 or AMASK<3:0> = 0b0001, an alarm will not occur if the lower nibble of the ALRMSEC register, ALRMLSEC <3:0>, is configured to 0x0.

Work around

If an alarm is desired when the lower nibble of the SECONDS register = 0x0, configure ALRMLSEC<3:0> = 0xA.

Affected Silicon Revisions

A1	A3	A4					
X							

7. Module: Electrical Specifications

7.1 SMBus VIL Level

When the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus voltage level for the VIL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus voltage level for VIL drops to 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

7.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

7.3 Nonvolatile Memory (NVM) for LF Devices

Performing a row erase through the NVMREG access on LF devices may not execute as expected when VDD is lowered from >3.3V down to <2.0V before or during the row erase, while also operating between +25°C and -40°C.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

7.4 Minimum VDD Specification for LF Devices

VDD minimum parameter (D002) at -40°C to +25°C = 2.3V. (See Table 39-1 for reference.)

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

8. Module: Device Information Area (DIA)

8.1 Fixed Voltage Reference Data

Devices marked with date code 1846 and older, may or may not have the measured FVR reference data stored in DIA address locations 8118h through 811Dh. Devices marked with date code 1847 and newer are not affected.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001923**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

1.1 Table 39-1: Supply Voltage

The minimum V_{DD} specification for LF devices is shown below: V_{DD} minimum parameter (D002) at -40°C to 25°C = 2.3V.

TABLE 39-1: SUPPLY VOLTAGE

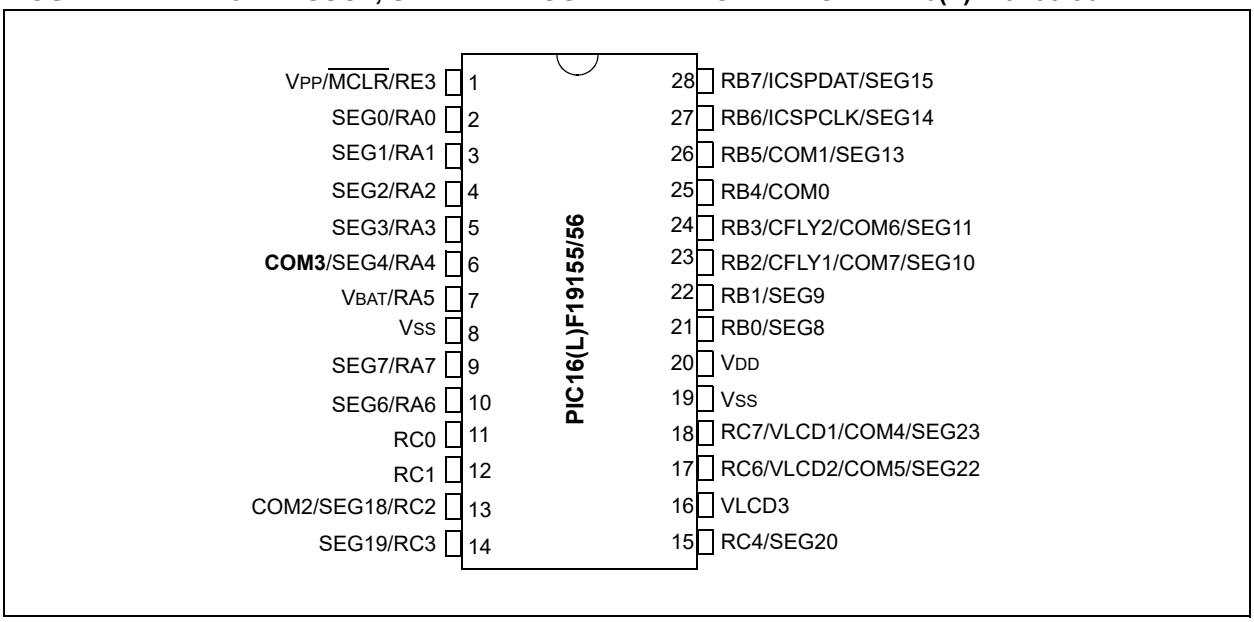
PIC16(L)F19155/56/75/76/85/86			Standard Operating Conditions (Unless Otherwise Stated)				
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D002	V_{DD}		1.8 2.3 2.5	— —	3.6 3.6 3.6	V V V	$F_{OSC} \leq 16$ MHz, $T_A > 25°C$ $F_{OSC} \leq 16$ MHz, $-40°C \leq T_A \leq 25°C$ $F_{OSC} > 16$ MH

2. Module: Pin Diagrams

2.1 Pin Diagrams, Figure 1

The COM0 function multiplexed to RA4 is changed to COM3, as shown below.

FIGURE 1: 28-PIN SSOP, SPDIP AND SOIC PIN DIAGRAM FOR PIC16(L)F19155/56



APPENDIX A: DOCUMENT REVISION HISTORY

Rev J Document (10/2022)

Added DS Clarification, Module 2: Pin Diagrams.

Rev H Document (11/2021)

Added silicon revision A4.

Rev G Document (02/2021)

Updated Table 2 and sub-section 7.4. Added DS Clarifications Module 1: Electrical Specifications. Other minor editorial corrections.

Rev F Document (06/2019)

Data Sheet Clarifications: Removed all modules (Data Sheet updated).

Rev E Document (04/2019)

Added silicon rev. A3.

Removed Module 1.5: ADC^2 Channel Switching.

Added Module 8: Device Information Area (DIA).

Data Sheet Clarifications: Added Module 1.2: TAD Parameters. Updated Section 3: Capture/Compare/ PWM Modules.

Rev D Document (09/2018)

Added Module 1.3 ADC^2 FRC Clock Sleep Mode. Added Module 1.4 ADC^2 FRC Clock ADGO Delay. Added Module 1.5 ADC^2 Channel Switching. Added Module 1.6 ADC^2 Conversion. Added Module 3.2 1/2 MUX, 1/2 Bias with External Resistor Ladder. Added 5.1 Watchdog Timer Clock Source. Added Module 6: Real-Time Clock and Calendar (RTCC) and 6.1 RTCC Alarm. Updated Table 2.

Rev C Document (05/2018)

Added silicon issue 5.4: Min VDD Specification for LF devices.

Data Sheet Clarifications: Added Module 1: Analog-to-Digital with Computation (ADC^2) and Module 2: Real-Time Clock and Calendar (RTCC).

Rev B Document (11/2017)

Added silicon issue 5.3: Nonvolatile Memory (NVM) for LF devices.

Rev A Document (06/2017)

Initial release of this document; issued for revision A1. Includes silicon issues 1.1 (ADC^2), 2.1 (VBAT), 3.1 (LCD), 4.1 (CMP), Electrical Specifications: 5.1 SMBus, 5.2 Program Flash Memory, and 5.3 FVR.

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