PIC16F19176-I/P
E

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RA0	2	17	19	19	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	CLCIN0(1)	—	SEG0	IOCA0	—	Y	—
RA1	3	18	20	20	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	CLCIN1(1)	—	SEG1	IOCA1	—	Y	—
RA2	4	19	21	21	ANA2	—	C1IN0+ C2IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	SEG2	IOCA2	—	Y	—
RA3	5	20	22	22	ANA3	VREF+	C1IN1+	—	DAC1REF+	—	—	—	—	—	—	—	—	SEG3	IOCA3	—	Y	—
RA4	6	21	23	23	ANA4	—	—	—	—	T0CKI(1)	—	—	—	—	—	—	—	SEG4 COM3	IOCA4	—	Y	—
RA5	7	22	24	24	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	—	IOCA5	—	—	VBAT
RA6	14	29	31	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	SEG6	IOCA6	—	Y	CLKOUT OSC2
RA7	13	28	30	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	SEG7	IOCA7	—	Y	OSC1 CLKIN
RB0	33	8	8	9	ANB0	—	C2IN1+	ZCD	—	—	—	—	CWG1IN(1)	—	—	—	—	SEG8	IOCB0	—	Y	INTPPS
RB1	34	9	9	10	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG9	IOCB1	HIB1	Y	—
RB2	35	10	10	11	ANB2	—	—	—	—	—	—	—	—	SCL, SDA(1, 3, 4, 5, 6)	—	—	—	SEG10 CFLY1	IOCB2	—	Y	—
RB3	36	11	11	12	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	SEG11 CFLY2	IOCB3	—	Y	—
RB4	37	12	14	14	ANB4 ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	COM0	IOCB4	—	Y	—
RB5	38	13	15	15	ANB5	—	—	—	—	T1G(1)	—	—	—	—	—	—	—	SEG13 COM1	IOCB5	—	Y	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	TX2(1) CK2(1)	CLCIN2(1)	—	SEG14	IOCB6	—	Y	ICDCLK/ ICSPCLK
RB7	40	15	17	17	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	RX2(1) DT2(1)	CLCIN3(1)	—	SEG15	IOCB7	—	Y	ICDDAT/ ICSPDAT

Note
1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.
5: These are alternative I^2C logic levels pins.
6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O[2]	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
RC0	15	30	32	34	—	—	—	—	—	T1CKI[1] SMTWIN1[1]	—	—	—	—	—	—	—	—	IOCC0	—	Y	SOSCO
RC1	16	31	35	35	—	—	—	—	—	SMTSIG1[1] T4IN[1]	CCP2[1]	—	—	—	—	—	—	—	IOCC1	—	Y	SOSCI
RC2	17	32	36	36	ANC2	—	—	—	—	—	CCP1[1]	—	—	—	—	—	—	COM2 SEG18	IOCC2	—	Y	—
RC3	18	33	37	37	ANC3	—	—	—	—	T2IN[1]	—	—	—	SCK[1] SCL[1,3,4]	—	—	—	SEG19	IOCC3	—	Y	—
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	—	—	SDI[1] SDA[1,3,4]	—	—	—	SEG20	IOCC4	—	Y	—
RC6	25	40	44	44	ANC6	—	—	—	—	—	—	—	—	—	TX1[1] CK1[1]	—	—	SEG22 VLCD2	IOCC6	—	Y	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	—	—	—	RX1[1] DT1[1]	—	—	SEG23 VLCD1	IOCC7	—	Y	—
RD0	19	34	38	38	AND0	—	—	—	—	—	—	—	—	—	—	—	—	SEG24	—	—	Y	—
RD1	20	35	39	39	AND1	—	—	—	—	—	—	—	—	—	—	—	—	SEG25	—	—	Y	—
RD2	21	36	40	40	AND2	—	—	—	—	—	—	—	—	—	TX2	—	—	COM5 SEG26	—	—	Y	—
RD3	22	37	41	41	AND3	—	—	—	—	—	—	—	—	—	RX2	—	—	COM4 SEG27	—	—	Y	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	SEG28	—	—	Y	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	SEG29	—	—	Y	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	SEG30	—	—	Y	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	SEG31	—	—	Y	—
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	SEG32	—	—	Y	—
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	COM6 SEG33	—	—	Y	—
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	COM7 SEG34	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	—	Y	MCLR

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F19175/76) (CONTINUED)

I/O[2]	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	44-Pin QFN	ADC	Reference	Comparator	Zero-Cross Detect	DAC	Timers/SMT	CCP	PWM	CWG	MSSP	EUSART	CLC	RTCC	LCD	Interrupt-on-Change	High Current	Pull-up	Basic
VLCD3	24	39	43	43	—	—	—	—	—	—	—	—	—	—	—	—	—	VLCD3	—	—	—	—
VDD	11 32	7 26	7 28	7 28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	12 31	6 27	6 29	6 30	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT[2]	—	—	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	—	TMR0	CCP1 CCP2	PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	SDO SCK SCL SDA	TX1 DT1 CK1 TX2 DT2 CK2	CLC1OUT	RTCC	—	—	—	—	—

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one or more PORTx pin options.

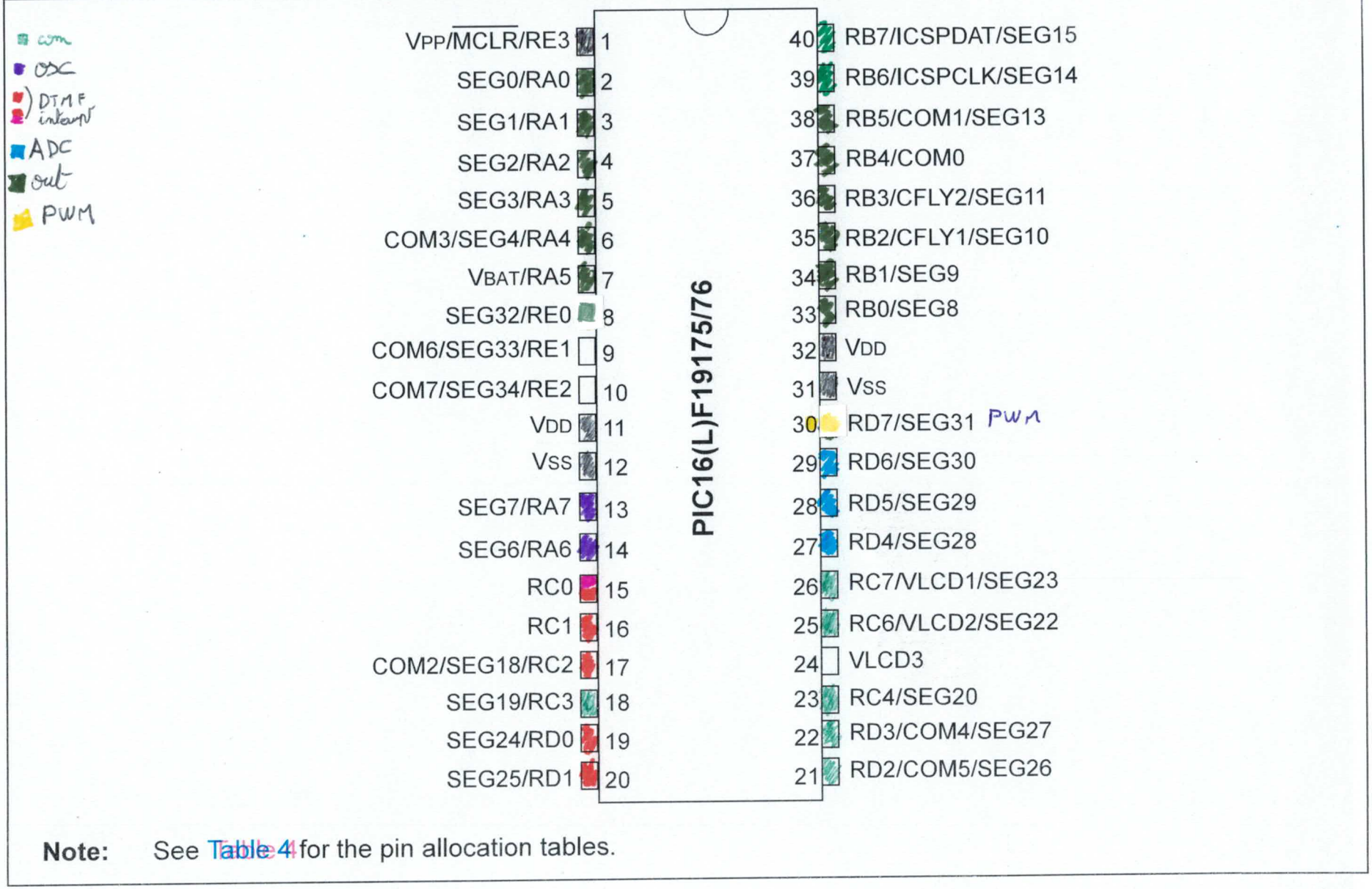
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by INLCVL register, instead of the I^2C specific or SMBUS input buffer thresholds.

5: These are alternative I^2C logic levels pins.

6: In I^2C logic levels configuration, these pins can operate as either SCL and SDA pins.

FIGURE 3: 40-PIN PDIP PIN DIAGRAM FOR PIC16(L)F19175/76



Note: See Table 4 for the pin allocation tables.

I/O In	I/O Interrupt	I/O Out	PWM Out	UART	I2c	SPI	Timer 8	Timer 16
DTMF1	DTMF Enable	PTT VHF	BIP	COM Matrice HDMI	Matrice video 2			1
DTMF2		PTT UHF		COM Accessoire	Ecran LCD Facade			
DTMF3		Watchdog						
DTMF4		FAN						
Capteur °C (ADC)		TX 1G2						
Capteur U (ADC)		TX 2G4						
Capteur I (ADC)		TX 10G - 1						
		TX 10G - 2						
		TX DATV						
		SD						
		AUX						
		AUX - 2						
		AUX -3						
Total 4	Total 1	Total 13	Total 1					
		Total IO : 19						

BIP : generation BIP 1Khz ou autre tone
I/O Out : Sortie pour commande ULN 2003
Watchdog : Compteur externe RAZ (voir si interne OK)
COM Acc : Bootloader ou IHM lors du boot sinon communication vers PC ou interface Moxa