Synopsys Design Flow Tutorial

Professor: Sci.D., Professor
Vazgen Melikyan

Synopsys Design Flow Tutorial
Lecture - 4
Developed By: Vazgen Melikyan

Course Overview

- Synopsys Design Flow
  - 2 lectures
- Logic Simulation (VCS)
  - 2 lectures
- Logic Synthesis (Design Compiler)
  - 2 lectures
- Physical Synthesis (IC Compiler II)
  - 2 lectures
- Static Timing Analysis (PrimeTime)
  - 2 lectures
- Formal Verification (Formality)
  - 2 lectures
- Automatic Test Pattern Generation (TetraMAX)
  - 2 lectures
- Physical Verification (IC Validator)
  - 2 lectures
- Layout Parasitics Extraction (StarRC)
  - 2 lectures
- SPICE-Level Simulation of Completed Design (HSpice)
  - 2 lectures

Physical Synthesis (IC Compiler II)

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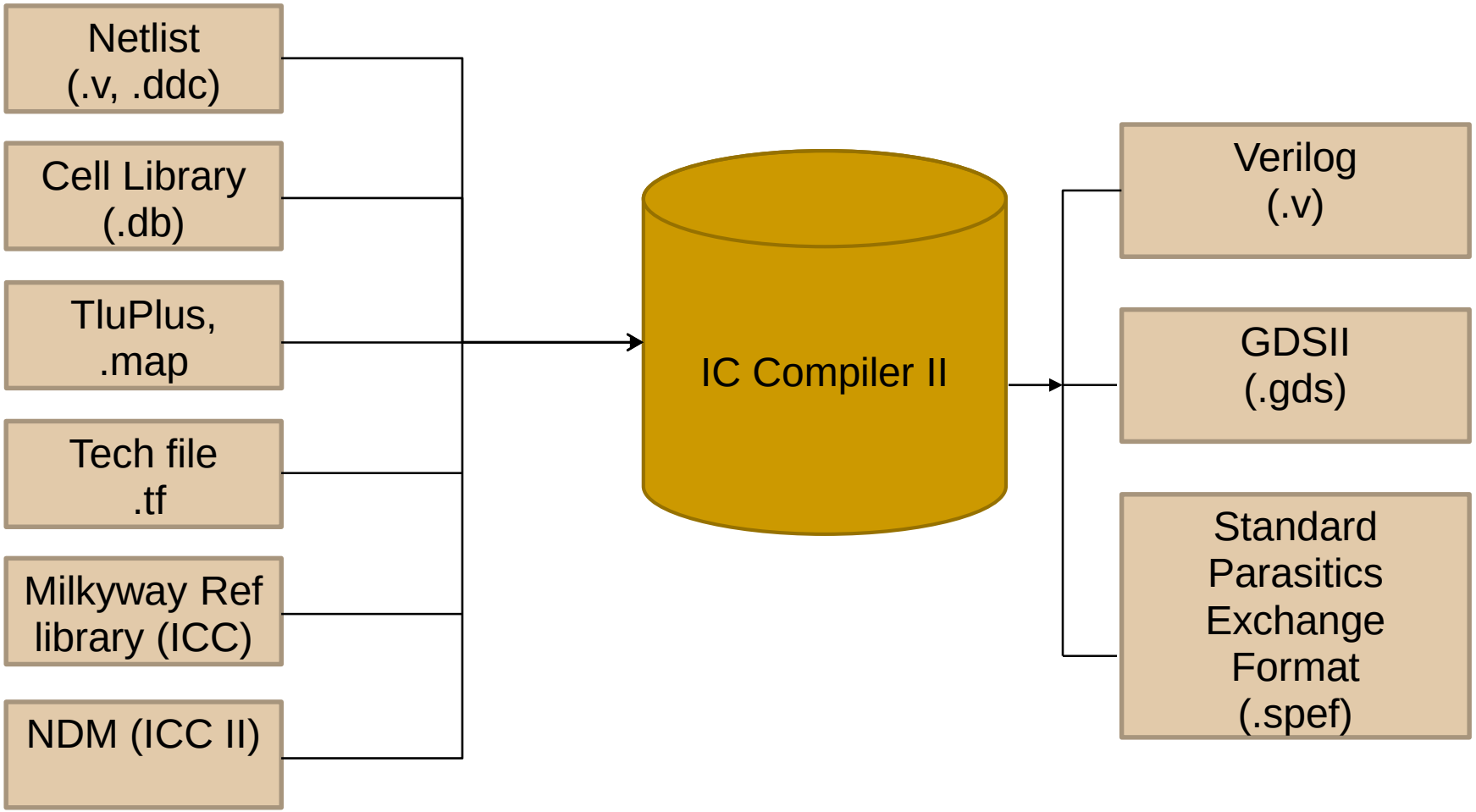
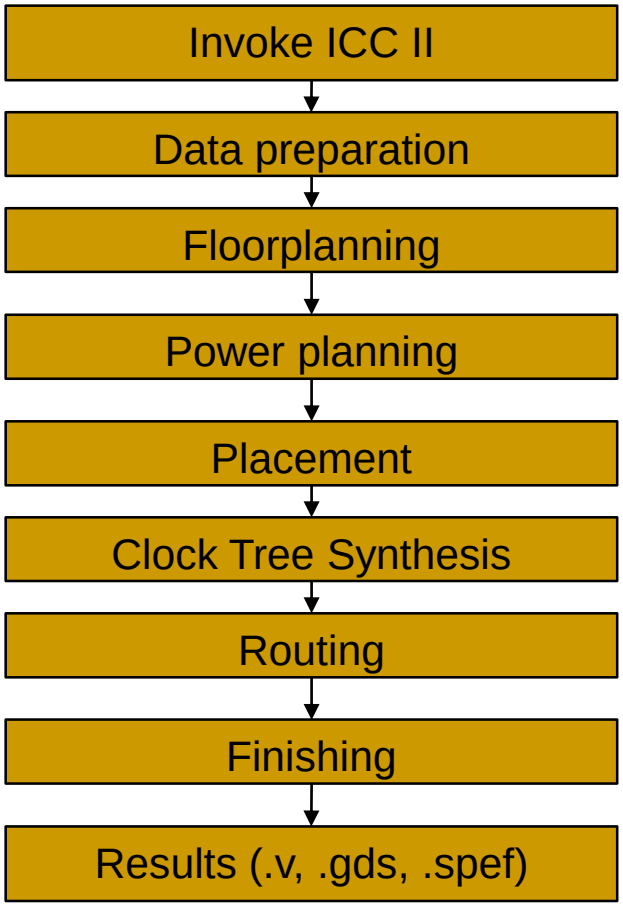
Input and Output Files of IC Compiler II



IC Compiler II Design Flow



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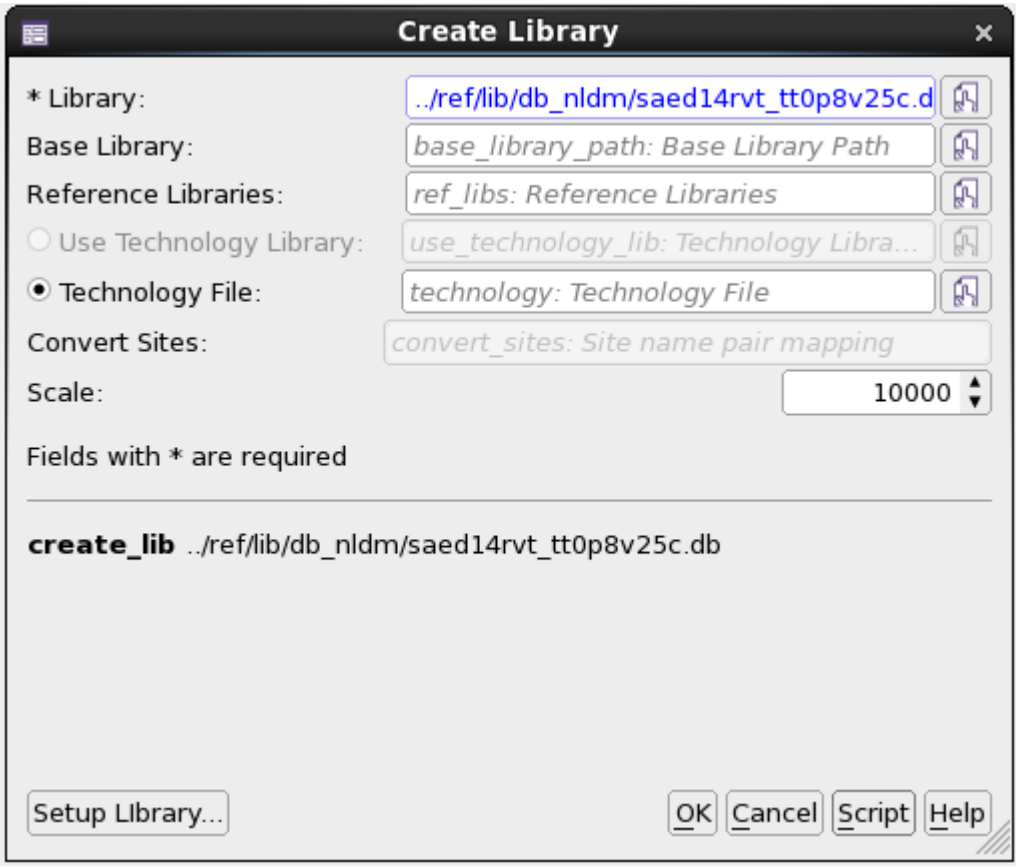
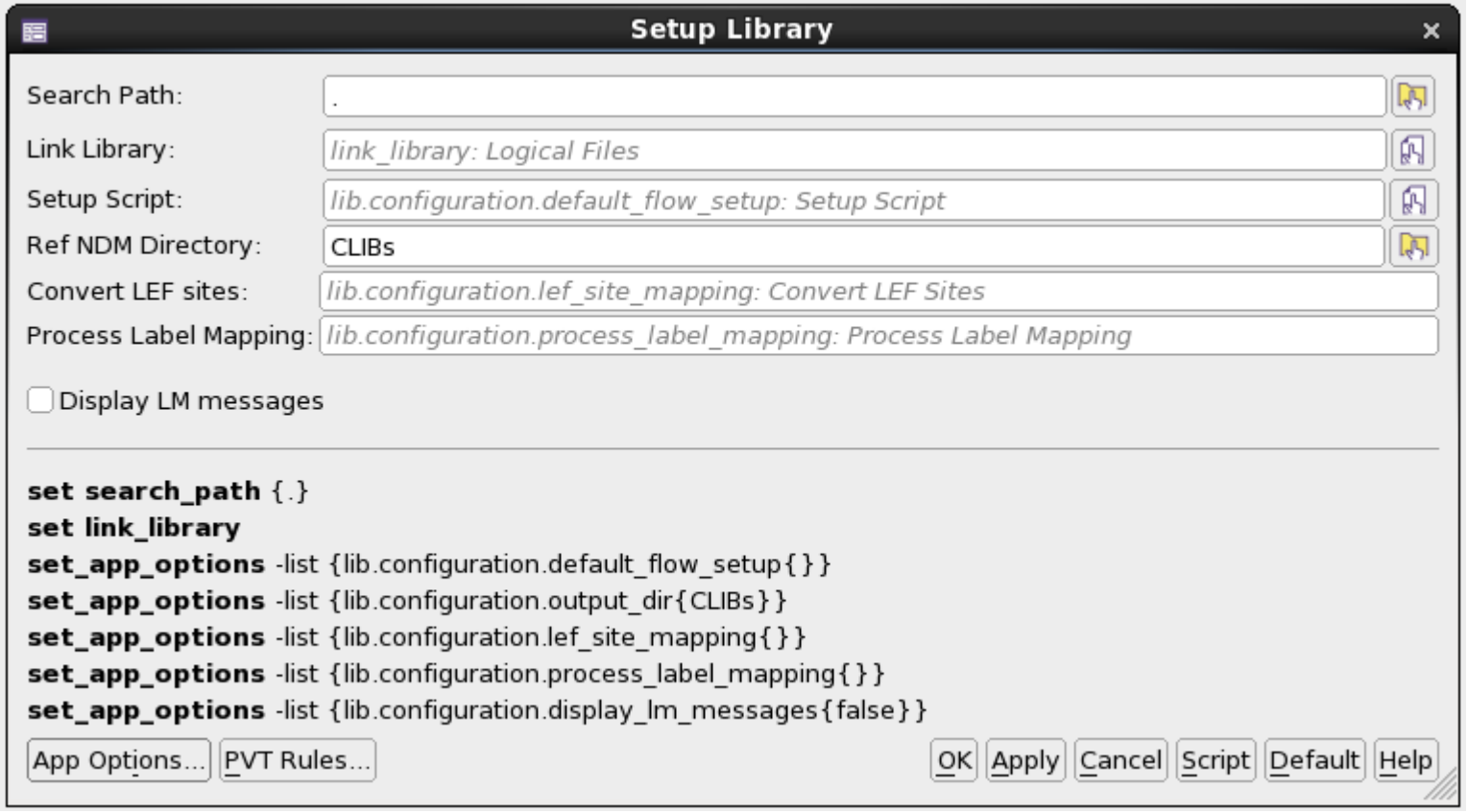
NDM Library Creation

- To create the NDM design library, Choose File > Create Library



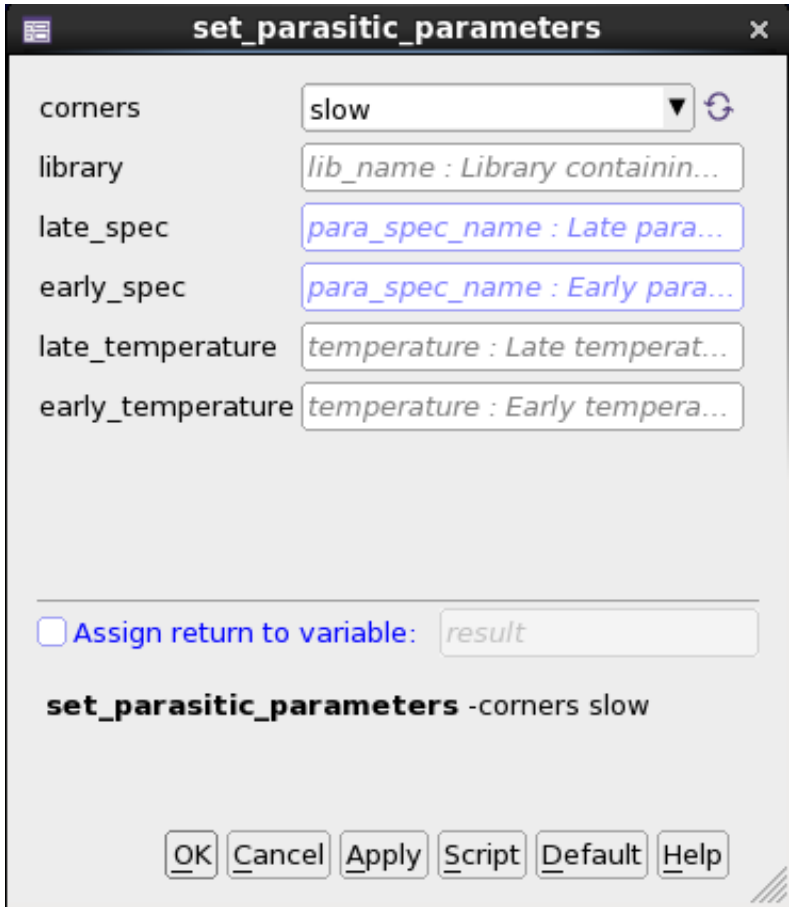
Setup Logic Libraries

- Choose File > Setup Library



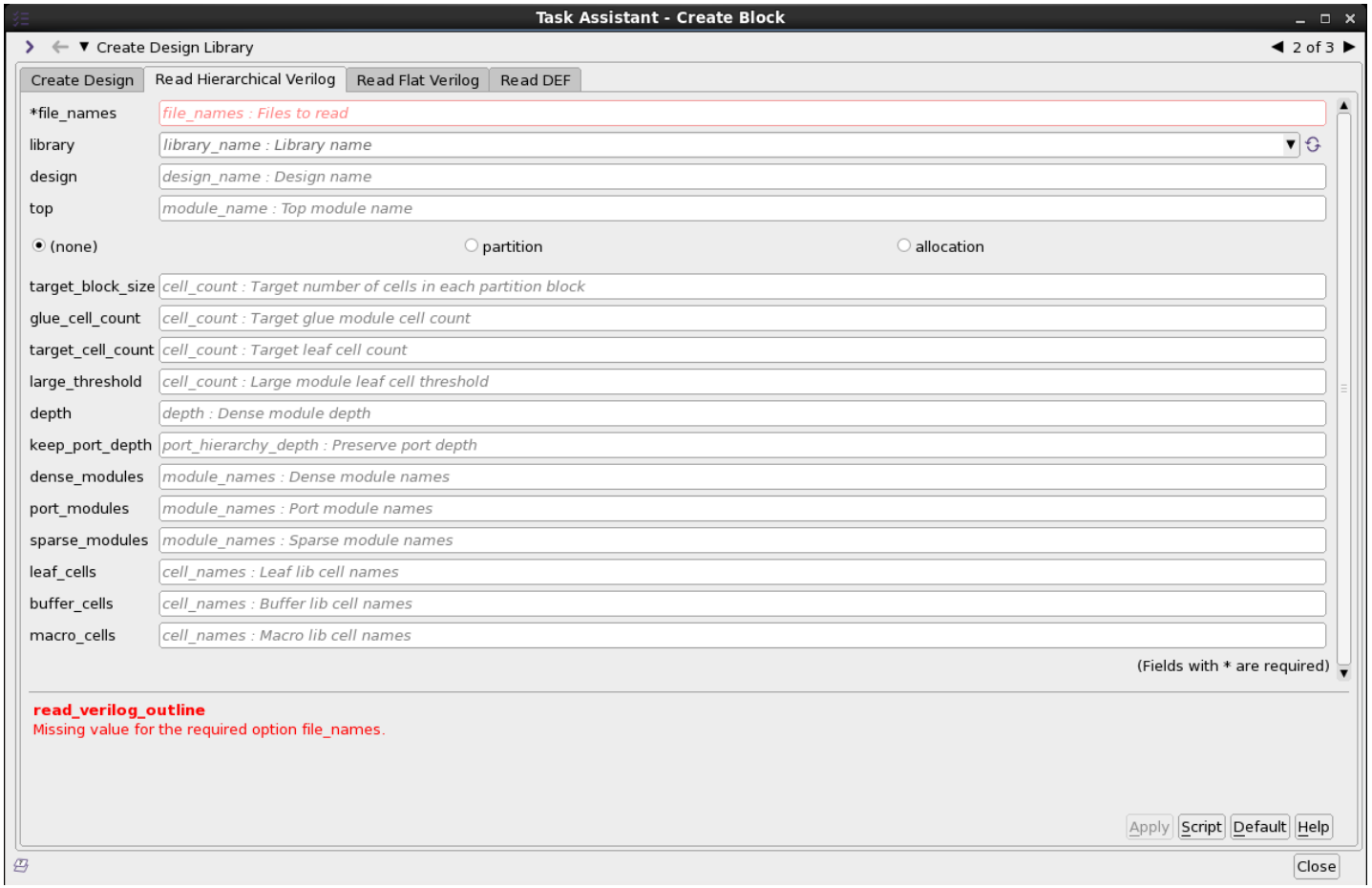
TluPlus Setup

- Choose View > Map > Rail Parasitics

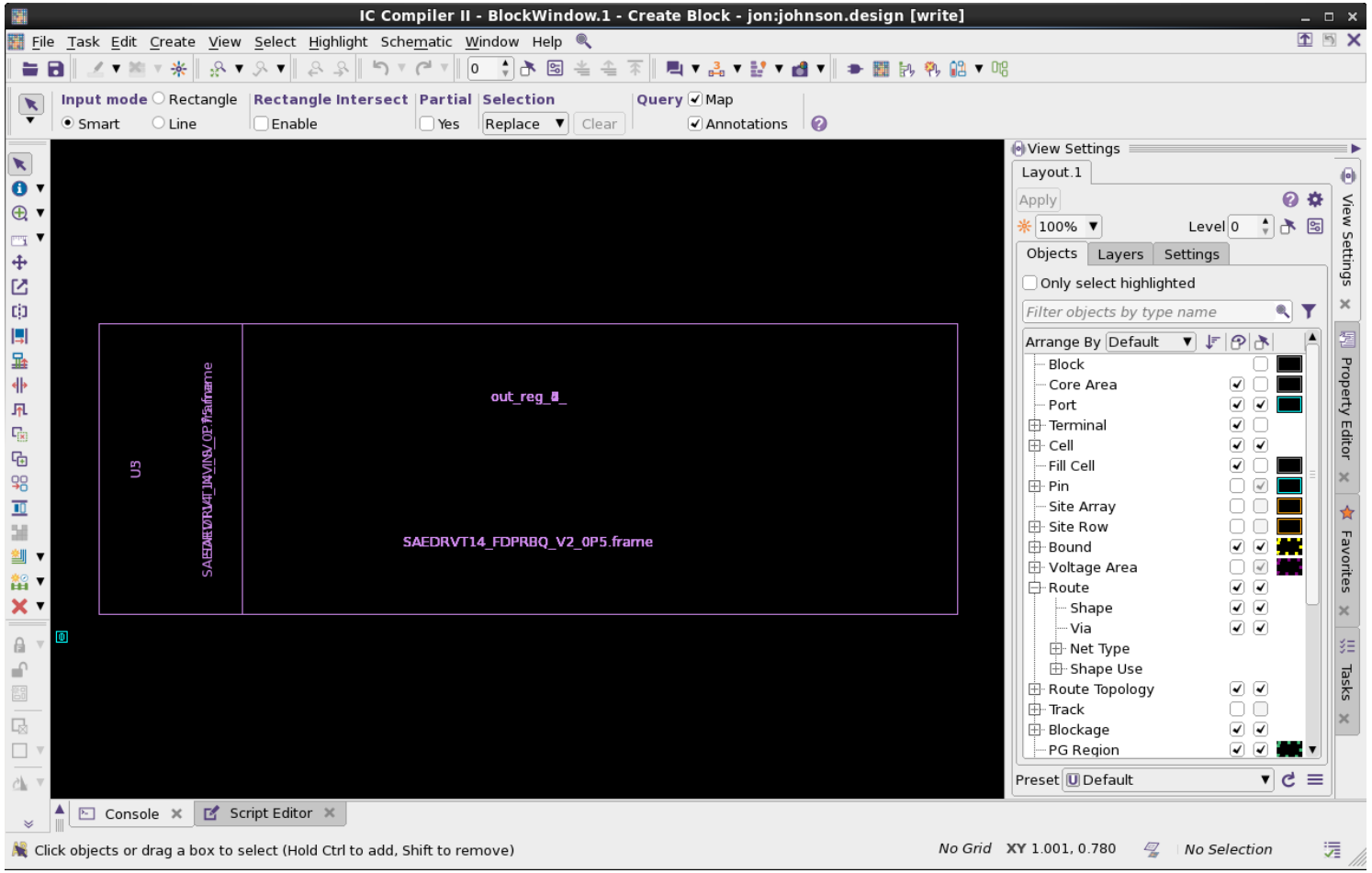


Design Importing

- Choose Task > Create Design > Create Design Library



Design Importing (2)



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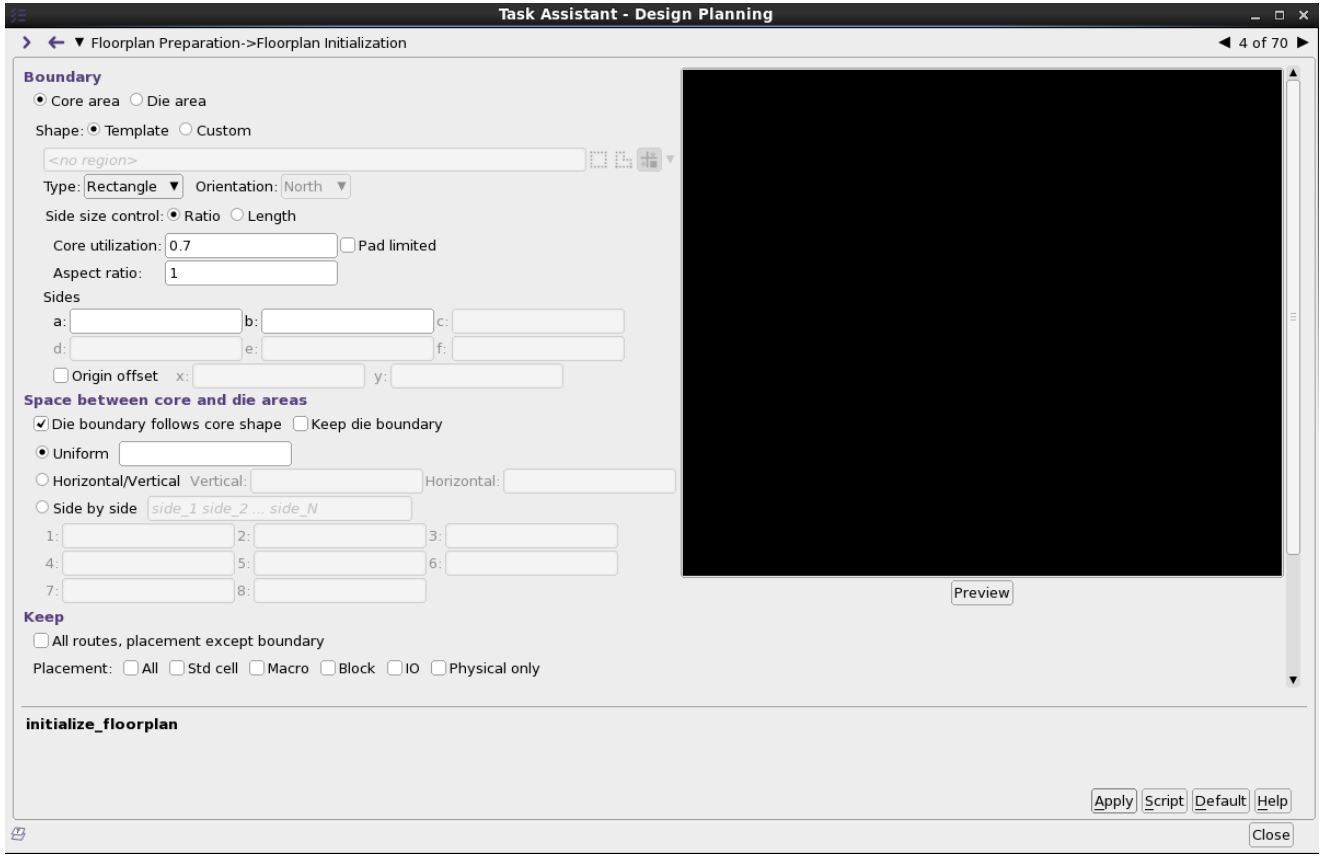
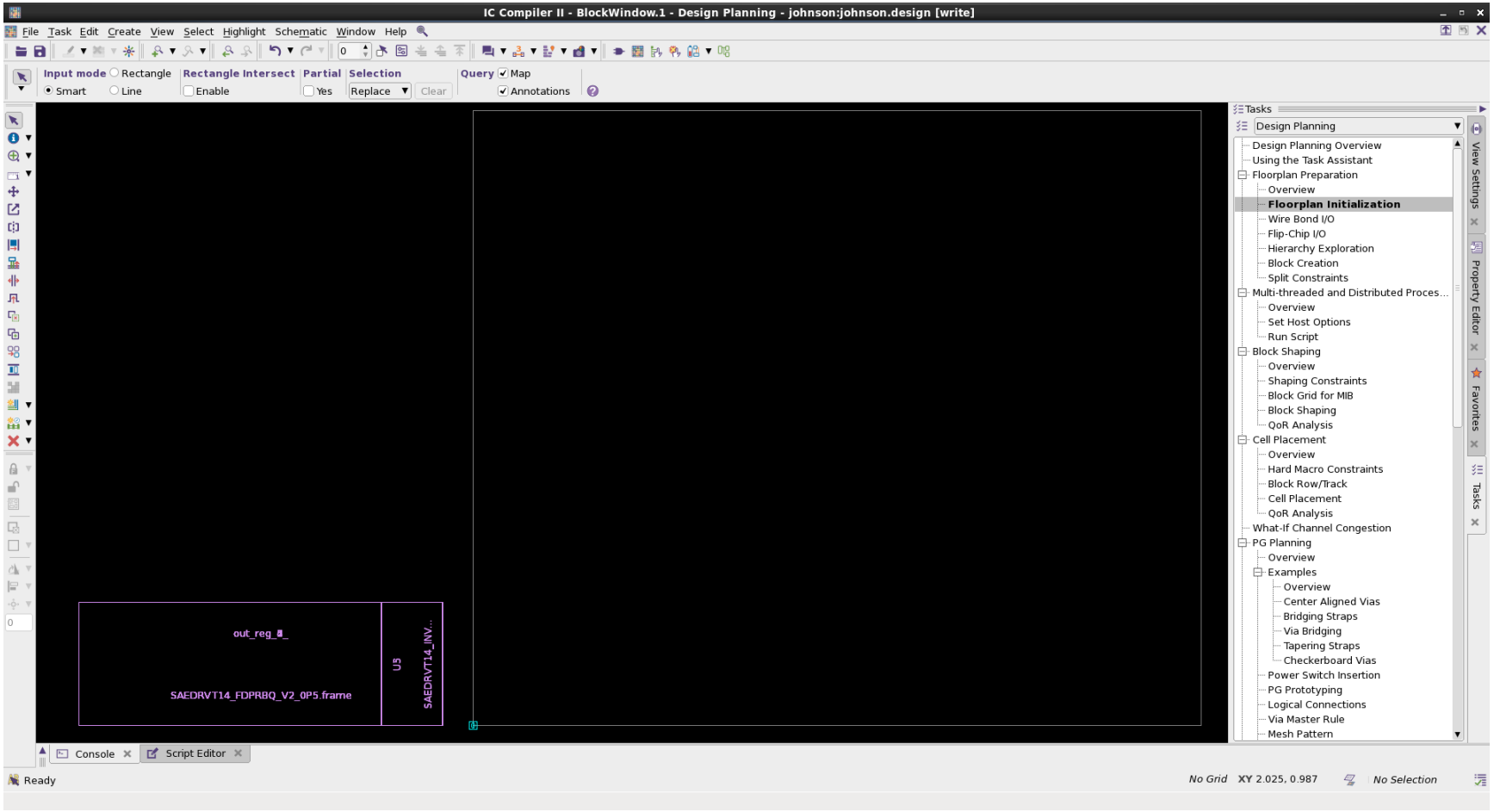
Floorplanning

- For floorplanning the design choose Task > Design Planning > Floorplan Initilization

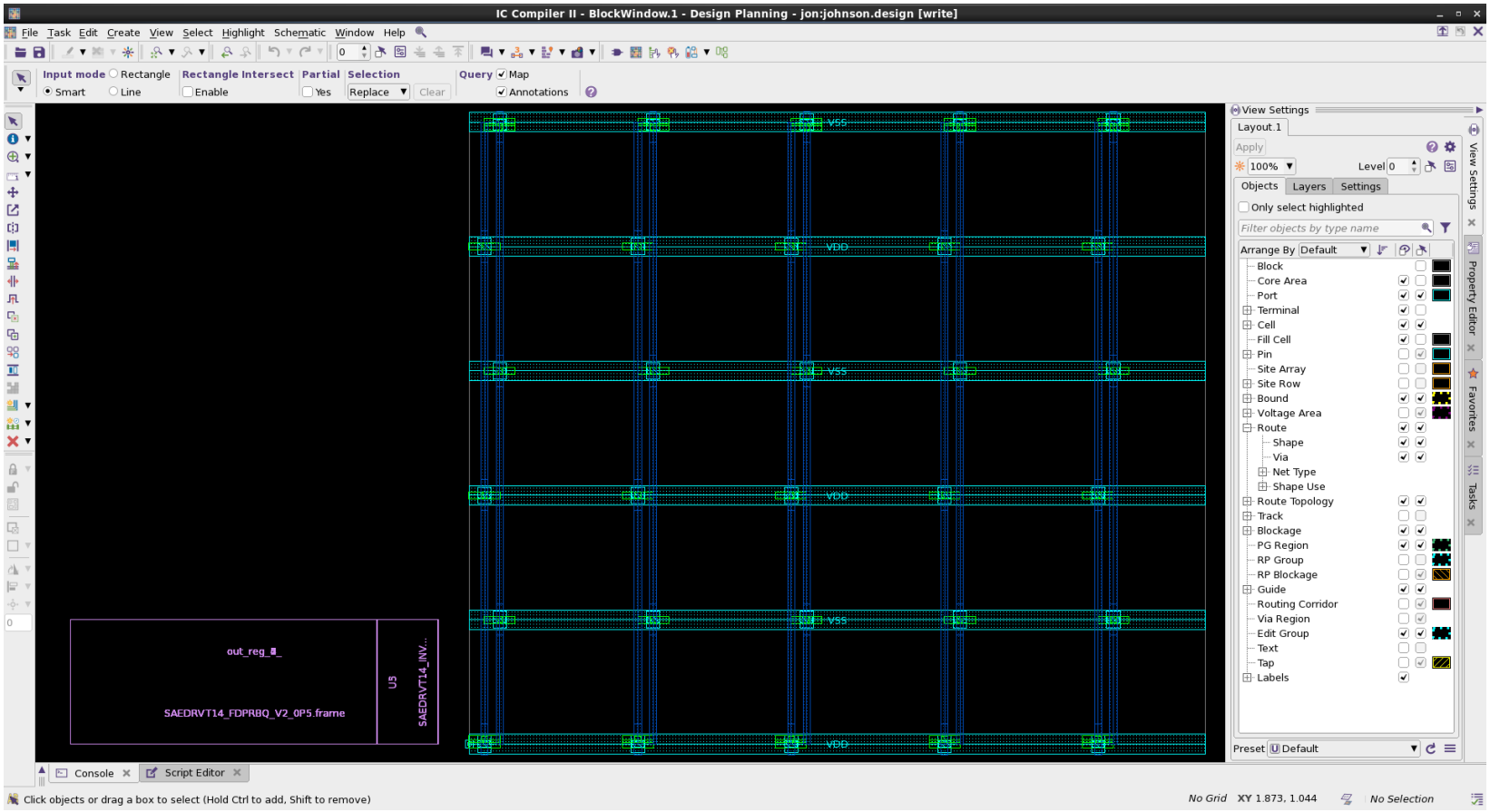


Floorplanning (2)



Power Straps

- Choose Task > Design Planning > Create PG



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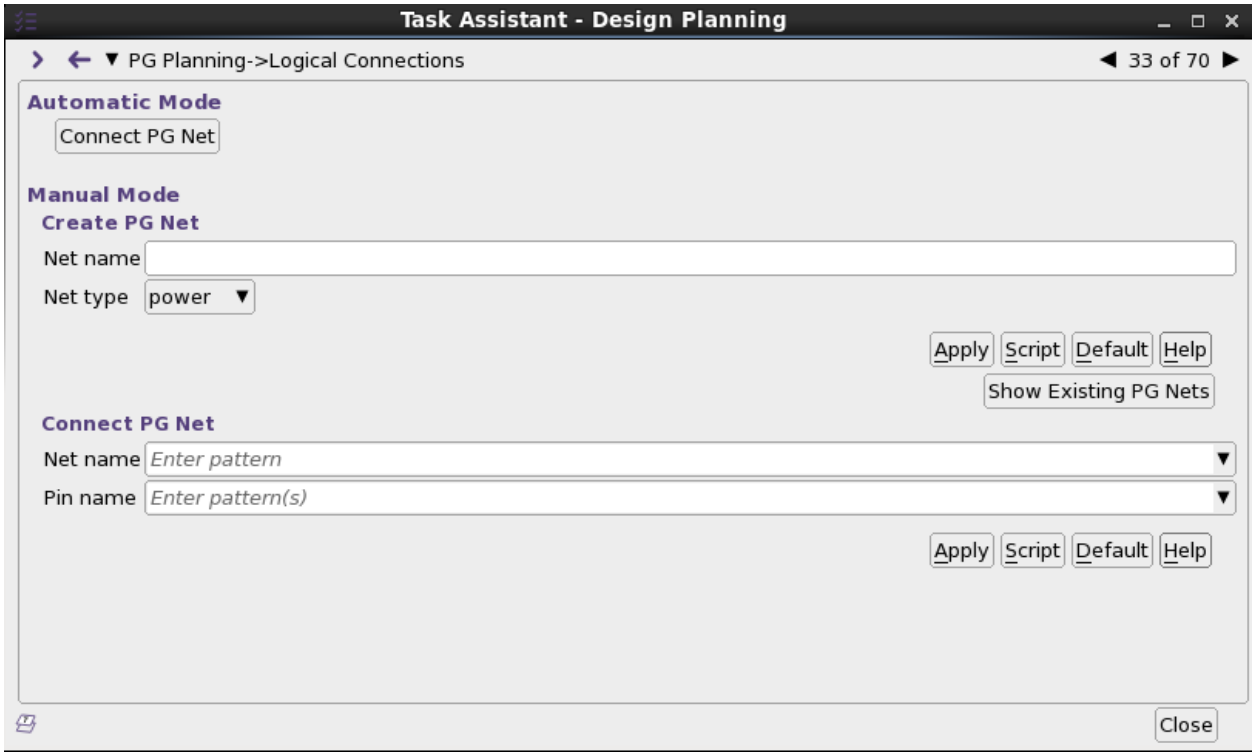
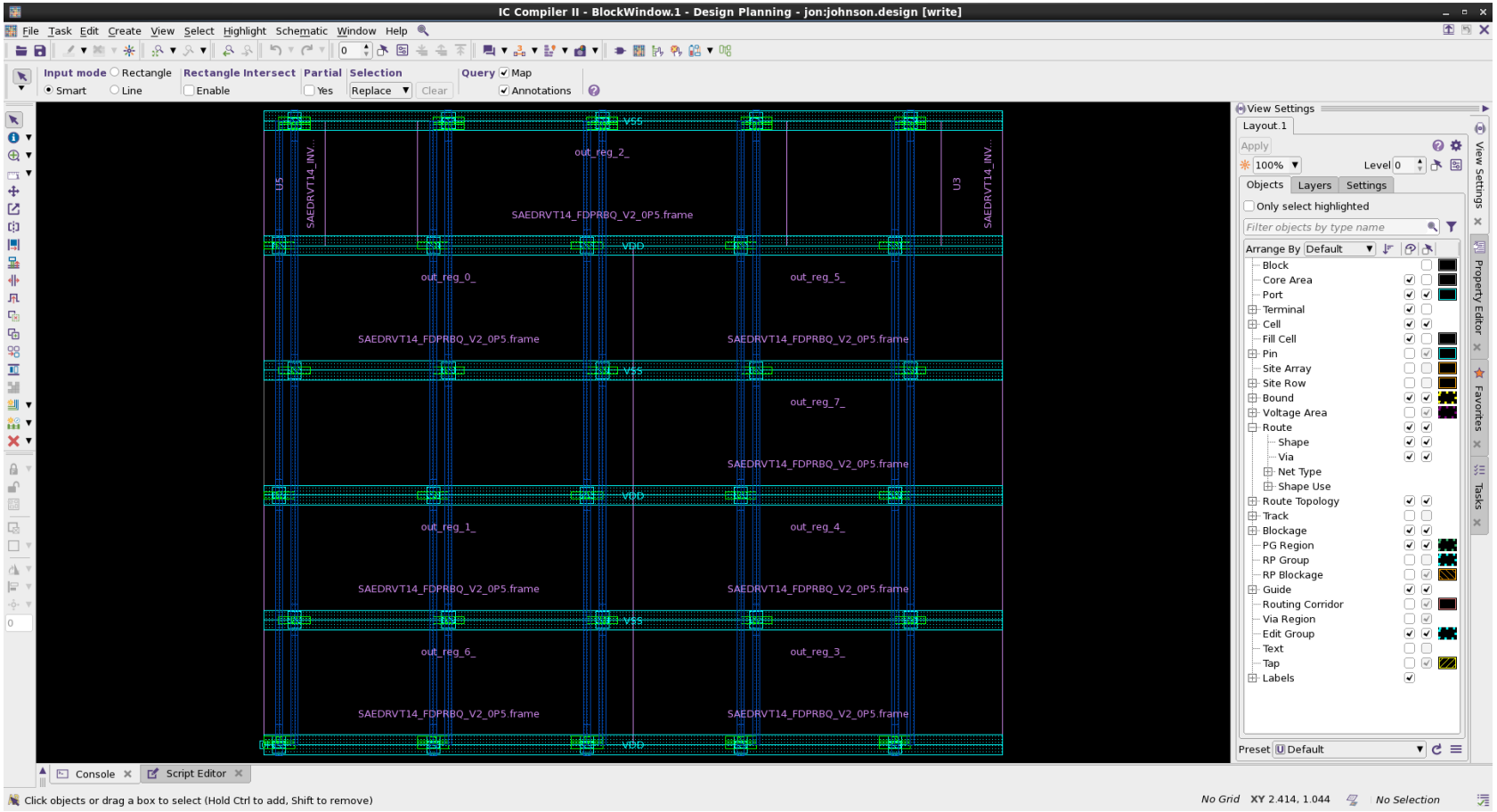
Core Placement and Optimization Dialog Box

- To run placement, choose Placement > Core Placement and Optimization Task > Placement > Placement > Create Placement



FP Placement

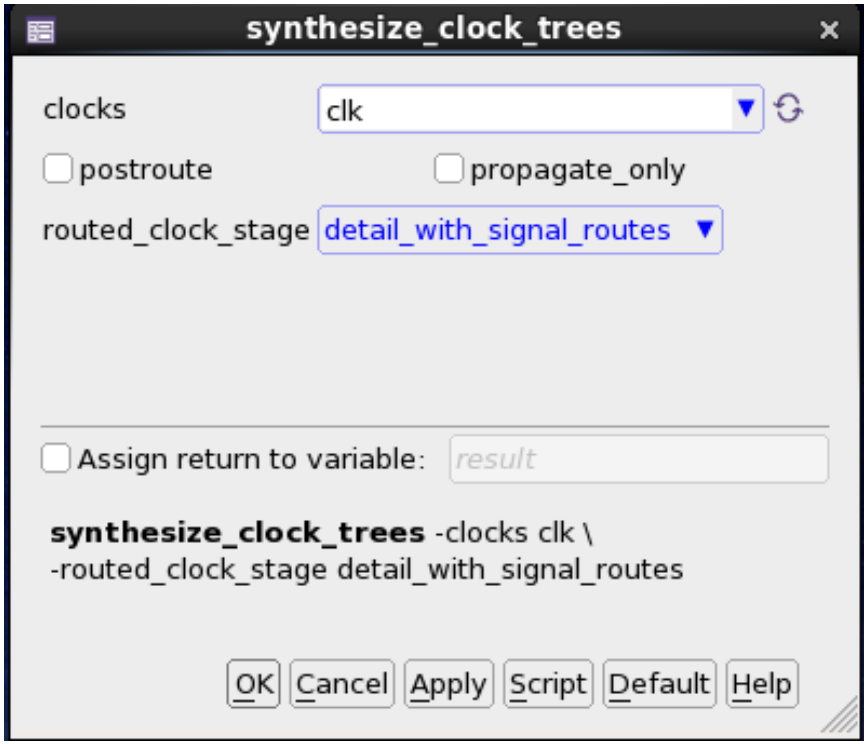


Script FRAGMENT for Placement

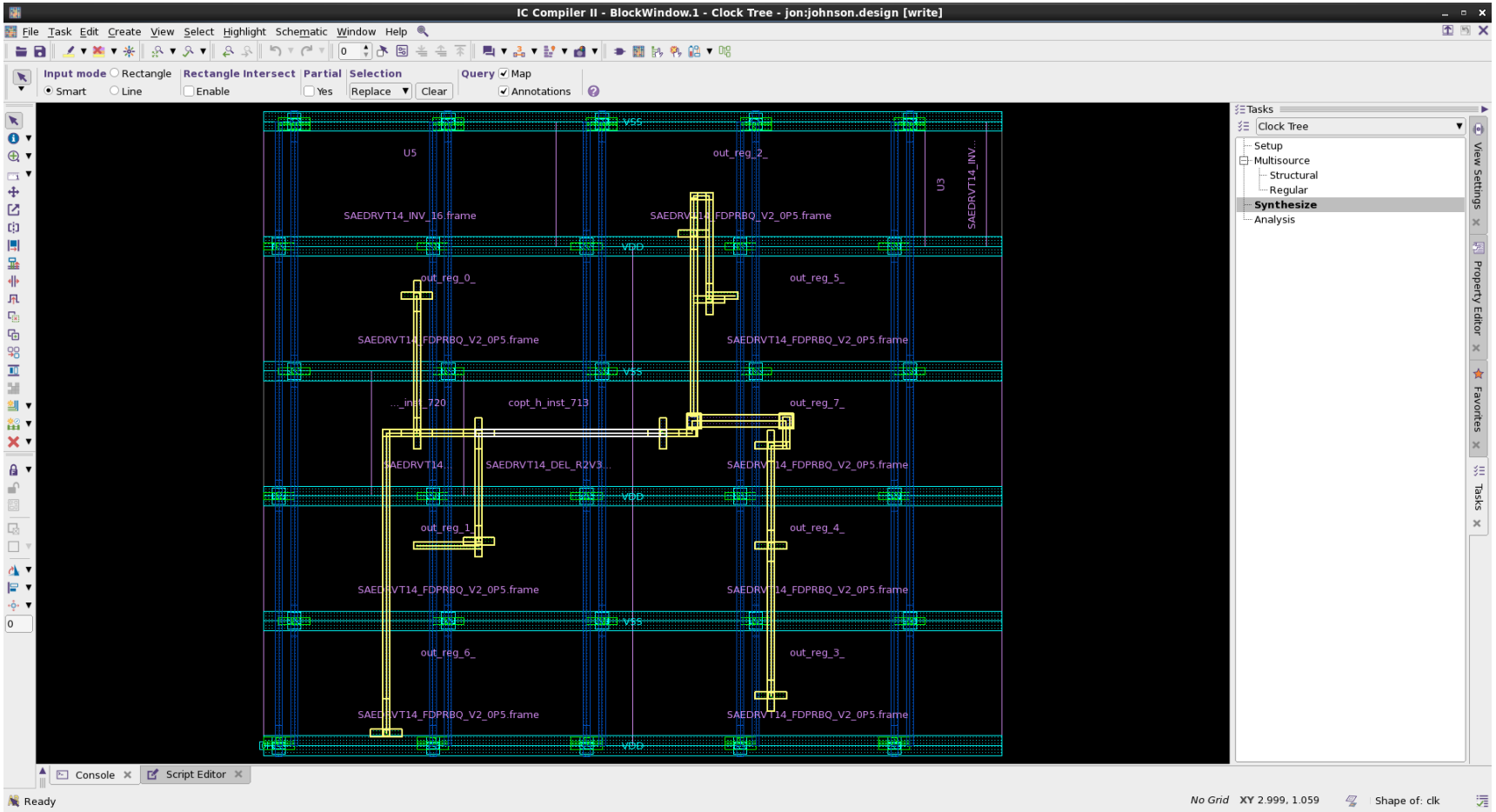
- Place_opt
  - -list_only
  - -from startStage
  - -to endStage

Clock Tree Synthesize

- To perform clock tree synthesis choose Task > Clock tree > Chack Clock Trees



Clock Tree Synthesis

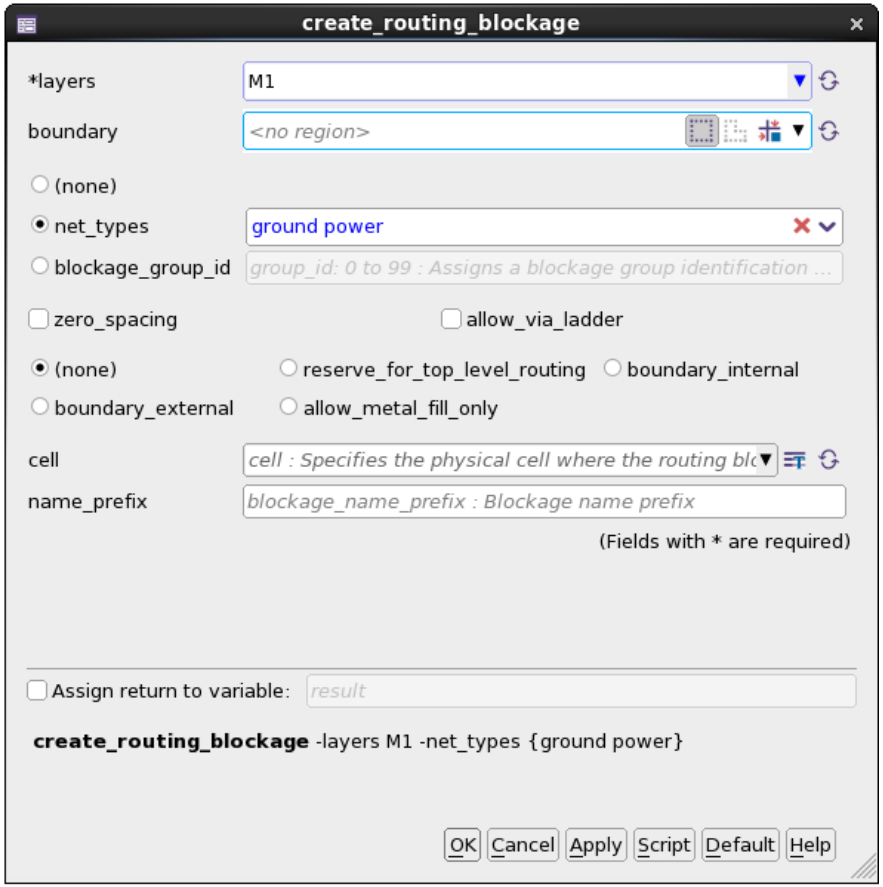


Command of CTS

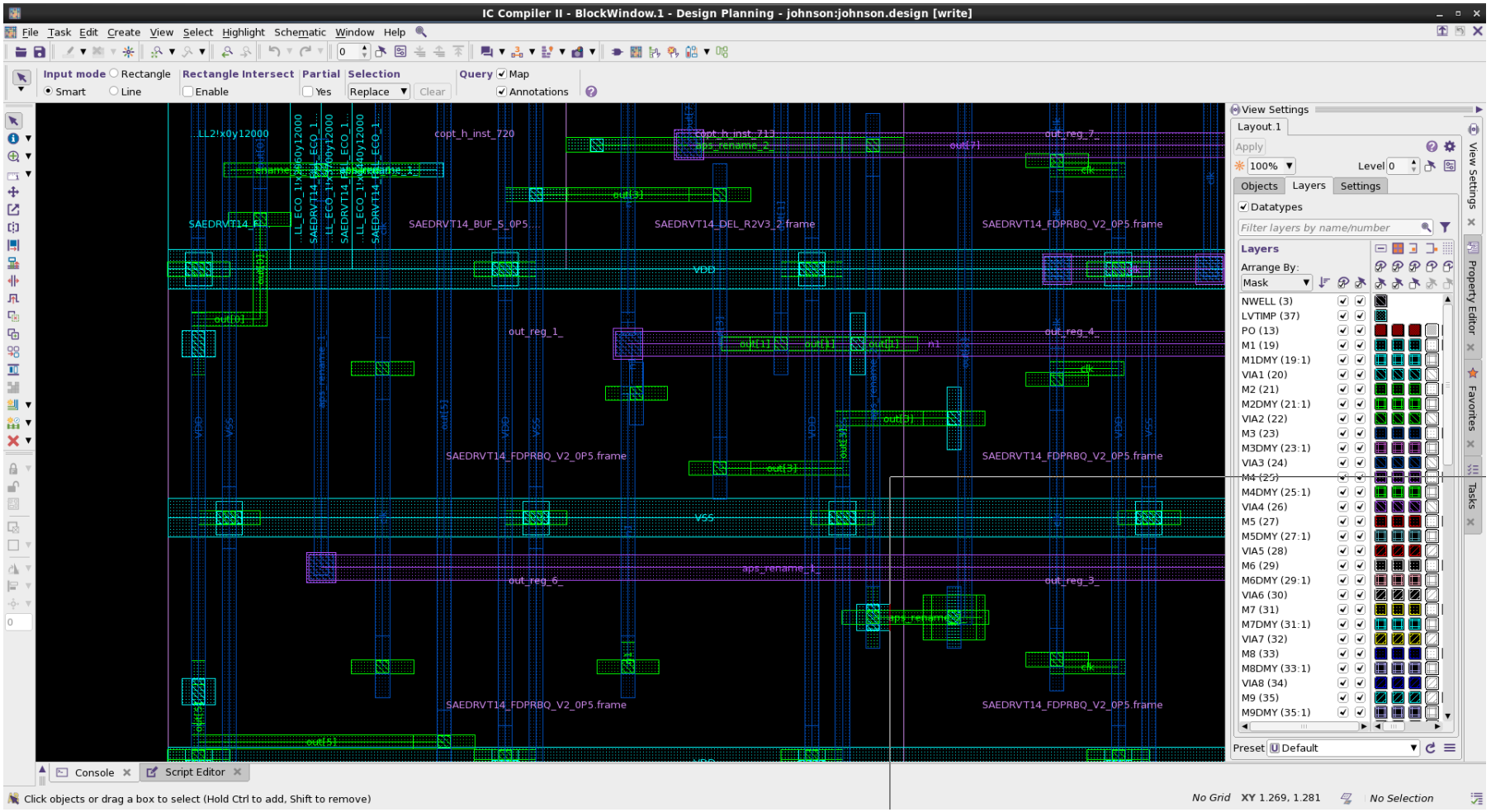
- clock_opt
  - -only_psyn
  - -fix_hold_all_clocks
  - -inter_clock_balance
  - -update_clock_latency
  - -operating_condition
  - -only_cts
  - -optimize_dft
  - -no_clock_route
  - -only_hold_time
  - -area_recovery
  - -size_only
  - -in_place_size_only
  - -power

Preroute Standard Cells

- From Menu bar choose Task > Routing> Create Routing Blockage



After Prerouting



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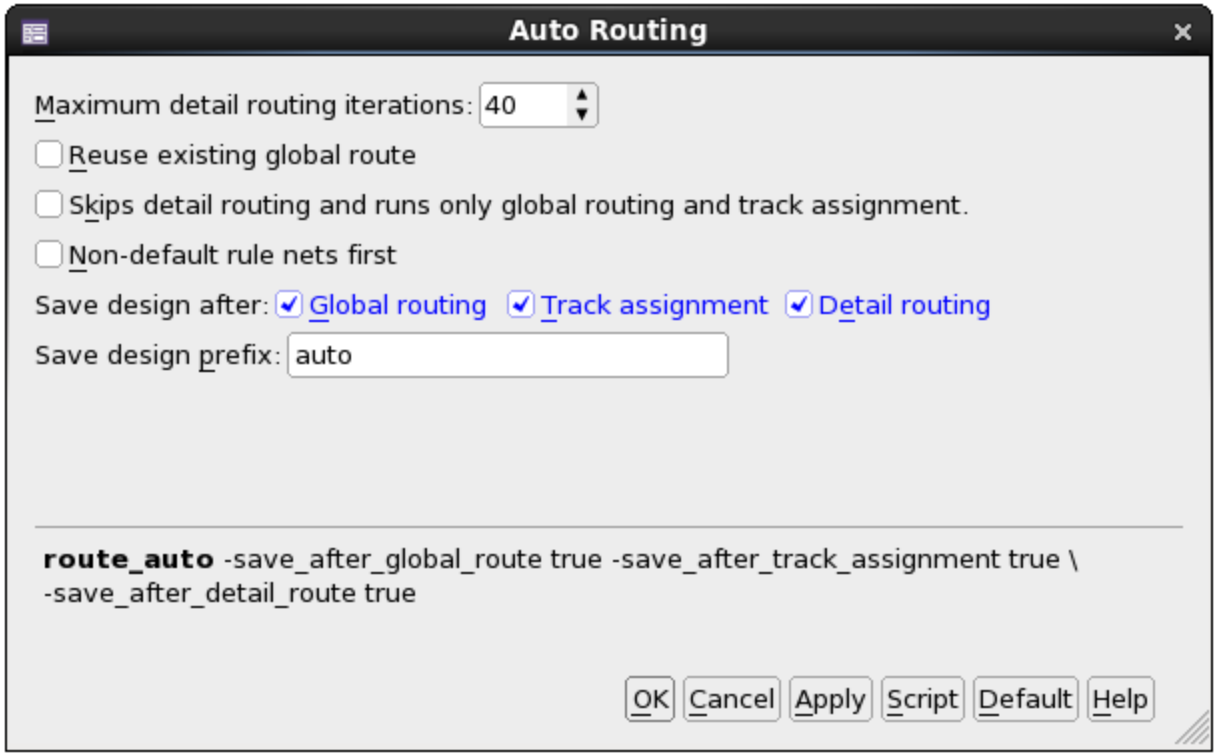
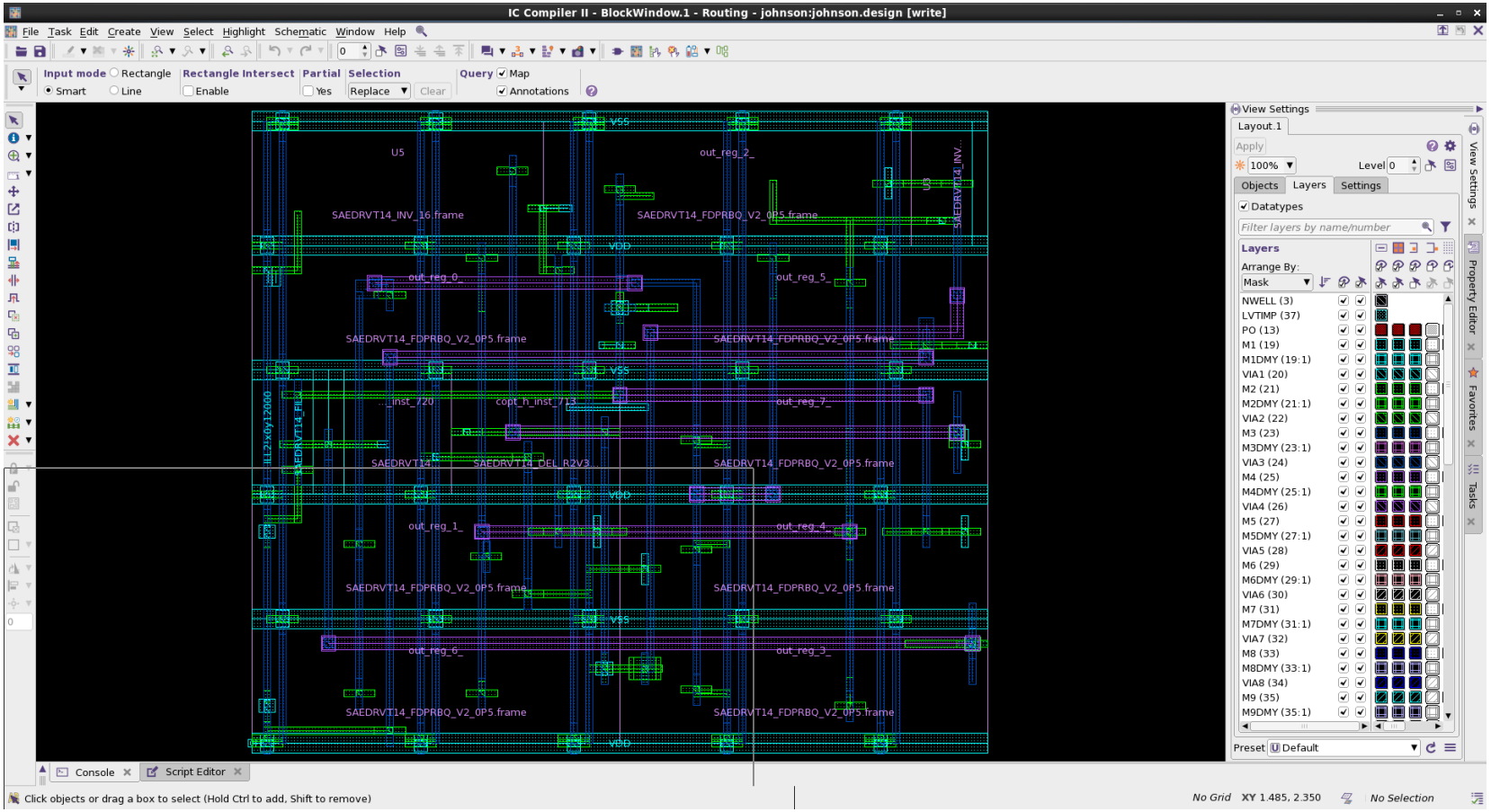
Routing from the GUI

- Choose Route > Core Routing and Optimization



Routing Dialog Box

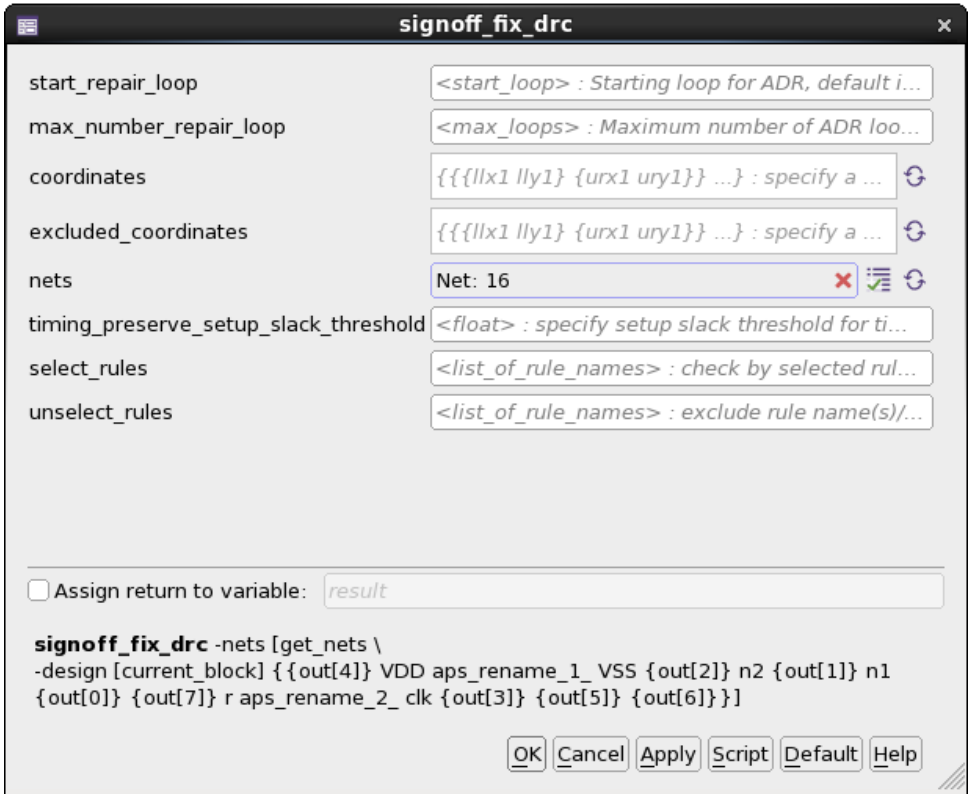


Command for Routing (2)

- route_auto
  - -max_detail_route_iterations num
  - -reuse_existing_global_route true | false
  - -route_nondefault_nets_first true | false
  - -stop_after_track_assignment true | false
  - -save_after_global_route true | false
  - -save_after_track_assignment true | false
  - -save_after_detail_route true | false
  - -save_cell_prefix name

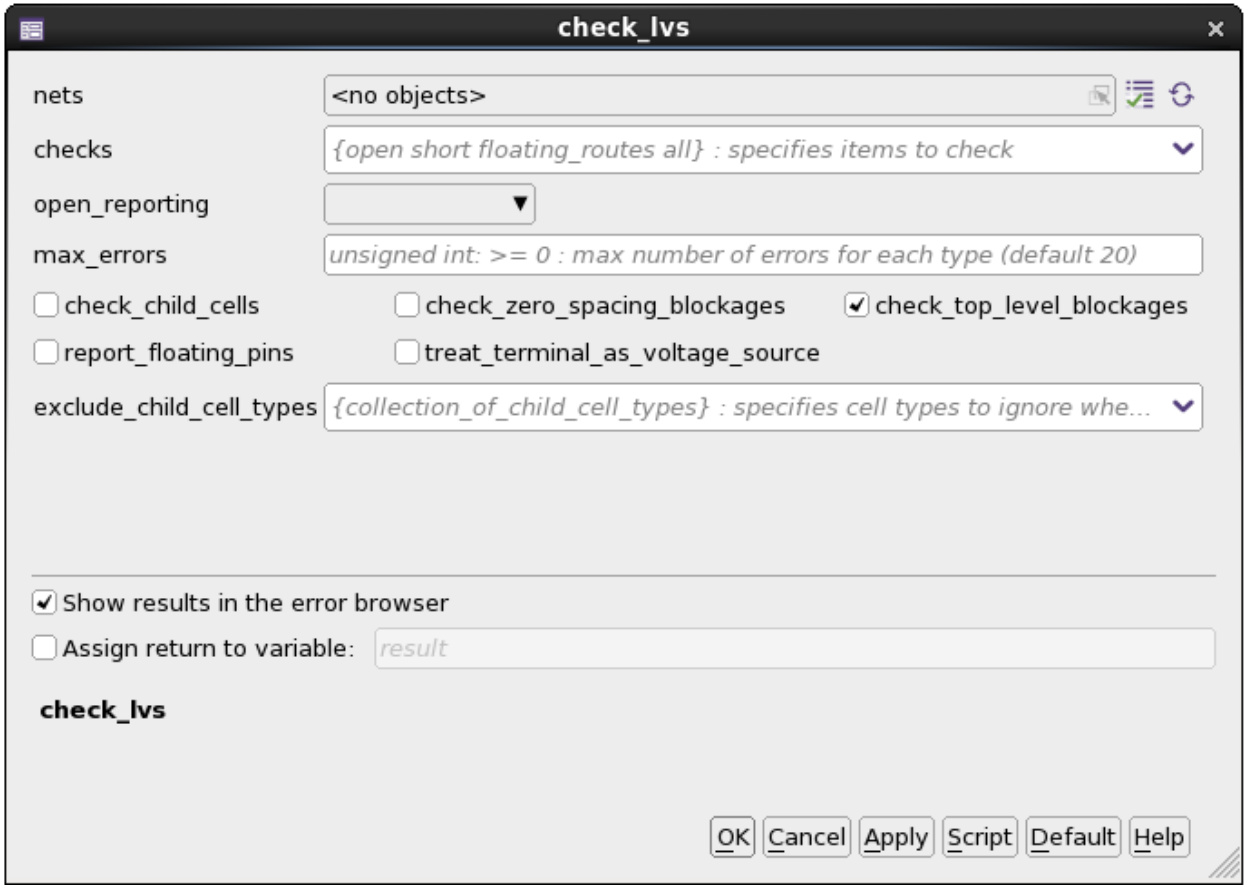
DRC (Design Rule Checking) Box

- To check DRC errors, choose Verification > Signoff DRC



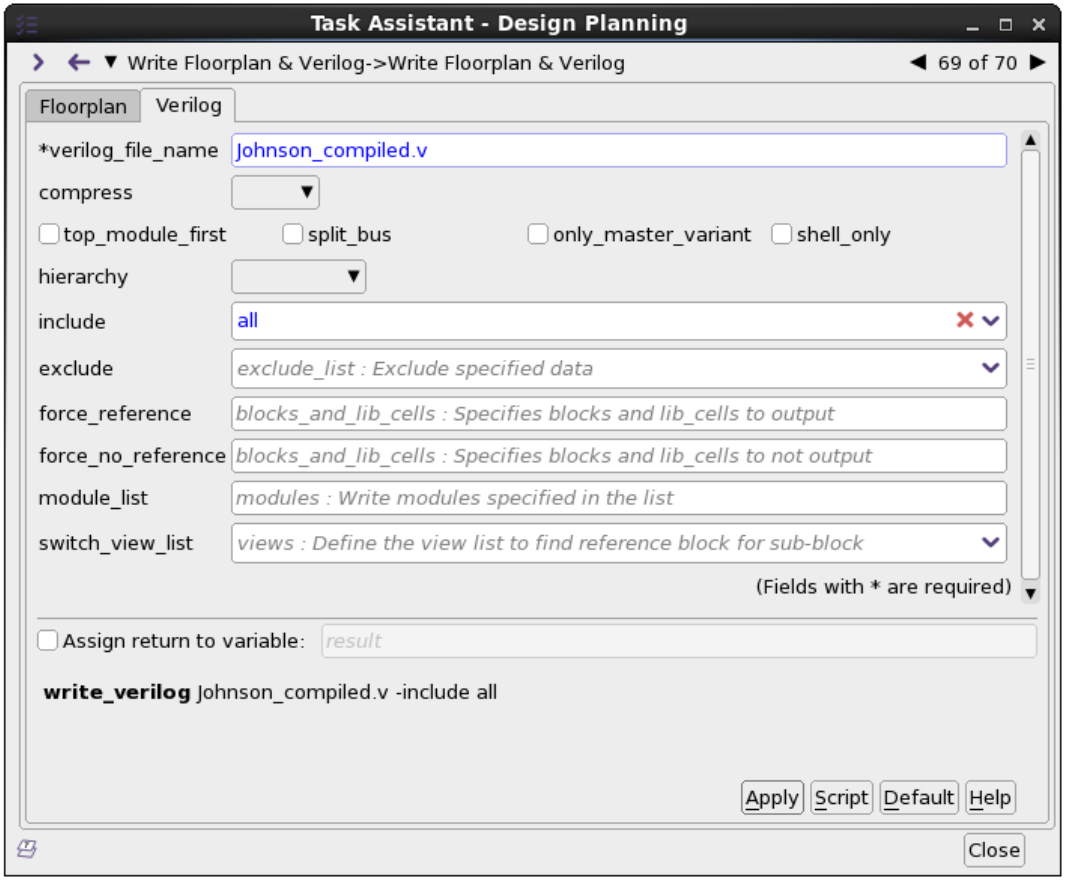
LVS (Layout-Versus-Schematic) Box

- To check LVS errors, choose Verification > LVS



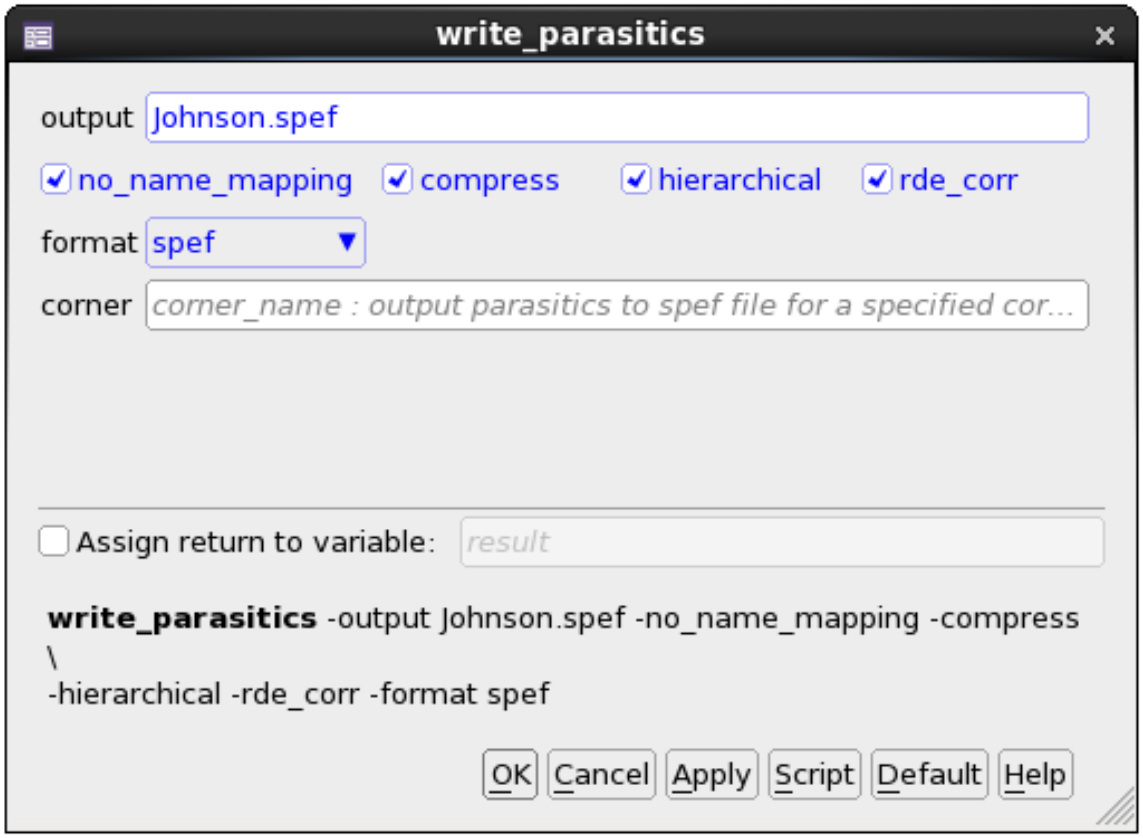
Write Verilog Format Box

- Choose Task > Design Planning > Write Floorplan & Verilog > Verilog

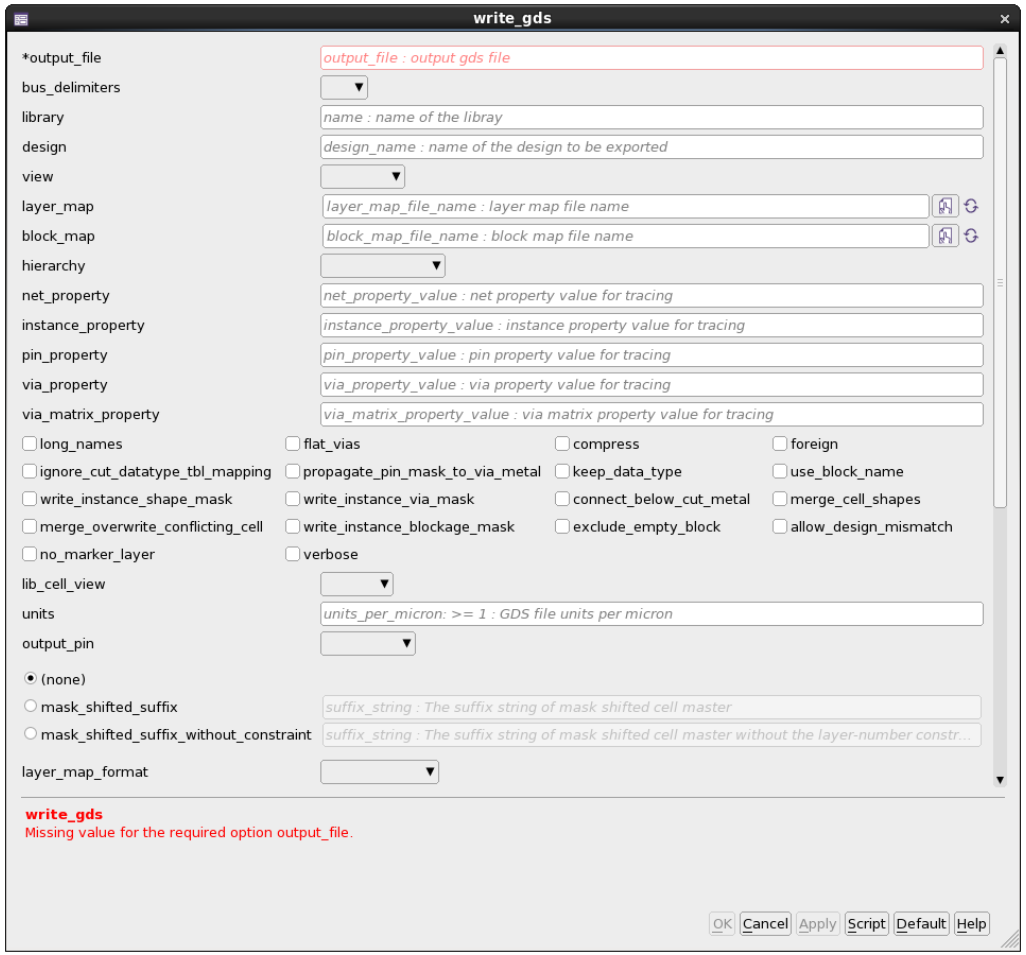


Write .spef Format Box

Choose File > Export > Write Parasitics



Write .gds Format Box

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