PROCESS DESIGN KIT

SAED_PDK90

DATABOOK

Revision : 1
Technology : SAED90nm
Process : SAED90nm 1P9M 1.2v / 2.5v

CONTENTS

LIST OF TABLES

1 Introduction

1.1 Goal of PDK development

This Databook describes possibilities, peculiarities of SAED_PDK90 Process Design Kit and technical parameters of Symbol library and OA Tcl Pcells included in it. SAED_PDK90 is free from intellectual property restrictions and is oriented at Synopsys Custom Designer (CD) tool. SAED_PDK90 is anticipated for the use of educational purposes and is aimed at training highly qualified specialists in microelectronics at:

- Synopsys Customer Education Services
- GTC
- Universities included in Synopsys University Program

SAED_PDK90 is foreseen to support the trainees to better master:

- Advanced Analog Design Methodologies;
- Capabilities of SYNOPSYS CD and other EDA tools.

For the use of PDK it is assumed that European or North American bundle of SYNOPSYS EDA tools, including CD is available to trainees.
SAED_PDK90 Process Design Kit is anticipated for designing different analog integrated circuits (ICs) or IPs by the application of 90nm technology and SYNOPSYS EDA tools.

1.2 Content of PDK

The content of SAED_PDK90 is shown in Table 1.1.

Table 1.1 Content of SAED_PDK90

Name	Directory	Extension	Description
Technology files	./SAED_PDK90/techfiles/	.tcl, .drf, .tf, .map	The technology file and display resource files
Physical verification files	./SAED_PDK90/hercules/	*.ev	The LVS and DRC runset files
Parasitic Extract files	./SAED_PDK90/starrcxt/	.nxtgrd, .itf, .map	Parasitic Extract files for STARRCXT Tool
Symbol library and OA Tcl Pcells	./SAED_PDK90/ SAED_PDK_90/	(OpenAccess database)	Symbols and OA Tcl Pcells
HSpice models	./SAED_PDK90/HSpice/	.lib	The HSpice models
Documentation	./SAED_PDK90/documentation/	.doc	
Setup files	./SAED_PDK90/	.tcl	

1.3 Methodology of getting PDK components

For the used SAED90nm educational abstract technology, simulation models were generated using the Predictive Technology Model (PTM) developed by the Nanoscale Integration and Modeling Group (NIMO) of Arizona State University (ASU) (http://eas.asu.edu/~ptm).
Layout design rules for SAED_90nm educational, abstract technology were obtained by using the latest known set of free, vendor-independent, scalable design rules of MOSIS

(http://mosis.com/Technical/Designrules/scmos/scmos-main) by scaling for 90nm technology. Parasitics extraction deck was formed using the models of parasitic estimation developed by NIMO group of ASU (http://eas.asu.edu/~ptm). Process Design Kit SAED_PDK90 supports the key processes as IBM 90nm and TSMC 90nm.
SAED_PDK90 Technology files have been generated by converting Milkyway technology file of SAED_90nm 1P9M 1.2v/2.5v technology[1] to OpenAccess[2] format.

2 Design Environment

2.1 Design environment setup general issues

Setup file is kit of commands, which is foreseen for running CD and in which user defines specific parameters and functions to the current design.
Setup files include configuration scripts and files. In parallel to running program, a call of setup files are automatically generated according to the priority of usage level:

Table 2.1 Tool Startup Sequence

Type of Setup	Directory
Install	SYNOPSYS_CUSTOM_INSTALL
Site	SYNOPSYS_CUSTOM_SITE
Project	SYNOPSYS_CUSTOM_PROJECT
User	SYNOPSYS_CUSTOM_USER
Local	SYNOPSYS_CUSTOM_LOCAL

User creates scripts – ".cdesigner.tcl".
The program sources ".cdesigner.tcl" file automatically during operation of the program from $Home, then from current directory. ".cdesigner.tcl" file contains procedures and variables, created by the user.

2.2 Design environment setup

The library contains " .cdesigner.tcl " file, where procedures for running DRC and LVS are written. They are necessary for Hercules to recognize interoperable Pcells. In order to run DRC and LVS from CD, it is necessary to run "drc" or "lvs" commands from CD console.

Designer> drc
Designer> lvs

- Session startup creates the following:
  cdesigner.log
  cdesigner.tcl
- If cdesigner.log/tcl file exists, it is renamed into
  cdesigner.username.timestamp.log
  cdesigner.username.timestamp.tcl

3 SAED_PDK90

SAED_PDK90 contains technology files, physical verification files, parasitic extract files, symbol library directories.

3.1 Technology files

Technology_file directory includes technology and display resource files.

3.1.1 Display resources

- display.drf

This file contains color, fill and stipple patterns for all the packets used in the technology file in CD format.

3.1.2 Technology file

- saed90nm_1p9m_cd.tf

This file is for library creation for generic process, which contains layer information and design rule definition.

3.1.3 Layer map file

- saed_pdk90_layer.map

This file maps the layer name with the layer purpose, layer number, layer data type and stipple patterns used to describe the layout for the layout editor, DRC, LVS and parasitic extraction tools.

3.2 Physical verification files

Physical verification files directory includes Hercules DRC and LVS runset files.

3.2.1 Hercules

DRC Runset file

- rules.drc.9nm_saed90.ev

This is executable file used by the DRC software program that analyzes the data in the layout and calculates its interaction (spacing and overlaps) to other layers.

LVS Runset file

- rules.lvs.9nm_saed90.ev

This is executable file used by the LVS software program that extracts the intended devices and their parameters to compare with schematic netlists. LVS performs a comparison process that

verifies whether the geometric or layout implementation of a circuit matches the schematic representation.

3.3 Parasitic extract files

Parasitic extract files are executable files used by the parasitic extraction software program that extracts parasitic capacitance, resistance and/or inductance from circuit layout.

3.3.1 STARRCXT

Star-RCXT is a software tool that extracts parasitics from connected databases that represent IC layout designs.

- *.nxtgrd is a database containing capacitance, resistance, inductance and layer information which can be encrypted.
- The Interconnect Technology Format (*.itf) is a file which contains specification of each layer's content.
- *.map file maps the devices extracted by StarRCXT with the interoperable Pcells to be used for each device in the StarRCXT view produced after running StarRCXT.

4 Support devices

4.1 MOSFETs

SAED_PDK90 contains MOSFETs which have 3 or 4 terminals. Length and width are given in nanometers, areas are given in square nanometers and perimeters are given in nanometers. Design variables are anticipated for length and width entries. The parameters of area for diffusion are calculated from the width and the number of used fingers. The width per finger is calculated by dividing the width by the number of fingers. This parameter is viewed by the designer.

Table 4.1 MOS Spice models list

Spice models name	Description
nmos3t	nmos 3 terminal (D G S) mosfet transistor 1.2 volt
nmos4t_25	nmos 4 terminal (D G S) mosfet transistor 2.5 volt
nmos4t	nmos 4 terminal (D G S B) mosfet transistor 1.2 volt
nmos4t_hvt	nmos 4 terminal (D G S B) high voltage threshold mosfet transistor
nmos4t_lvt	nmos 4 terminal (D G S B) low voltage threshold mosfet transistor
pmos3t	pmos 3 terminal (D G S) mosfet transistor 1.2 volt
pmos4t_25	pmos 4 terminal (D G S) mosfet transistor 2.5 volt
pmos4t	pmos 4 terminal (D G S B) mosfet transistor 1.2 volt
pmos4t_hvt	pmos 4 terminal (D G S B) high voltage threshold mosfet transistor
pmos4t_lvt	pmos 4 terminal (D G S B) low voltage threshold mosfet transistor

Table 4.2 MOS symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
w	Width of each finger
wtot	Total width of MOSFET transistors
l	Length of each finger
entryMode	Gate width divided total width
nf	Number of fingers of gate
m	Multiplicity factor to place number of parallel devices
drainTerm	Right Terminal
sourceTerm	Left Terminal
strapSource	Strap source
strapDrain	Strap drain
internalStrapping	Allows Strap Source and Strap Drain Parameters
keepOut	Keep Out metal blockage
p2cs	Source contact to gate spacing

p2cd	Drain contact to gate spacing
DFMRules	Design For Manufacturing Rules
diffPolySpacing	Diffusion to poly spacing
diffContactEnclose	Diffusion enclose contact

4.2 Resistors

The resistors in the library consist of two types: diffused and poly resistors, which have 2 terminals. The diffused types are with diode backplates. The width for schematic simulation is specified in nanometers. All parameters entered into the resistor must be integers or floating-point numbers. No design variables are supported due to calculations that must be performed on the entries. The width and length are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

Table 4.3 Resistor Spice models list

Spice models name	Description
rnpoly	N+ poly unsalicided 2 terminal (PLUS MINUS) resistor
rppoly	P+ poly unsalicided 2 terminal (PLUS MINUS) resistor
rnpoly_wos	N+ poly salicided 2 terminal (PLUS MINUS) resistor
rppoly_wos	P+ poly salicided 2 terminal (PLUS MINUS) resistor
rndiff	N+ diffusion unsalicided 2 terminal (PLUS MINUS) resistor
rpdiff	P+ diffusion unsalicided 2 terminal (PLUS MINUS) resistor

Table 4.4 Resistor symbol parameters

Spice Model	HSpice model name
lvs_model	LVS model
model	HSpice model
r	Resistance
w	Resistor width
l	Resistor length
entryMode	width (r & w) mode or length and width (l & w) mode and length(r & l) mode
m	Multiplicity factor to place number of parallel devices
DFMRules	Design For Manufacturing Rules

4.3 Capacitor

This PDK contains ccap, which has 2 terminals. The ccap is metal on metal capacitor. The length and width for schematic simulation are specified in nanometers. All parameters entered into the capacitor must be integers or floating-point numbers. The width and length are snapped to grid, and the capacitance is recalculated and updated on the component form based on actual dimensions.

Table 4.5 Capacitor Spice models list

Spice models name	Description
ccap	2 terminal (PLUS MINUS) capacitor

Table 4.6 Capacitor symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
c	Capacitance
l	Length of capacitor
w	Width of capacitor
entryMode	length and width calculation based on the modes selected “c” or “l & w” or “c & w”. Default mode is “c”
m	Multiplicity factor to place number of parallel devices
mtot	Total multiplicity used in simulation. (Rows*Columns)
ceff	Effective capacitance

4.4 Diodes

The diodes in the PDK library consist of two types which have 2 terminals.

Table 4.7 Diode Spice models list

Spice models name	Description
nd	N+ 2 terminal (PLUS MINUS) diode
pd	P+ 2 terminal (PLUS MINUS) diode

Table 4.8 Diode symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
l	Length of diode
w	Width of diode
area	Area of the diode
DFMRules	Design For Manufacturing Rules
dioType	The type of diode, used in Pcells

4.5 BJTs

This PDK contains a vertical pnp (vpnp) and npn (vnpn) transistors, which have substrate collectors. The device has fixed dimensions for its emitter size. This device is typical of a CMOS process. The emitter width for schematic entry is specified in nanometers. All parameters entered into the npn and pnp must be integers or floating point numbers.

Table 4.9 BJT Spice models list

Spice models name	Description
vnpn	3 terminal (C B E) vertical bjt 1.2 volt
vpnp	3 terminal (C B E) vertical bjt 2.5 volt

Table 4.10 BJT symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
area	Area of the diode
emitterSize	The sizes of BJT are 2x2, 5x5
m	Multiplicity factor to place number of parallel devices
DFMRules	Design For Manufacturing Rules

4.6 Inductors

The inductor in the PDK library has 2 terminals. The inductor for this process is created using the top layer of metal interconnect. All parameters entered into the inductor form must be integers or floating-point numbers. The width space and inner radius are snapped to grid, and the inductance is calculated and updated on the component form based on actual dimensions.

Table 4.11 Inductor Spice models list

Spice models name	Description
spiind	2 terminal (PLUS MINUS) inductor

Table 4.12 Inductor symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
w	Width of inductor
Turns	Number of turns
R	Radius of Inductor
S	Spacing between turns
L	Approximated inductance
m	Multiplicity factor to place number of parallel devices
indType	The inductor type used in Pcells

4.7 Varactors

The varactors in the PDK library consist of two types, which have 2 terminals.

Table 4.13 Varactor Spice models list

Spice models name	Description
nvar	nmoscap 2 terminal (PLUS MINUS) varctor 1.2 volt
pvar	pmoscap 2 terminal (PLUS MINUS) varctor 1.2 volt

Table 4.14 Varactor symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
c	Capacitance of varactor
Lr	Length of varactor
Wr	Width of varactor
entryMode	“c” mode or “lr & wr” mode or “c & wr” mode
M	Multiplicity factor to place number of parallel devices
DFMRules	Design For Manufacturing Rules

5 Device Datasheets

5.1 NMOS Transistor

5.1.1 nmos3t

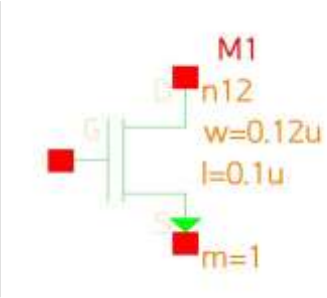

Figure 5.1 Symbol of nmos3t transistor

Table 0.1 nmos3t Spice model

Spice models name	Netlist
n12	m1 net1 net3 net2 gnd! n12 w='0.12u' l='0.1u' m=1

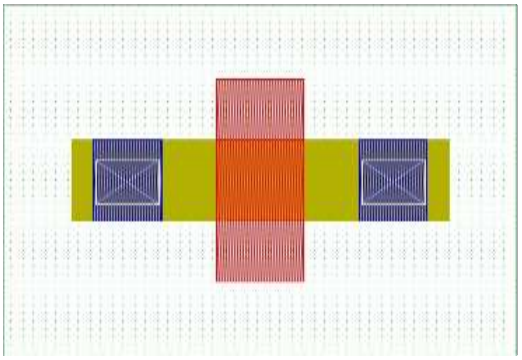

Figure 5.2 Layout of nmos3t transistor

Table 0.2 nmos3t Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	

Table 0.3 nmos3t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP CONTAINS PO
G	PO
D	DIFF AND NIMP NOT PO
S	DIFF AND NIMP NOT PO
B	Substrate

Table 0.4 nmos3t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.1.2 nmos4t

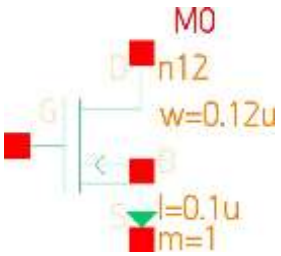

Figure 5.3 Symbol of nmos4t transistor

Table 0.1 nmos4t Spice model

Spice models name	Netlist
n12	m0 net1 net3 net2 net4 n12 w='0.12u' l='0.1u' m=1

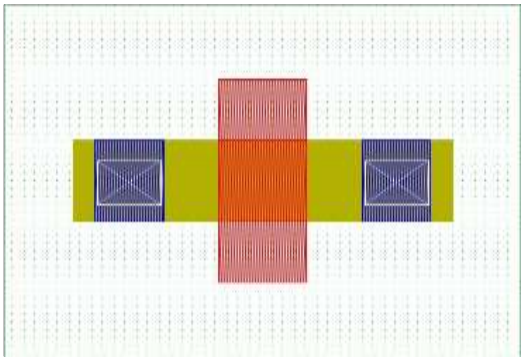

Figure 5.4 Layout of nmos3t transistor

Table 0.2 nmos4t Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	

Table 0.3 nmos4t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP CONTAINS PO
G	PO
D	DIFF AND NIMP NOT PO
S	DIFF AND NIMP NOT PO
B	Substrate

Table 0.4 nmos4t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.1.3 nmos4t_25

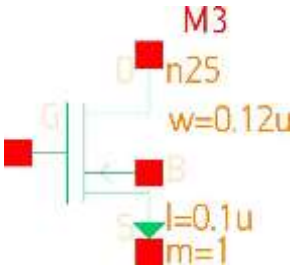

Figure 5.5 Symbol of nmos4t_25 transistor

Table 0.1 nmos4t_25 Spice model

Spice models name	Netlist
n25	m3 net1 net3 net2 gnd! n25 w='0.12u' l='0.1u' m=1

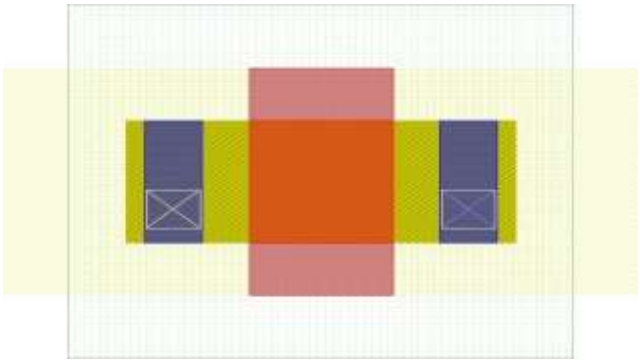

Figure 5.6 Layout of nmos4t_25 transistor

Table 0.2 nmos4t_25 Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
DIFF_25	

Table 0.3 nmos4t_25 Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND DIFF_25 CONTAINS PO
G	PO
D	DIFF AND NIMP AND DIFF_25 NOT PO
S	DIFF AND NIMP AND DIFF_25 NOT PO
B	Substrate

Table 0.4 nmos4t_25 LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.1.4 nmos4t_hvt

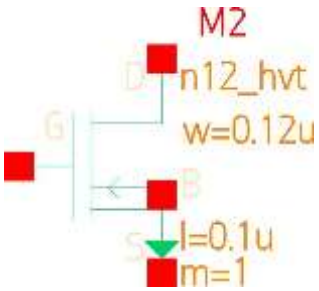

Figure 5.7 Symbol of nmos4t_hvt transistor

Table 0.1 nmos4t_hvt Spice model

Spice models name	Netlist
n12_hvt	m2 net1 net3 net2 gnd! n12_hvt w='0.12u' l='0.1u' m=1

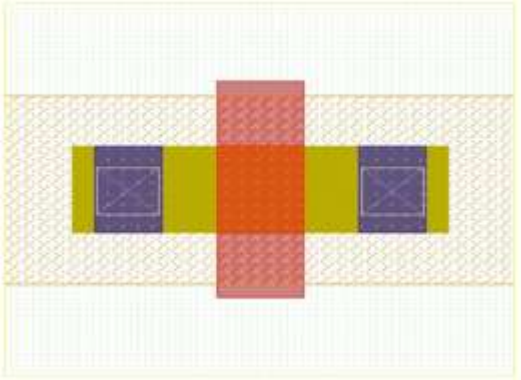

Figure 5.8 Layout of nmos4t_hvt transistor

Table 0.2 nmos4t_hvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
HVTIMP	

Table 0.3 nmos4t_hvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND HVTIMP CONTAINS PO
G	PO
D	DIFF AND NIMP AND HVTIMP NOT PO
S	DIFF AND NIMP AND HVTIMP NOT PO
B	Substrate

Table 0.4 nmos4t_hvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.1.5 nmos4t_lvt

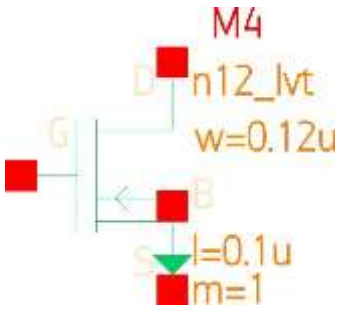

Figure 5.9 Symbol of nmos4t_lvt transistor

Table 0.1 nmos4t_lvt Spice model

Spice models name	Netlist
n12_lvt	M4 net1 net3 net2 gnd! n12_lvt w='0.12u' l='0.1u' m=1

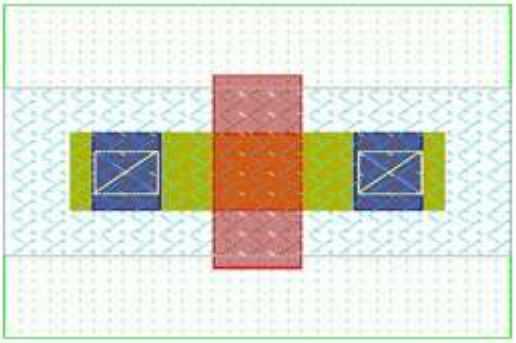

Figure 5.10 Layout of nmos4t_lvt transistor

Table 0.2 nmos4t_lvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
LVTIMP	

Table 0.3 nmos4t_lvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND LVTIMP CONTAINS PO
G	PO
D	DIFF AND NIMP AND LVTIMP NOT PO
S	DIFF AND NIMP AND LVTIMP NOT PO
B	Substrate

Table 0.4 nmos4t_lvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.2 PMOS Transistor

5.2.1 pmos3t

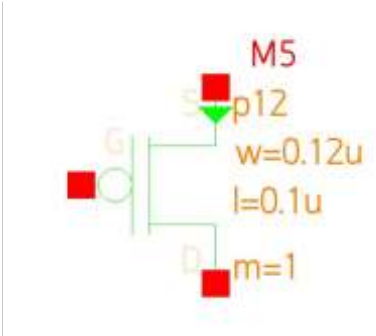

Figure 5.11 Symbol of pmos3t transistor

Table 0.1 pmos3t Spice model

Spice models name	Netlist
p12	m5 net1 net3 net2 gnd! p12 w='0.12u' l='0.1u' m=1

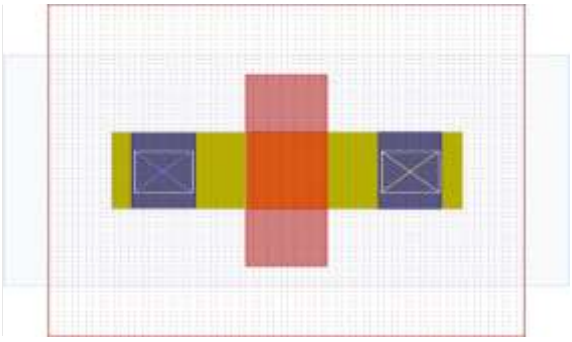

Figure 5.12 Layout of pmos3t transistor

Table 0.2 pmos3t Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
NWELL	

Table 0.3 pmos3t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL CONTAINS PO
G	PO
D	DIFF AND PIMP AND NWELL NOT PO
S	DIFF AND PIMP AND NWELL NOT PO
B	Substrate

Table 0.4 pmos3t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.2.2 pmos4t

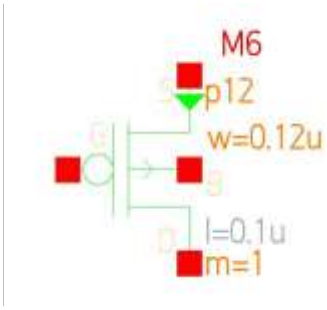

Figure 5.13 Symbol of pmos4t transistor

Table 0.1 pmos4t Spice model

Spice models name	Netlist
p12	m6 net1 net3 net2 net4 p12 w='0.12u' l='0.1u' m=1

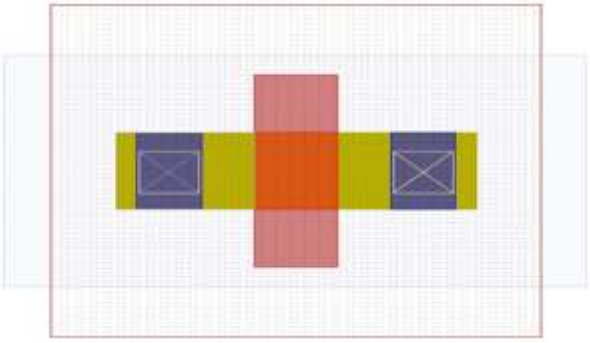

Figure 5.14 Layout of pmos3t transistor

Table 0.2 pmos4t Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
NWELL	

Table 0.3 pmos4t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL CONTAINS PO
G	PO
D	DIFF AND PIMP AND NWELL NOT PO
S	DIFF AND PIMP AND NWELL NOT PO
B	Substrate

Table 0.4 pmos4t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.2.3 pmos4t_25

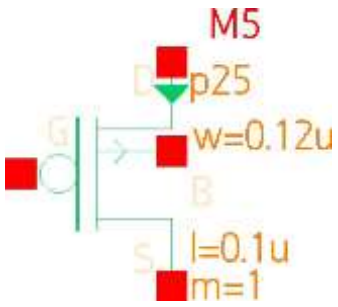

Figure 5.15 Symbol of pmos4t_25 transistor

Table 0.1 pmos4t_25 Spice model

Spice models name	Netlist
p25	m7 net1 net3 net2 gnd! p25 w='0.12u' l='0.1u' m=1

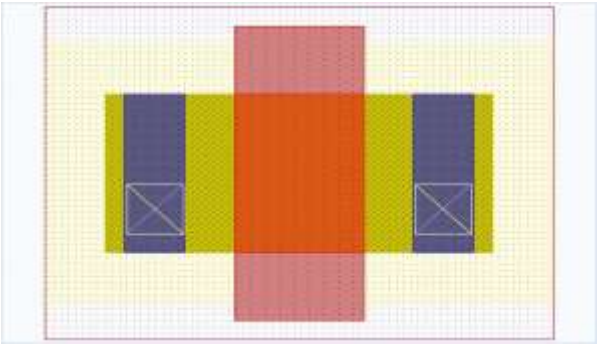

Figure 5.16 Layout of pmos4t_25 transistor

Table 0.2 pmos4t_25 Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
DIFF_25	
NWELL	

Table 0.3 pmos4t_25 Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND DIFF_25 AND NWELL CONTAINS PO
G	PO
D	DIFF AND PIMP AND DIFF_25 AND NWELL NOT PO
S	DIFF AND PIMP AND DIFF_25 AND NWELL NOT PO
B	Substrate

Table 0.4 pmos4t_25 LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.2.4 pmos4t_hvt

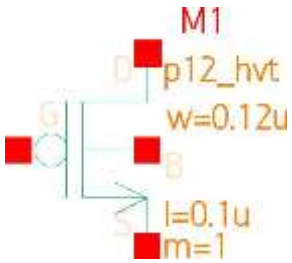

Figure 5.17 Symbol of pmos4t_hvt transistor

Table 0.1 pmos4t_hvt Spice model

Spice models name	Netlist
p12_hvt	m8 net1 net3 net2 gnd! p12_hvt w='0.12u' l='0.1u' m=1

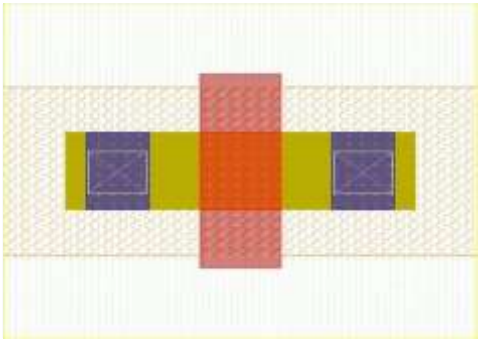

Figure 5.18 Layout of pmos4t_hvt transistor

Table 0.2 pmos4t_hvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
HVTIMP	
NWELL	

Table 0.3 pmos4t_hvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND HVTIMP CONTAINS PO
G	PO
D	DIFF AND PIMP AND HVTIMP AND NWELL NOT PO
S	DIFF AND PIMP AND HVTIMP AND NWELL NOT PO
B	Substrate

Table 0.4 pmos4t_hvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.2.5 pmos4t_lvt

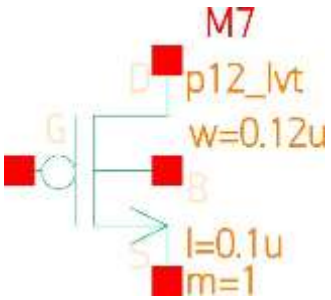

Figure 5.19 Symbol of pmos4t_lvt transistor

Table 0.1 pmos4t_lvt Spice model

Spice models name	Netlist
p12_lvt	m7 net1 net3 net2 gnd! p12_lvt w='0.12u' l='0.1u' m=1

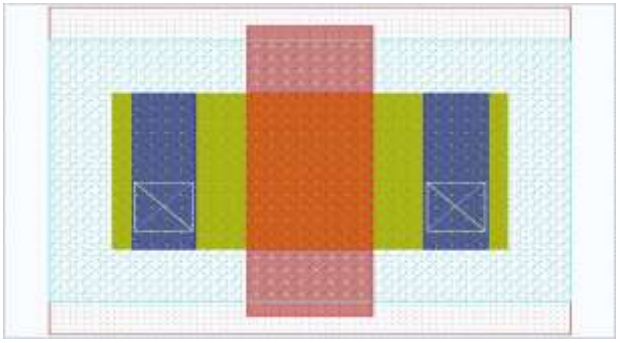

Figure 5.20 Layout of pmos4t_lvt transistor

Table 0.2 pmos4t_lvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
LVTIMP	
NWELL	

Table 0.3 pmos4t_lvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND LVTIMP CONTAINS PO
G	PO
D	DIFF AND PIMP AND LVTIMP AND NWELL NOT PO
S	DIFF AND PIMP AND LVTIMP AND NWELL NOT PO
B	Substrate

Table 0.4 pmos4t_lvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.3 Resistor

5.3.1 rnpoly

Figure 5.21 Symbol of rnpoly resistor

Table 0.1 rnpoly Spice model

Spice models name	Netlist
rnpoly	xr6 net28 net29 rnpoly w='0.4u' l='2u' m=1

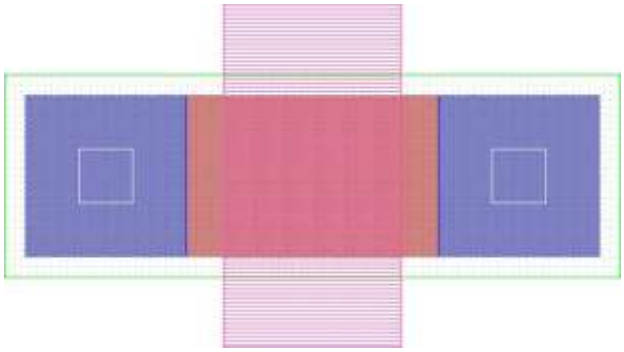

Figure 5.22 Layout of rnpoly resistor

Table 0.2 rnpoly Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
NIMP	

Table 0.3 rnpoly Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND NIMP
PLUS	PO NOT RPOLY
MINUS	PO NOT RPOLY

Table 0.4 rnpoly LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

5.3.2 rppoly

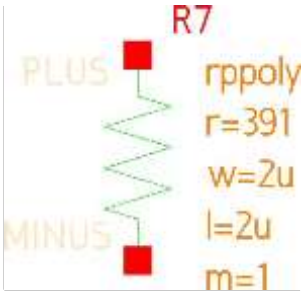

Figure 5.23 Symbol of rppoly resistor

Table 0.1 rppoly Spice model

Spice models name	Netlist
rppoly	xr7 net28 net29 rppoly w='0.4u' l='2u' m=1

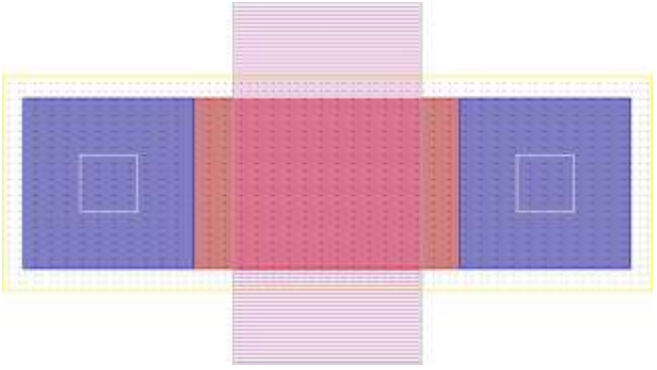

Figure 5.24 Layout of rppoly resistor

Table 0.2 rppoly Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
PIMP	

Table 0.3 rppoly Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND PIMP
PLUS	PO NOT RPOLY
MINUS	PO NOT RPOLY

Table 0.4 rppoly LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

5.3.3 rnpoly_wos

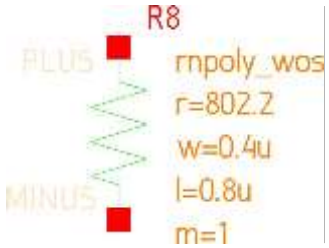

Figure 5.25 Symbol of rnpoly_wos resistor

Table 0.1 rnpoly_wos Spice model

Spice models name	Netlist
rnpoly_wos	xr8 net28 net29 rnpoly_wos w='0.4u' l='2u' m=1

Figure 5.26 Layout of rnpoly_wos resistor

Table 0.2 rnpoly_wos Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
NIMP	
SBLK	

Table 0.3 rnpoly_wos Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND SBLK AND NIMP
PLUS	PO NOT RPOLY NOT SBLK
MINUS	PO NOT RPOLY NOT SBLK

Table 0.4 rnpoly_wos LVS Checking

Parameter	Calculation
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

5.3.4 rppoly_wos

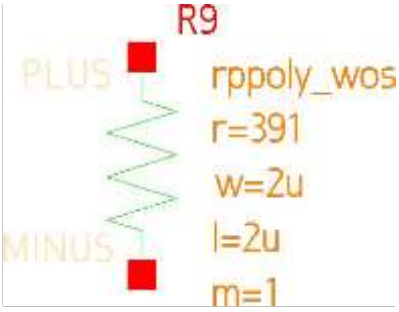

Figure 5.27 Symbol of rppoly_wos resistor

Table 0.1 rppoly_wos Spice model

Spice models name	Netlist
rppoly_wos	xr9 net28 net29 rppoly_wos w='0.4u' l='2u' m=1

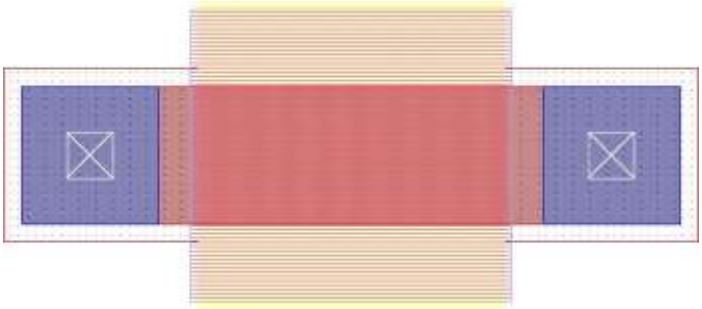

Figure 5.28 Layout of rppoly_wos resistor

Table 0.2 rppoly_wos Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
PIMP	
SBLK	

Table 0.3 rppoly_wos Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND SBLK AND PIMP
PLUS	PO NOT RPOLY NOT SBLK
MINUS	PO NOT RPOLY NOT SBLK

Table 0.4 rppoly_wos LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

5.3.5 rndiff

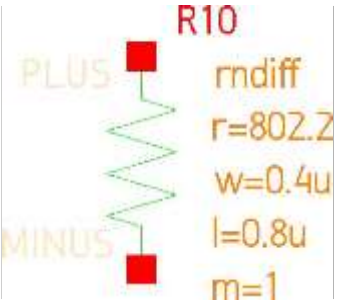

Figure 5.29 Symbol of rndiff resistor

Table 0.1 rndiff Spice model

Spice models name	Netlist
rndiff	xr10 net36 net37 rndiff w='0.4u' l='2u' m=1

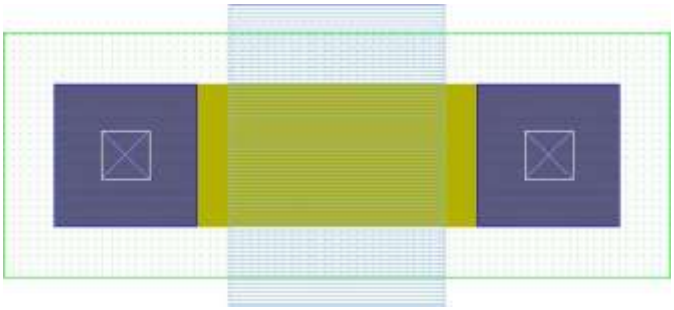

Figure 5.30 Layout of rndiff resistor

Table 0.2 rndiff Device Layers

Device Layers	Layer Color and Fill
DIFF	
RDIFF	
CO	
M1	
NIMP	

Table 0.3 rndiff Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND RDIFF AND NIMP
PLUS	DIFF NOT RDIFF
MINUS	DIFF NOT RDIFF

Table 0.4 rndiff LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

5.3.6 rpdiff

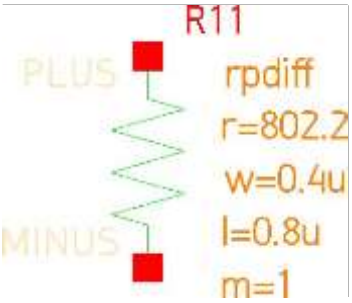

Figure 5.31 Symbol of rpdiff resistor

Table 0.1 rpdiff Spice model

Spice models name	Netlist
rpdiff	xr11 net36 net37 rpdiff w='0.4u' l='2u' m=1

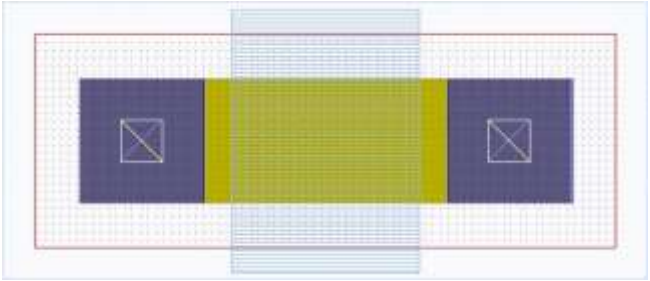

Figure 5.32 Layout of rpdiff resistor

Table 0.2 rpdiff Device Layers

Device Layers	Layer Color and Fill
DIFF	
RDIFF	
CO	
M1	
PIMP	
NWELL	

Table 0.3 rpdiff Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND RDIFF AND PIMP AND NWELL
PLUS	DIFF NOT RDIFF
MINUS	DIFF NOT RDIFF

Table 0.4 rpdiff LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

5.4 Capacitor

5.4.1 ccap

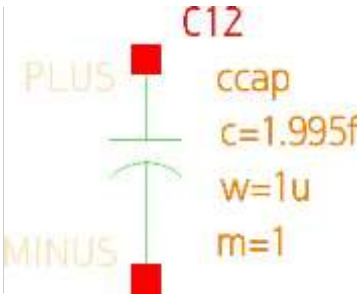

Figure 5.33 Symbol of ccap capacitor

Table 0.1 ccap Spice model

Spice models name	Netlist
ccap	xc12 net40 net41 ccap l='1u' w='1u' m=1

Figure 5.34 Layout of ccap capacitor

Table 0.2 ccap Device Layers

Device Layers	Layer Color and Fill
M1	
M2	
M3	
M4	
M5	
VIA1	
VIA2	
VIA3	
VIA4	
METDMY	
CBMMARK	
CTMMARK	

Table 0.3 ccap Device Derivation

Device Derivation	Device Layer Derivation
Recognition	MX AND M1 (X<6)
PLUS	MX
MINUS	M1 UNDER MX

Table 0.4 ccap LVS Checking

Parameter Calculation	
AreaArea	Area of MX
Capacitance	CperA * Area

5.5 Diode

5.5.1 nd

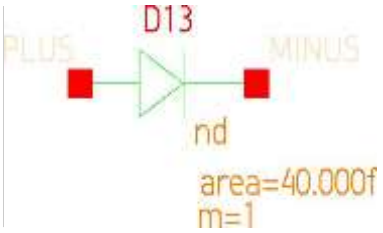

Figure 5.35 Symbol of nd diode

Table 0.1 nd Spice model

Spice models name	Netlist
nd	d13 net45 net44 nd area='40.000f' m=1

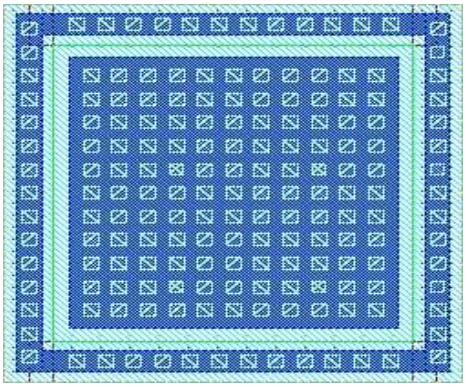

Figure 5.36 Layout of nd diode

Table 0.2 nd Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF	
CO	
NWELL	
PIMP	
NIMP	
DIOD	

Table 0.3 nd Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NIMP AND PIMP
PLUS	DIOD AND PIMP
MINUS	DIOD AND NIMP

Table 0.4 nd LVS Checking

Parameter Calculation	
area	Area of MINUS

5.5.2 pd

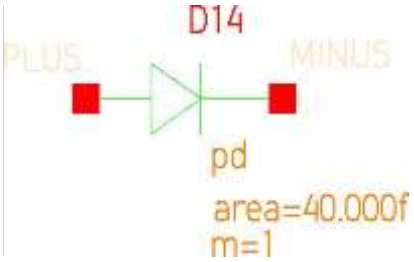

Figure 5.37 Symbol of pd diode

Table 0.1 pd Spice model

Spice models name	Netlist
pd	d14 net45 net44 pd area='40.000f' m=1

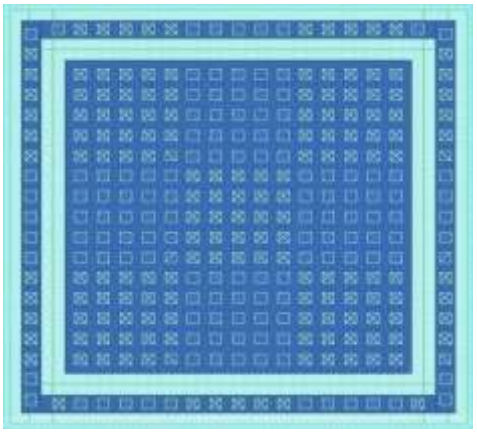

Figure 5.38 Layout of pd diode

Table 0.2 pd Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF	
CO	
NWELL	
PIMP	
NIMP	
DIOD	

Table 0.3 pd Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NWELL AND NIMP AND PIMP
PLUS	DIOD AND NWELL AND NIMP
MINUS	DIOD AND NWELL AND PIMP

Table 0.4 pd LVS Checking

Parameter	Calculation
area	Area of MINUS

5.6 Inductor

5.6.1 spiind

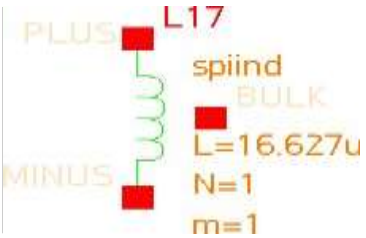

Figure 5.39 Symbol of spiind inductor

Table 0.1 spilnd Spice model

Spice models name	Netlist
spiind	xl17 net55 net56 net54 spiind w='5u' N=1 R='40u' S=0 m=1

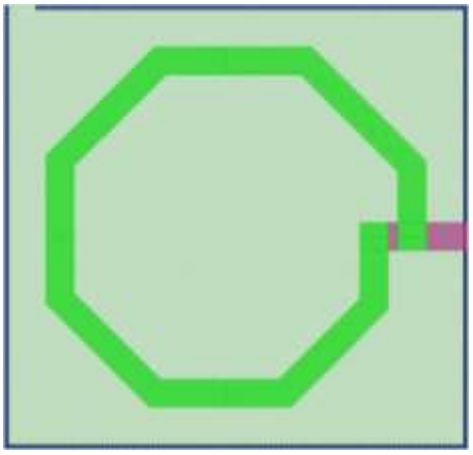

Figure 5.40 Layout of spiind inductor

Table 0.2 spiind Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
CO	
M1	
M2	
M3	
M4	
VIA1	
VIA2	
VIA3	
INDMARK	

Table 0.3 spiind Device Derivation

Device Derivation	Device Layer Derivation
Recognition	INDMARK AND M4
PLUS	M4 AND INDMARK
MINUS	M3 AND INDMARK

Table 0.4 spiind LVS Checking

Parameter Calculation	
r	radius
s	M4 space
w	M4 width
nr	Number of M4 turns
Inductance	(N*da*do+N)*1.0e-9 di=2*R*1e6 do=2*(R*1e6)+(int(N+0.5)*(w*1e6+3)-3)+((int(N)+1)*(w*1e6+3)-3) da=(di+do)/2

5.7 BJT

5.7.1 vnpn

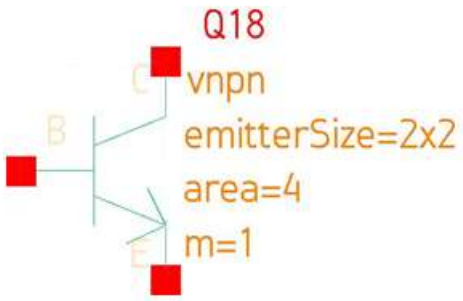

Figure 5.41 Symbol of vnpn transistor

Table 0.1 vnpn Spice model

Spice models name	Netlist
vnpn	q18 net48 net50 net49 vnpn m=1

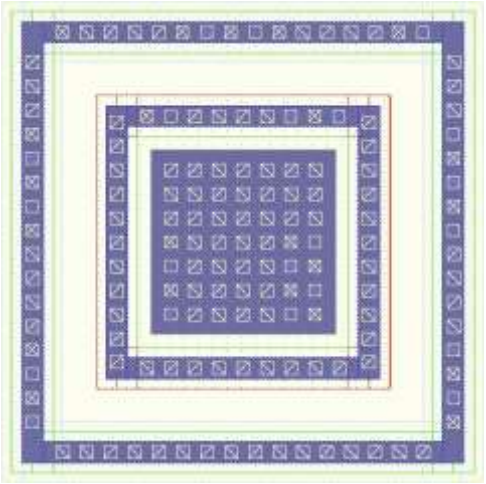

Figure 5.42 Layout of vnpn transistor

Table 0.2 vnpn Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PIMP	
NWELL	
CO	
M1	
BJTMARK	

Table 0.3 vnpn Device Derivation

Device Derivation	Device Layer Derivation
Recognition	BJTMARK AND PIMP AND NWELL
E	BJTMARK AND NIMP NOT NWELL
B	BJTMARK AND PIMP
C	BJTMARK AND NIMP AND NWELL

Table 0.4 vnpn LVS Checking

Parameter Calculation	
area	Area of Emitter

5.7.2 vpnp

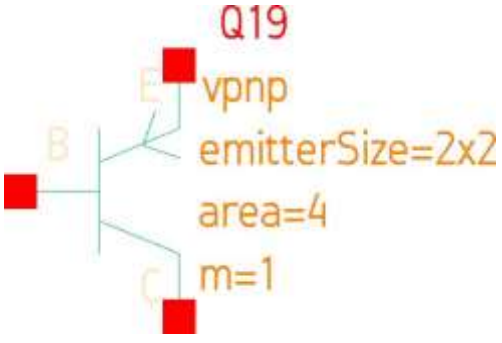

Figure 5.43 Symbol of vpnp transistor

Table 0.1 vpnp Spice model

Spice models name	Netlist
vpnp	q19 net48 net50 net49 vpnp m=1

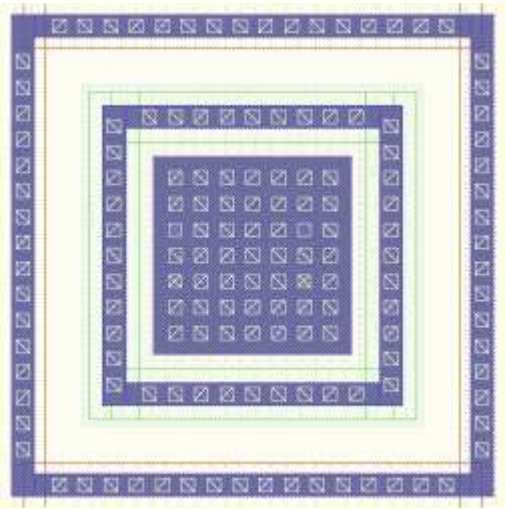

Figure 5.44 Layout of vpnp transistor

Table 0.2 vpnp Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PIMP	
NWELL	
CO	
M1	
BJTMARK	

Table 0.3 vpnp Device Derivation

Device Derivation	Device Layer Derivation
Recognition	BJTMARK AND PIMP AND NWELL
E	BJTMARK AND Nburied AND NIMP AND Pwell
B	BJTMARK AND Nburied AND PIMP AND Pwell
C	BJTMARK AND Nburied AND NIMP ANDNOT Pwell

Table 0.4 vpnp LVS Checking

Parameter Calculation	
area	Area of Emitter

5.8 Varactor

5.8.1 nvar

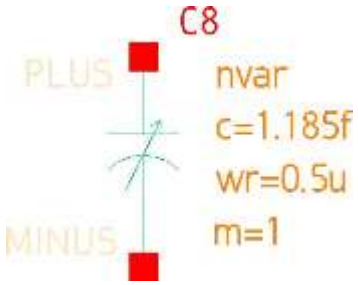

Figure 5.45 Symbol of nvar varactor

Table 0.1 nvar Spice model

Spice models name	Netlist
nvar	q8 net48 net50 net49 vnpn m=1

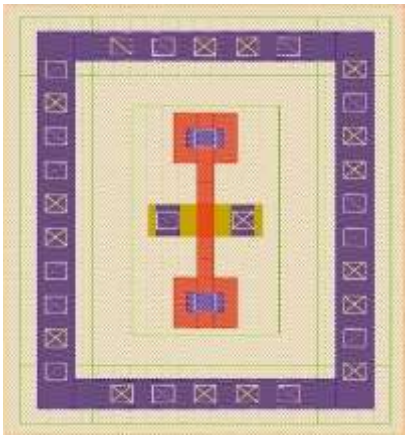

Figure 5.46 Layout of nvar varactor

Table 0.2 nvar Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
NWELL	
CO	
M1	
PO	
VARMARK	

Table 0.3 nvar Device Derivation

Device Derivation	Device Layer Derivation
Recognition	VARMARK AND DIFF AND NIMP CONTAINS PO
PLUS	VARMARK AND DIFF AND NIMP NOT PO
MINUS	VARMARK AND DIFF AND NIMP NOT PO

Table 0.4 nvar LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

5.8.2 pvar

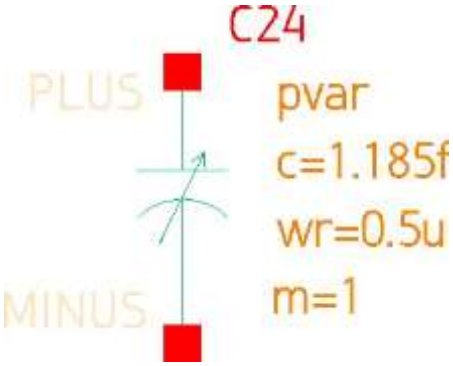

Figure 5.47 Symbol of pvar varactor

Table 0.1 pvar Spice model

Spice models name	Netlist
vpnp	q19 net48 net50 net49 vpnp m=1

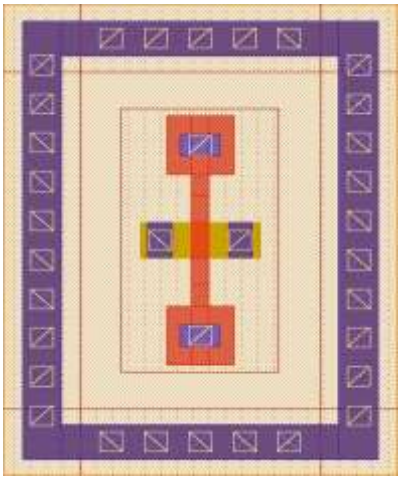

Figure 5.48 Layout of pvar varactor

Table 0.2 pvar Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
NWELL	
CO	
M1	
PO	
VARMARK	

Table 0.3 pvar Device Derivation

Device Derivation	Device Layer Derivation
Recognition	VARMARK AND DIFF AND PIMP AND NWELL CONTAINS PO
PLUS	VARMARK AND DIFF AND PIMP AND NWELL NOT PO
MINUS	VARMARK AND DIFF AND PIMP AND NWELL NOT PO

Table 0.4 pvar LVS Checking

Parameter	Calculation
Length	PO intersecting DIFF
Width	PO inside DIFF

6 References

1 SAED90nm EDK Documentation (**https://solvnet.synopsys.com/redauthftp/labs/90nm_Generic_Libraries**)
2 OpenAccess (**http://www.si2.org/?page=621**)