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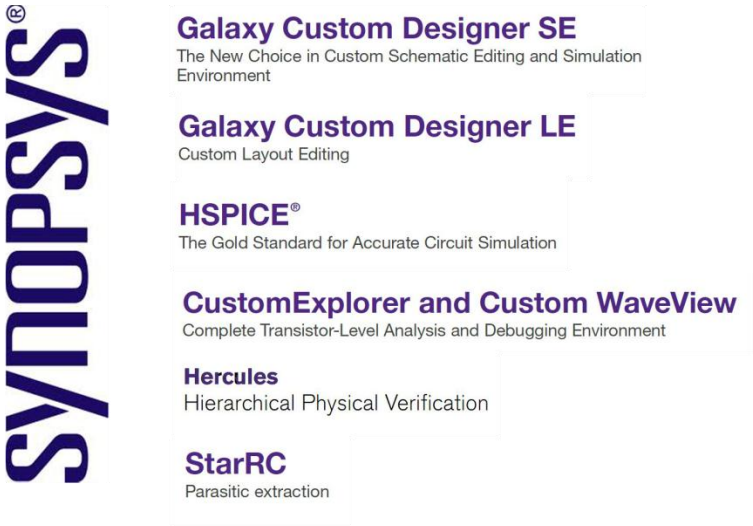

Full Custom IC Design Using Synopsys Galaxy Design

DESIGN & SIMULATION OF CMOS INVERTER IN 90NM TECHNOLOGY USING CUSTOM DESIGNER – SYNOPSY

By

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Introduction

In this tutorial, you will design and simulate a CMOS inverter using **90nm technology PDK** and **Synopsys Galaxy Custom Design Tools** listed below. The tutorial includes detailed step-by-step instructions on how to do schematic entry, layout entry, verification, and pre-layout and post layout simulations.

Tools Used in this tutorial:

Tool	Version	Platform & OS
Custom Design	E-2010.09-SP1-1	RHEL 5.3-4 ; 32-Bit
HSPICE	E-2010.12	RHEL 5.3-4 ; 32-Bit
Hercules	B-2008.09-SP3-1	RHEL 5.3-4 ; 32-Bit
StarRC	E-2010.12-1	RHEL 5.3-4 ; 32-Bit
Custom Explorer	E-2010.12	RHEL 5.3-4 ; 32-Bit

Starting Custom Designer

Students should use the PC-LAB to do this tutorial. When you turn on the PC, use the Linux boot option OS on that PC. Use user name SY-LAB and password VLSI. Double click on the "terminal" shortcut on the desktop, and you will see a screen similar to figure 1 below. If the short cut "terminal" is not present, right click and click terminal on drop down menu. In the terminal widow, write the following lines.

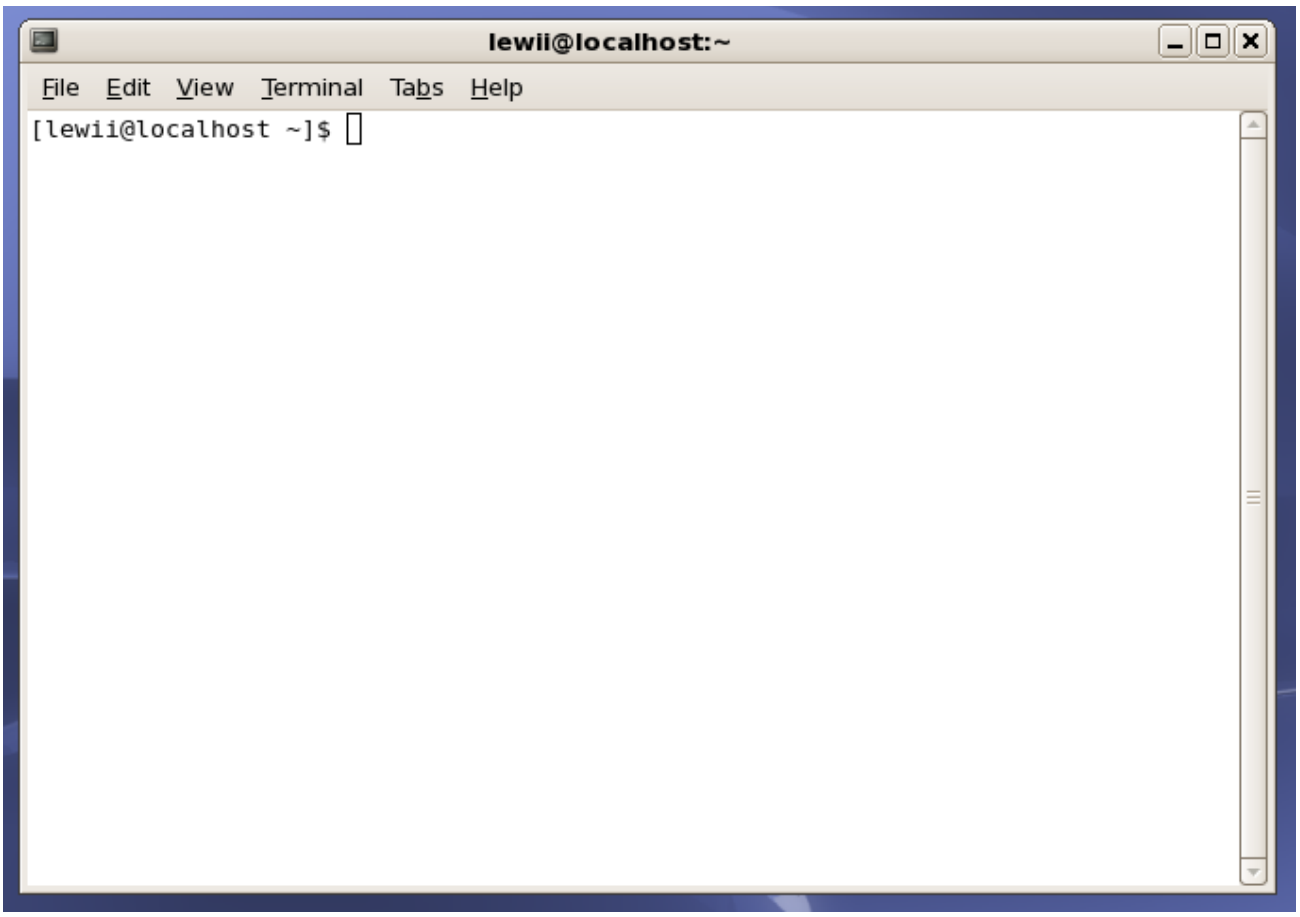

Figure 1: terminal

% cd Desktop/work/cdesigner/ (press ENTER)

% cdesigner (press ENTER)

Wait for a second and the program main screen will appear like that in fig (2).

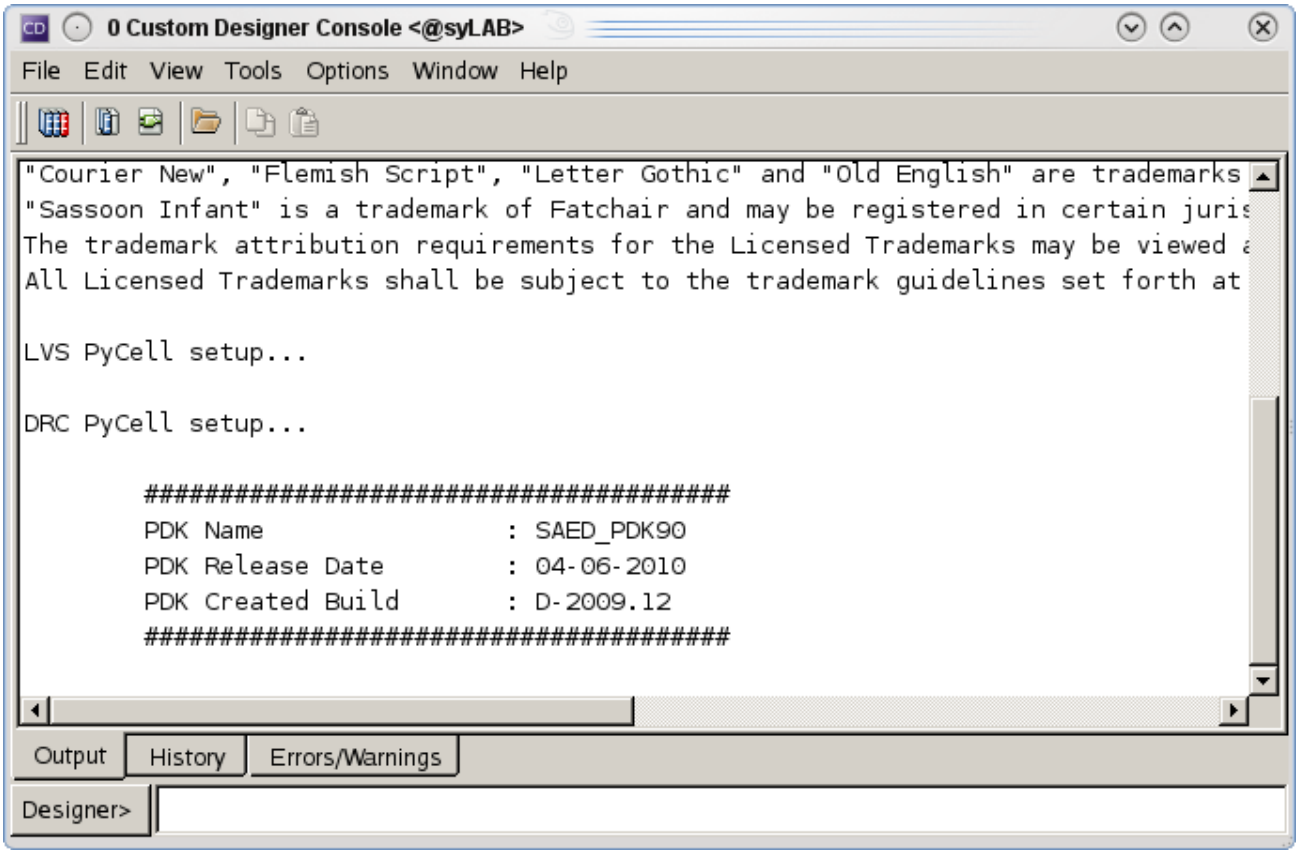

Figure 2: Custom Designer Main window

Creating Libraries and Cells

After running the program, you need to create a library to keep all your work inside it.

Create Library

Click the file menu in menu bar (upper left corner in fig (2)), click: *Files* > *Library*, the window in fig (3) will show up. In this window fill up the following information:

1. Library Name in the first Field, make sure no spaces or dashes are used. Only underscore is allowed.
2. Keep directory the default one. In the TYPE, section chooses *filesys.*
3. In the technology section, use attaches SAED_PDK_90.
4. In the TYPE, section chooses *filesys.*
5. Check the two boxes on the left, so you can use technology libraries.

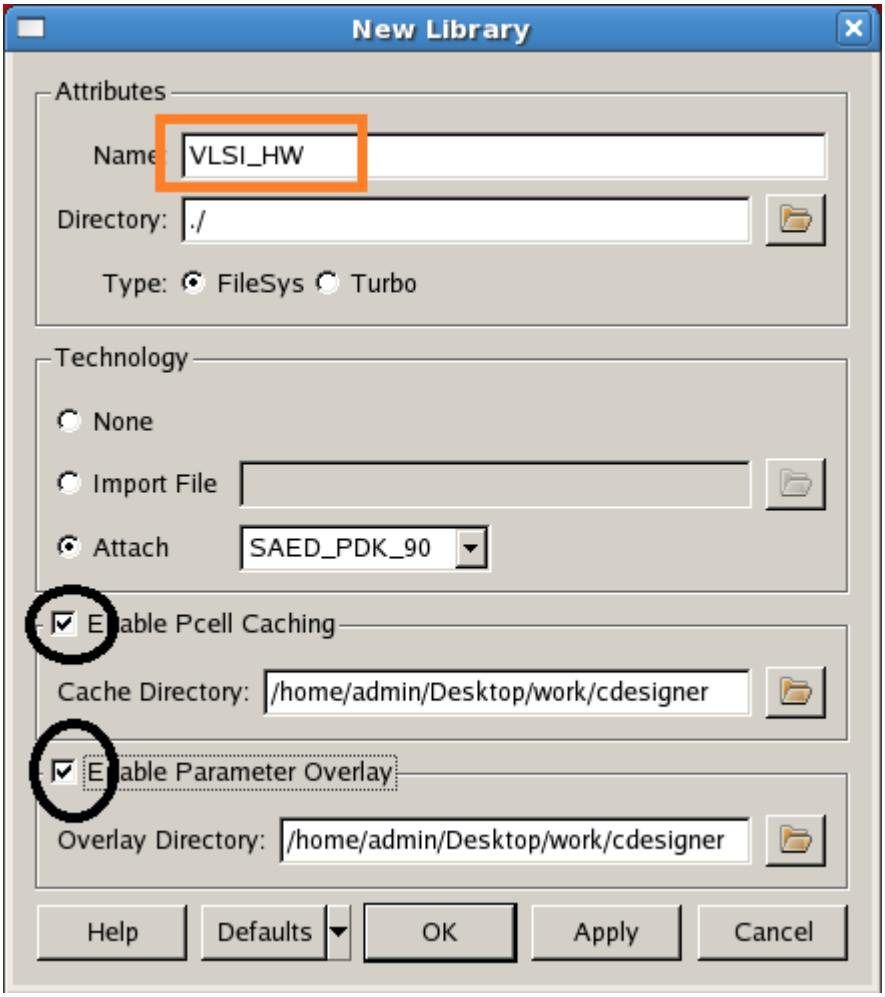

Figure 3 : New Library Window.

Create Category

To be organized, you will need to create categories.

Go to TOOLs menu in figure 2. *Tools > Library Manager*. You will get the window in fig (4).

1. Select your library created previously from the left column.
2. Go to edit menu. *Edit > cell category*. Window in fig (5) will pop up.
3. Select a library in the left field, then fill in the category name (ex, HW1) and click create.
4. The column on the right shows that text now.
5. Now repeat step 4 twice to create HW2 and PROJ.
6. Click OK.
7. The second column in fig (4) now changes and contains the new categories.
8. Close the window in fig (4).

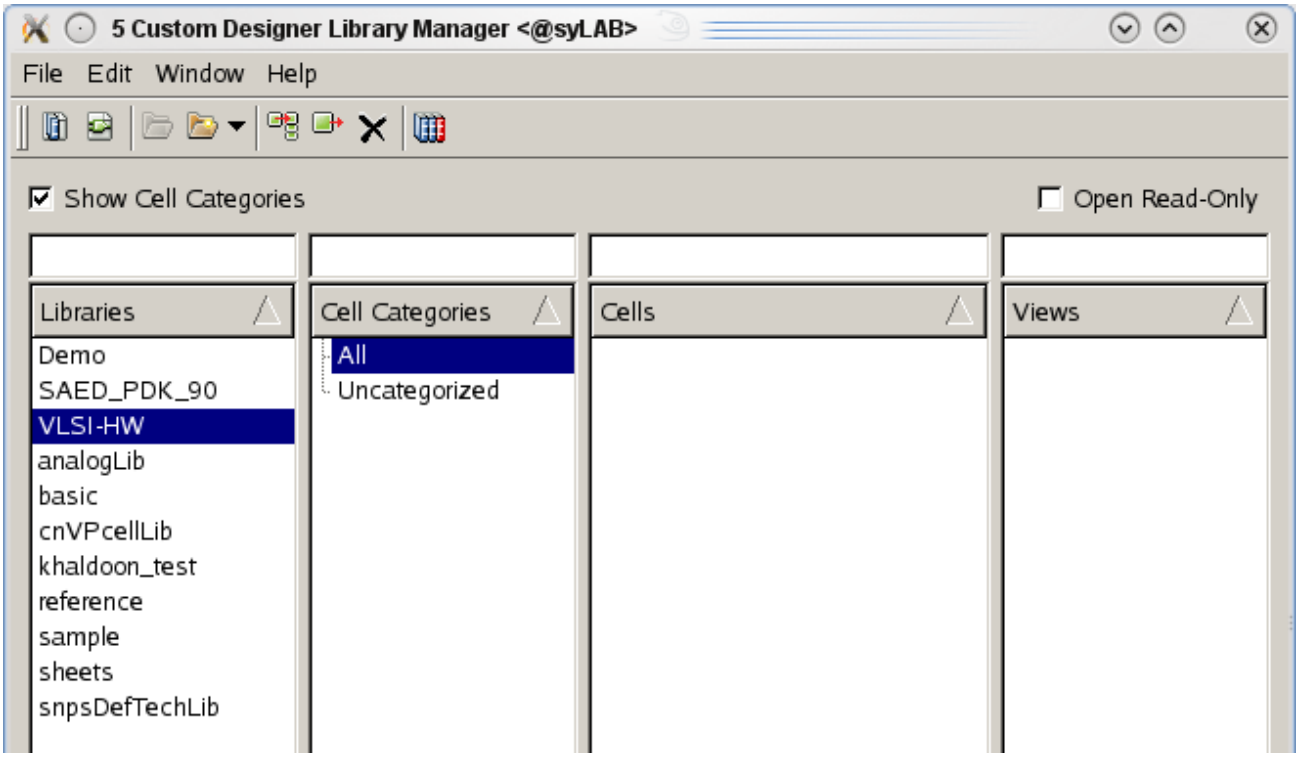

Figure 4 : Library manager window.

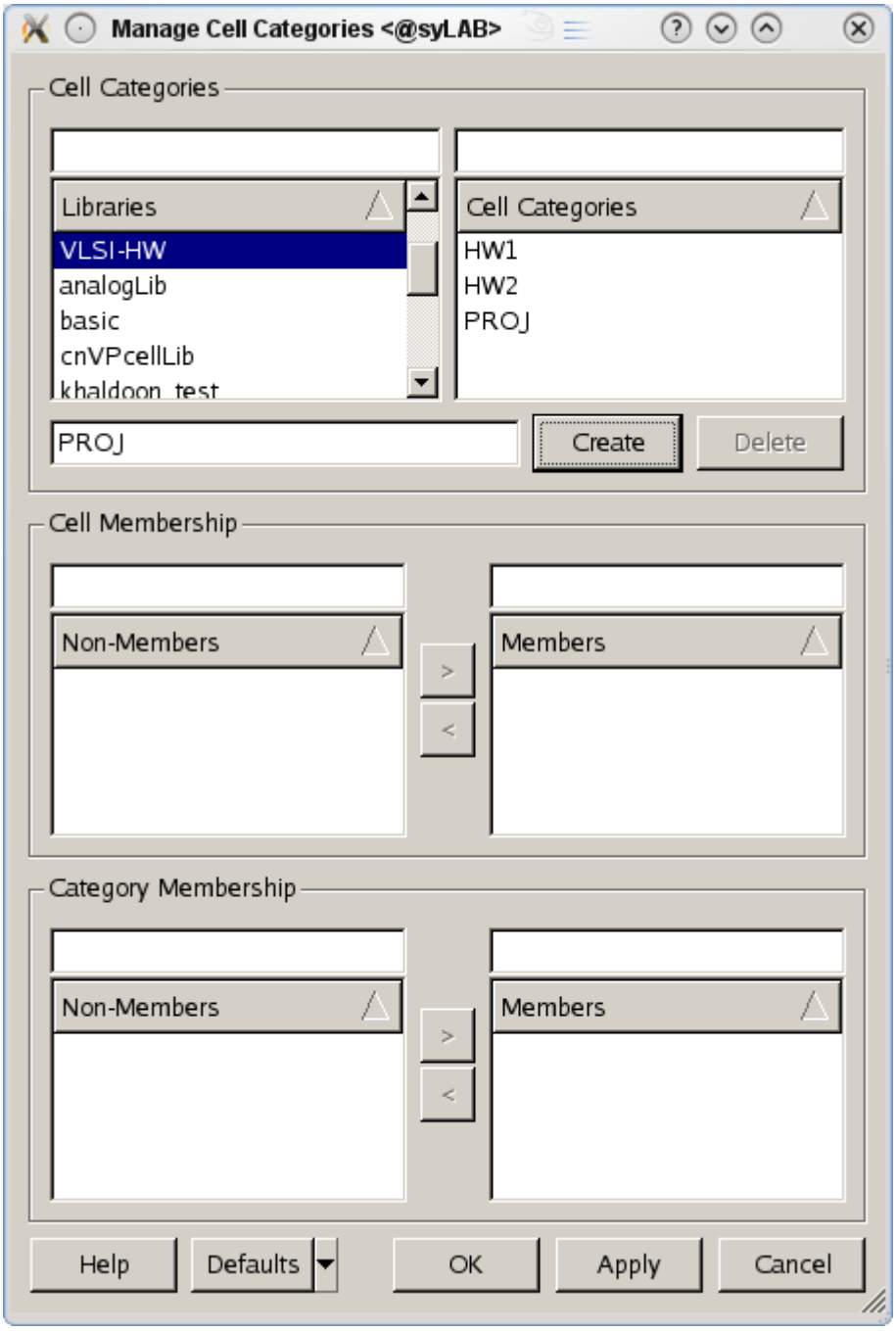

Figure 5 : Cell Category Window.

Create Cell

In the main window, go to File > *New* > *Cell view*. The menu in fig (6) will open.

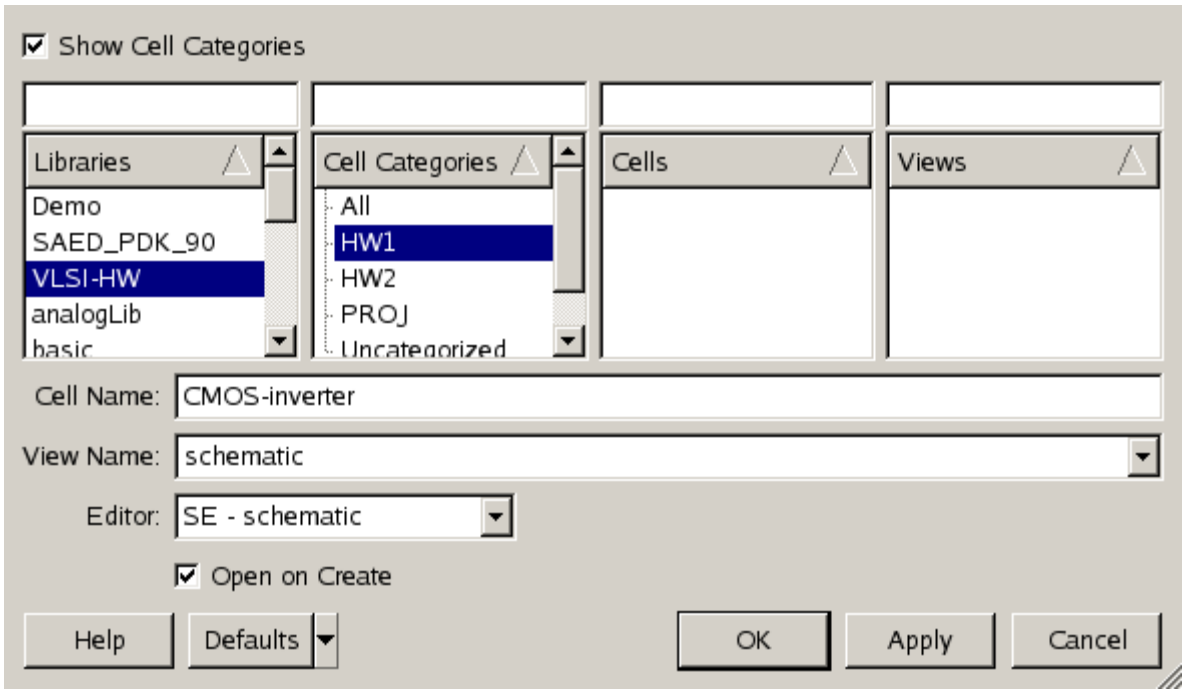

Figure 6 : New Cell window.

Steps:

1. Select your library created previously.
2. Select category – HW1 for example.
3. Write cell name in its field.
4. Select *schematic* in the dropdown list for the view name.
5. Editor should be set to *SE-schematic*.
6. Checks the Box open on create.
7. Click OK.

This will open the window in fig (7) which is the main GUI for the *schematic editor* in ***Custom Designer.***

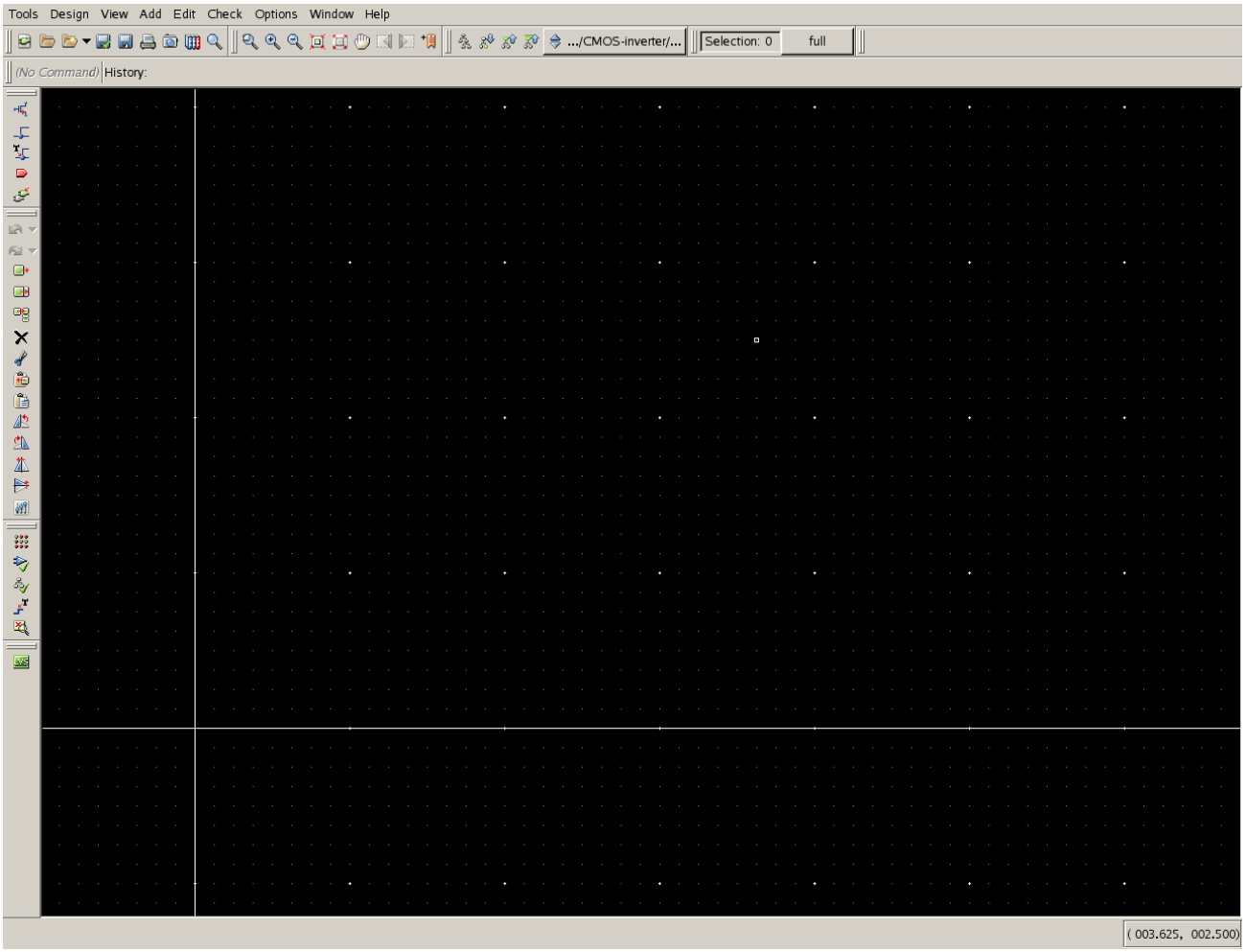

Figure 7 : main window of schematic Editor – Custom Designer

Creating Design

If you look at the left side of the window in fig (7), you will see a bar that contains the short cuts of the most commonly used commands. Those commands are explained as shown below.

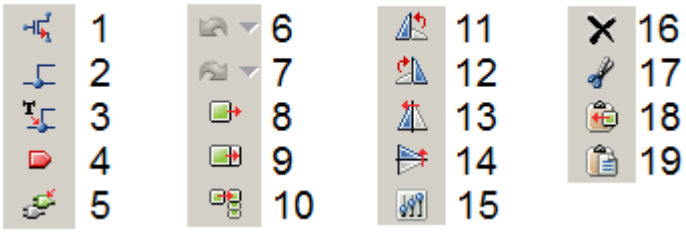

Figure 8 : left bar tools.

Tools function:

1. Add instance.
2. Add node.
3. Name wire or node.
4. Add PIN.
5. New Cell view from cell view.
6. Undo.
7. Redo.
8. Move instance.
9. Stretch Instance.
10. Copy cell.
11. Rotate 90 left.
12. Rotate 90 right.
13. Flip horizontal.
14. Flip vertical.
15. Delete Instance.
16. Cut.
17. Copy.
18. Paste.

Figure (9) shows a different path to do the short cut commands.

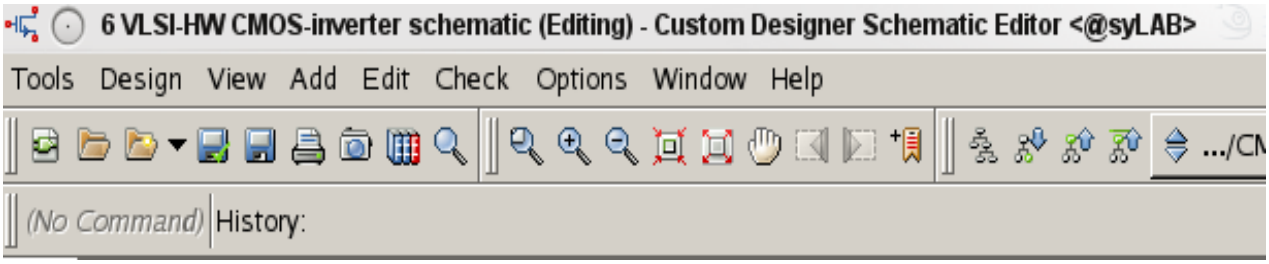

Figure 9 : Menu Bar and the Tools Bar.

After introducing the program main GUI, we move to the design stage. For this tutorial, we will use the CMOS inverter as our example.

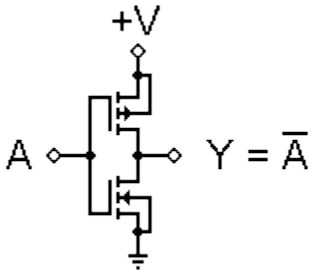

Figure 10 : CMOS inverter Schematics and truth table.

To construct the above design on your workplace you should follow these steps:

1. Place instance (component) in the work place, there are two ways:
    a. Go to *ADD* menu > *Instance or*
    b. Press (I) key on your keyboard.
2. You will get the window in fig (11).
3. In this window, do the following:
    a. Select library. (SEAD_PDK_90).
    b. Select Cell. (nmos4t).
    c. Select view. (Symbol).
    d. Name the instance (N1).
    e. Move the cursor to your workspace and click.
    f. The window will stay opened.
    g. Repeat steps (3a-3g) but select (pmos4t) and name it (P1), click cancel to close.

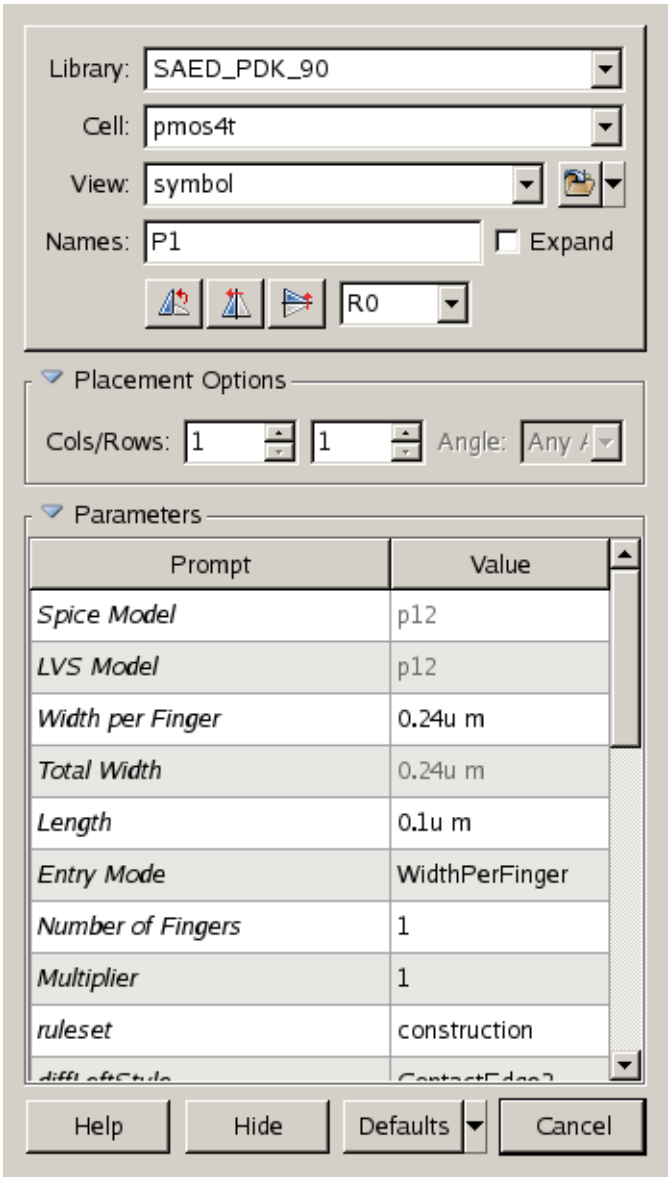

Figure 11 : Adding instance window.

Press (f) on your keyboard. This will fit the view on the parts you placed. Your workspace will look like the one in fig (12).

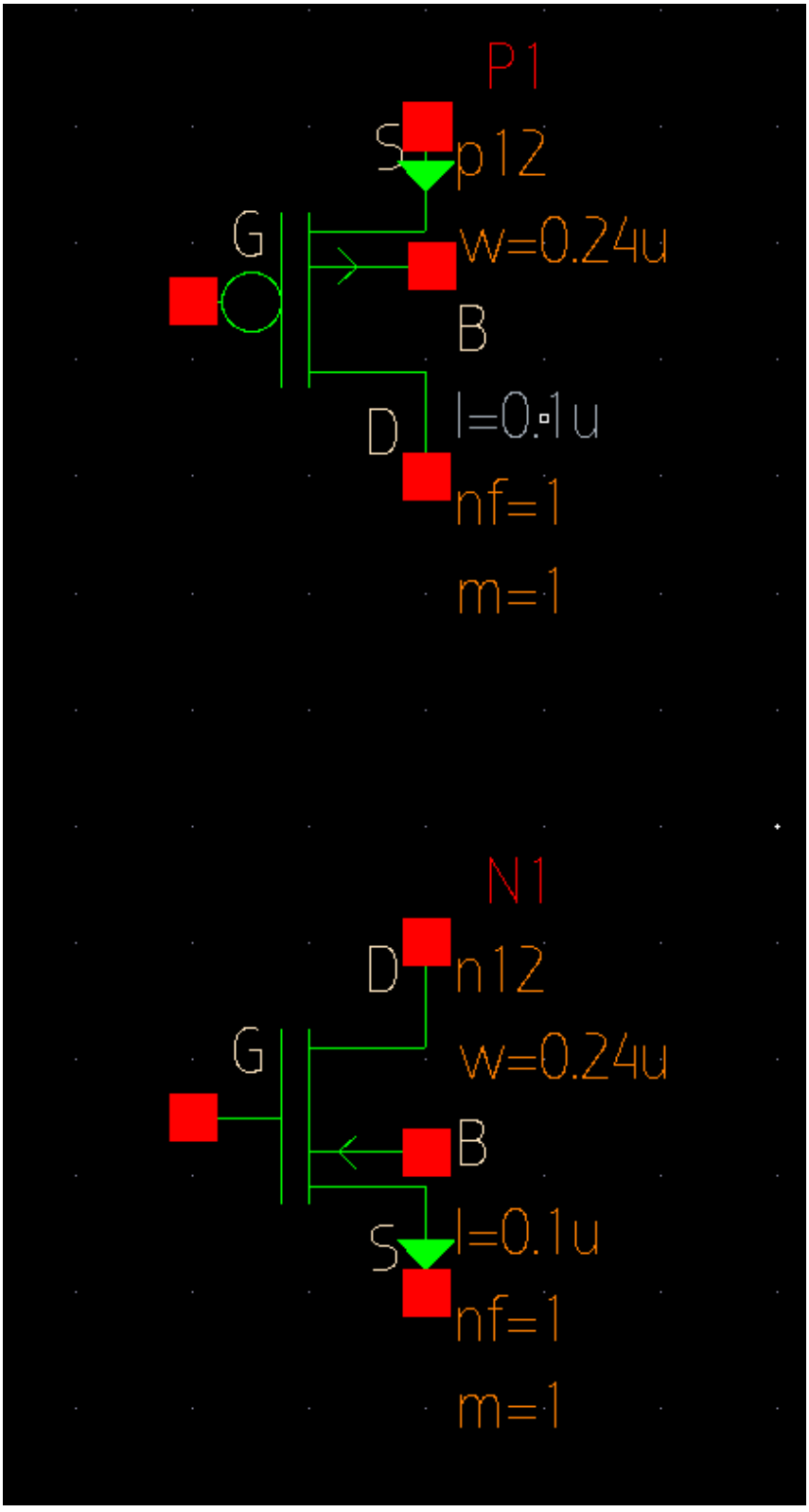

Figure 12 : work space.

Now, you need to connect the instances (transistors) to each other to form the schematic in fig (10):

1. Move the cursor to the red square at the instance terminal you want to connect.

2. Click and Hold the mouse button.
3. Move the mouse to the other terminal you want connected.
4. Release the button.
5. To add a wire to connect wires, go Add > wire
6. Connect wire.

Add pins to the schematic to define the terminals.

a) Go to , Add > Pin or
b) Ctrl+P

Pins can only be placed on wire ends. When placing a pin after selecting it from the top menu, the bar in fig (13) will appear at the top of the workspace.

Figure 13 : PIN properties bar.

Fill the information you need under each field (name, pin type, and its orientation).

Last step before getting the final result is to name the wires and nodes. Use tool #3 in fig (8).

Your workspace should look like that in fig (14) which is an inverter cell schematic view.

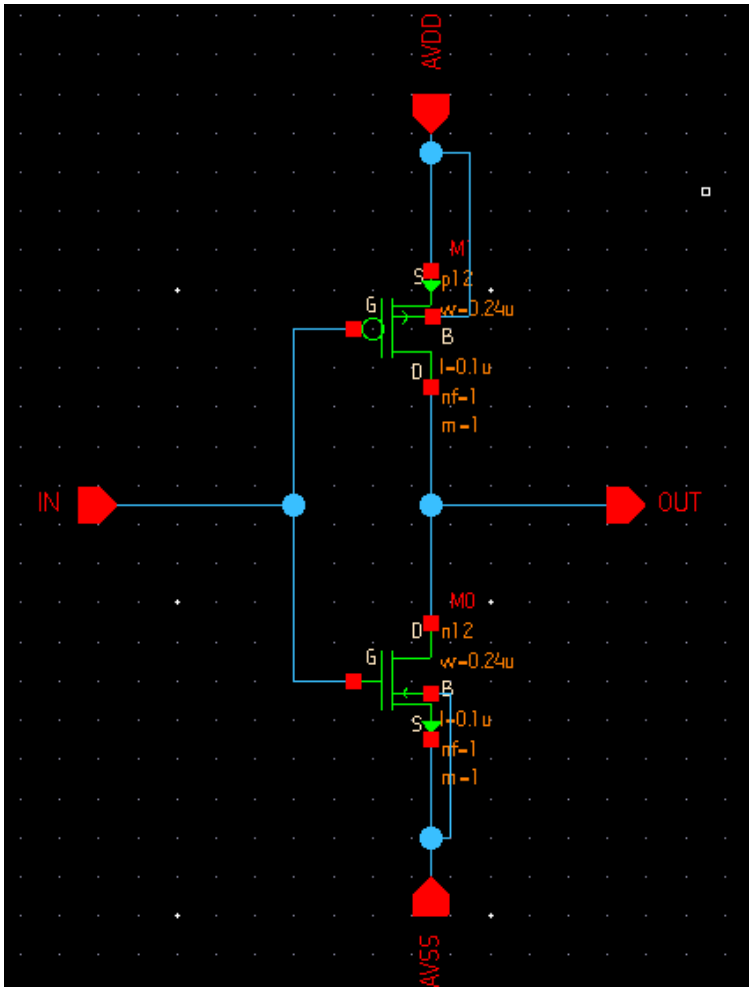

Figure 14 : workspace view.

Now we need to create a symbol view for the inverter, so we can use it as single instance in future designs. While you are in the schematic view, go to *Design menu > New cell view > from cell view*, the screen in fig (15) will pop up.

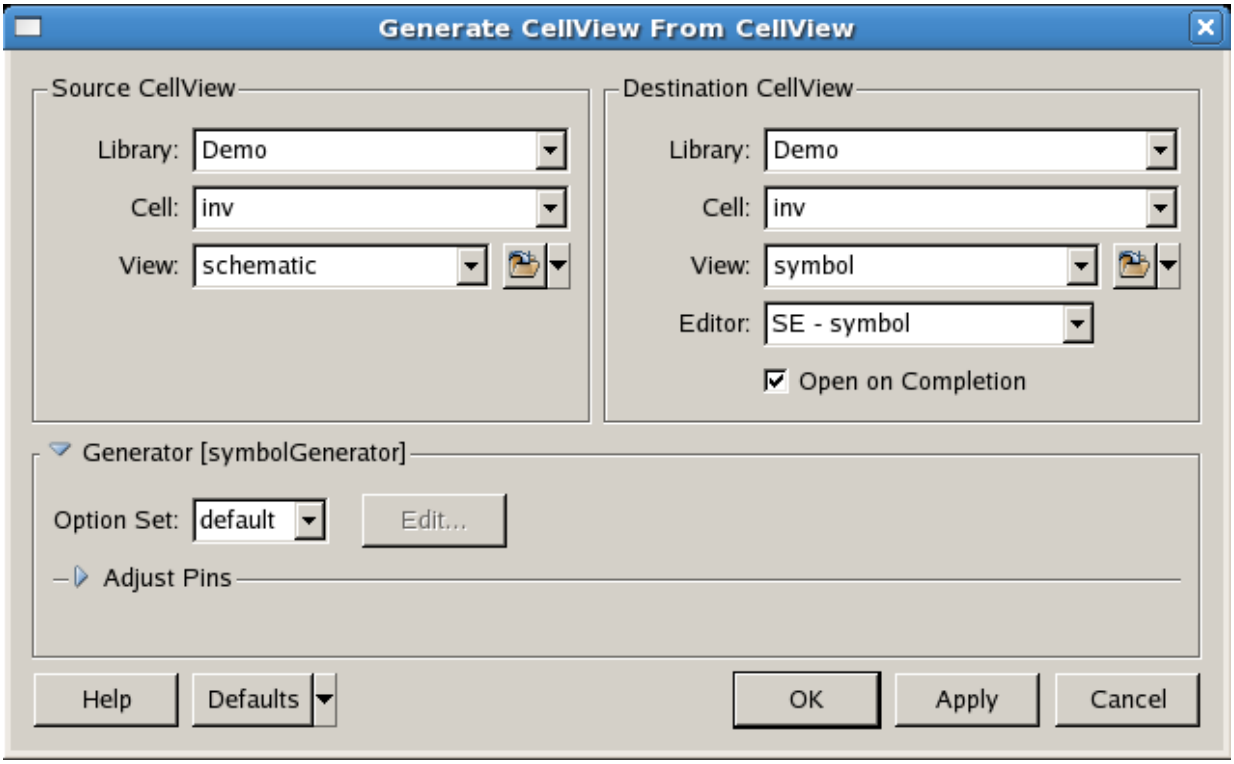

Figure 15 : create symbol cell view from schematic cell view window.

The form is filled by defaults with include the current schematics. By clicking OK, the symbol editor window will appear as in fig (16). The shape of the symbol can be modified.

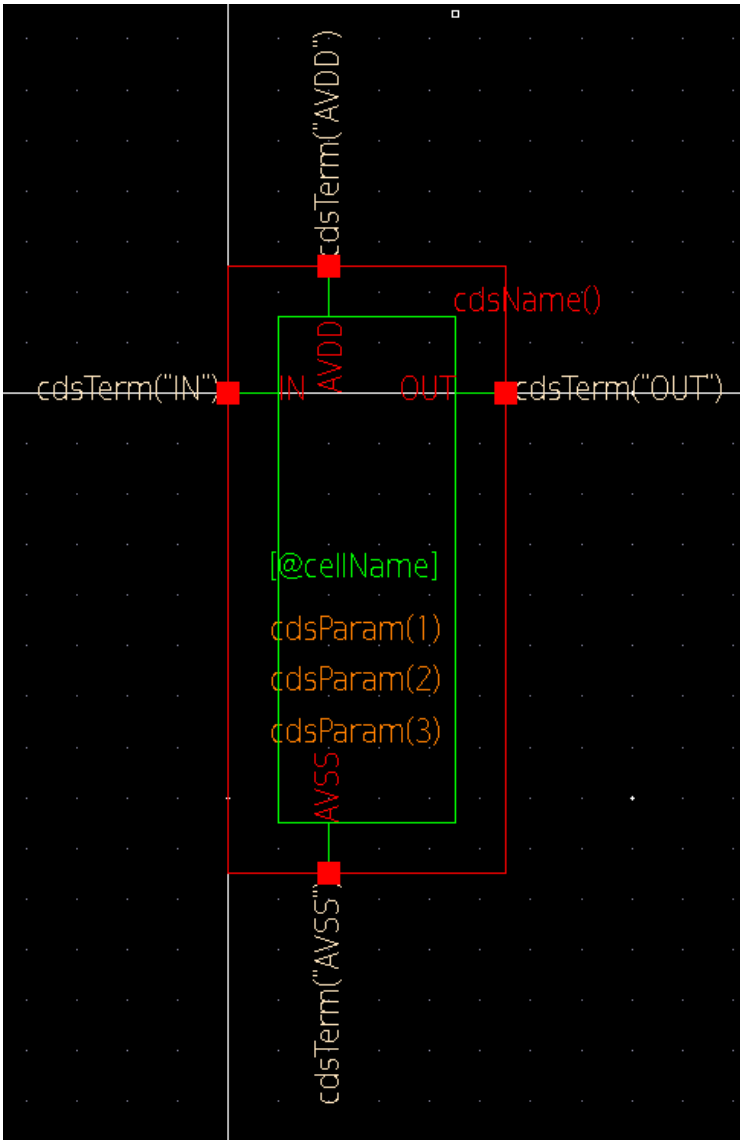

Figure 16 : Symbol editor window

In fig (17), you can see your cell with all views under it, including the new one (symbol view).

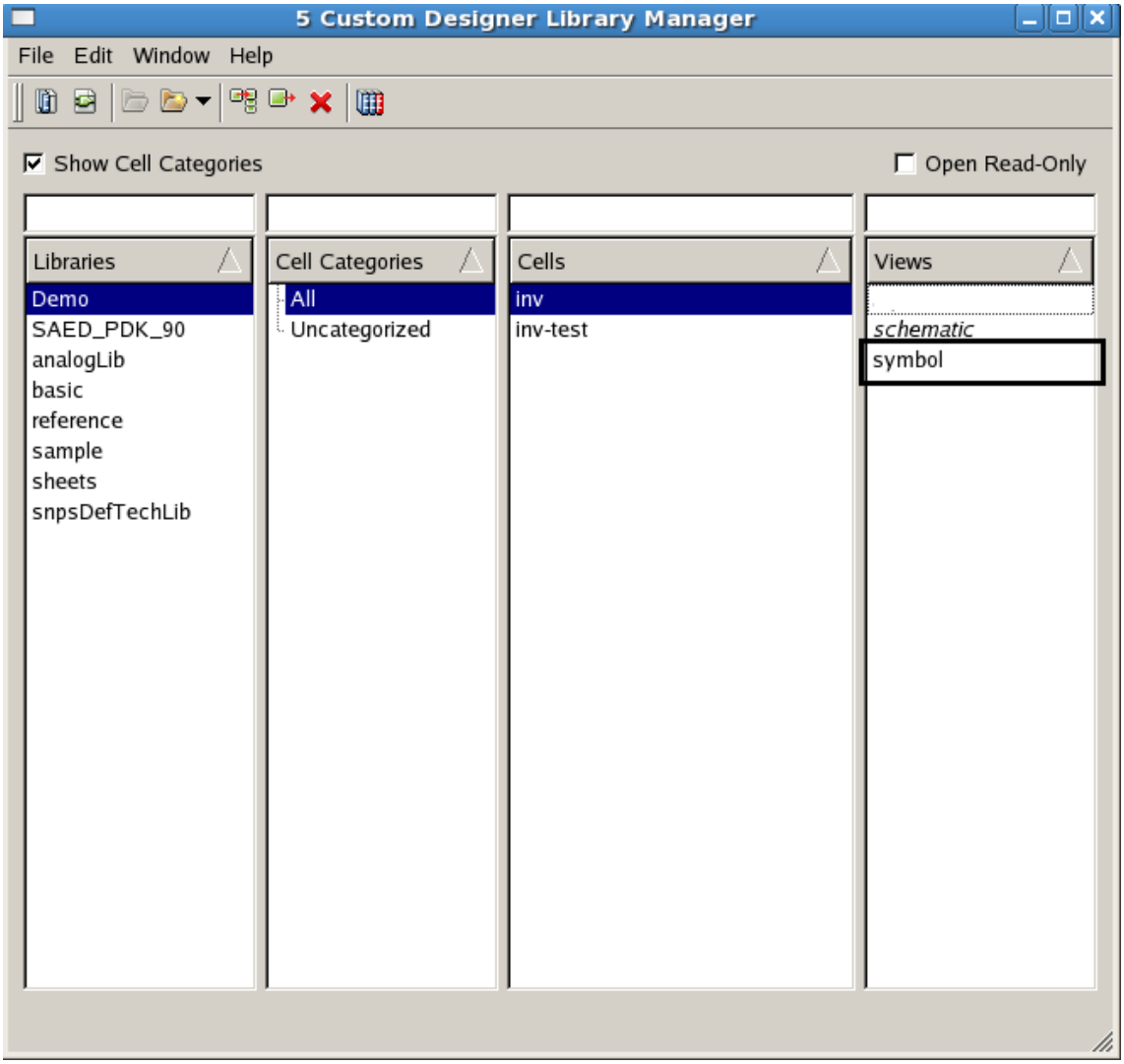

Figure 17 : library manager window.

To create a test bench where all inverter cell can be simulated, use the steps below:

1. Create a new cell view called "**testbench**"; this will be your sandbox. Use the schematic view.
2. Place the **inv** instance inside it. This is the same cell you created under **VLSI_HW** library.
3. From the **analoglib** add:
    a. **CL**,
    b. **Vsource**.
    c. **Vpulse**

Your workspace should look like that in fig (18).

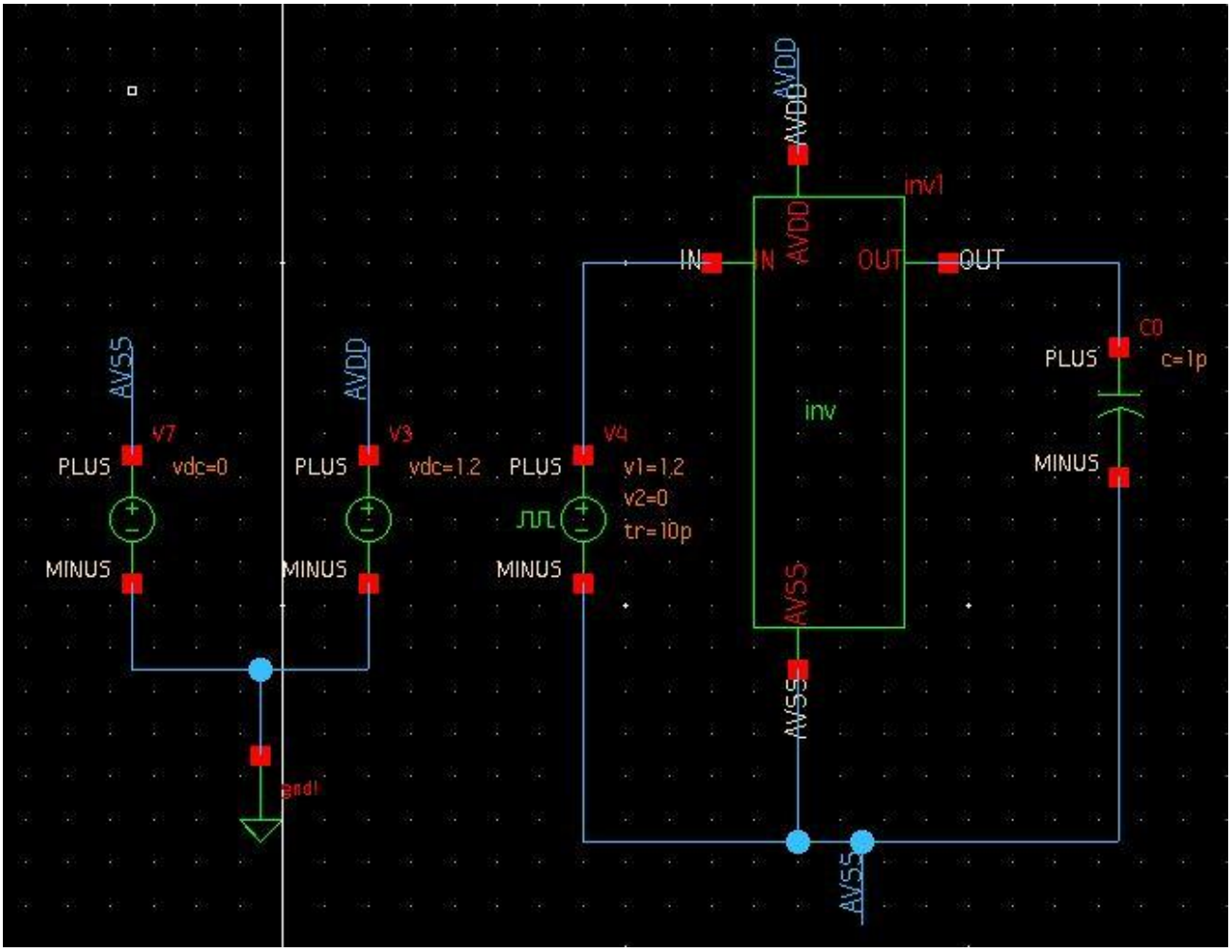

Figure 18 : Testbench workspace

Schematics entry is finished and the design is ready for simulation.

USING SAE "Simulation & Analysis Environment"

We need to run two types of simulation on our design:

a) DC sweep analysis. (dc)
b) Transient Analysis.(tran)

To run SAE, go to *Tools menu > SAE*. This will launch the window in fig (19), which consists of three main parts.

1. Design Variables section.
2. Output Section. (Choose the variables to be displayed after simulation).
3. Enabled analysis for this test bench.

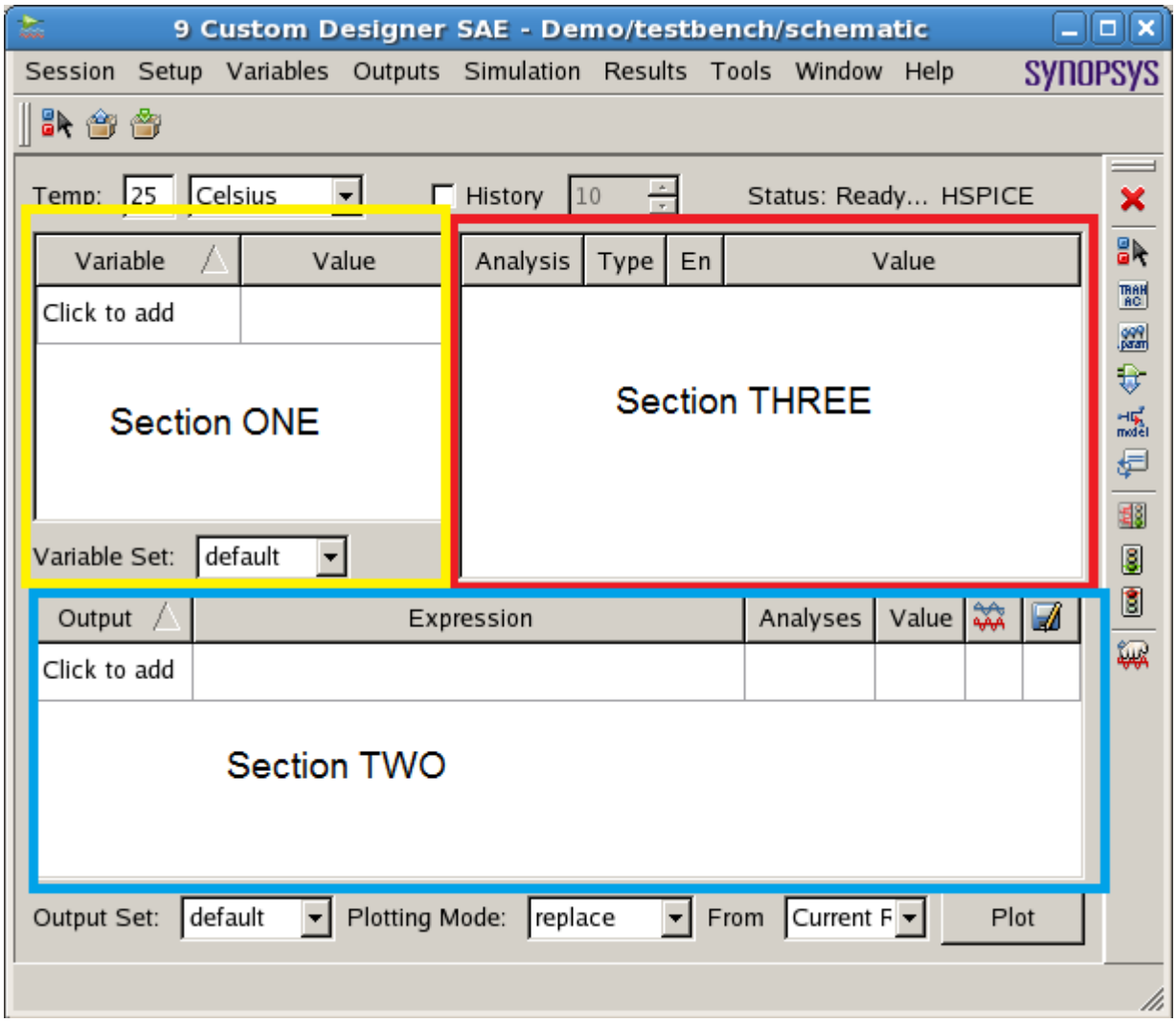

Figure 19 : SEA main window.

The bar on the right contains the short cuts for the most commonly used commands in **SAE.**

To set up simulation options:

1. Choose the appropriate Models for you instances.(transistors)

a. Go to *Setup* > *Models Files.*
b. See window in fig (20).
c. Click in section one. Use the file browser to determine the directory of your models library file. (In the example, you will find it under >> *work/90nm /hspice/*.lib)*
d. In section two chose your transistor corner type (i.e. TT,FF,SS,SF and FS). Pick TT_12.
e. Click OK.

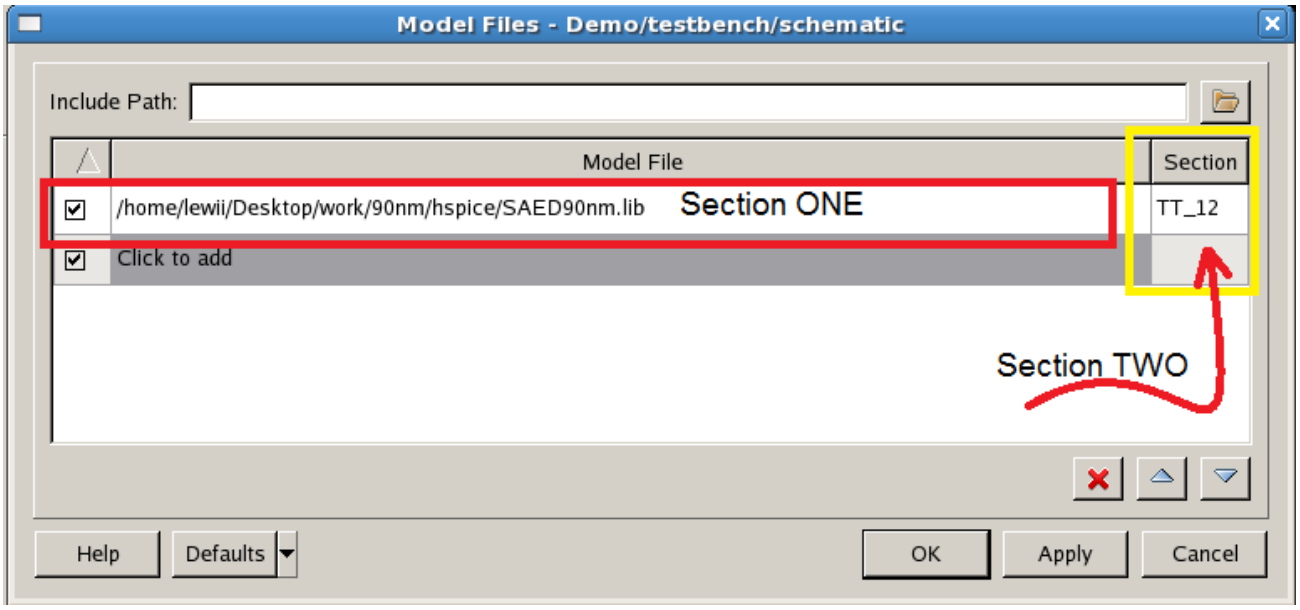

Figure 20 : Models Include Window.

2. To select the analysis type:
   a. Go to *Setup* > *Analysis*, window in fig (21) will appear.
   b. Stay in the *General* tab.
   c. Select **tran. (**For transient analysis).
      i. Fill the option like the ones in fig (21). Where :
      ii. Start Time = when the simulation begins.
      iii. Time Step = when to recalculate the variables.
      iv. Stop Time = when to stop your simulation.
   d. Now check the box at the lower left corner.
   e. Click **Apply**.
   f. Select **dc.** (For DC sweep).
      i. Fill the option like the one in fig (22). Where:
      ii. Sweep Variable = the variable you want to change. (Select **Source**)
      iii. Sweep type= describe the relation between sweep points.
      iv. Start = min value for the variable.
      v. Stop = the Max value for the variable.
      vi. Step size= the difference between each two reading.
   g. Now check the box at the lower left corner.
   h. Click **OK**.

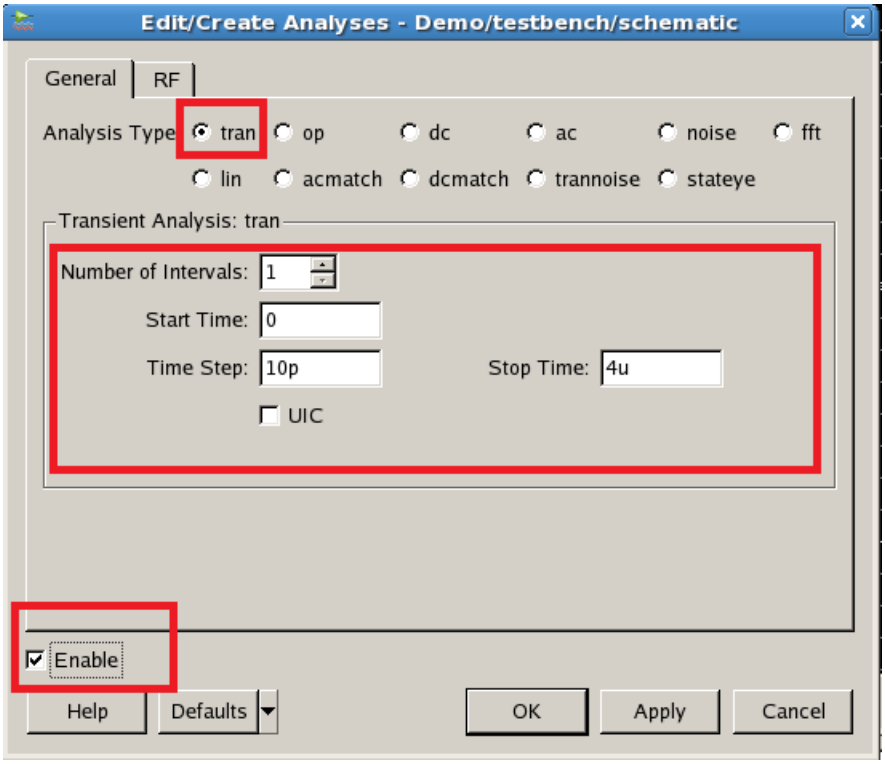

Figure 21 : Transient simulation window.

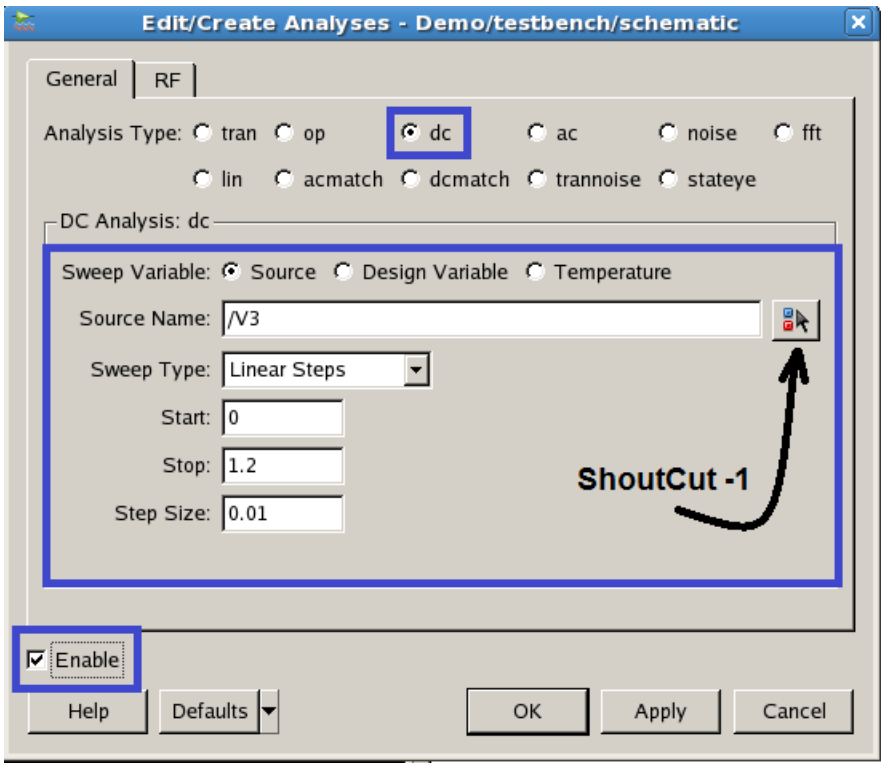

Figure 22 : DC simulation window.

3. The following step is to choose the desired simulations results. In section TWO in fig (19), do the following steps:
    a. Click under output field, and write the name for a specific output variable.

b. Click under expression column and choose the node from the schematic, or write an equation that uses the values of some nodes in that schematic.
c. Under analysis, just check the simulation option. Select the one that applies for this variable. (For now select both of them **dc** and **tran**).

4. Save your simulation option by going to *Session* > *save state*, select *Openaccess* from the main three options at the top. Then name the state without any spaces in the name. See fig (23).

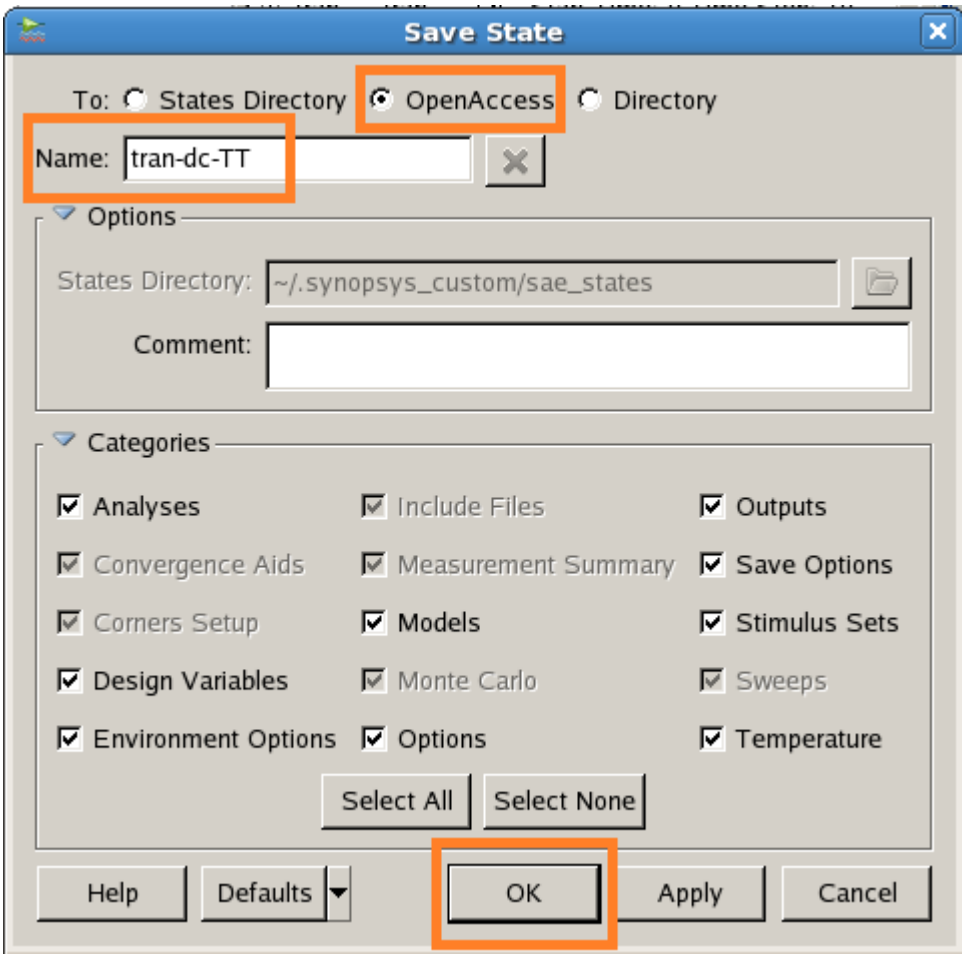

Figure 23 : Save Stat window with the options.

To run the simulation as shown in figure 24,

1. Go to *Simulation* > *Netlist and Run*, in the main window of **SAE**.
2. Simulation time depends on the complexity of the design.
3. A Wave View program window will appear which contains the graphs for the output variables you specified.
4. At the lower left corner, there are two tabs. (dc and tran)
5. See fig (25) for the **tran** tab results.
6. See fig (26) for the **dc** tab results

At this point, you have created a schematic cell and ran a DC and transient simulation. Congratulations. ☺.

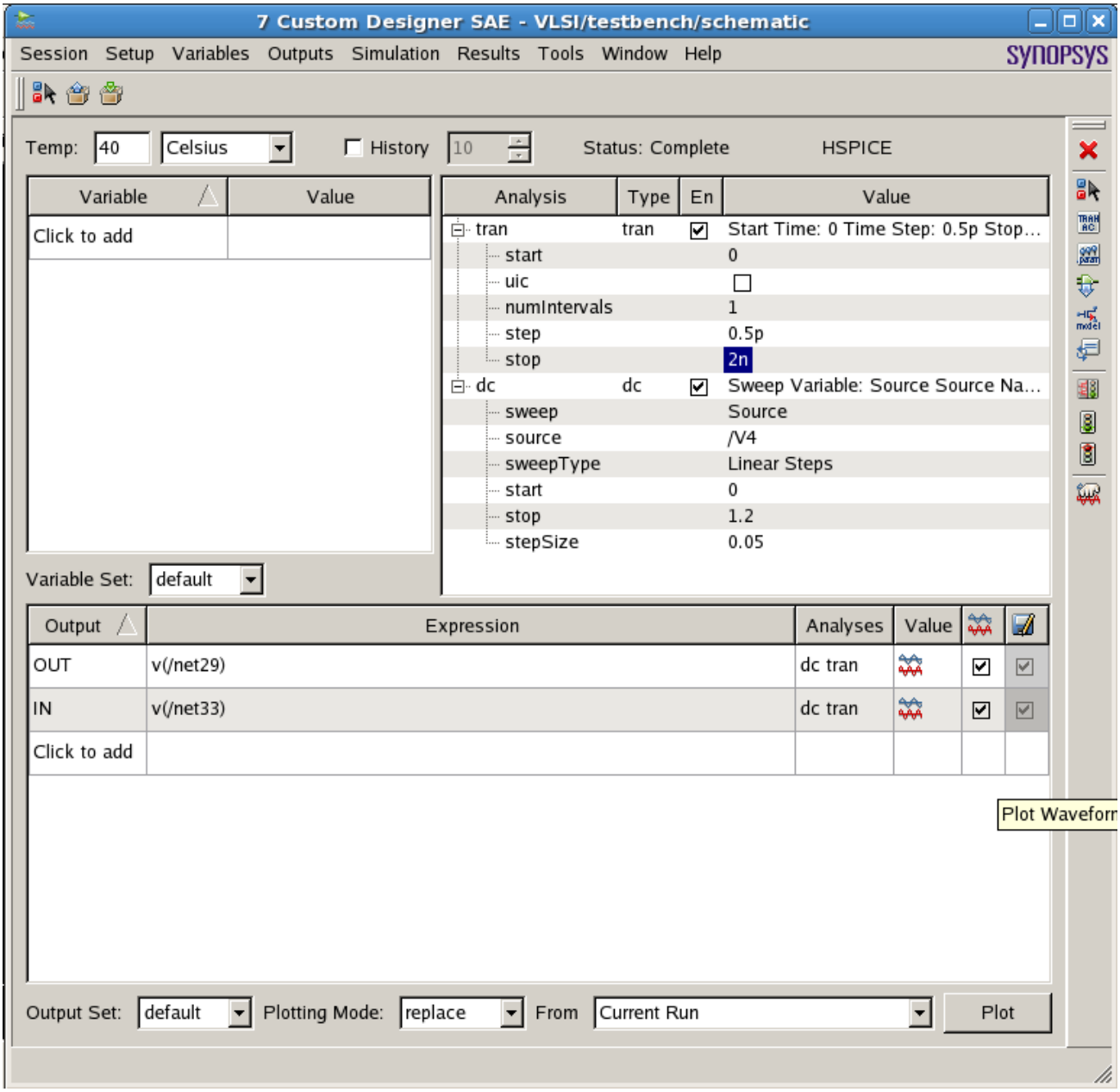

Figure 24 : SAE window with all options selected.

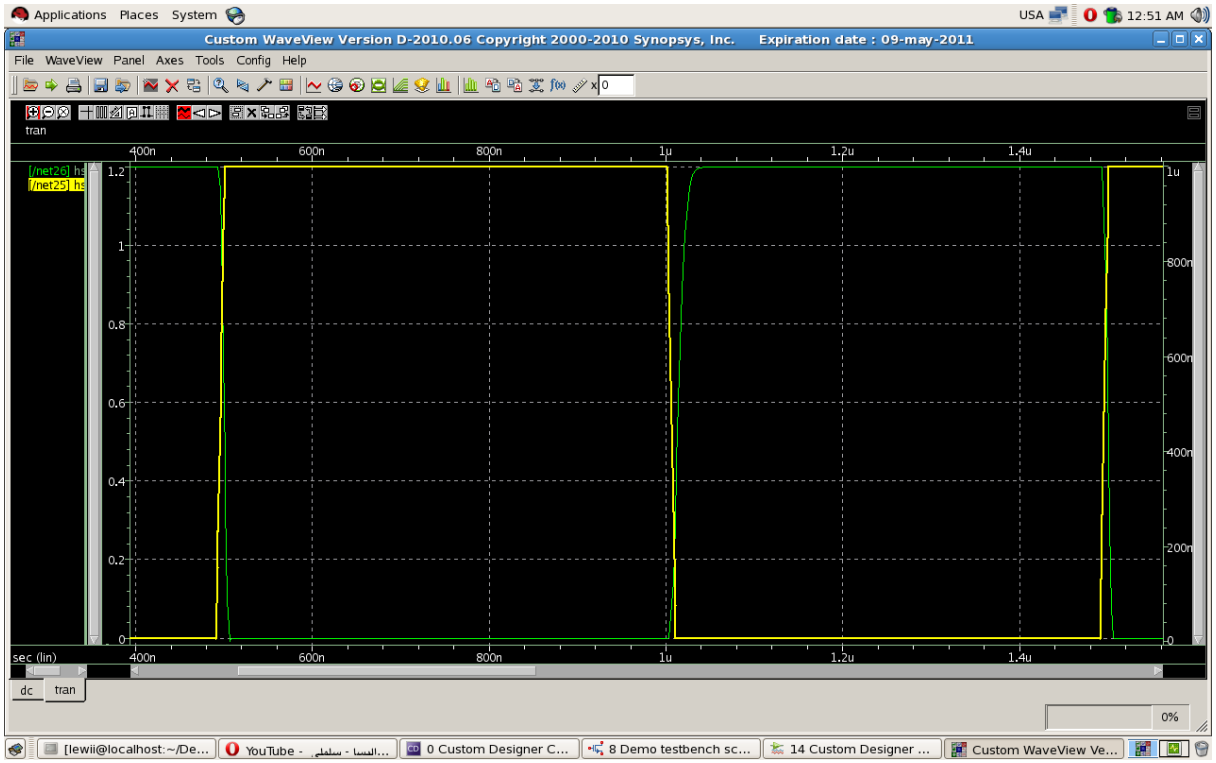

Figure 25 : Transient analysis tab.

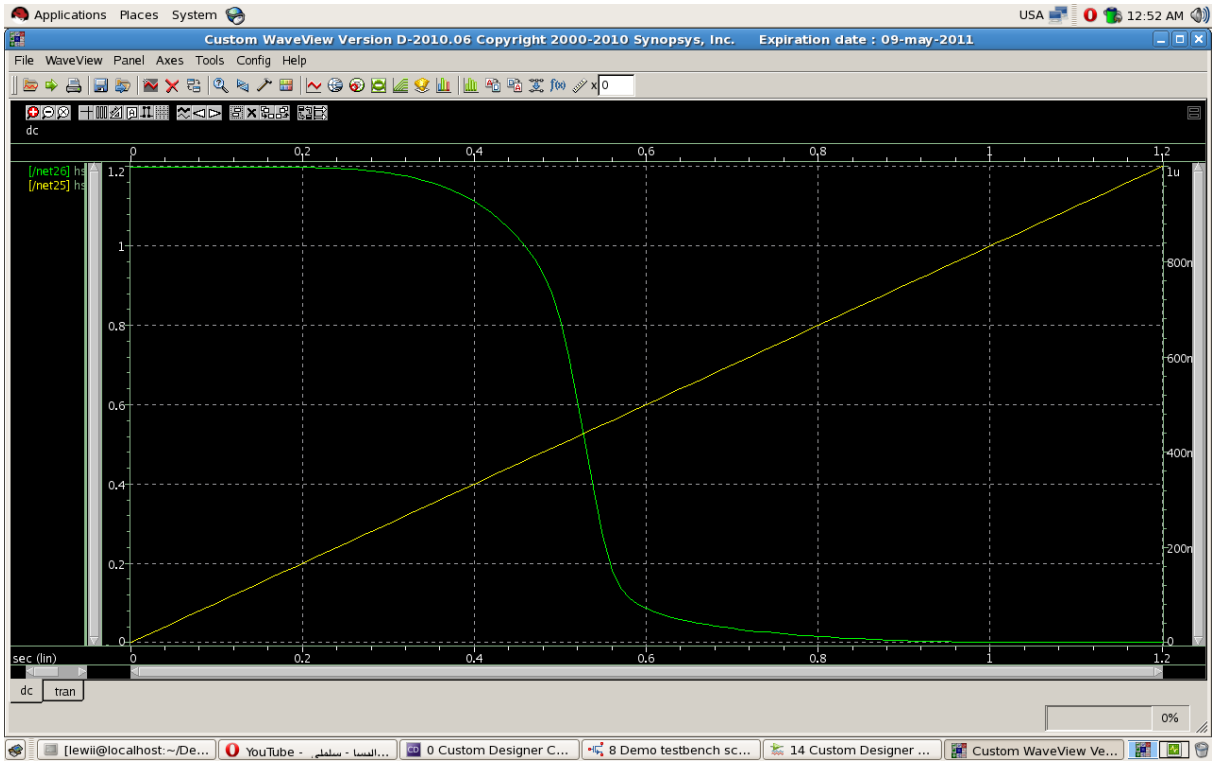

Figure 26 : DC sweep analysis tab.

Layout Editor

In the previous sections, you finished creating and simulating a CMOS inverter cell. You created a schematic and symbol view for the cell.

In this section, we are going to create a layout view for the same inverter. Go to ***Custom Design*** menu. Create a new cell view after selecting the library and cell (i.e. CMOS inverter cell), select layout view. Click OK and you will get a new window like that in fig (27) which is the main window of the layout editor.

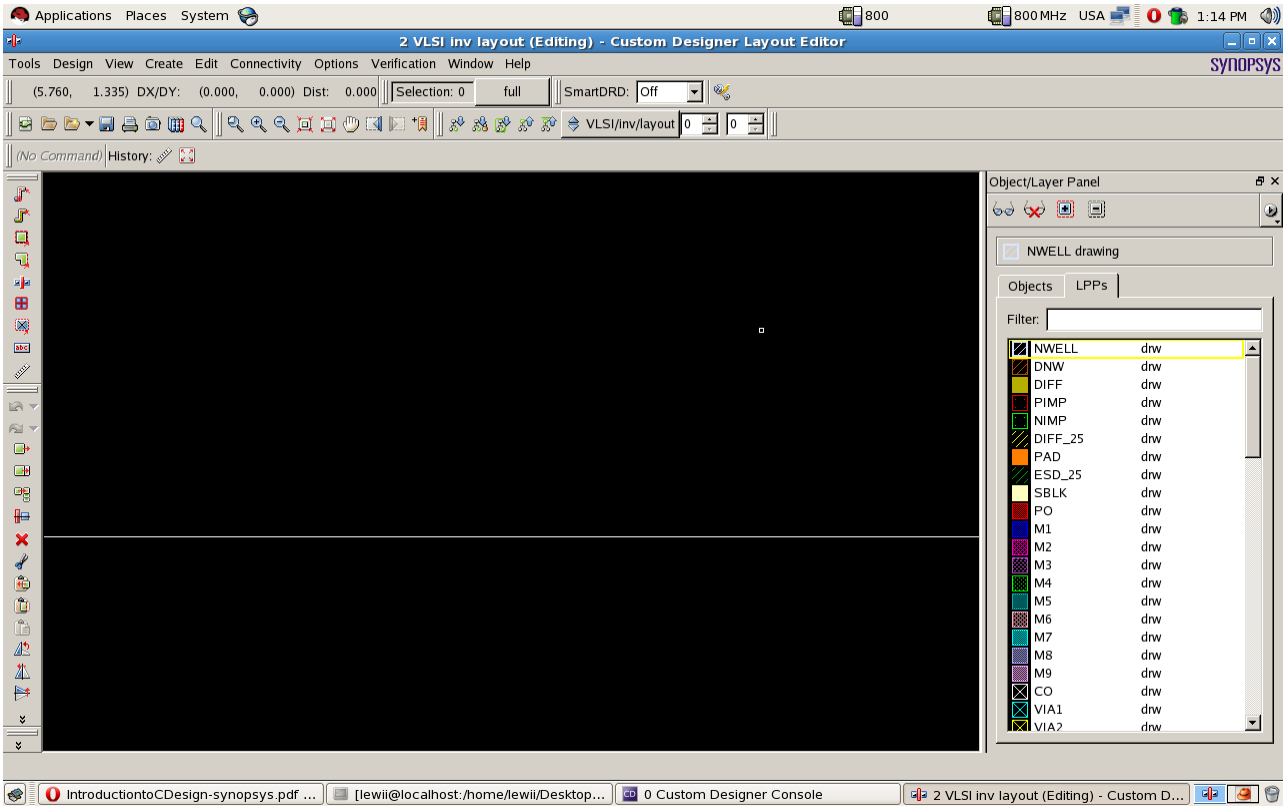

Figure 27 : Layout editor main window.

Like the schematic editor, we have the shortcut bar to left of the window, see fig (28). The object/layer panel on the right side of the window, see fig (29). All the layers that can be used in the design are included in that panel.

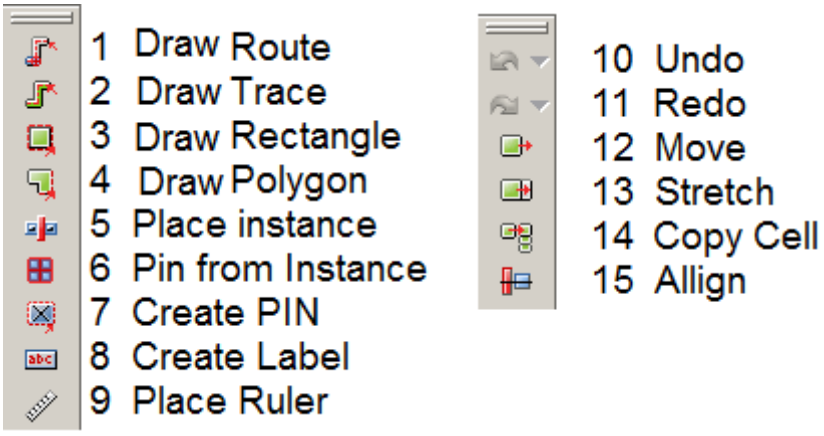

Figure 28 : Layout Shortcut Bar.

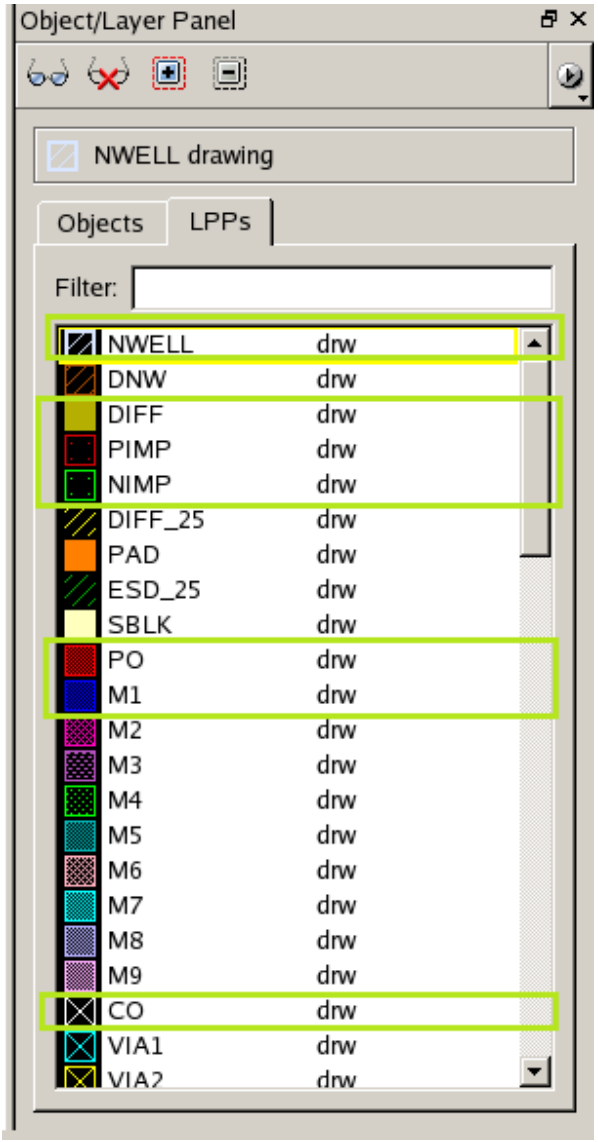

Figure 29 : Object/Layers Panel

Layers marked inside the green rectangles, in figure 29, are the one we are going to use in this tutorial. The left portion is the color and look of the layer, the middle portion is the layer name, and the right portion ***drw*** indicates a drawing layer. The meaning of each layer is the following:

- NWELL = = is the N-type Well.
- DIFF = = Diffusion Layer.
- PIMP = = P-type Diffusion (to define the P-diffusion type)
- NIMP = = N-type Diffusion (to define the N-diffusion type)
- PO = = its polysilicon layer.
- M1 = = is Metal #1 layer.
- CO = = is contact layer.

Figure 30 is the finished layout of the inverter schematic done previously in the tutorial.

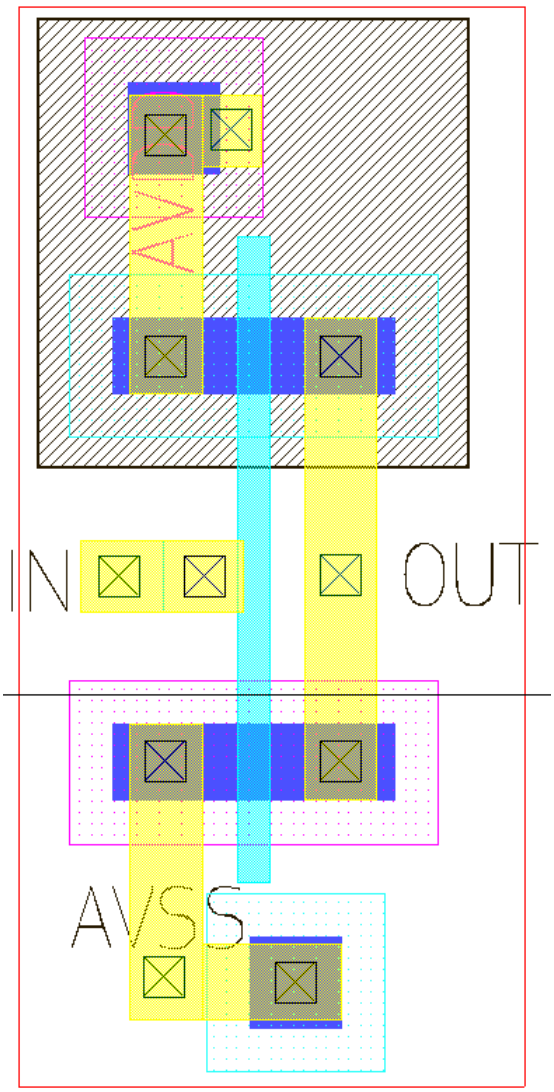

Figure 30 : Inverter Layout.

Steps of creating this layout are:

1. Go to *Create menu* > *Ruler.*
2. Measure the dimensions of the object you need to create. (Ex. Diffusion layer).see fig(31)
3. Now go to *Create menu* > *Rectangle.*
4. Select ***DIFF*** from the layer panel.
5. Draw it according to you measurements in step 2. See fig (32).

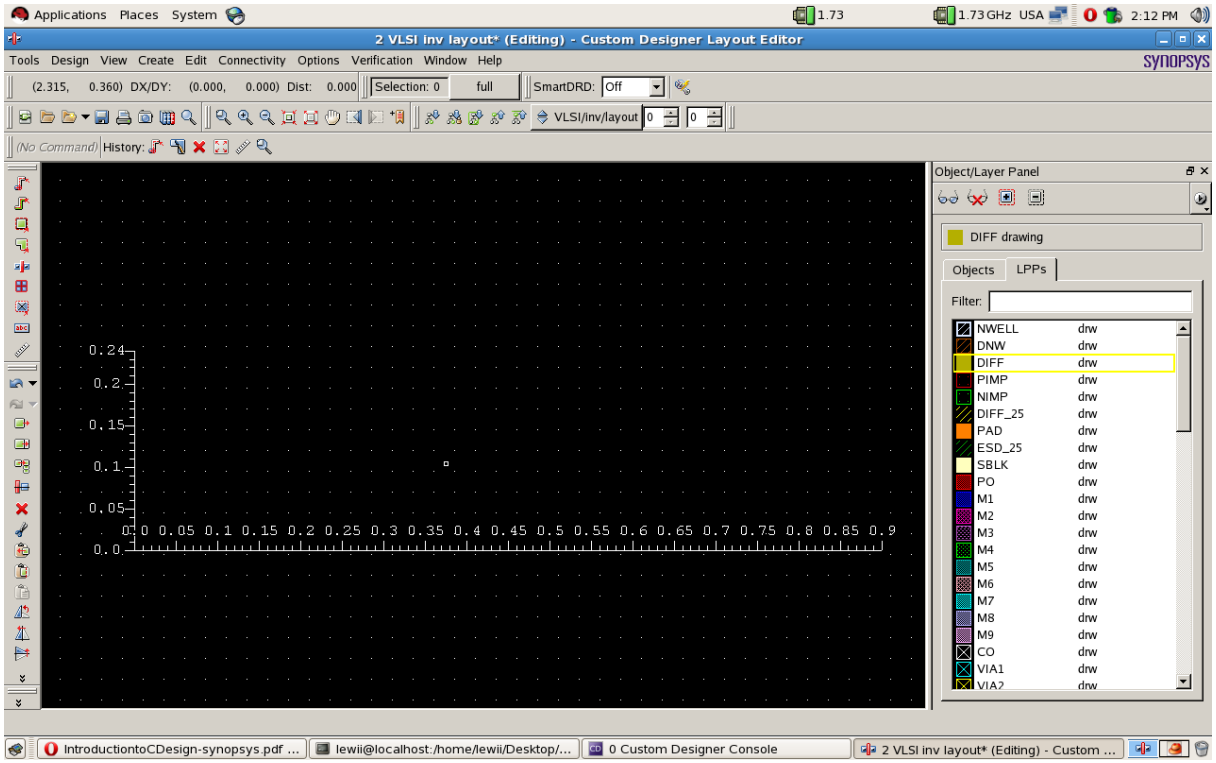

Figure 31 : Diffusion Ruler placement.

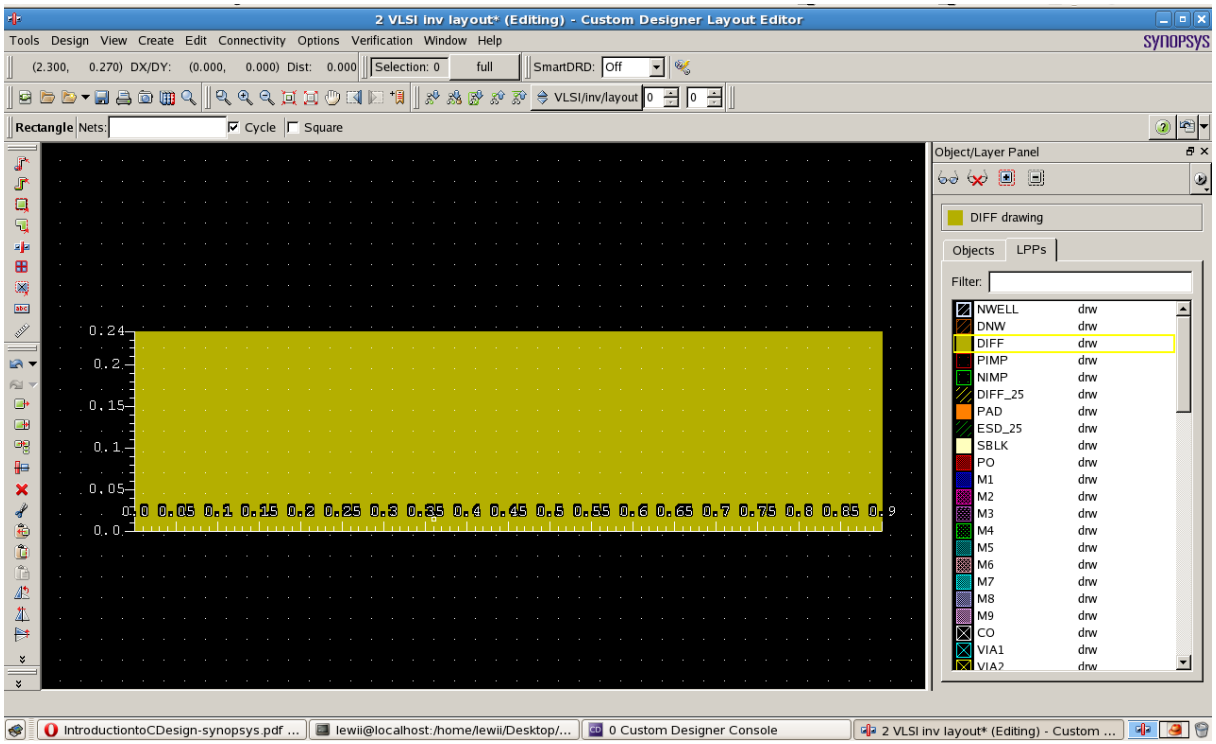

Figure 32 : Drawing Diffusion layer.

6. Select both rulers placed before and delete them by pressing the delete key on the keyboard.
7. Create a new ruler. Start at the upper left corner of the DIFF layer and measure (0.4um).
8. Now select ***PO*** (polysilicon) layer and create the gate as in fig (33).

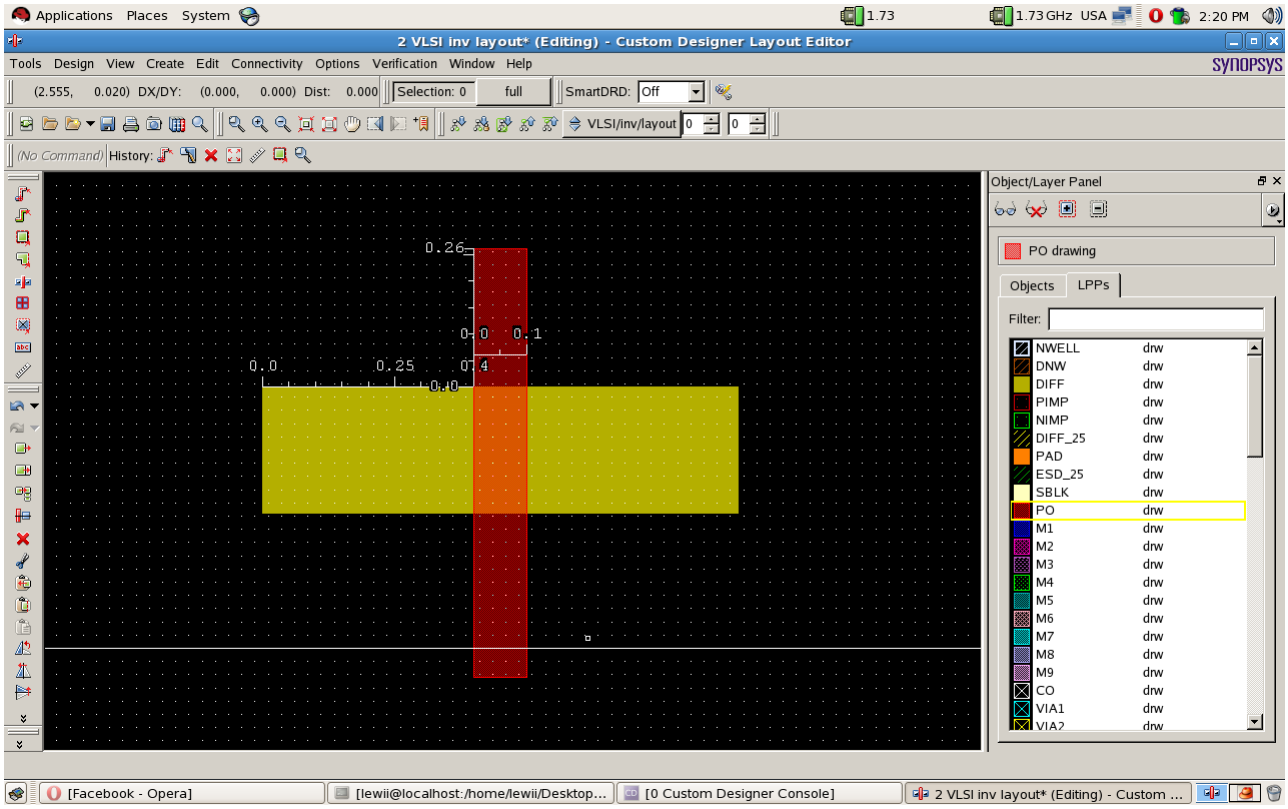

Figure 33 : Steps 6 to 10 results.

9. Create new rulers at the upper right angle and the lower left one, then create *PIMP* layer as shown in fig (34).
10. Draw an *NWELL* layer that encloses the *PIMP* layer with at least (0.1um). See fig (35).
11. Place Metal one layer (*M1*) at (0.05um) from the *DIFF* end with (0.23um) length and the same width as the *DIFF* layer. See fig (36).
12. Add Contact (*CO*) between *M1* & *DIFF* layers with the following dimensions, (0.13x0.13um), and a min enclosed by metal of (0.05um). See fig (37).

At this point we have a full PMOS transistor, repeat the previous steps to get an NMOS transistor, but take care of the layers difference between the two types. The NMOS transistor will not use NWELL and will replace the PIMP layer by the NIMP layer.

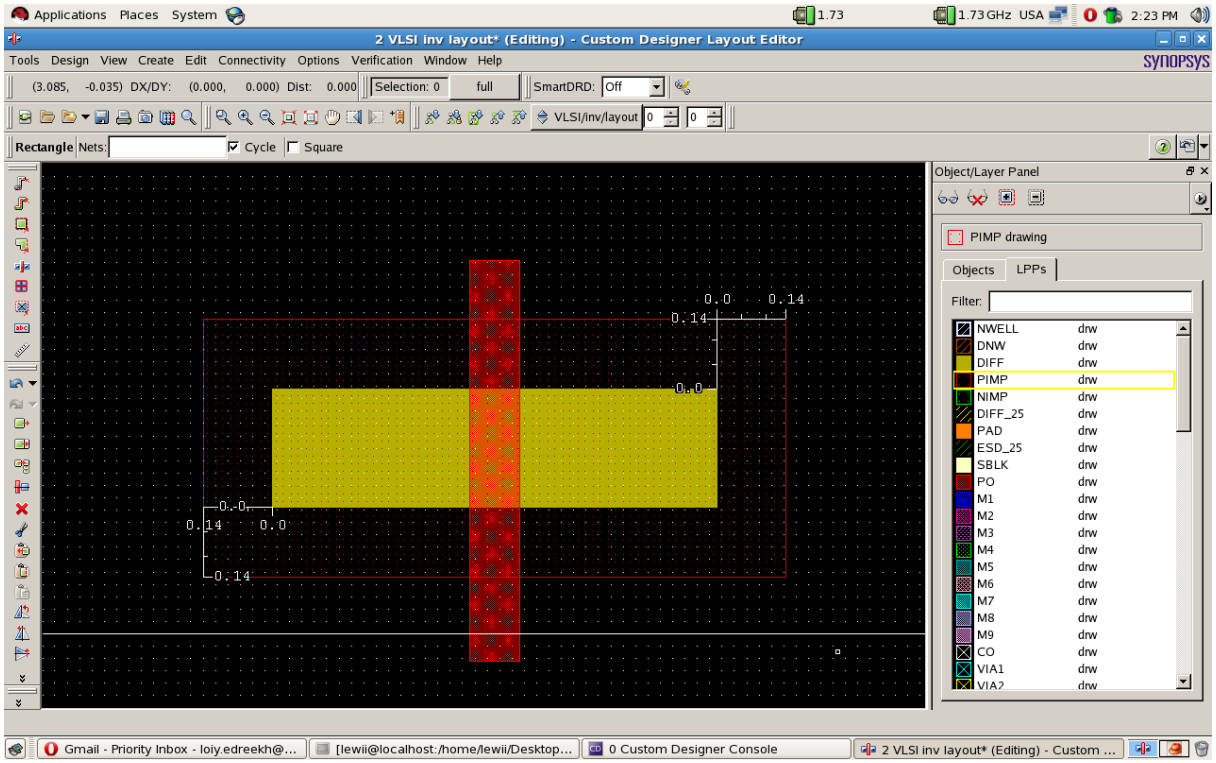

Figure 34 : PIMP Placement.

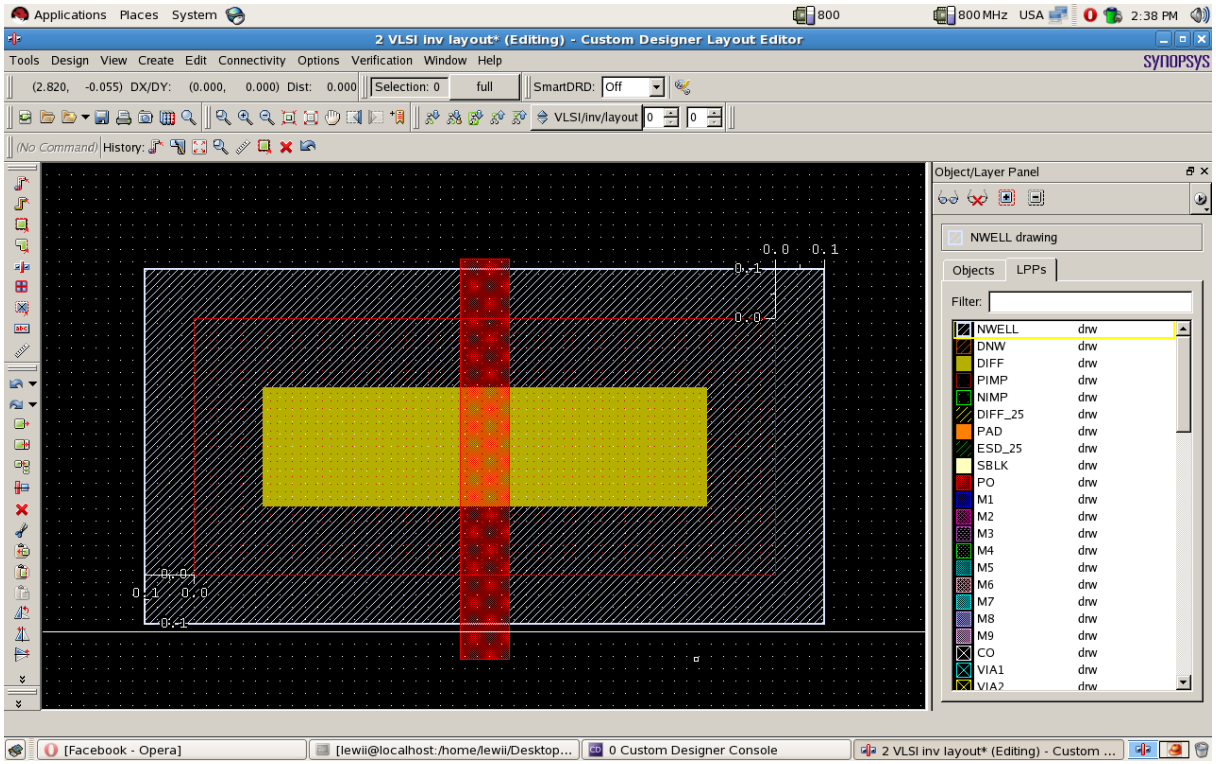

Figure 35 : NWELL placement.

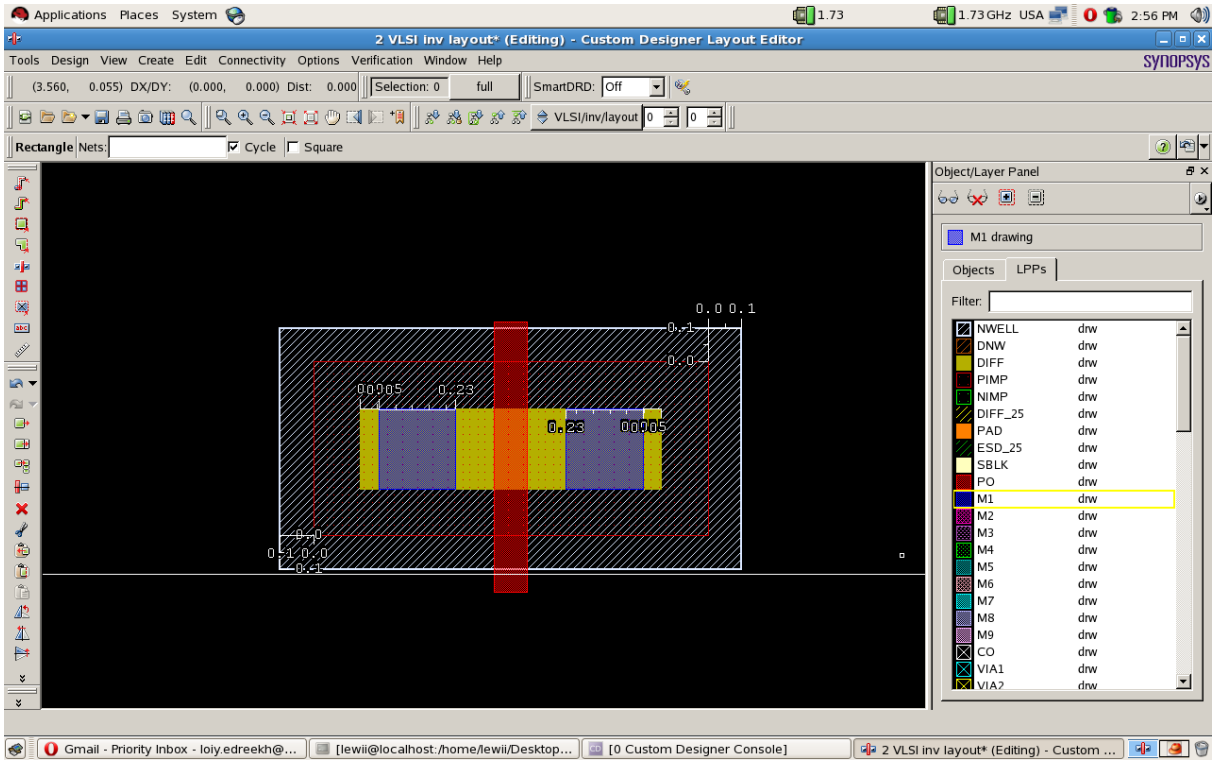

Figure 36 : Metal Placements.

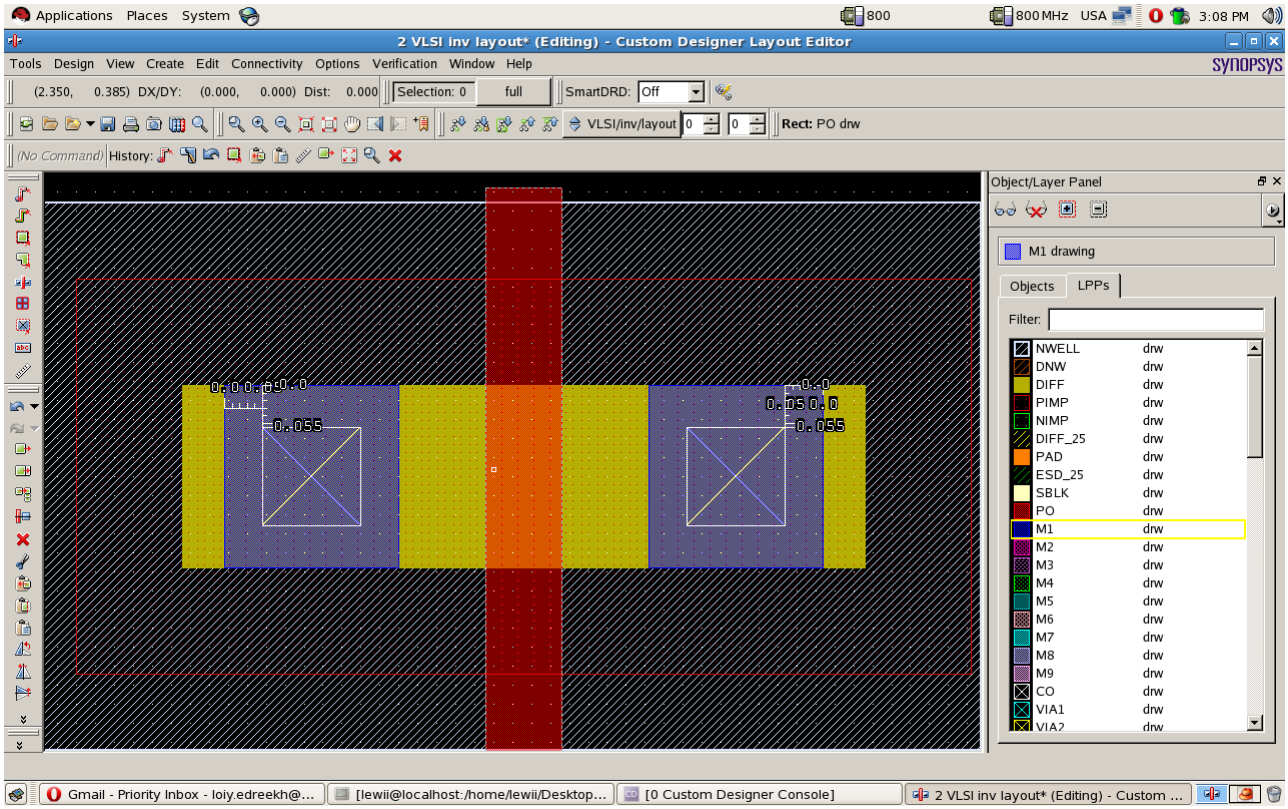

Figure 37 : CO placements between DIFF & M1 layers.

Layout Design Rule Check - DRC

To check that the layout does not violate design rules, follow these steps in the layout editor window:

i. Go to *Verification menu > DRC >Setup and Run.*
ii. A window like the one in fig (38) will pop up. This window is used to set the options for the DRC (Design Rules Check).
iii. Do not change the defaults.
iv. Define the path for the Runset file.
    a. Click the folder icon to the right of runset field.
    b. Browse to the directory of the file.
    /work/90nm/Hercules/drc/*.ev
    c. Click OK.
    d. You will see a screen like the one in fig (39).
    e. Go to customdesigner console window (main window, fig (2)). If your design is clean of errors, you will see a massage like the one in fig (42).

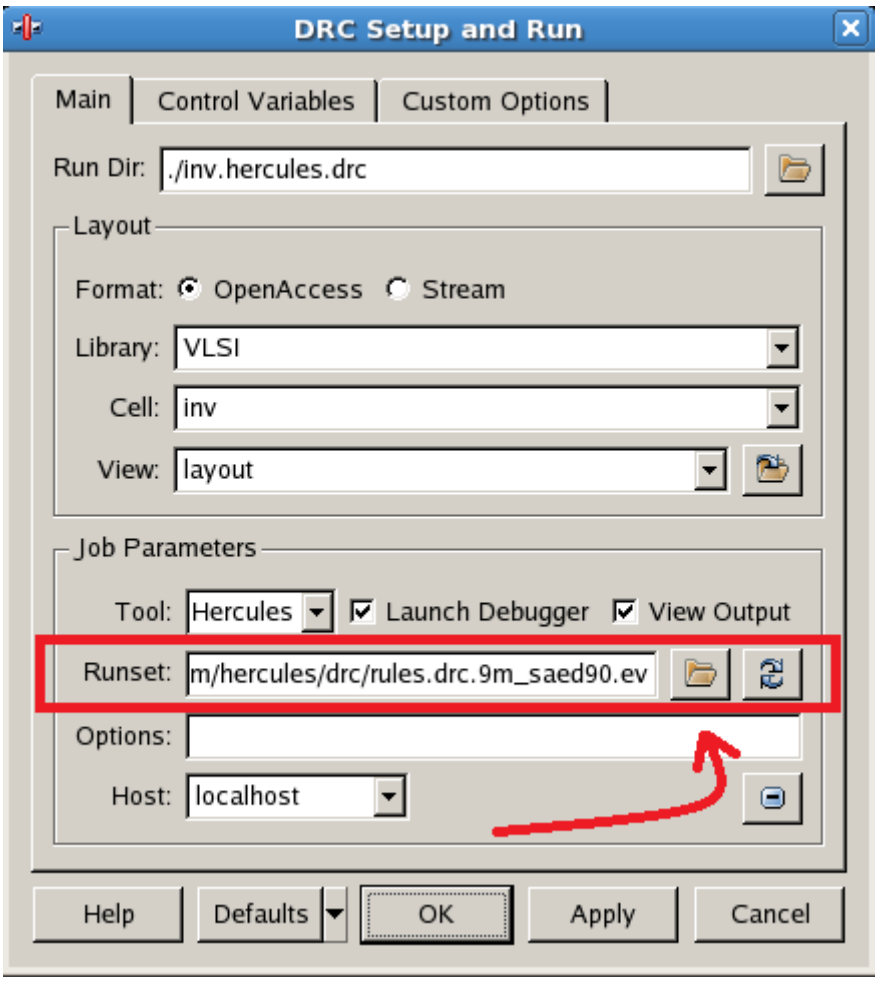

Figure 38 : DRC Setup and Run window.

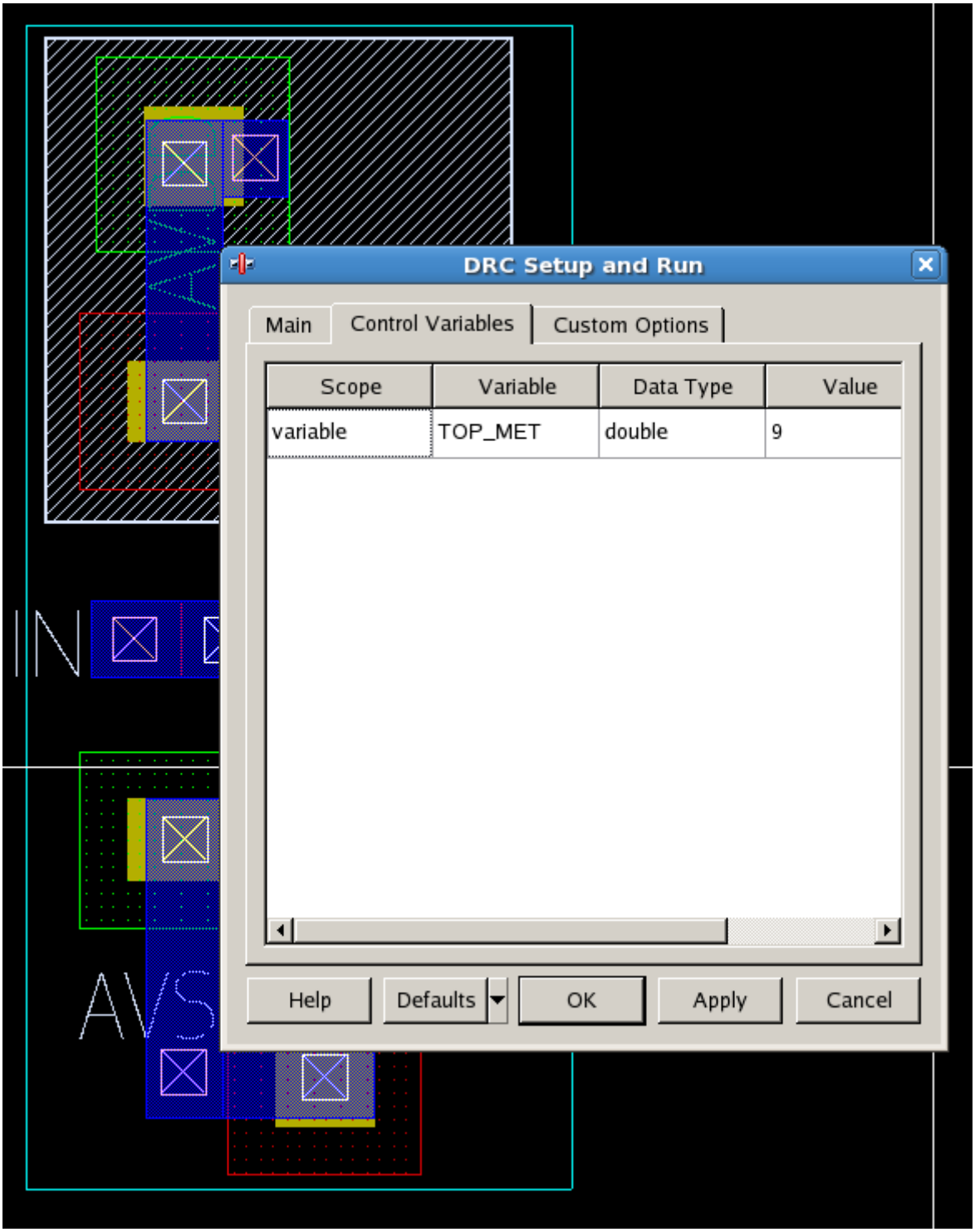

Figure 39 : DRC control variabel tab.

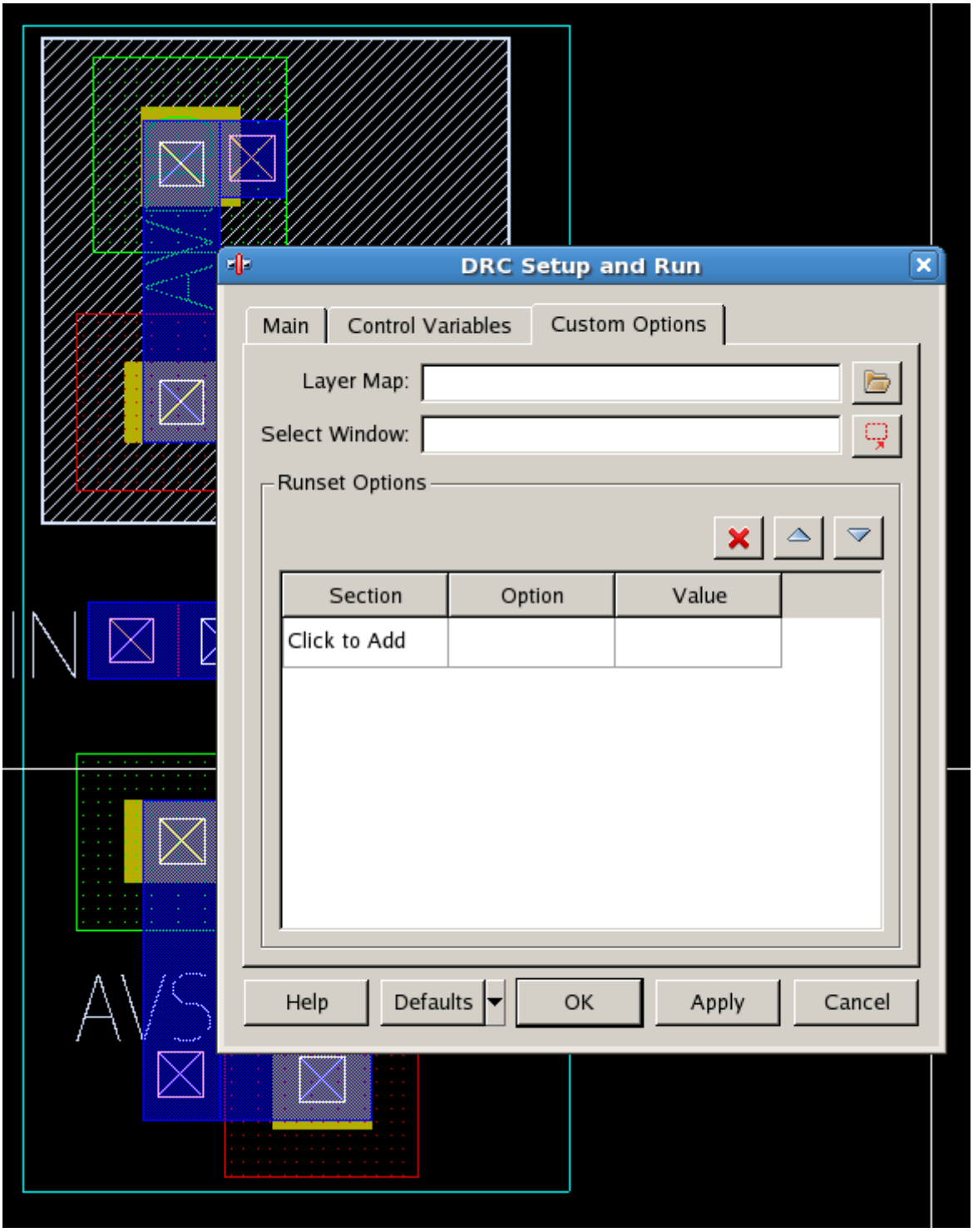

Figure 40 : DRC Custome Options tab

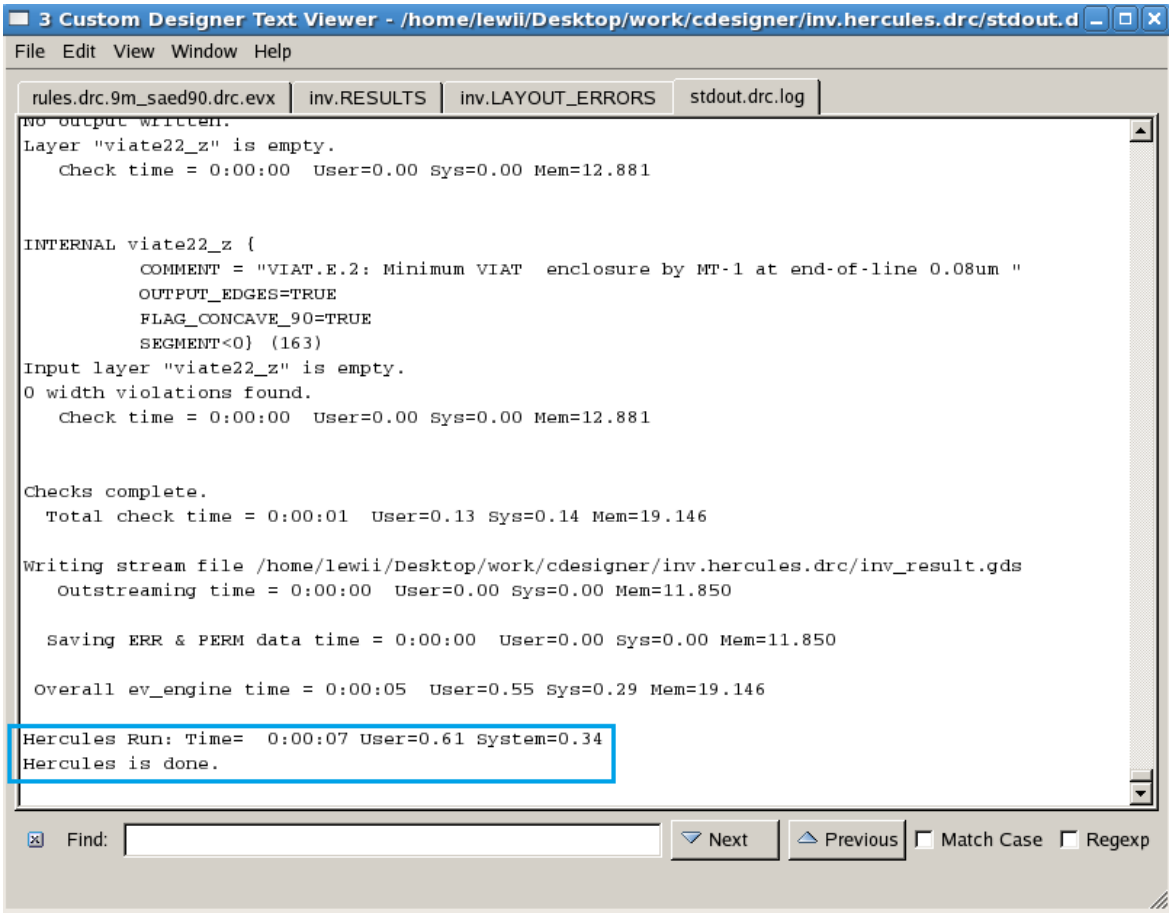

Figure 41 : Run log, results and errors viewer window.

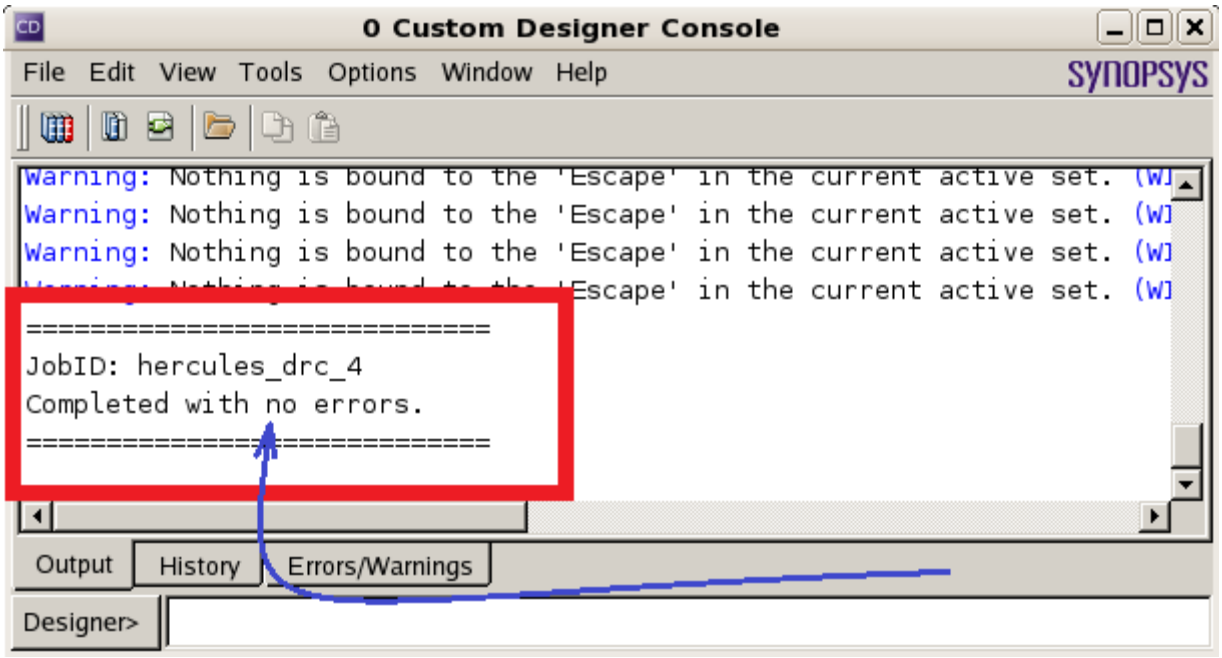

Figure 42 : Message in customdesigner console window.

f. If your design has layout violations, a window like fig (43) will pop up.

g. Figure 43 can also be obtained by going to *verification* > *DRC* > *Debug*. This window will give you a list of the errors in your design and will help you identify them by highlighting them as shown in fig (44) and fig (45).

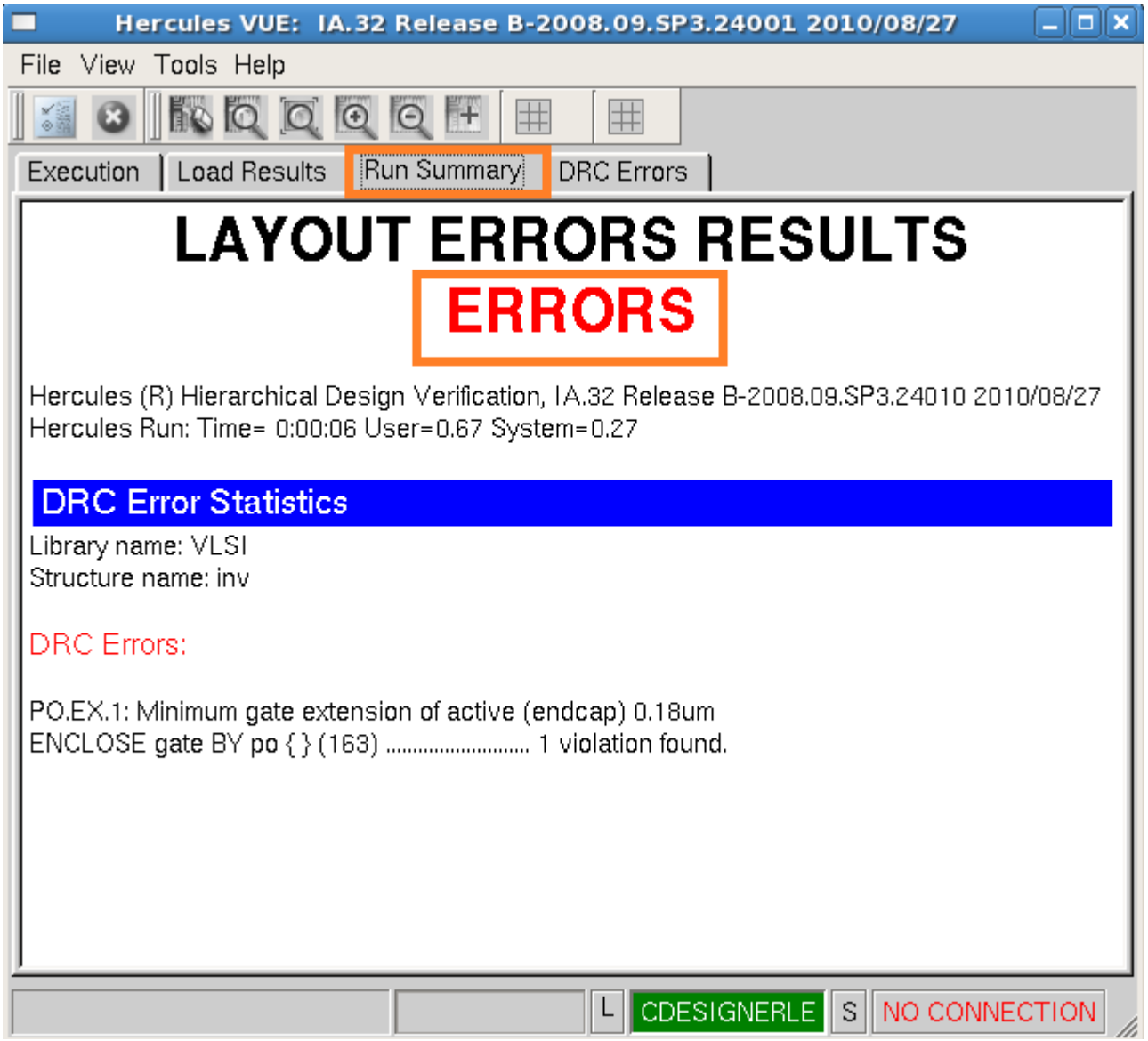

Figure 43 : DRC debug window.

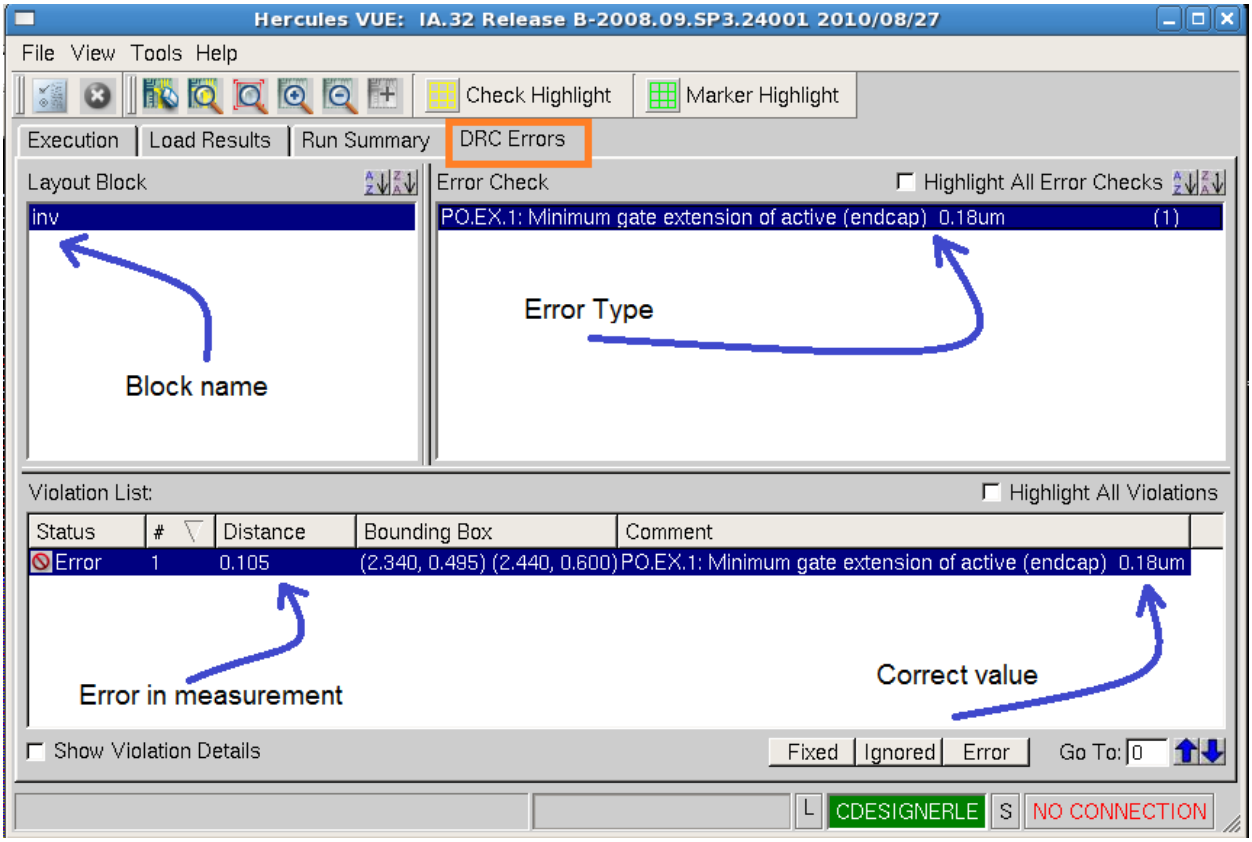

Figure 44 : Hercules VUE window, error details.

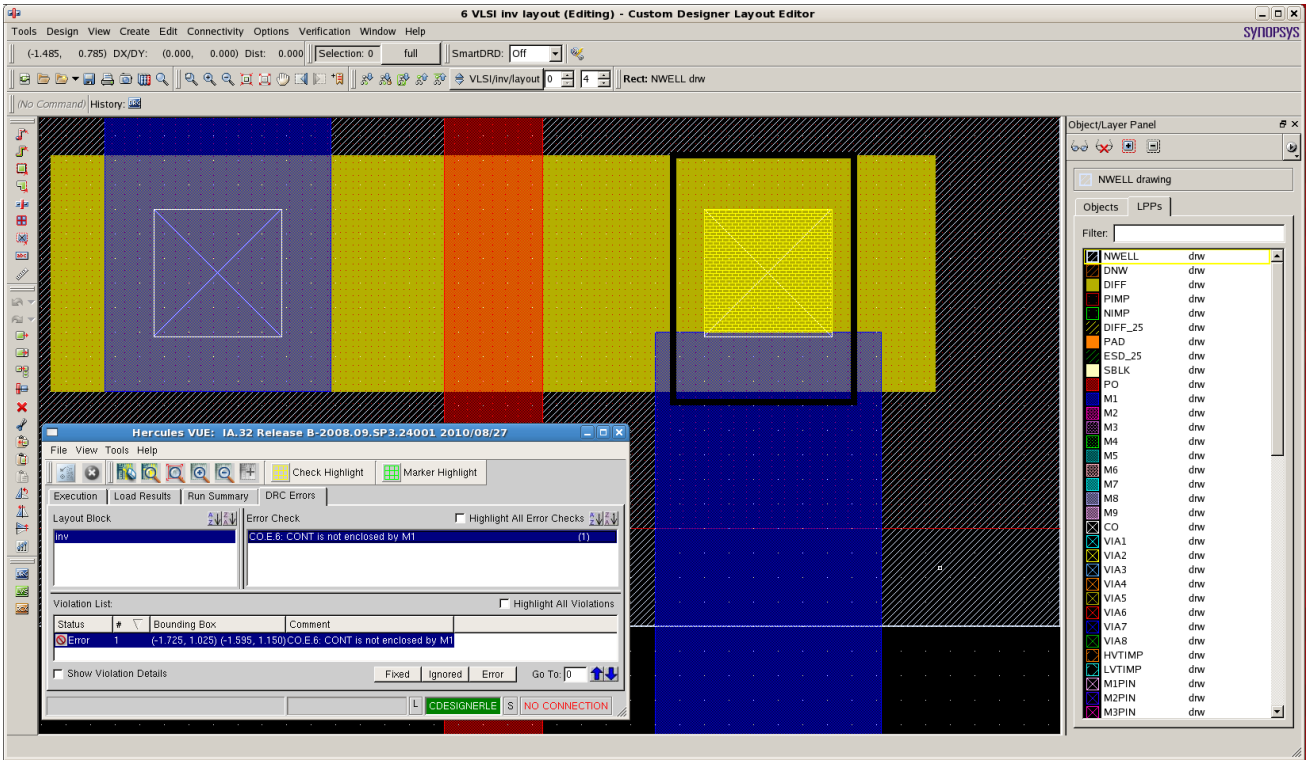

Figure 45 : Error highlighted.

Layout vs. Schematic Run - LVS

Once your design is DRC clean, next step is to do *LVS* test, which is layout vs. schematic. They need to match.

Note under your SDK file go and check Hercules-Runset File,

Under ***Option section*** >>

IGNORE_CASE = FALSE , if its valu is TRUE change it to FALSE.

Make sure all the layout pins have names that match the schematic pin names by following these steps:

1. Go to *Create menu> Text > Labels.*
2. A bar like that in fig (46) will appear at the top of your workspace.
3. Write the net name in the text field.
4. The texts will appear over the mouse curser.
5. In the layout editor, click at the layer where the text needs to be attached.

Figure 46 : Text label bar.

A different way to create text labels in layout is to:

1. Select a metal layer or a polysilicon layer in the layout editor.
2. Press (Q) on your keyboard. A form like shown in fig (47) will appear.
3. Under connectivity, enter the desired net name.

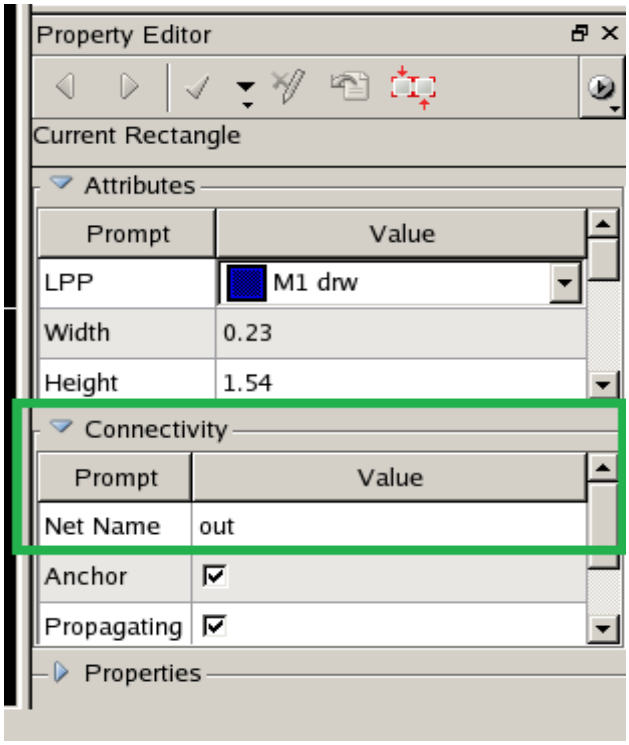

Figure 47 : Connectivity window.

To run finally LVS,

1. Go to *Verification menu >LVS > Setup & Run.*
2. See fig (48).
3. Do not change the defaults for now.
4. Select the Runset file from the directory (/work/90nm/Hercules/lvs/*.ev)
5. Click OK.
6. See figures (49-54) for more details.
7. Fix the mismatch error, and you will see a window like shown in fig (55). Your design is LVS clean.

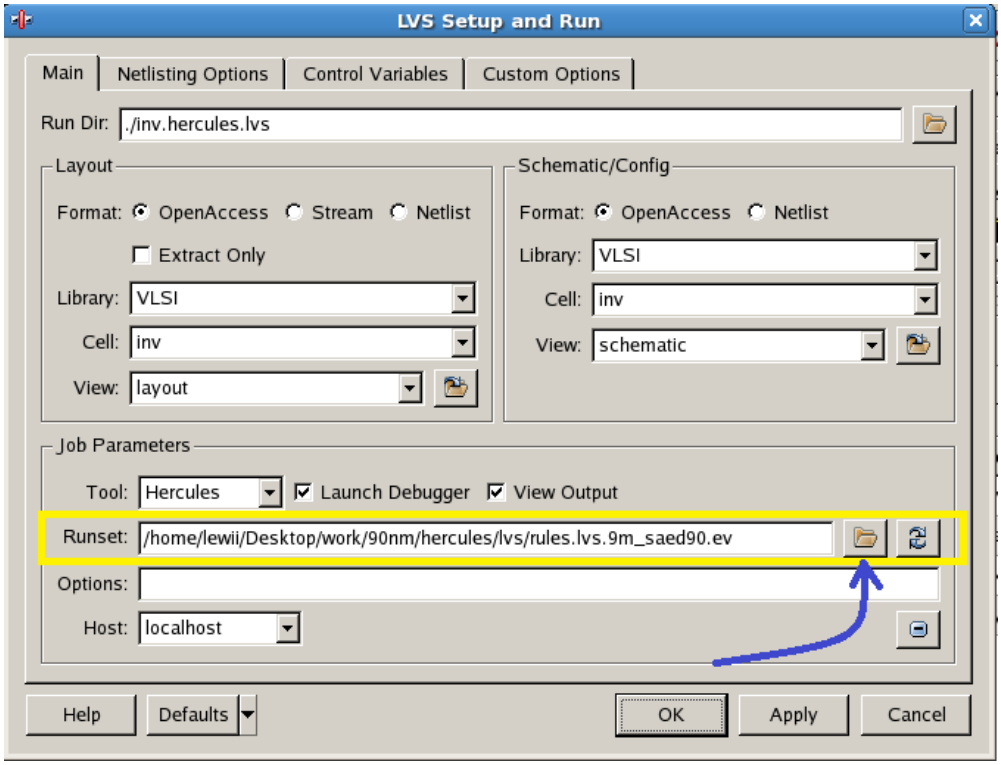

Figure 48 : LVS setup window.

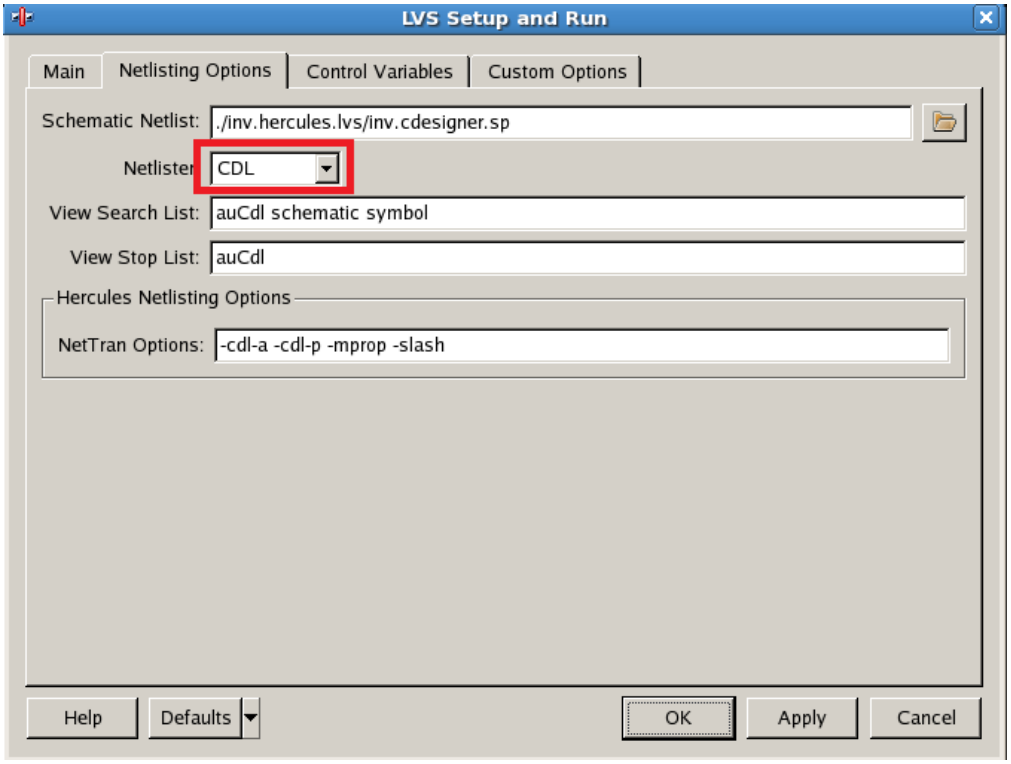

Figure 49 : LVS Setup "Netlisting options".

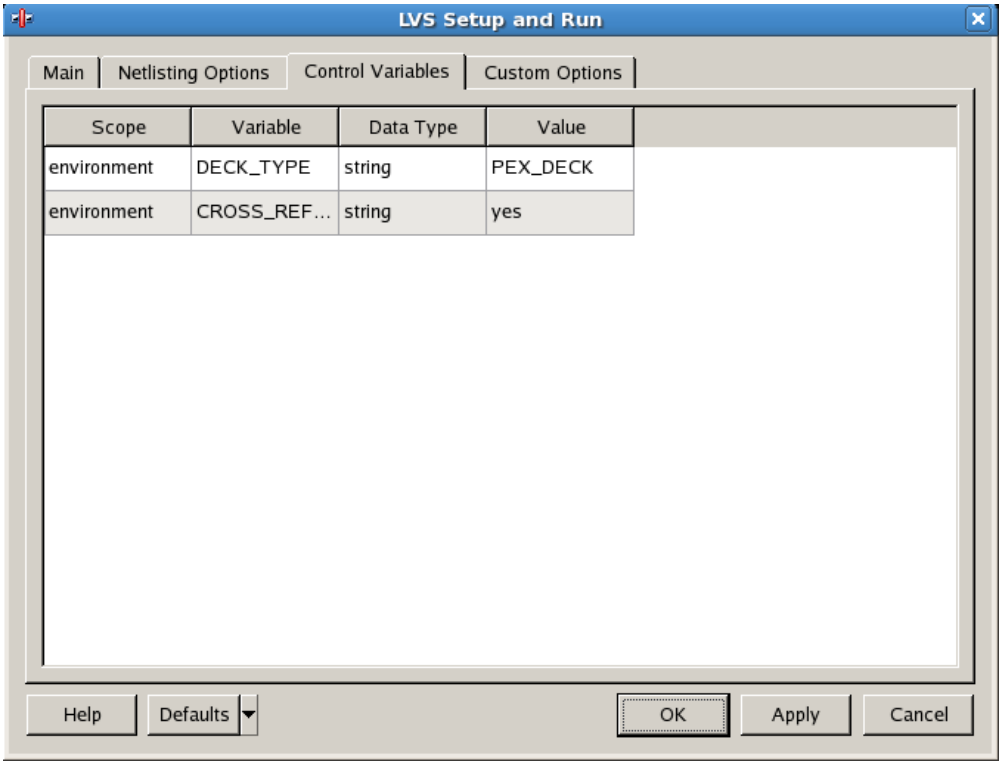

Figure 50 : LVS Setup "Control variable " tab.

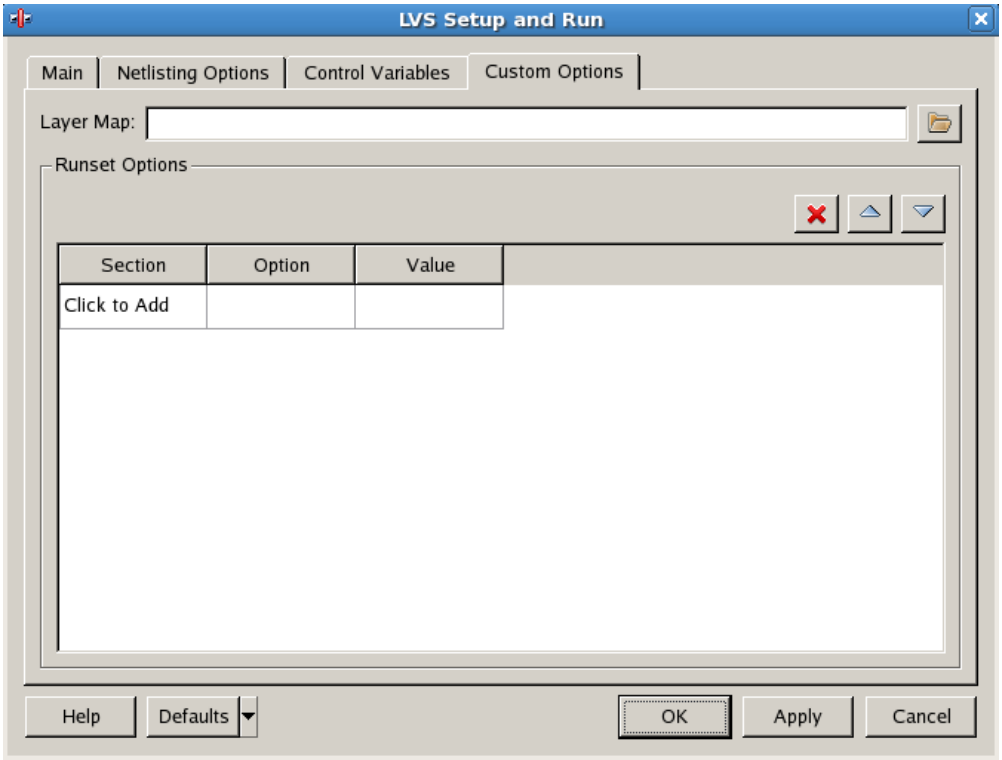

Figure 51 : LVS Setup "Custom option" tab.

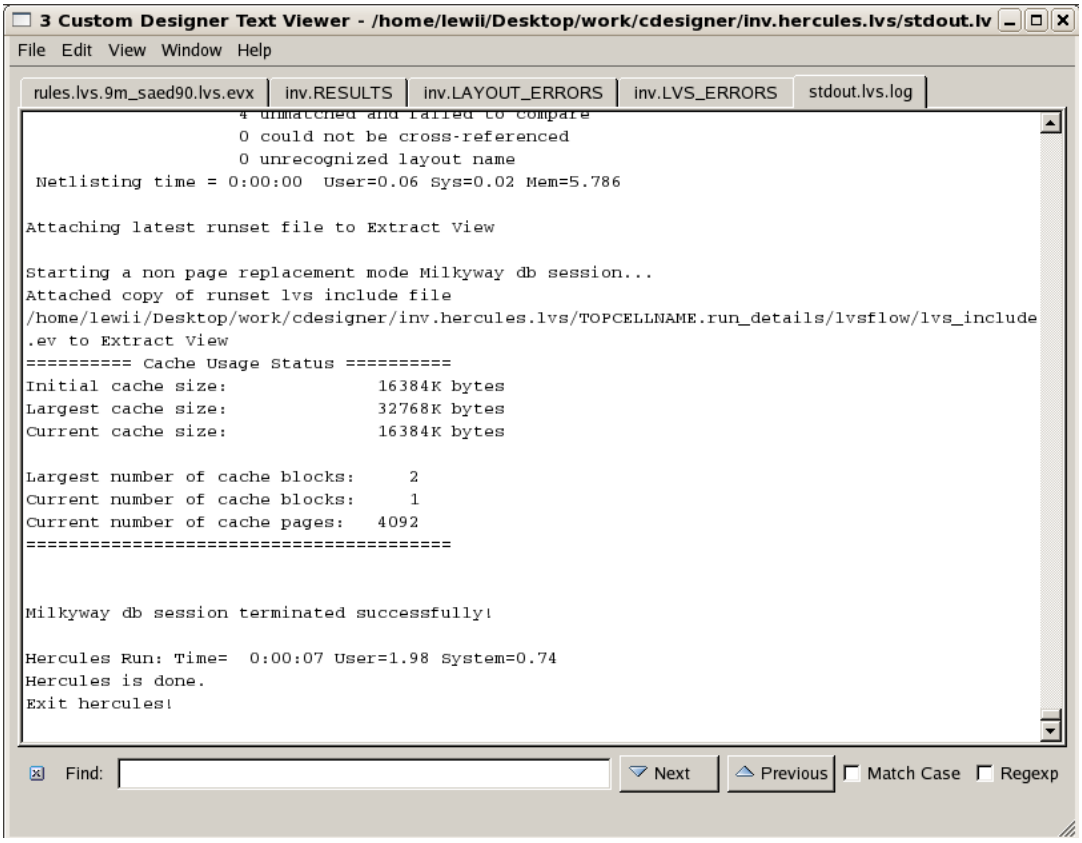

Figure 52 : Run log, results and errors viewer window.

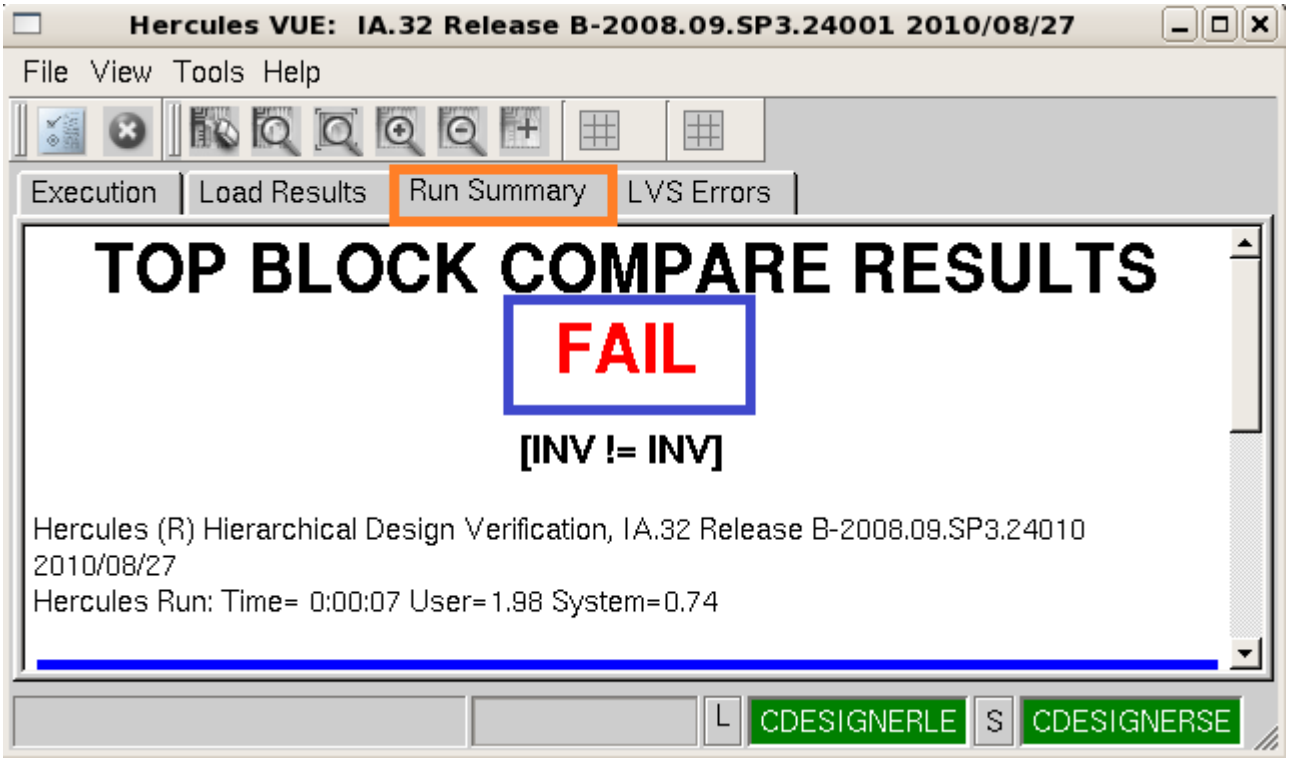

Figure 53 : Run summary of the LVS.

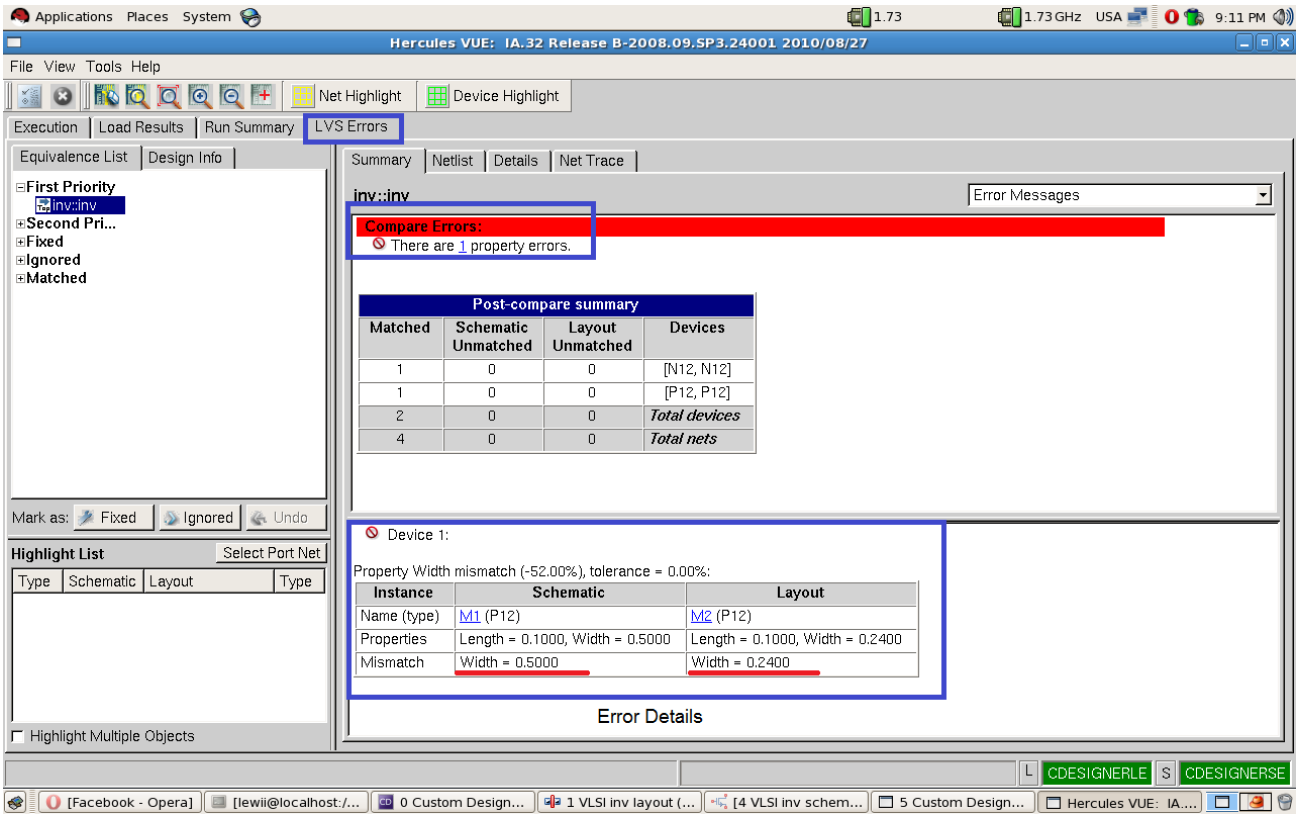

Figure 54 : Error details & mismatch between layout and schematics.

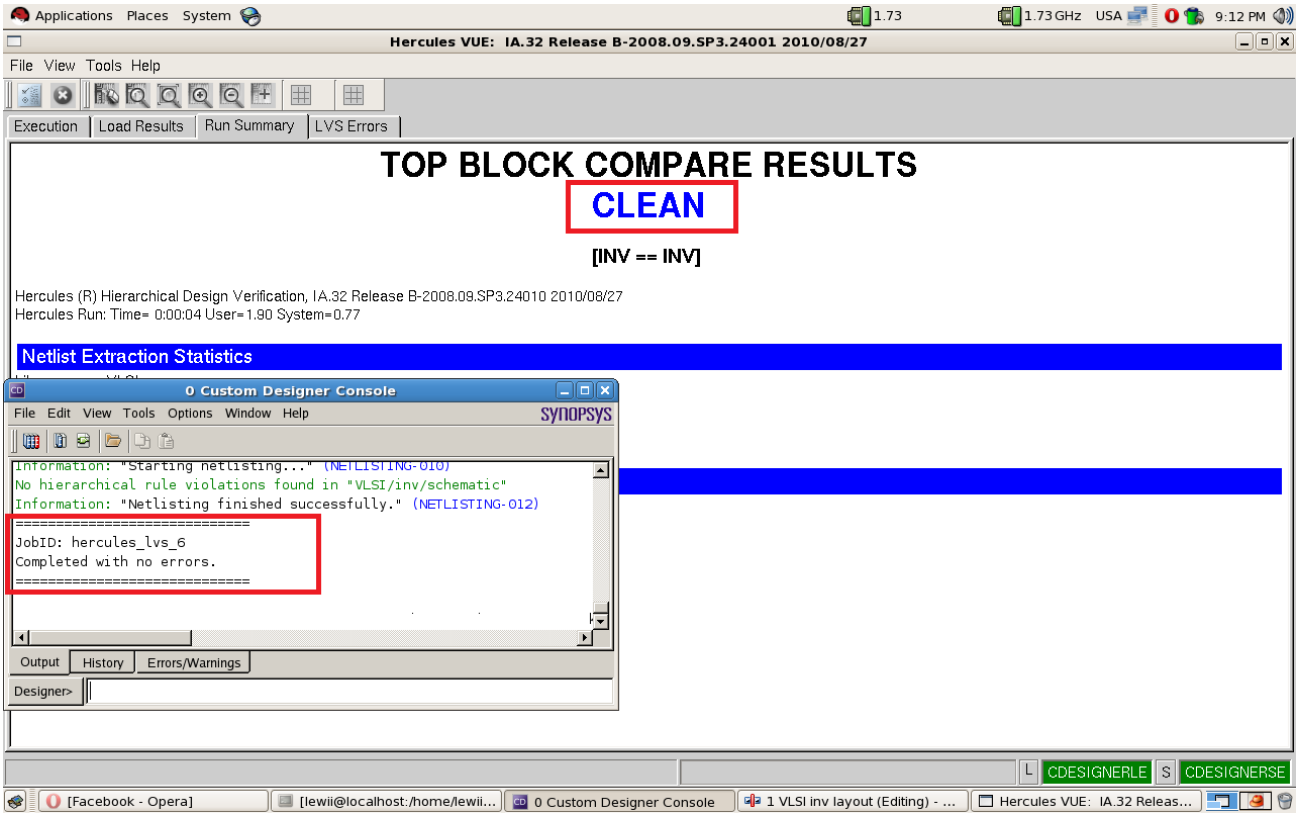

Figure 55 : LVS Debug window and the main customdesigner window with no errors.

LPE (RC extraction)

Last step before doing post layout simulation is to extract the RC components of the circuit that were not captured in schematic simulations. The only way to reach this point is to finish the design with clean DRC and LVS. Then in the layout editor, go to *Verification menu* > *LPE* > *Setup and Run*, you will get a window like that in fig (56), with a view of all the tabs in the following figures (57 – 59).

Fill the options in these windows as shown figures (56-59), and then click OK. You will get a new editor view like the one in figure (60-61). If no errors are shown, the next step is post-layout-simulation.

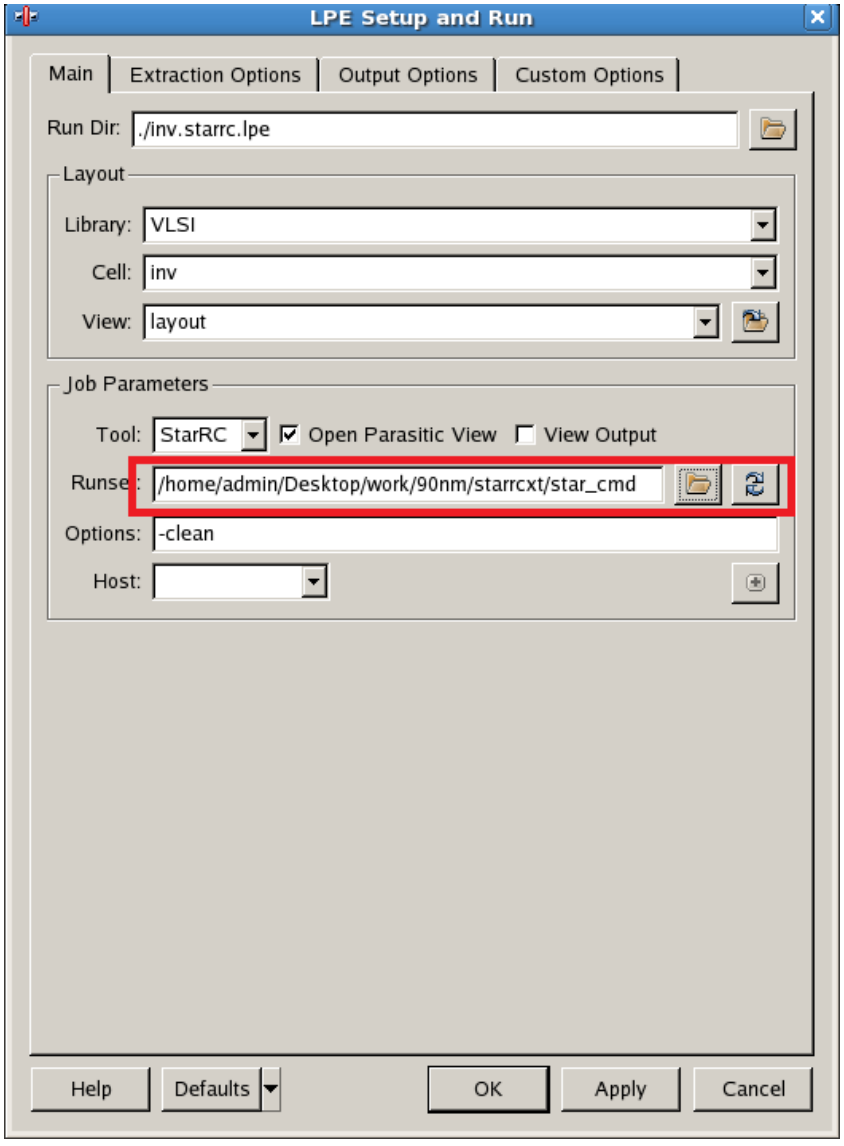

Figure 56 : LPE Setup " Main tab".

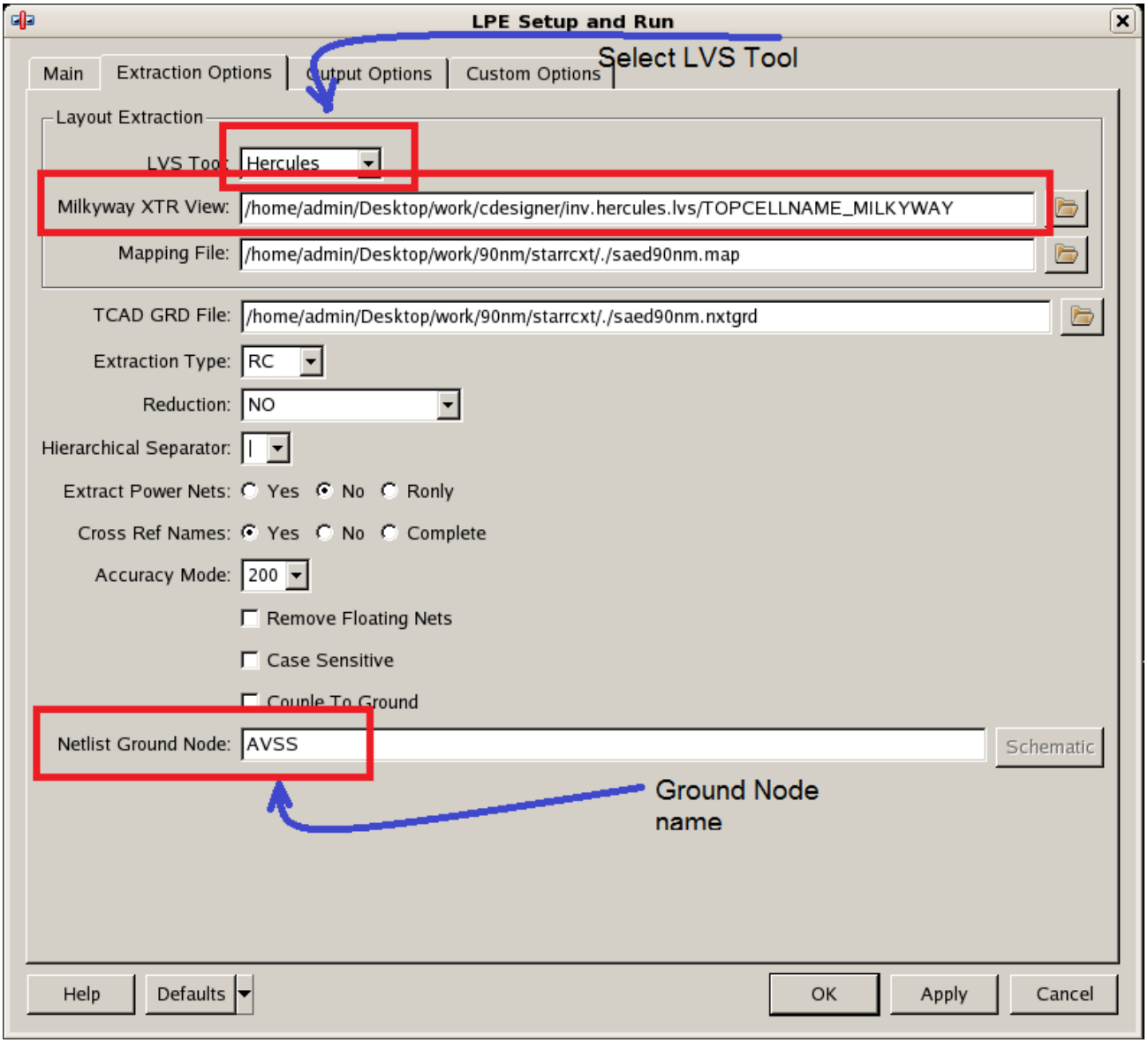

Figure 57 : LPE Setup "Extraction Options" tab.

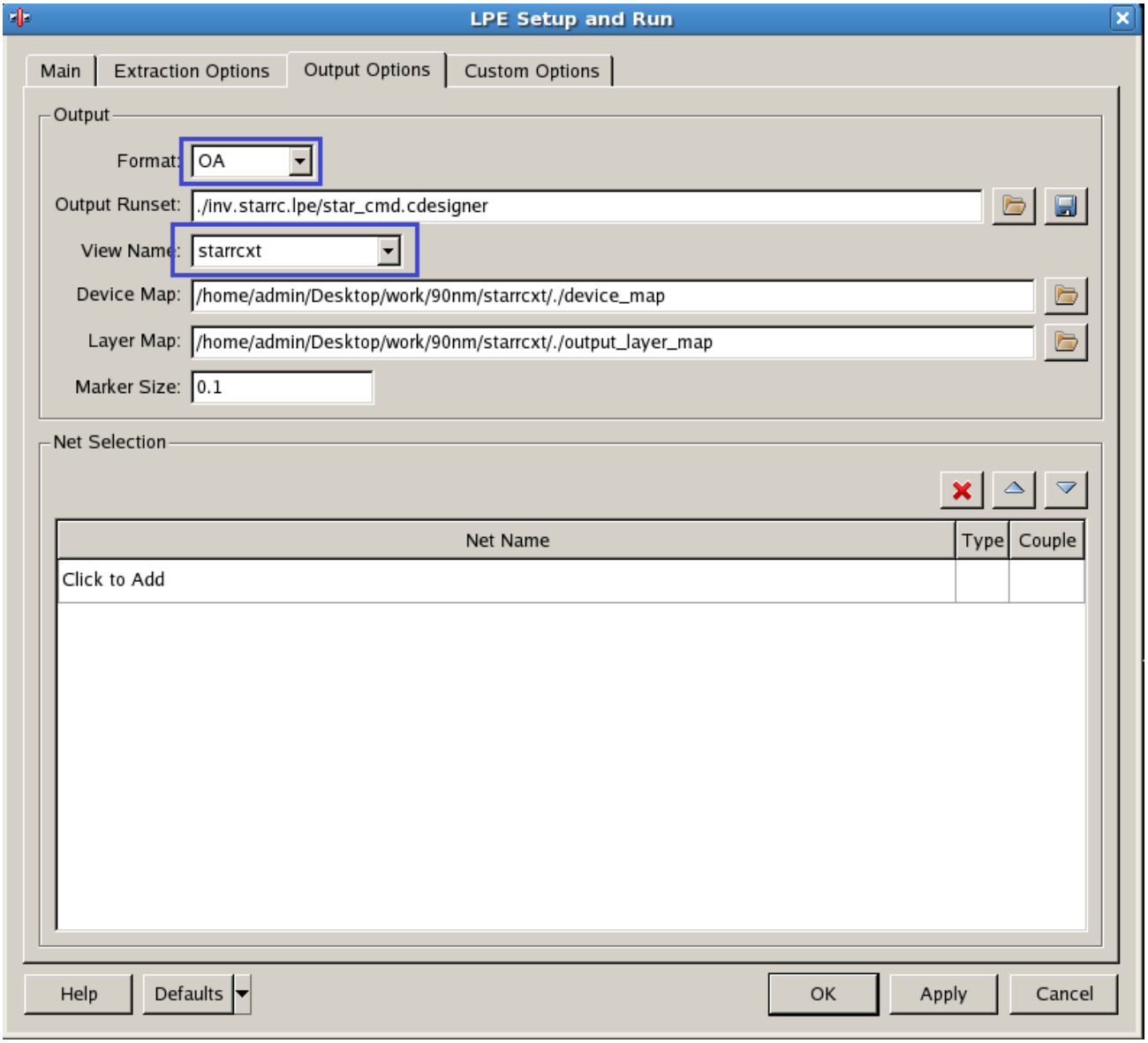

Figure 58 : LPE Setup "Output Option" tab.

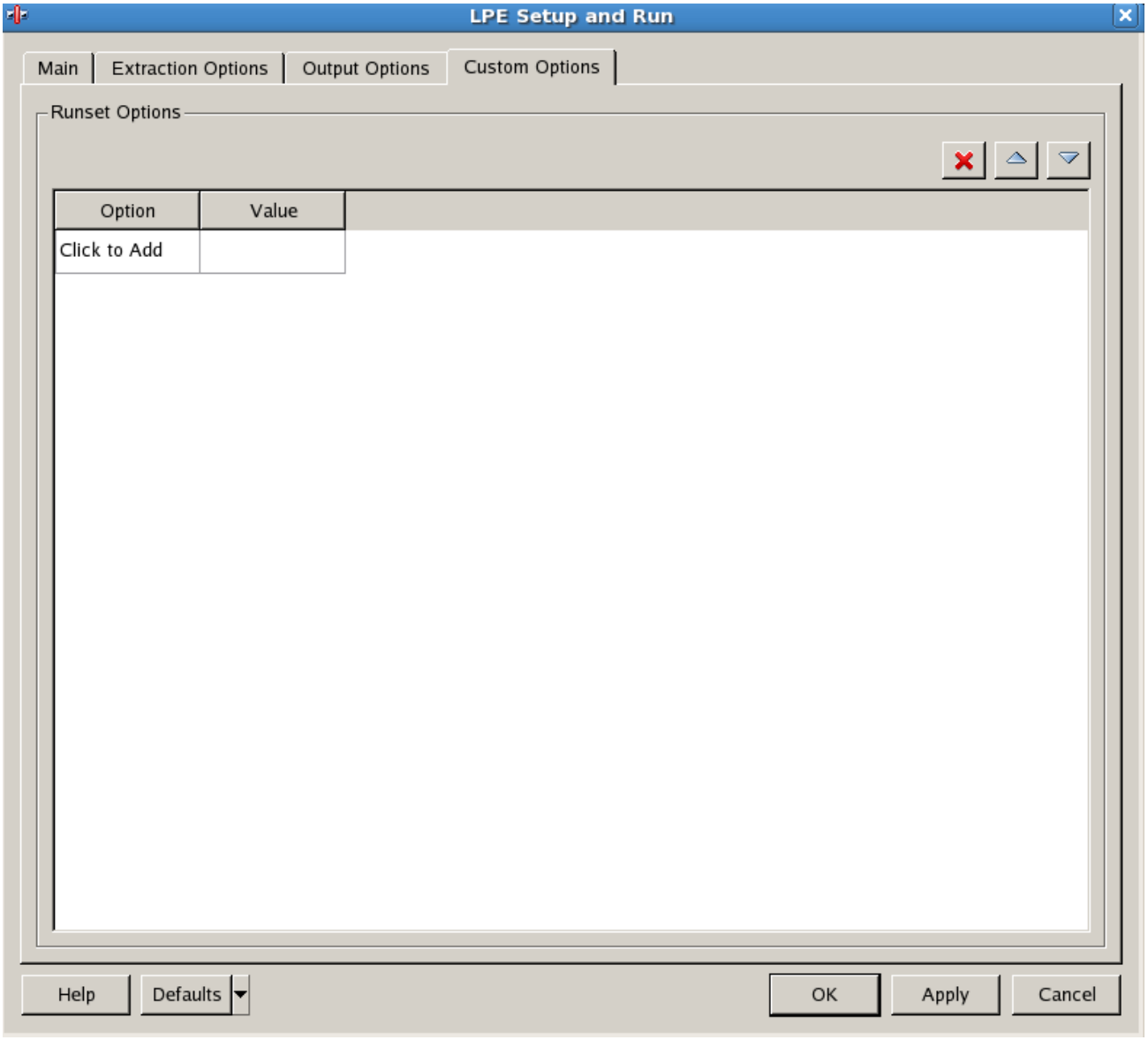

Figure 59 : LPE Setup "Custom Option" tab

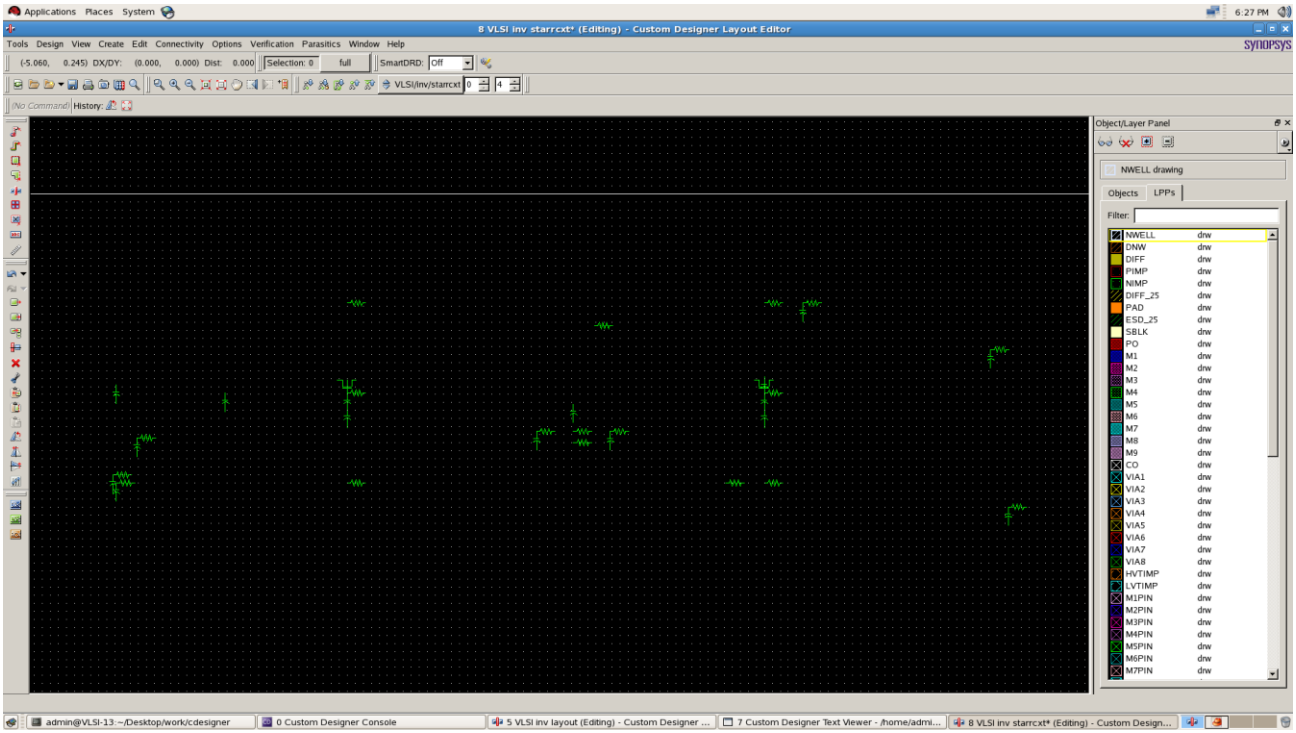

Figure 60 : StarRC view (LPE Results).

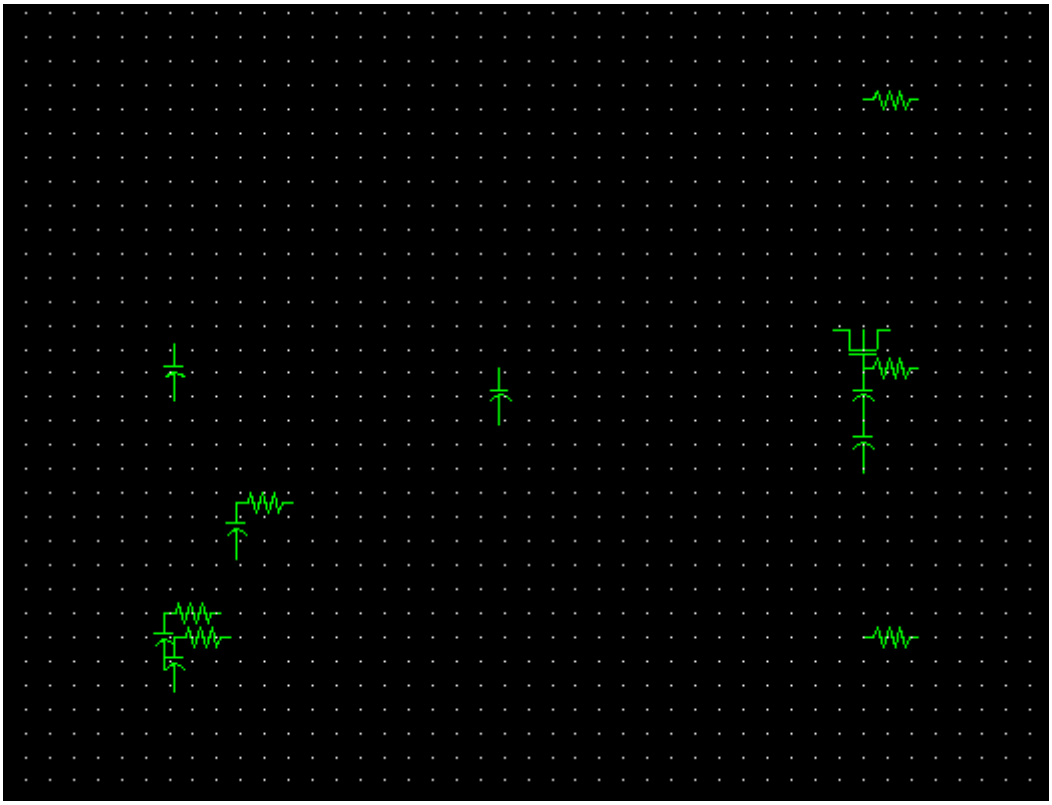

Figure 61 : Zoom of fig (60)

Creating Config view & Post Simulation

Create Config view

To run post layout simulation, follow these steps:

1. Go to ***Custom Design*** main window.
2. File > new Cell view.
3. Select the testbench cell.
4. Moreover, create new cell view under it.
5. Choose *Config* in view type field.
6. Moreover, *Config* editor in the second field, see fig (62).
7. You will get a window like that in fig (63).
8. In this window, fill empty fields with same data as shown in fig (63) which are marked with blue boxes.
9. Click under selected column, in your cell line, and you will see drop down menu.
10. Select *starrcxt* from that menu as shown in fig (64) - red marked areas.
11. Please note that the test bench has two instances on the inverter. One can be extracted view and the other can schematic view as shown in fig (65).

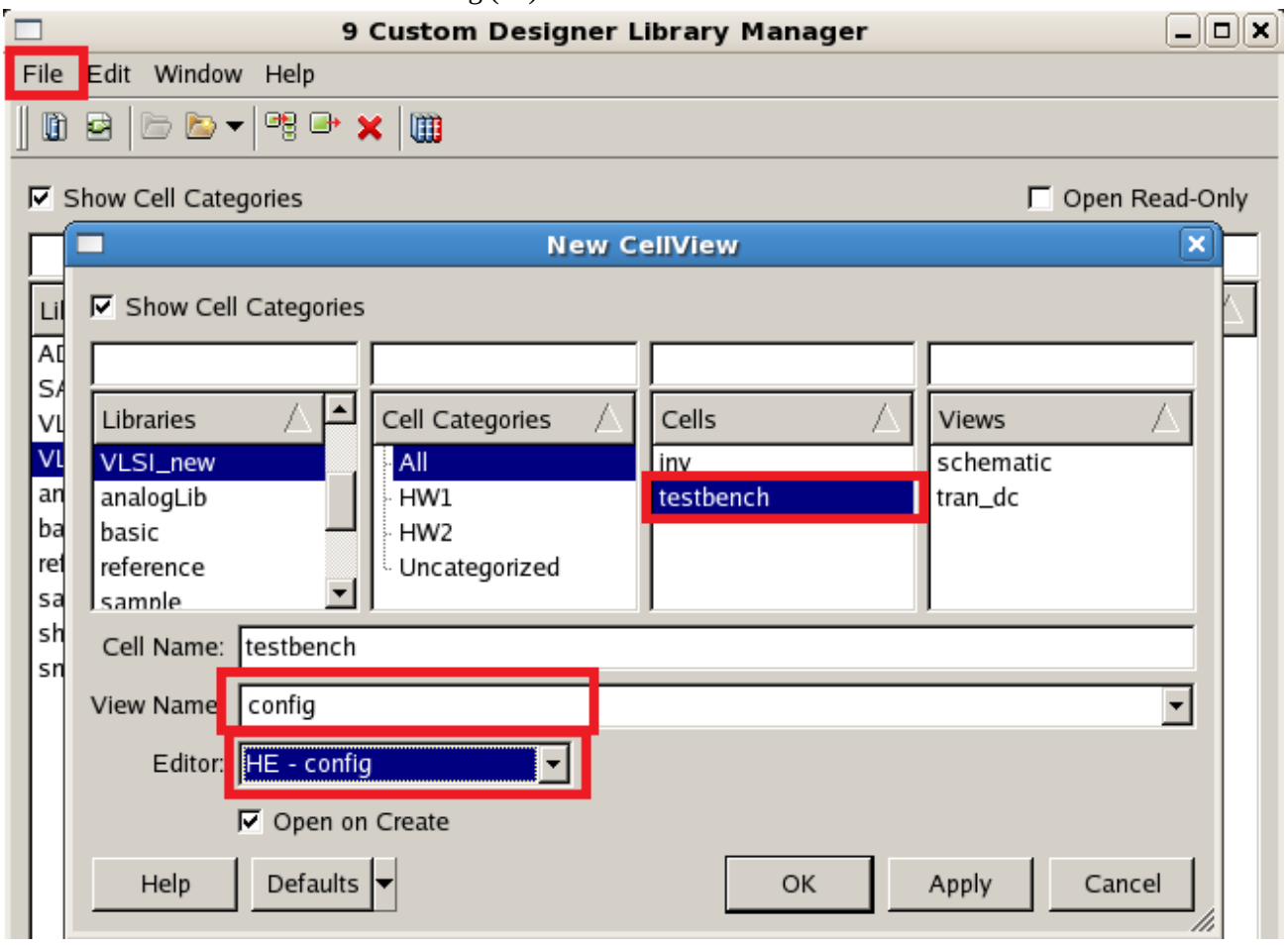

Figure 62 : New CellView window.

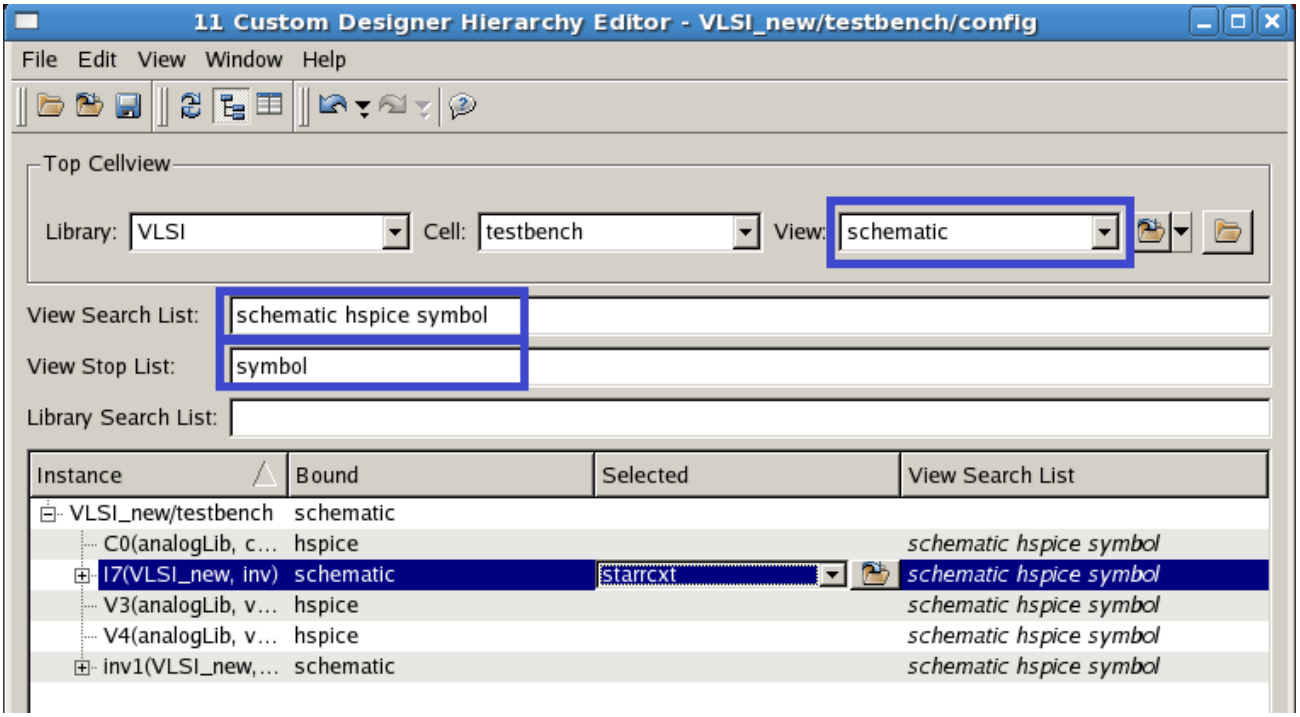

Figure 63 : Config editor window.

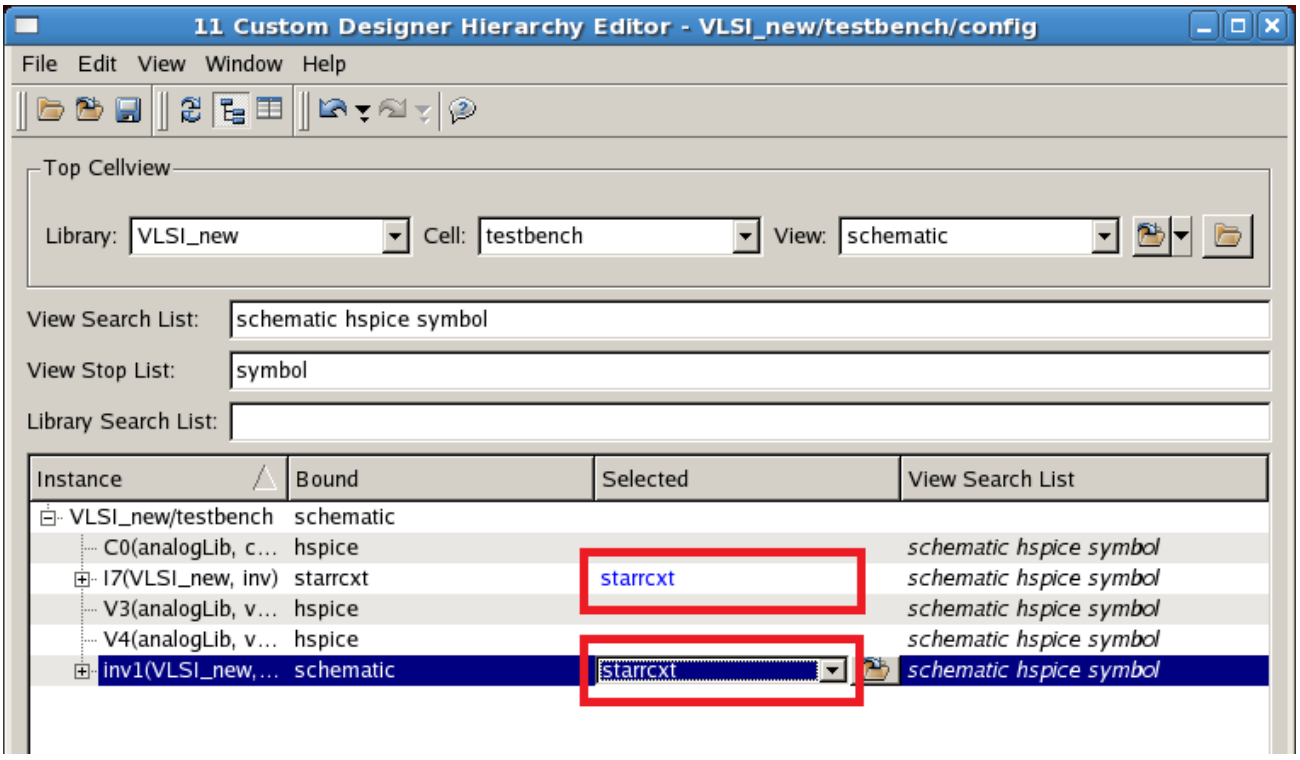

Figure 64 : Config editor window (selecting view).

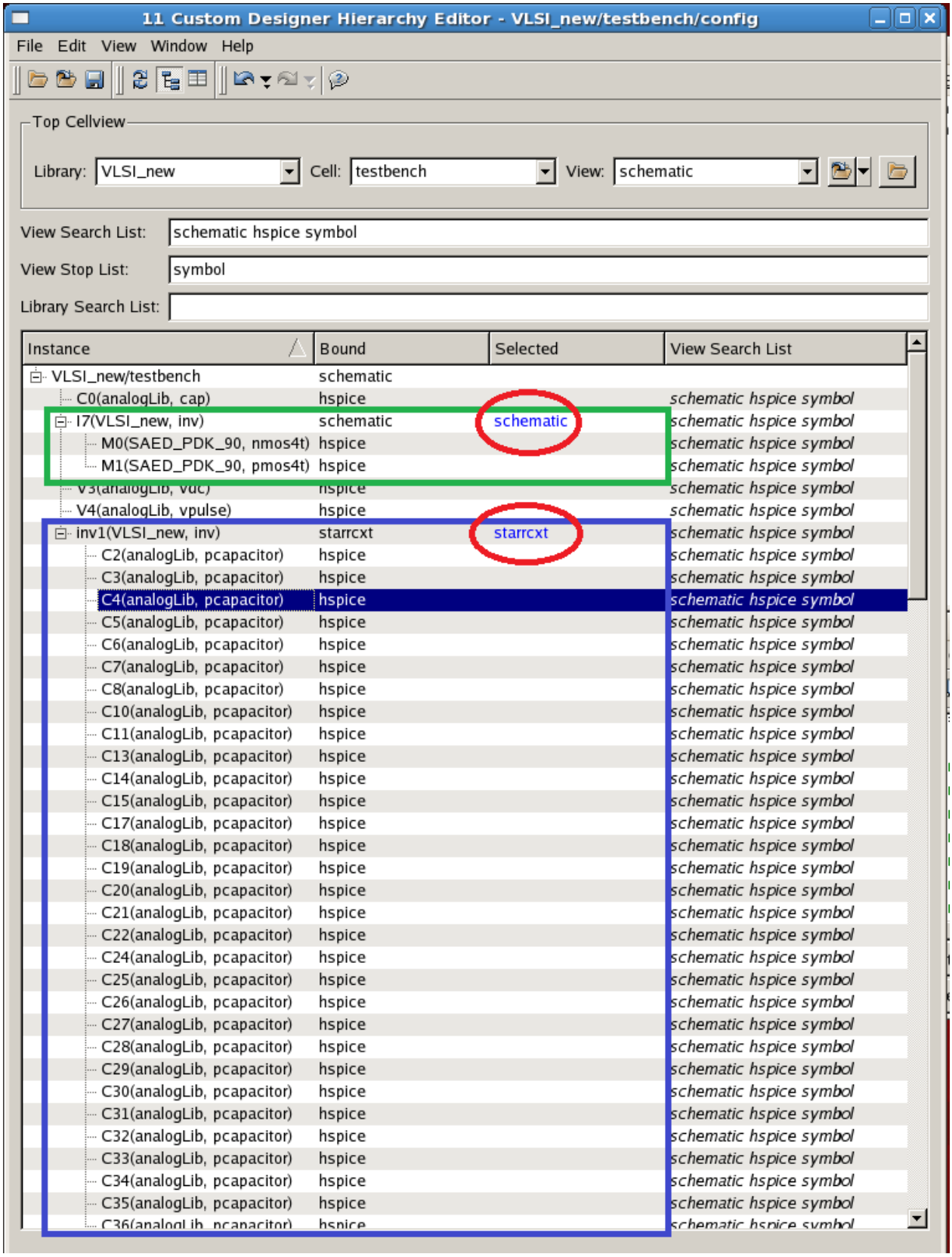

Figure 65 : Config editor window (difference between views).

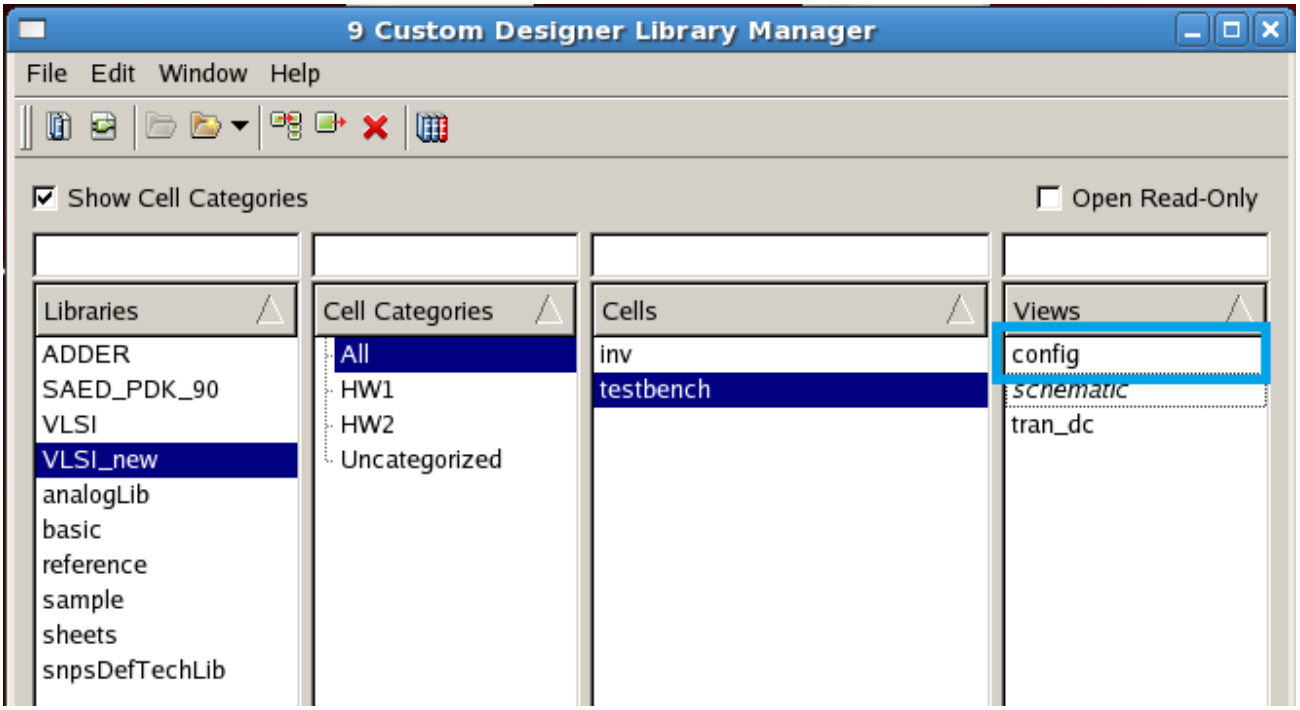

Figure 66 : CustomeDesigner library manager.

Post-layout-Simulation

To start post-simulation open ***CustomeDesigner*** library manager fig (66), and follow the steps:

1. Right click on Config under Views.
2. From drop menu select, *open both.*
3. Two windows will open, the one in Fig (65) and another one that look like schematics editor window.
4. To check if your Config viewpoints to *starrcxt view double* click on the inverter cell in schematics editor view, you will see starrcxt view.
5. Now in the schematics view window, go to *Tools menu* > *SAE*. (Refer to SAE section for details how to run simulation).
6. Run the simulation and see the difference between pre-layout-simulation and post-layout-simulation.

You have now learned to use Synopsys Full Custom Design Tools. Congratulations. ☺