

Synopsys Design Flow Tutorial

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Synopsys Design Flow Tutorial
Lecture - 4
Developed By: Vazgen Melikyan



Course Overview

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 - 2 lectures
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 - 2 lectures
- Physical Synthesis (IC Compiler II)
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- Physical Verification (IC Validator)
 - 2 lectures
- Layout Parasitics Extraction (StarRC)
 - 2 lectures
- SPICE-Level Simulation of Completed Design (HSpice)
 - 2 lectures



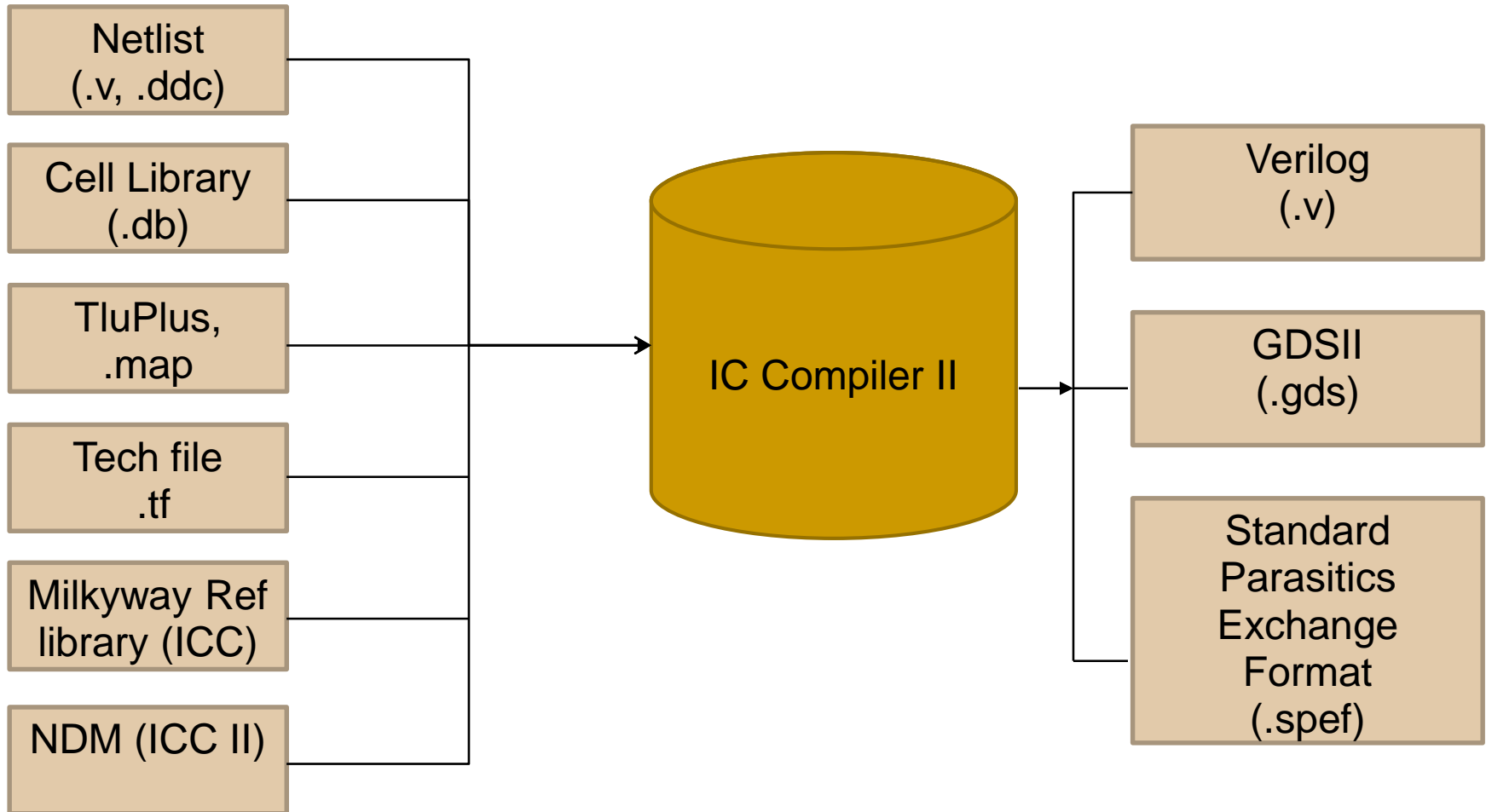
Physical Synthesis (IC Compiler II)



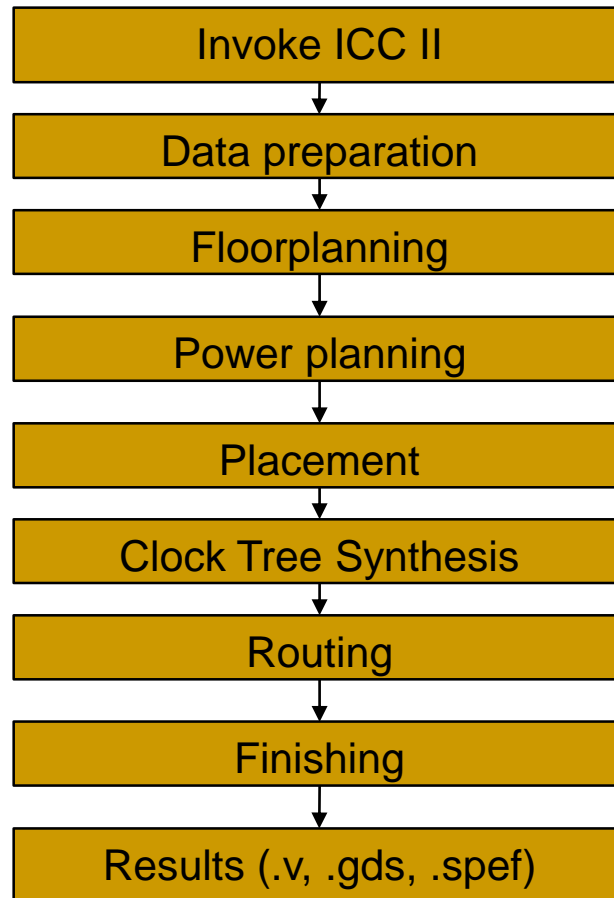
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Input and Output Files of IC Compiler II

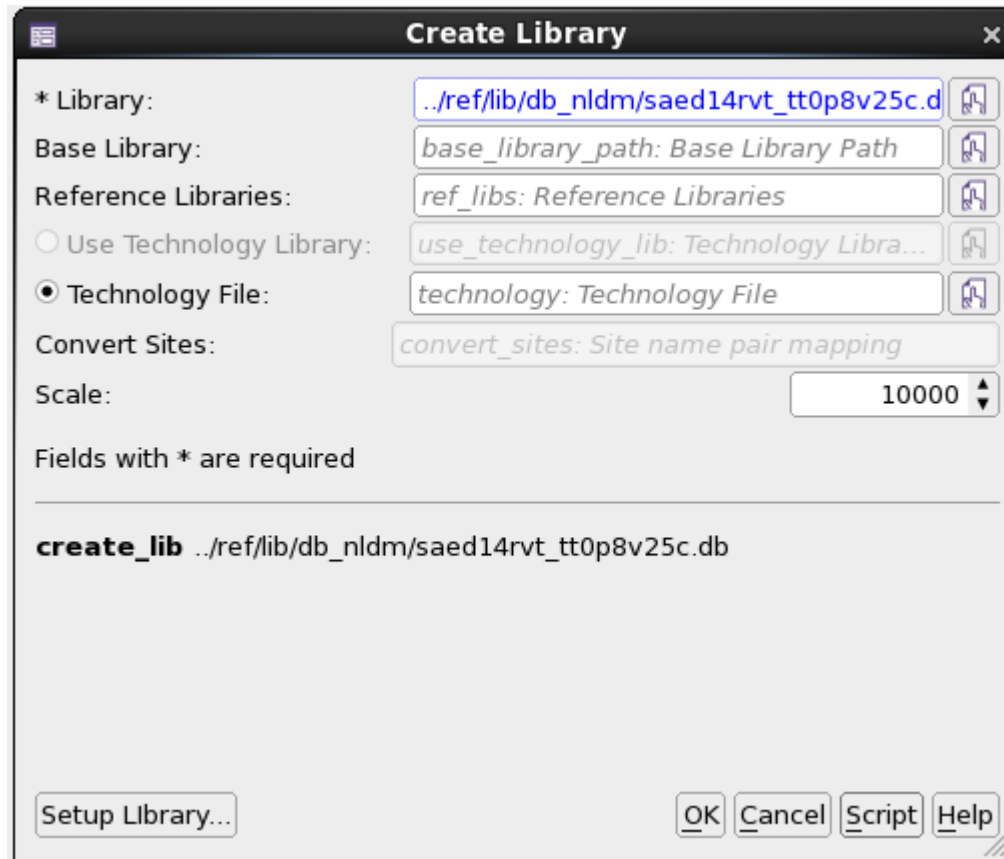


IC Compiler II Design Flow



NDM Library Creation

- To create the NDM design library, Choose **File > Create Library**



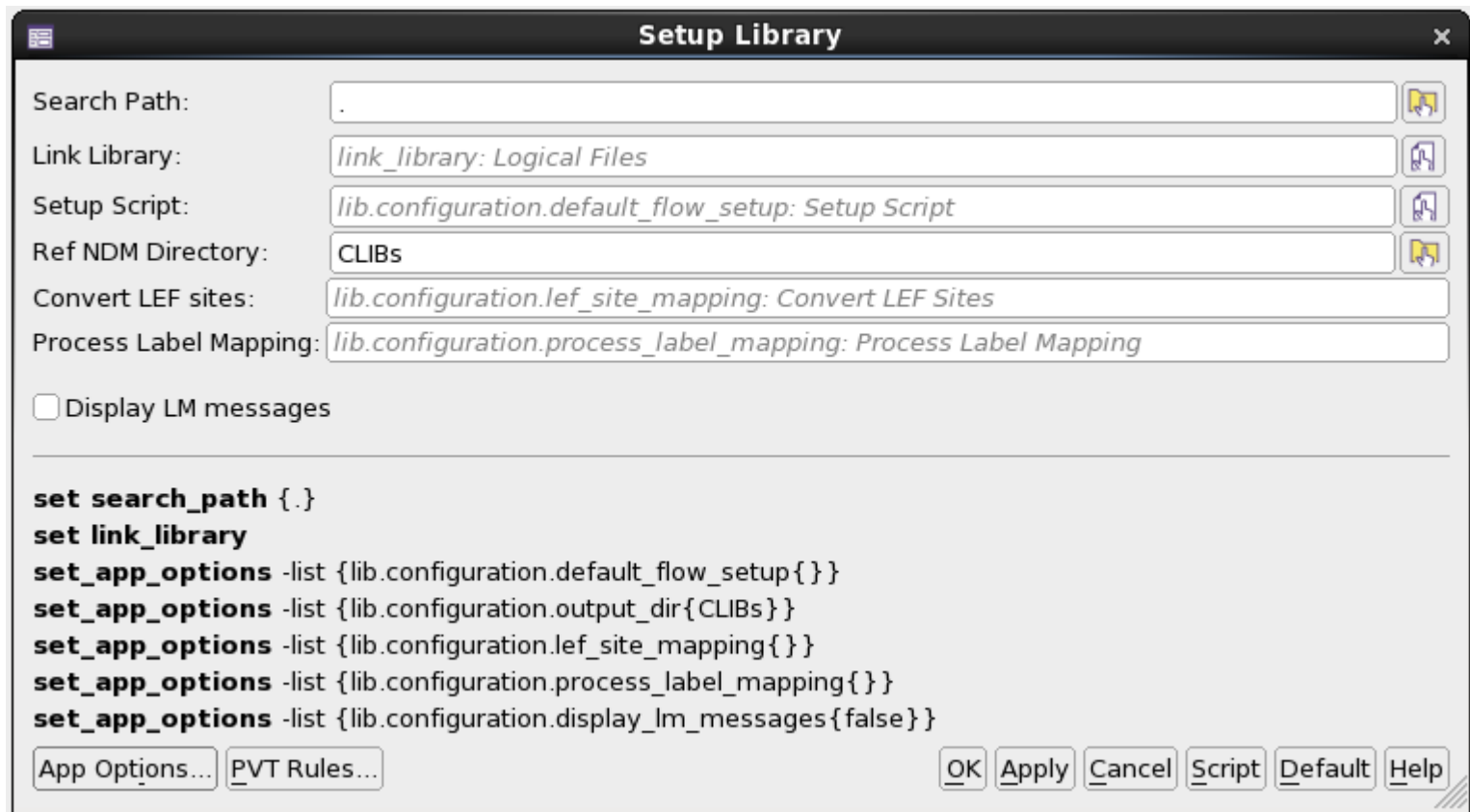
The screenshot shows the 'Create Library' dialog box with the following fields and options:

- * Library:** `../ref/lib/db_nldm/saed14rvt_tt0p8v25c.d`
- Base Library:** `base_library_path: Base Library Path`
- Reference Libraries:** `ref_libs: Reference Libraries`
- ☐ **Use Technology Library:** `use_technology_lib: Technology Libra...`
- ☒ **Technology File:** `technology: Technology File`
- Convert Sites:** `convert_sites: Site name pair mapping`
- Scale:** `10000`
- Fields with * are required**
- create_lib** `../ref/lib/db_nldm/saed14rvt_tt0p8v25c.db`
- Buttons:** Setup Library..., OK, Cancel, Script, Help



Setup Logic Libraries

- Choose **File > Setup Library**



The screenshot shows the 'Setup Library' dialog box with the following fields and options:

- Search Path: .
- Link Library: link_library: Logical Files
- Setup Script: lib.configuration.default_flow_setup: Setup Script
- Ref NDM Directory: CLIBs
- Convert LEF sites: lib.configuration.lef_site_mapping: Convert LEF Sites
- Process Label Mapping: lib.configuration.process_label_mapping: Process Label Mapping
- ☐ Display LM messages

Below the fields, the following configuration script is displayed:

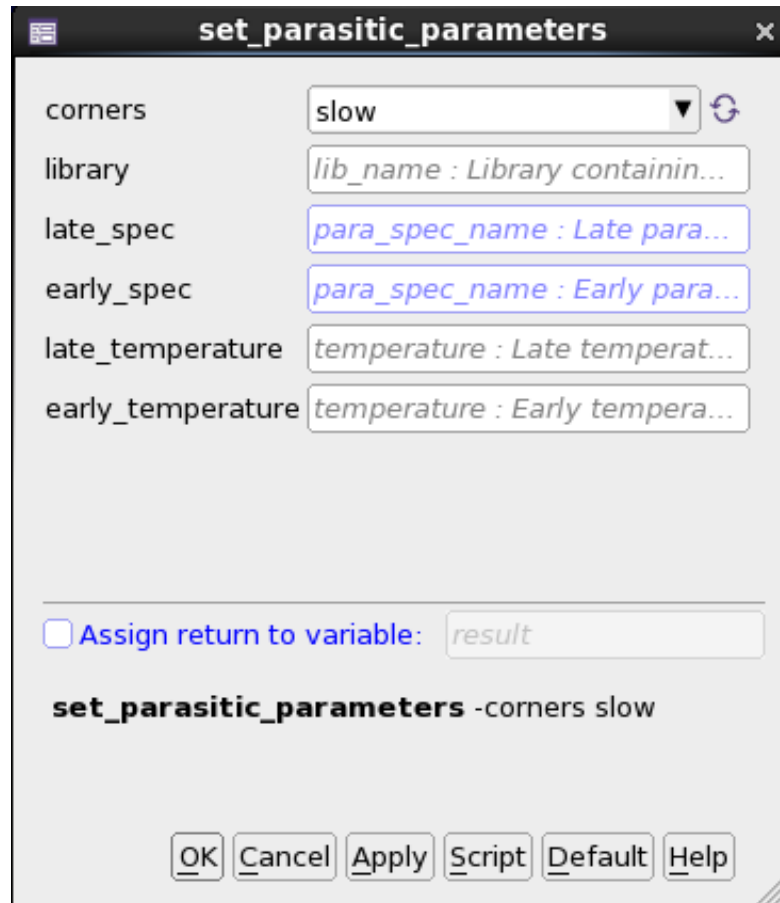
```
set search_path { . }  
set link_library  
set_app_options -list {lib.configuration.default_flow_setup{}}  
set_app_options -list {lib.configuration.output_dir{CLIBs}}  
set_app_options -list {lib.configuration.lef_site_mapping{}}  
set_app_options -list {lib.configuration.process_label_mapping{}}  
set_app_options -list {lib.configuration.display_lm_messages{false}}
```

At the bottom, there are buttons for 'App Options...', 'PVT Rules...', 'OK', 'Apply', 'Cancel', 'Script', 'Default', and 'Help'.



TluPlus Setup

- Choose **View > Map > Rail Parasitics**



The screenshot shows the 'set_parasitic_parameters' dialog box. It has a title bar with a menu icon, the text 'set_parasitic_parameters', and a close button. The dialog contains several input fields and a checkbox. The 'corners' field is a dropdown menu set to 'slow' with a refresh icon. The 'library' field is a text box with the value 'lib_name : Library containin...'. The 'late_spec' field is a text box with the value 'para_spec_name : Late para...'. The 'early_spec' field is a text box with the value 'para_spec_name : Early para...'. The 'late_temperature' field is a text box with the value 'temperature : Late temperat...'. The 'early_temperature' field is a text box with the value 'temperature : Early tempera...'. Below these fields is a checkbox labeled 'Assign return to variable:' which is unchecked, followed by a text box containing the word 'result'. At the bottom of the dialog, there is a summary line: 'set_parasitic_parameters -corners slow'. At the very bottom are six buttons: 'OK', 'Cancel', 'Apply', 'Script', 'Default', and 'Help'.

corners	slow
library	lib_name : Library containin...
late_spec	para_spec_name : Late para...
early_spec	para_spec_name : Early para...
late_temperature	temperature : Late temperat...
early_temperature	temperature : Early tempera...

☐ Assign return to variable: result

set_parasitic_parameters -corners slow

OK Cancel Apply Script Default Help



Design Importing

- Choose Task > Create Design > Create Design Library

The screenshot shows the 'Task Assistant - Create Block' dialog box with the 'Create Design Library' tab selected. The dialog has a breadcrumb trail: 'Create Design Library' > '2 of 3'. The 'Create Design' tab is active, showing various input fields for creating a design library. The fields are organized into sections: 'file_names' (with a red border and a hint 'file_names : Files to read'), 'library' (with a hint 'library_name : Library name'), 'design' (with a hint 'design_name : Design name'), and 'top' (with a hint 'module_name : Top module name'). Below these are three radio buttons: '(none)' (selected), 'partition', and 'allocation'. The next section contains several fields with hints: 'target_block_size' (cell_count : Target number of cells in each partition block), 'glue_cell_count' (cell_count : Target glue module cell count), 'target_cell_count' (cell_count : Target leaf cell count), 'large_threshold' (cell_count : Large module leaf cell threshold), 'depth' (depth : Dense module depth), 'keep_port_depth' (port_hierarchy_depth : Preserve port depth), 'dense_modules' (module_names : Dense module names), 'port_modules' (module_names : Port module names), 'sparse_modules' (module_names : Sparse module names), 'leaf_cells' (cell_names : Leaf lib cell names), 'buffer_cells' (cell_names : Buffer lib cell names), and 'macro_cells' (cell_names : Macro lib cell names). A note at the bottom right states '(Fields with * are required)'. At the bottom left, there is a red error message: 'read_verilog_outline' and 'Missing value for the required option file_names.'. At the bottom right, there are buttons for 'Apply', 'Script', 'Default', 'Help', and 'Close'.

Task Assistant - Create Block

Create Design Library

Create Design Read Hierarchical Verilog Read Flat Verilog Read DEF

*file_names file_names : Files to read

library library_name : Library name

design design_name : Design name

top module_name : Top module name

☒ (none) ☐ partition ☐ allocation

target_block_size cell_count : Target number of cells in each partition block

glue_cell_count cell_count : Target glue module cell count

target_cell_count cell_count : Target leaf cell count

large_threshold cell_count : Large module leaf cell threshold

depth depth : Dense module depth

keep_port_depth port_hierarchy_depth : Preserve port depth

dense_modules module_names : Dense module names

port_modules module_names : Port module names

sparse_modules module_names : Sparse module names

leaf_cells cell_names : Leaf lib cell names

buffer_cells cell_names : Buffer lib cell names

macro_cells cell_names : Macro lib cell names

(Fields with * are required)

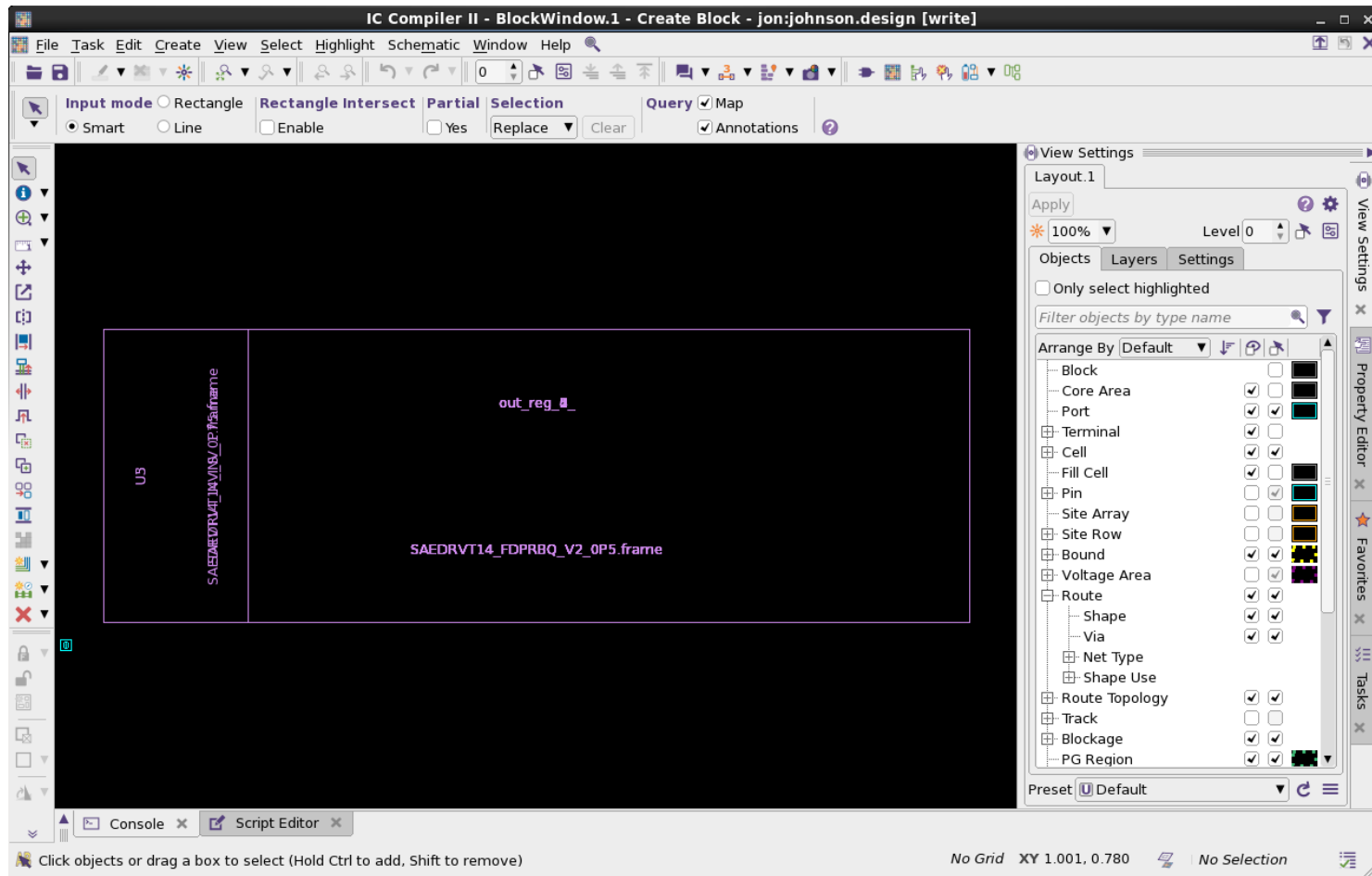
read_verilog_outline
Missing value for the required option file_names.

Apply Script Default Help

Close

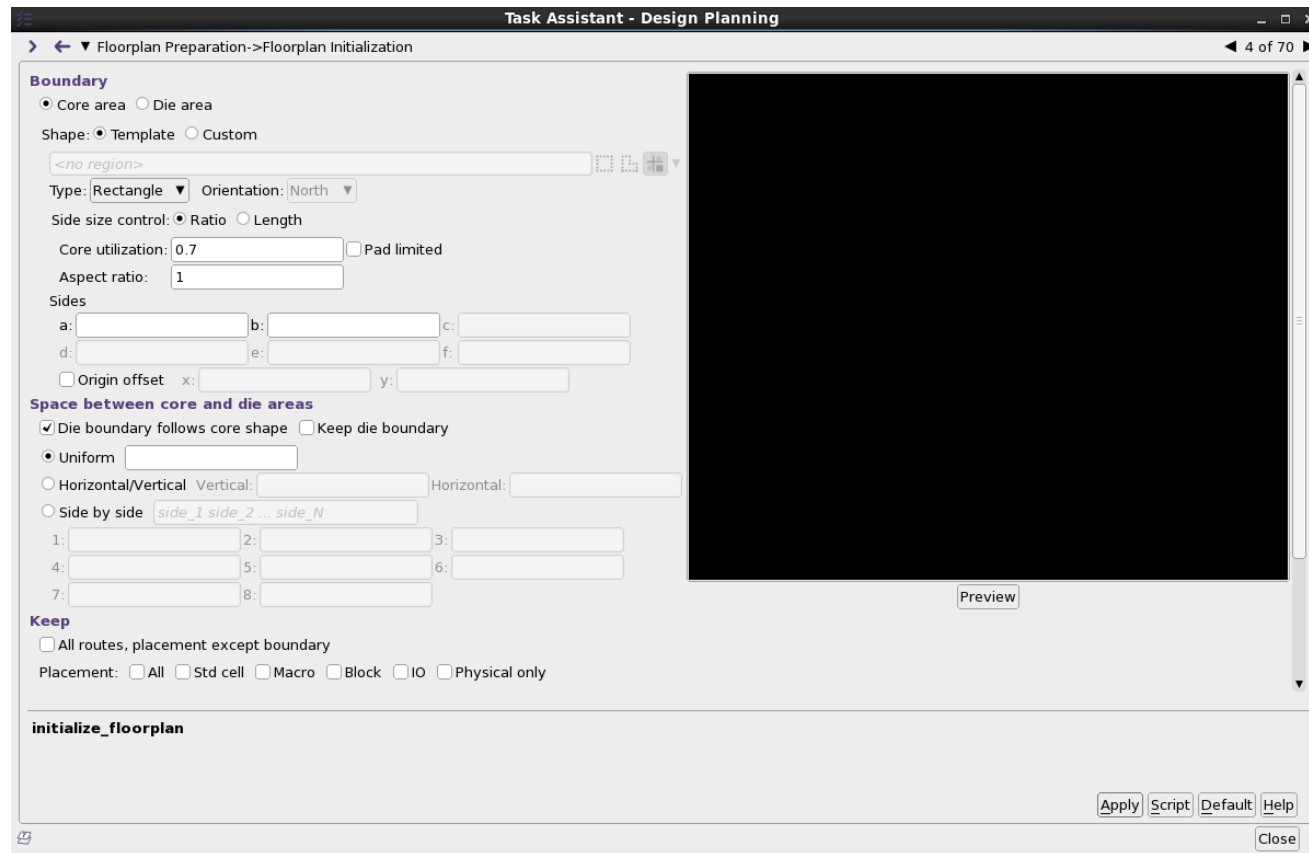


Design Importing (2)

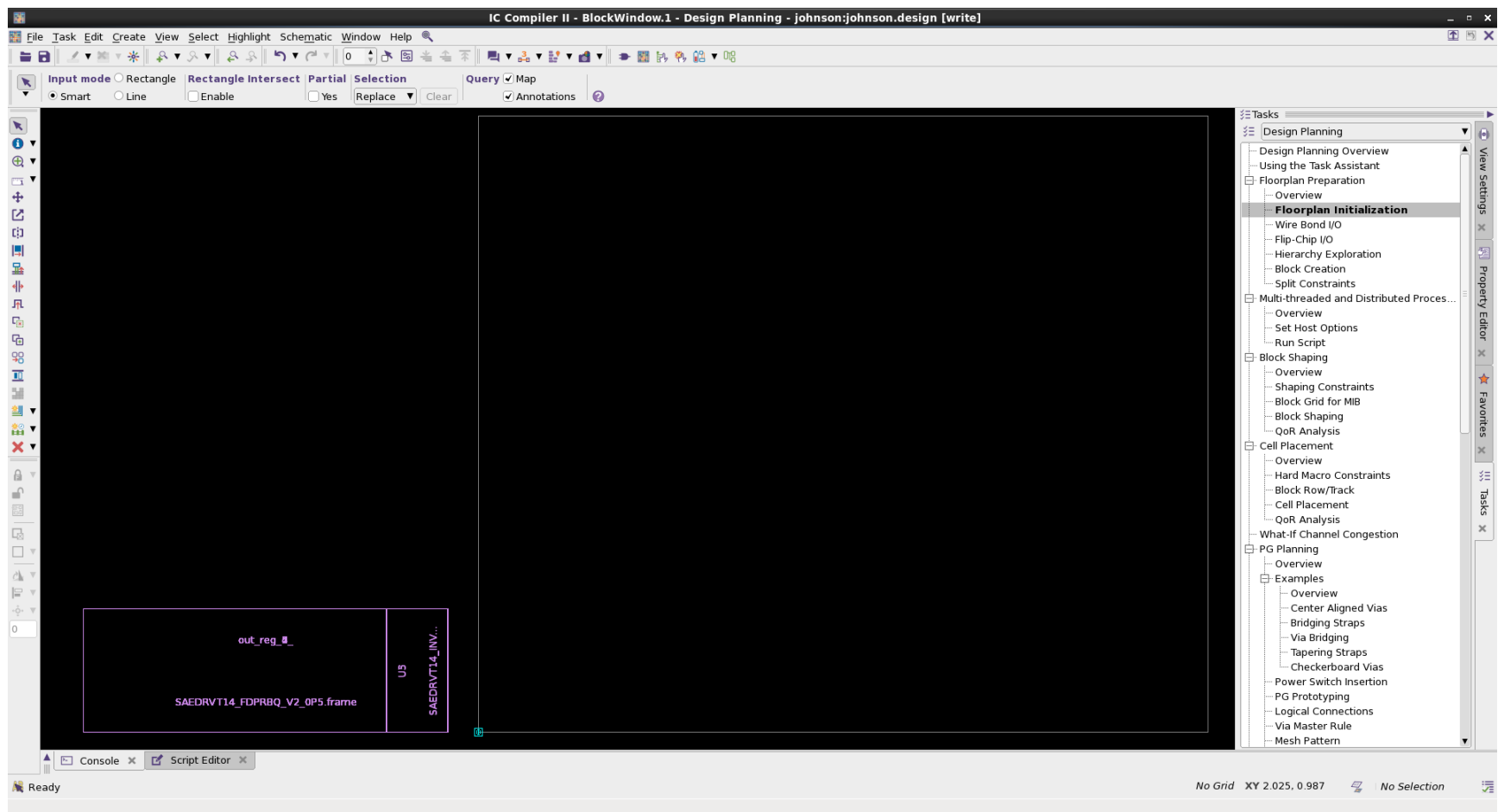


Floorplanning

- For floorplanning the design choose **Task > Design Planning > Floorplan Initialization**

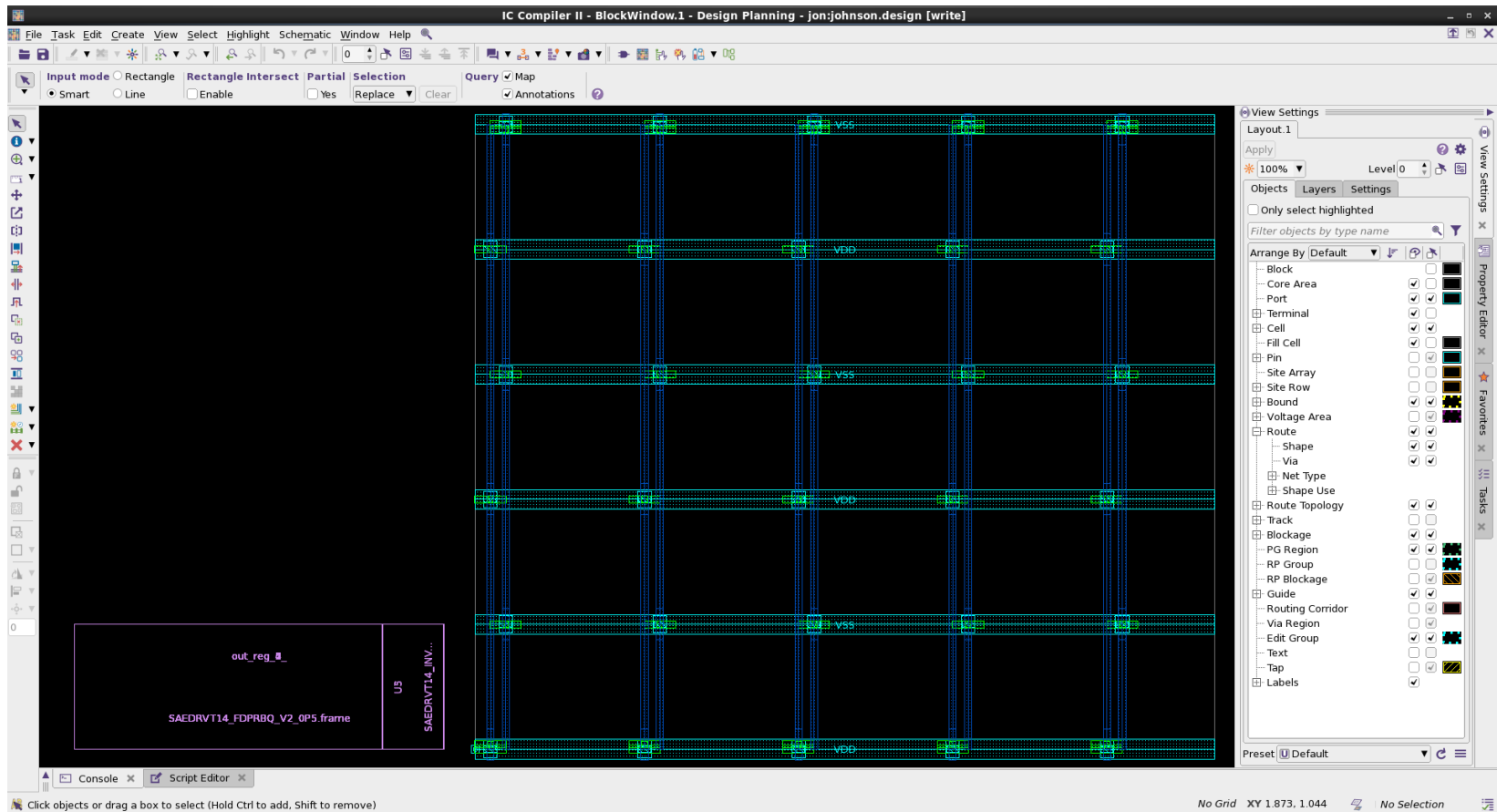


Floorplanning (2)



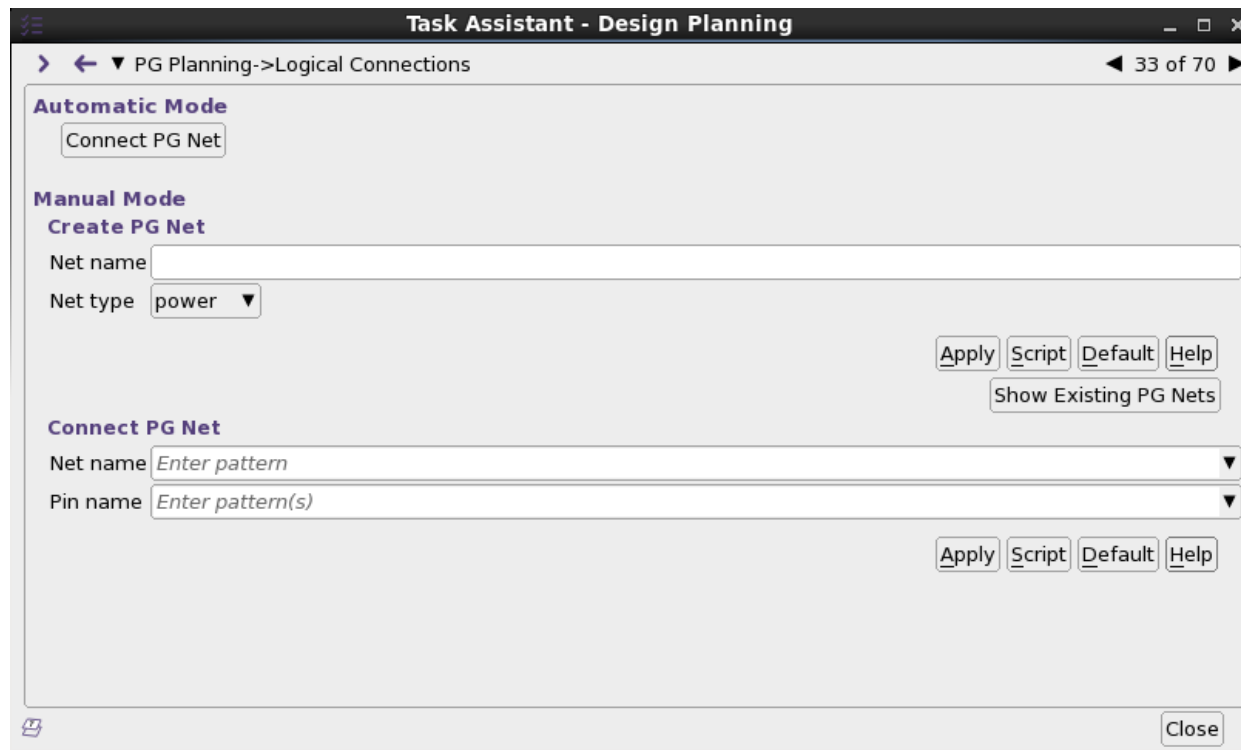
Power Straps

- Choose Task > Design Planning > Create PG

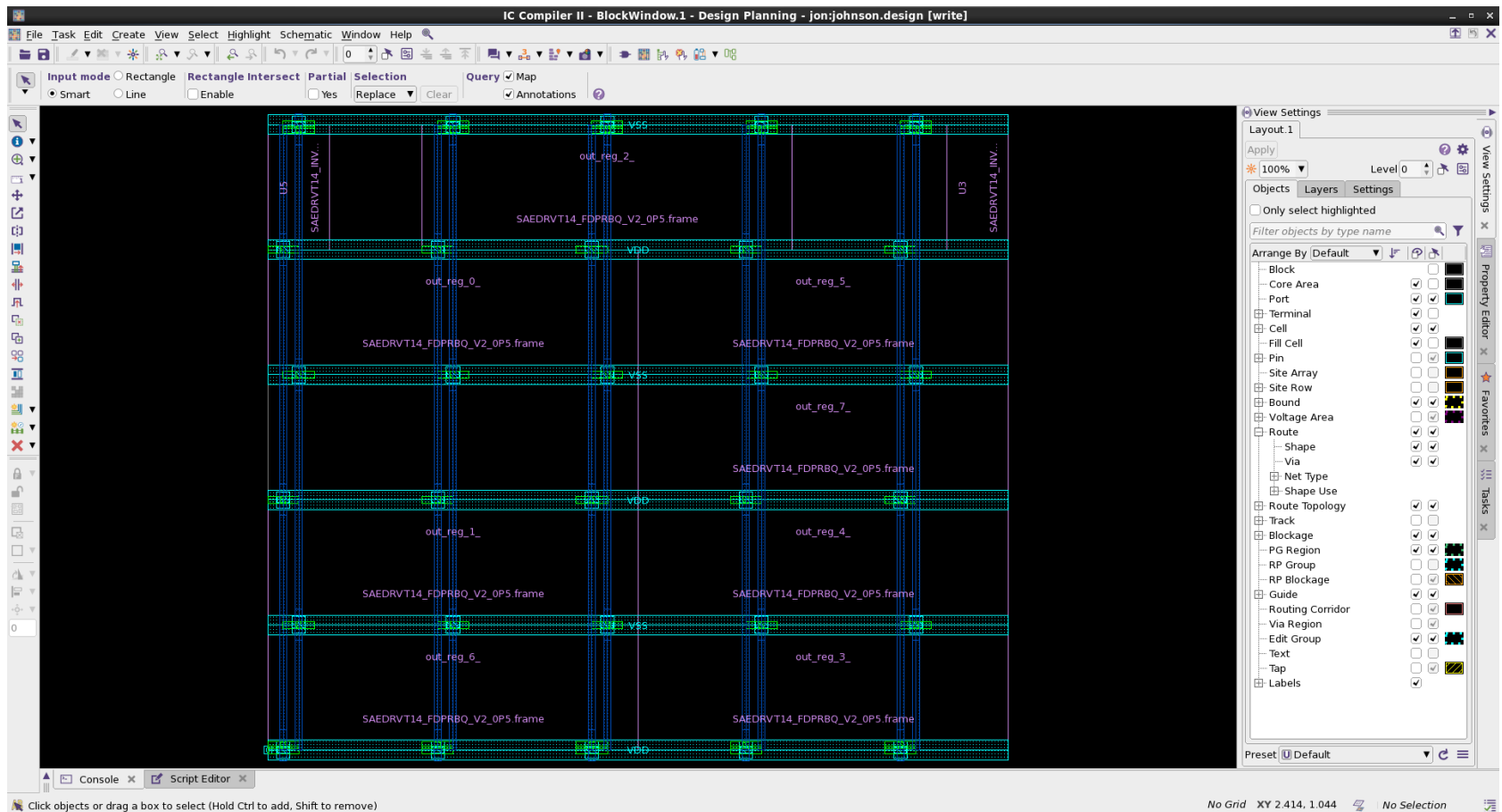


Core Placement and Optimization Dialog Box

- To run placement, choose Placement > Core Placement and Optimization Task > Placement > Placement > Create Placement



FP Placement



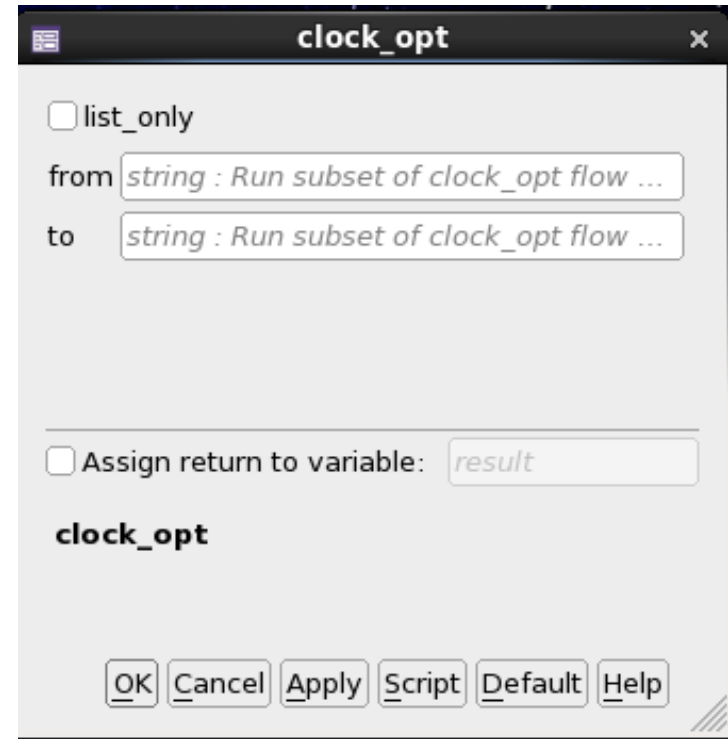
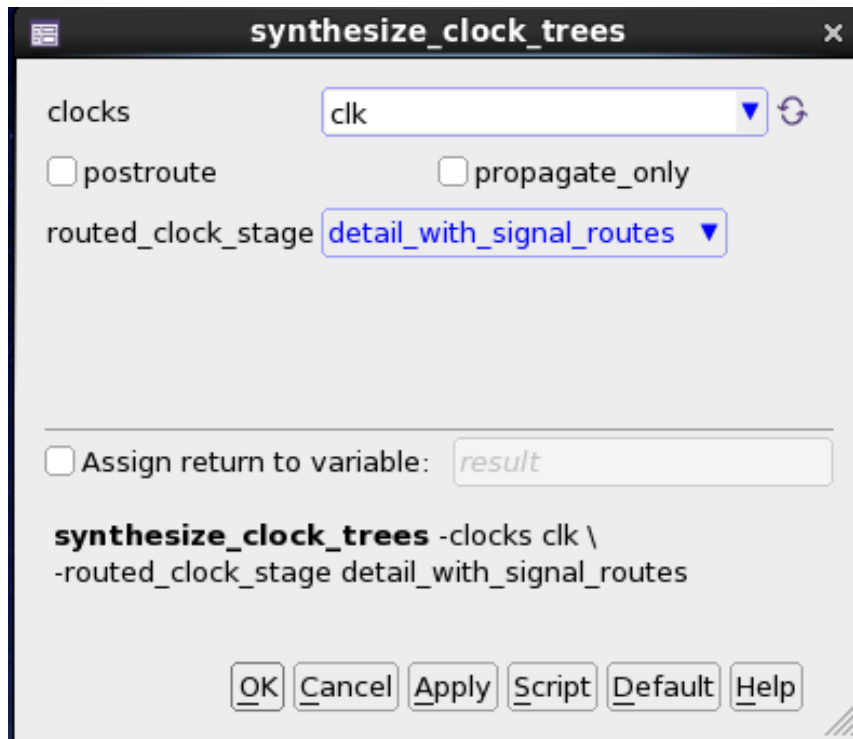
Script FRAGMENT for Placement

- Place_opt
 - -list_only
 - -from startStage
 - -to endStage

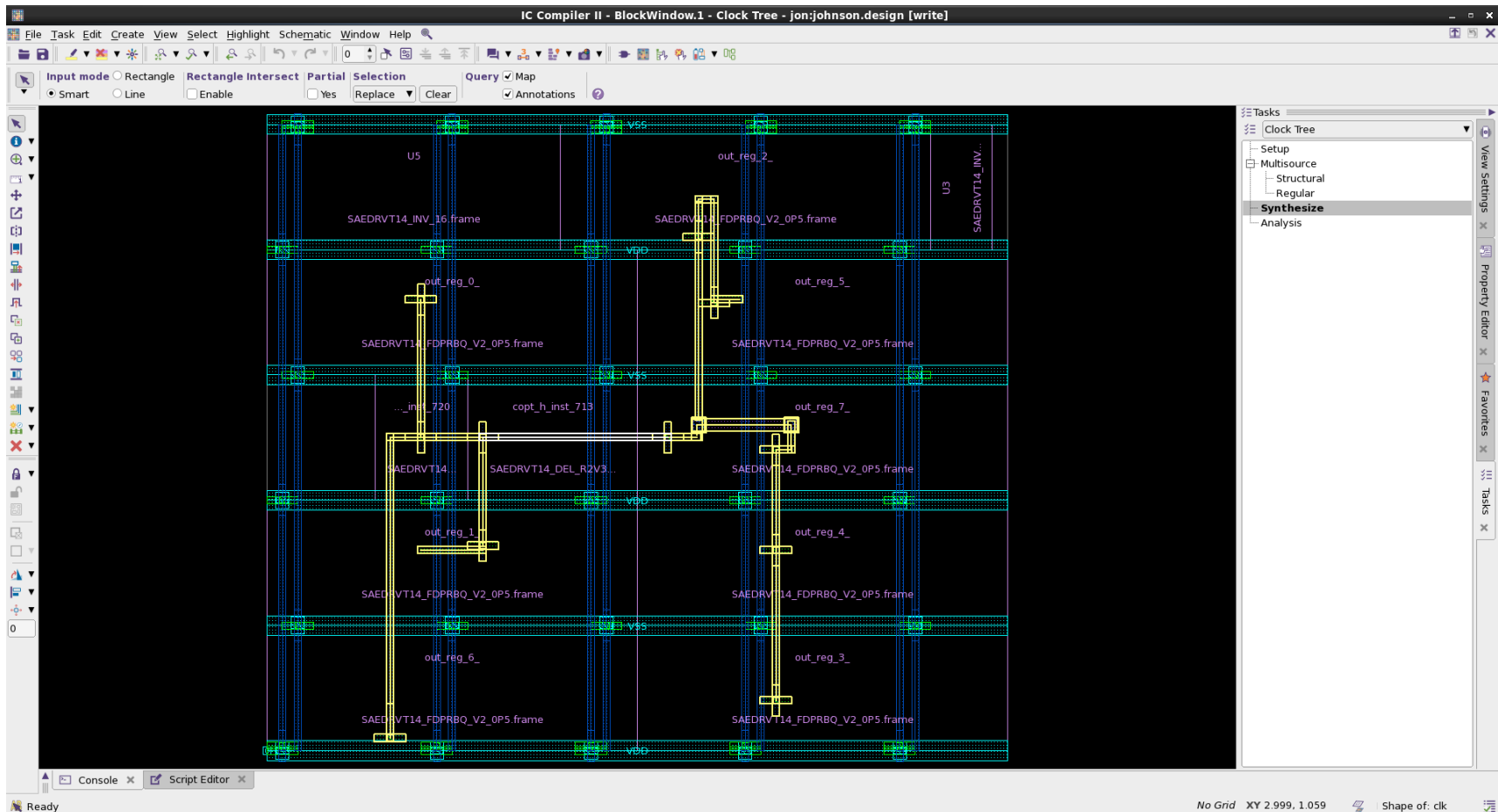


Clock Tree Synthesize

- To perform clock tree synthesis choose **Task > Clock tree > Chack Clock Trees**



Clock Tree Synthesis



Command of CTS

- clock_opt
 - ❑ -only_psyn
 - ❑ -fix_hold_all_clocks
 - ❑ -inter_clock_balance
 - ❑ -update_clock_latency
 - ❑ -operating_condition
 - ❑ -only_cts
 - ❑ -optimize_dft
 - ❑ -no_clock_route
 - ❑ -only_hold_time
 - ❑ -area_recovery
 - ❑ -size_only
 - ❑ -in_place_size_only
 - ❑ -power



Preroute Standard Cells

- From Menu bar choose Task > Routing> Create Routing Blockage

create_routing_blockage

*layers: M1

boundary: <no region>

☐ (none)

☒ net_types: ground power

☐ blockage_group_id: group_id: 0 to 99 : Assigns a blockage group identification ...

☐ zero_spacing ☐ allow_via_ladder

☒ (none) ☐ reserve_for_top_level_routing ☐ boundary_internal

☐ boundary_external ☐ allow_metal_fill_only

cell: cell : Specifies the physical cell where the routing blockage is located

name_prefix: blockage_name_prefix : Blockage name prefix

(Fields with * are required)

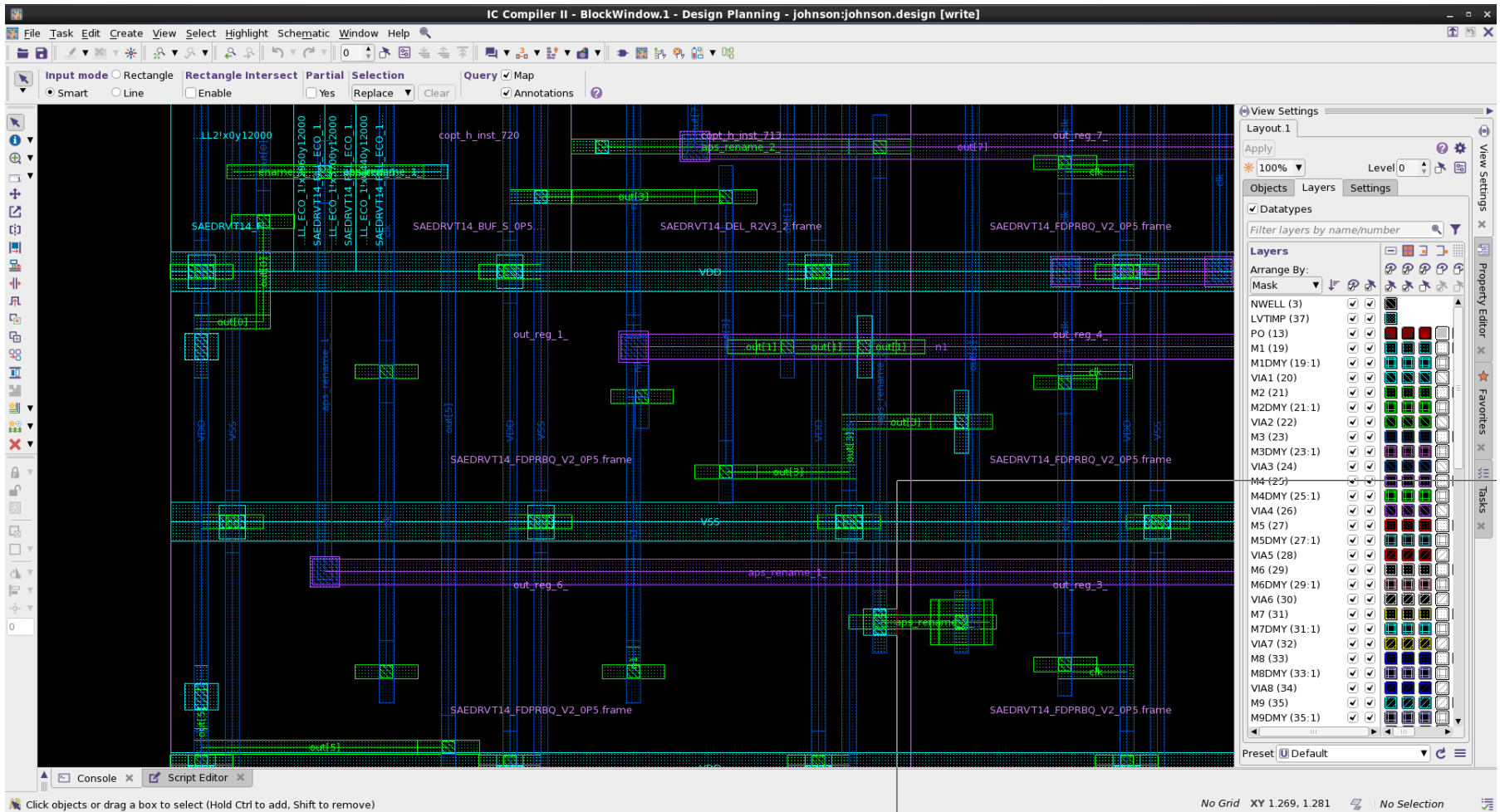
☐ Assign return to variable: result

create_routing_blockage -layers M1 -net_types {ground power}

OK Cancel Apply Script Default Help

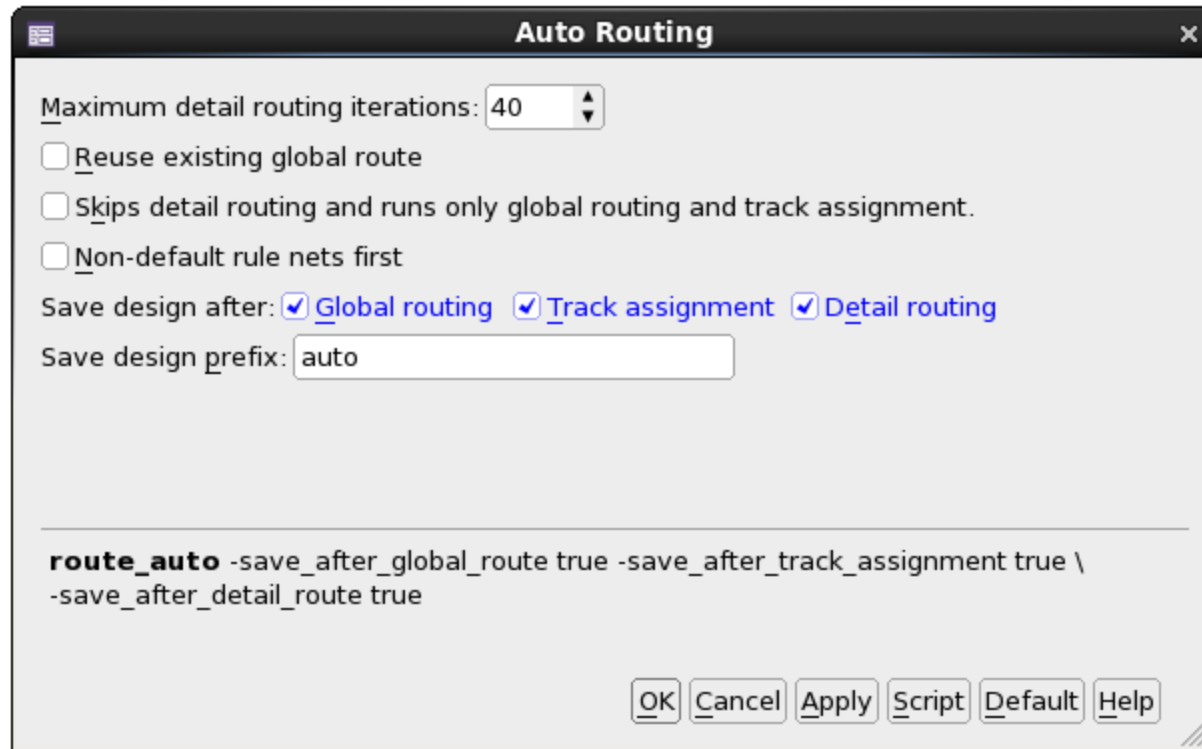


After Prerouting

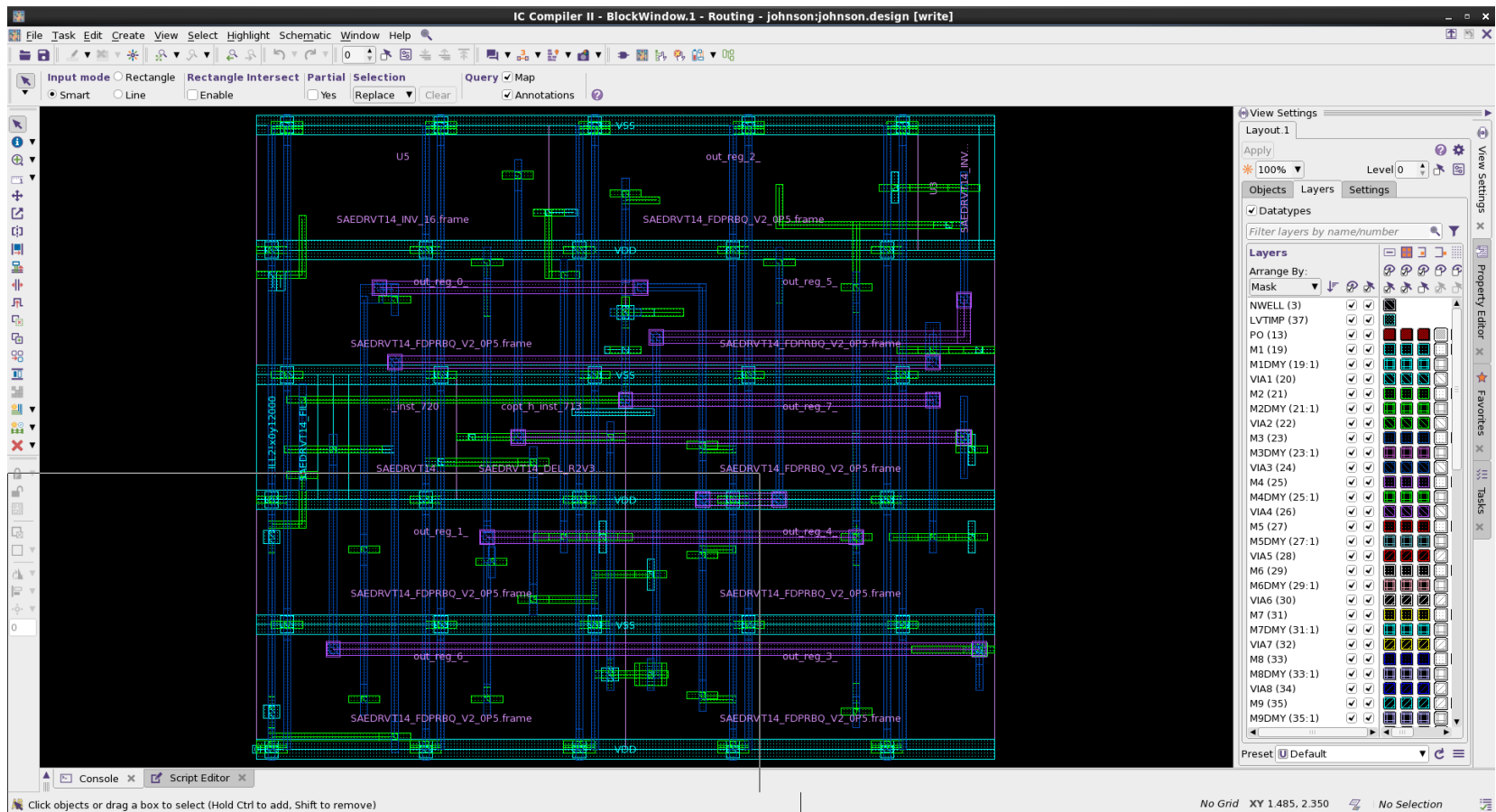


Routing from the GUI

- Choose **Route > Core Routing and Optimization**



Routing Dialog Box



Command for Routing (2)

■ route_auto

- ❑ -max_detail_route_iterations num
- ❑ -reuse_existing_global_route true | false
- ❑ -route_nondefault_nets_first true | false
- ❑ -stop_after_track_assignment true | false
- ❑ -save_after_global_route true | false
- ❑ -save_after_track_assignment true | false
- ❑ -save_after_detail_route true | false
- ❑ -save_cell_prefix name



DRC (Design Rule Checking) Box

- To check DRC errors, choose **Verification > Signoff DRC**

The screenshot shows the 'signoff_fix_drc' dialog box. It contains several input fields for configuring the Design Rule Checking (DRC) process. The 'nets' field is set to 'Net: 16'. The 'Assign return to variable' checkbox is checked, and the variable 'result' is specified. The dialog also includes a section for command-line options and a set of buttons at the bottom.

Parameter	Value
start_repair_loop	<start_loop> : Starting loop for ADR, default i...
max_number_repair_loop	<max_loops> : Maximum number of ADR loo...
coordinates	{{{llx1 lly1} {urx1 ury1}} ...} : specify a ...
excluded_coordinates	{{{llx1 lly1} {urx1 ury1}} ...} : specify a ...
nets	Net: 16
timing_preserve_setup_slack_threshold	<float> : specify setup slack threshold for ti...
select_rules	<list_of_rule_names> : check by selected rul...
unselect_rules	<list_of_rule_names> : exclude rule name(s)/...

☒ Assign return to variable:

signoff_fix_drc -nets [get_nets \
-design [current_block] {{{out[4]} VDD aps_rename_1_VSS {out[2]} n2 {out[1]} n1
{out[0]} {out[7]} r aps_rename_2_clk {out[3]} {out[5]} {out[6]}}}

OK Cancel Apply Script Default Help



LVS (Layout-Versus-Schematic) Box

- To check LVS errors, choose [Verification > LVS](#)

The screenshot shows the 'check_lvs' dialog box with the following settings:

- nets:** <no objects>
- checks:** {open short floating_routes all} : specifies items to check
- open_reporting:** (dropdown arrow)
- max_errors:** unsigned int: >= 0 : max number of errors for each type (default 20)
- check_child_cells:** ☐
- check_zero_spacing_blockages:** ☐
- check_top_level_blockages:** ☒
- report_floating_pins:** ☐
- treat_terminal_as_voltage_source:** ☐
- exclude_child_cell_types:** {collection_of_child_cell_types} : specifies cell types to ignore whe...
- Show results in the error browser:** ☒
- Assign return to variable:** result

Buttons at the bottom: OK, Cancel, Apply, Script, Default, Help.



Write Verilog Format Box

- Choose Task > Design Planning > Write Floorplan & Verilog > Verilog

The screenshot shows the 'Task Assistant - Design Planning' dialog box with the 'Verilog' tab selected. The 'Floorplan' tab is also visible. The 'Verilog' tab contains the following fields and options:

- *verilog_file_name**: `johnson_compiled.v`
- compress**: ☐ (dropdown menu)
- top_module_first**: ☐ **split_bus**: ☐ **only_master_variant**: ☐ **shell_only**: ☐
- hierarchy**: ☐ (dropdown menu)
- include**: `all` (dropdown menu)
- exclude**: `exclude_list : Exclude specified data` (dropdown menu)
- force_reference**: `blocks_and_lib_cells : Specifies blocks and lib_cells to output` (text field)
- force_no_reference**: `blocks_and_lib_cells : Specifies blocks and lib_cells to not output` (text field)
- module_list**: `modules : Write modules specified in the list` (text field)
- switch_view_list**: `views : Define the view list to find reference block for sub-block` (dropdown menu)

(Fields with * are required)

☐ Assign return to variable: `result`

write_verilog johnson_compiled.v -include all

Buttons: Apply, Script, Default, Help, Close



Write .spef Format Box

Choose **File > Export > Write Parasitics**

write_parasitics

output

☒ no_name_mapping ☒ compress ☒ hierarchical ☒ rde_corr

format

corner

☐ Assign return to variable:

write_parasitics -output Johnson.spf -no_name_mapping -compress
\
-hierarchical -rde_corr -format spfe



Write .gds Format Box

write_gds



*output_file:



bus_delimiters:

library:

design:

view:

layer_map:  

block_map:  

hierarchy:

net_property:

instance_property:

pin_property:

via_property:

via_matrix_property:

☐ long_names ☐ flat_vias ☐ compress ☐ foreign

☐ ignore_cut_datatype_tbl_mapping ☐ propagate_pin_mask_to_via_mask ☐ keep_data_type ☐ use_block_name

☐ write_instance_shape_mask ☐ write_instance_via_mask ☐ connect_below_cut_mask ☐ merge_cell_shapes

☐ merge_overwrite_conflicting_cell ☐ write_instance_blockage_mask ☐ exclude_empty_block ☐ allow_design_mismatch

☐ no_marker_layer ☐ verbose

lib_cell_view:

units:

output_pin:

☒ (none) ☐ mask_shifted_suffix ☐ mask_shifted_suffix_without_constraint

☐ mask_shifted_suffix:

☐ mask_shifted_suffix_without_constraint:

layer_map_format:

write_gds
Missing value for the required option output_file.

OK Cancel Apply Script Default Help



