SAED 90nm
Design Rules Document

Revision : 1.9
Technology : SAED90nm
Process : SAED90nm 1P9M 1.2v / 2.5v

CONTENTS

1 Introduction

This document is the part of SAED_EDK90 Design Kit documentation.
These design rules are free from intellectual property restrictions. It was considered to develop 90nm rules but sizes can be larger by 5-20% than in real processes to provide further portability of projects designed by this design rules to real processes (TSMC90nm or IBM90nm).

As basis for layer names and design rules SCN6M (TSMC 0.18) process was used described in the following site:

http://mosis.com/Technical/Layermaps/lm-scmos_scn6m.html

as well as documentation (manual_lite_v31.pdf) available at www.microwind.org .

Some layers such as dummy, marking and text, have been added to the layer map. Design rule values for 90nm process are obtained by scaling available rules values.

2 Layer Map

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
1	0	YES	Drawing	NWELL	NWELLi	NWELLi	NWELL
2	0	YES	Drawing	DNW	DNWi	DNWi	Deep NWELL
3	0	YES	Drawing	DIFF	DIFFi	DIFFi	Active area, thin oxide for device, or interconnection.
3	1	YES	Drawing	DDMY	DDMYi	DDMYi	Dummy DIFF layer; must be added if there's DIFF density rule violation.
4	0	YES	Drawing	PIMP	PIMPi	PIMPi	P+ source/drain ion implantation
5	0	YES	Drawing	NIMP	NIMPi	NIMPi	N+ source/drain ion implantation
6	0	YES	Drawing	DIFF_25	DIFF_25i	DIFF_25i	2.5v thick oxide (second gate oxide).
7	0	YES	Drawing	PAD	PADi	PADi	Bonding Pad
8	0	YES	Drawing	ESD_25	ESD_25	ESD_25	Layer for DRC and logic operation to form ESD implant. Use “ESD_25” to cover high voltage tolerant IO using 2.5V NMOS
9	0	YES	Drawing	SBLK	SBLKi	SBLKi	Resist protection oxide, non silicided area definition.
10	0	YES	Drawing	PO	POi	POi	Gate poly, poly-silicon
10	1	YES	Drawing	PODMY	PODMYi	PODMYi	Dummy PO layer, must be added if there’s PO density rule violation.
11	0	YES	Drawing	M1	M1i	M1i	Melal1
11	1	YES	Drawing	M1DMY	M1DMYi	M1DMYi	Dummy of metal1
12	0	YES	Drawing	M2	M2i	M2i	Melal2
12	1	YES	Drawing	M2DMY	M2DMYi	M2DMYi	Dummy of metal2
13	0	YES	Drawing	M3	M3i	M3i	Melal3
13	1	YES	Drawing	M3DMY	M3DMYi	M3DMYi	Dummy of metal3
14	0	YES	Drawing	M4	M4i	M4i	Melal4
14	1	YES	Drawing	M4DMY	M4DMYi	M4DMYi	Dummy of metal4
15	0	YES	Drawing	M5	M5i	M5i	Melal5
15	1	YES	Drawing	M5DMY	M5DMYi	M5DMYi	Dummy of metal5
16	0	YES	Drawing	M6	M6i	M6i	Melal6
16	1	YES	Drawing	M6DMY	M6DMYi	M6DMYi	Dummy of metal6
17	0	YES	Drawing	M7	M7i	M7i	Melal7
17	1	YES	Drawing	M7DMY	M7DMYi	M7DMYi	Dummy of metal7
18	0	YES	Drawing	M8	M8i	M8i	Melal8
18	1	YES	Drawing	M8DMY	M8DMYi	M8DMYi	Dummy of metal8
19	0	YES	Drawing	M9	M9i	M9i	Melal9
19	1	YES	Drawing	M9DMY	M9DMYi	M9DMYi	Dummy of metal9
20	0	YES	Drawing	CO	COi	COi	Contact
21	0	YES	Drawing	VIA1	VIA1i	VIA1i	Via12
22	0	YES	Drawing	VIA2	VIA2i	VIA2i	Via23
23	0	YES	Drawing	VIA3	VIA3i	VIA3i	Via34
24	0	YES	Drawing	VIA4	VIA4i	VIA4i	Via45
25	0	YES	Drawing	VIA5	VIA5i	VIA5i	Via56
26	0	YES	Drawing	VIA6	VIA6i	VIA6i	Via67
27	0	YES	Drawing	VIA7	VIA7i	VIA7i	Via78
28	0	YES	Drawing	VIA8	VIA8i	VIA8i	Via89
29	0	YES	Drawing	HVTIMP	HVTIMPi	HVTIMPi	Implant layer for hvt nmos/pmos drawing
30	0	YES	Drawing	LVTIMP	LVTIMPi	LVTIMPi	Implant layer for lvt nmos/pmos drawing
31	0	NO	Drawing	M1PIN	M1PIN	M1PIN	Metal1 text layer
32	0	NO	Drawing	M2PIN	M2PIN	M2PIN	Metal2 text layer
33	0	NO	Drawing	M3PIN	M3PIN	M3PIN	Metal3 text layer
34	0	NO	Drawing	M4PIN	M4PIN	M4PIN	Metal4 text layer
35	0	NO	Drawing	M5PIN	M5PIN	M5PIN	Metal5 text layer
36	0	NO	Drawing	M6PIN	M6PIN	M6PIN	Metal6 text layer

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
37	0	NO	Drawing	M7PIN	M7PIN	M7PIN	Metal7 text layer
38	0	NO	Drawing	M8PIN	M8PIN	M8PIN	Metal8 text layer
39	0	NO	Drawing	M9PIN	M9PIN	M9PIN	Metal9 text layer
40	0	NO	N/A				Reserved layer.
41	0	NO	Drawing	HOTNWL	HOTNWLi	HOTNWLi	Hot NWELL marking layer for DRC. Use “HOTNWL” to cover hot-NWEL width.
42	0	NO	N/A				Reserved layer.
43	0	NO	Drawing	DIOD	DIODi	DIODi	Diode marking layer for LVS. Cover P+DIFF for P+/NWELL diode, N+DIFF for N+/PWELL diode, and NWELL for NWELL/PWELL diode.
44	0	NO	Drawing	BJTDMY	BJTDMYi	BJTDMYi	BJT marking layer to cover BJT device for analog layout rules.
45	0	NO	Drawing	RNW	RNWi	RNWi	NWELL resistor marking layer for DRC and LVS.
46	0	NO	Drawing	RPOLY	RPOLYi	RPOLYi	Poly resistor marking layer for LVS. The cutting edge of RPOLY over PO determines W/L of resistors.
47	0	NO	Drawing	RDIFF	RDIFFi	RDIFFi	DIFF resistor marking layer for LVS. The cutting edge of RDIFF over DIFF determines W/L of resistors.
48	0	NO	Drawing	LOGO	LOGO		DRC dummy layer for product label and logo
49	0	NO	Drawing	IP	IP		IP tagging text layer
50	0	NO	Drawing	prBoundary			prBoundary – P&R cell boundary
51	0	NO	Drawing	RM1	RM1i	RM1i	Metal1 resistor marking layer for LVS. The cutting edge of RM1 over metals determines W/L of metal resistors.
52	0	NO	Drawing	RM2	RM2i	RM2i	Metal2 resistor marking layer for LVS. The cutting edge of RM2 over metals determines W/L of metal resistors.
53	0	NO	Drawing	RM3	RM3i	RM3i	Metal3 resistor marking layer for LVS. The cutting edge of RM3 over metals determines W/L of metal resistors.
54	0	NO	Drawing	RM4	RM4i	RM4i	Metal4 resistor marking layer for LVS. The cutting edge of RM4 over metals determines W/L of metal resistors.
55	0	NO	Drawing	RM5	RM5i	RM5i	Metal5 resistor marking layer for LVS. The cutting edge of RM5 over metals determines W/L of metal resistors.
56	0	NO	Drawing	RM6	RM6i	RM6i	Metal6 resistor marking layer for LVS. The cutting edge of RM6 over metals determines W/L of metal resistors.
57	0	NO	Drawing	RM7	RM7i	RM7i	Metal7 resistor marking layer for LVS. The cutting edge of RM7 over metals determines W/L of metal resistors.
58	0	NO	Drawing	RM8	RM8i	RM8i	Metal8 resistor marking layer for LVS. The cutting edge of RM8 over metals determines W/L of metal resistors.
59	0	NO	Drawing	RM9	RM9i	RM9i	Metal9 resistor marking layer for LVS. The cutting edge of RM9 over metals determines W/L of metal resistors.
60	0	NO	N/A				Reserved layer.
61	0	NO	Drawing	DM1EXCL	DM1EXCLi		Dummy layer to avoid dummy metal1 insertion, used in dummy metal insertion utility.
62	0	NO	Drawing	DM2EXCL	DM2EXCLi		Dummy layer to avoid dummy metal2 insertion, used in dummy metal insertion utility.

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
63	0	NO	Drawing	DM3EXCL	DM3EXCLi		Dummy layer to avoid dummy metal3 insertion, used in dummy metal insertion utility.
64	0	NO	Drawing	DM4EXCL	DM4EXCLi		Dummy layer to avoid dummy metal4 insertion, used in dummy metal insertion utility.
65	0	NO	Drawing	DM5EXCL	DM5EXCLi		Dummy layer to avoid dummy metal5 insertion, used in dummy metal insertion utility.
66	0	NO	Drawing	DM6EXCL	DM6EXCLi		Dummy layer to avoid dummy metal6 insertion, used in dummy metal insertion utility.
67	0	NO	Drawing	DM7EXCL	DM7EXCLi		Dummy layer to avoid dummy metal7 insertion, used in dummy metal insertion utility.
68	0	NO	Drawing	DM8EXCL	DM8EXCLi		Dummy layer to avoid dummy metal8 insertion, used in dummy metal insertion utility.
69	0	NO	Drawing	DM9EXCL	DM9EXCLi		Dummy layer to avoid dummy metal9 insertion, used in dummy metal insertion utility.
70	0	NO	Drawing	VARMARK	VARMARKi	VARMARKi	Varactor marking layer for LVS.
71	0	NO	Drawing	INDMARK	INDMARKi	INDMARKi	Inductor marking layer for LVS.
72	0	NO	Drawing	CBMMARK	CBMMARKi	CBMMARKi	Capacitor bottom marking layer for LVS.
73	0	NO	Drawing	CTMMARK	CTMMARKi	CTMMARKi	Capacitor top marking layer for LVS.
74	0	NO	Drawing	CAPDAMY	CAPDAMYi	CAPDAMYi	Capacitor dummy layer for LVS.
75	0	NO	Drawing	PWELL	PWELLi	PWELLi	Pwell

3 Design Rules

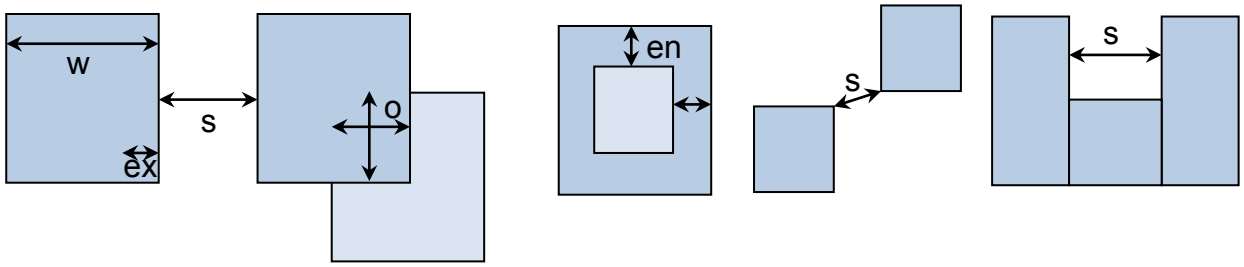


Figure 1. Definitions of layout geometrical terminology

w: Width
distance between inside parts of the same layer
s: Space
distance between outside of the edge of 1st layer and outside of the edge of 2nd layer
o: Overlap
distance between inside of the edge of 1st layer and inside of the edge of 2nd layer
en: Enclosure
distance between inside of the edge of 1st layer and outside of the edge of 2nd layer
ex: Extension
distance between inside of the edge of 1st layer and outside of the edge of 2nd layer

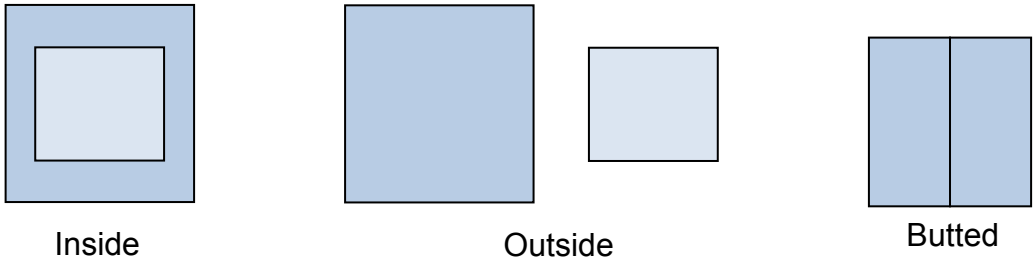


Figure 2. Object relationships

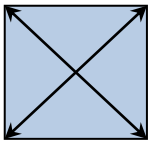


Figure 3. Area

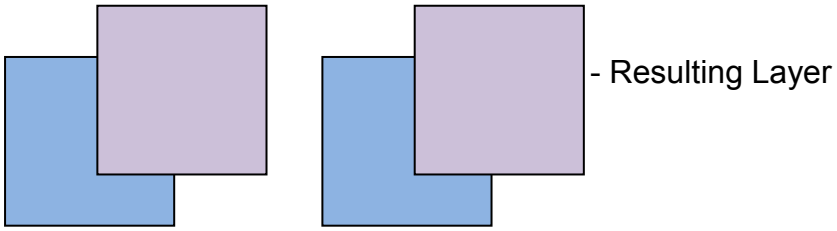


Figure 4. AND

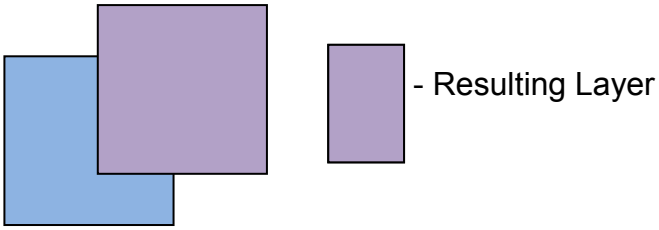


Figure 5. OR

Logic layers, generated during DRC and LVS from physical layers using Boolean operations

IMP = PIMP **or** NIMP
NDIFF = DIFF **and** NIMP
PDIFF = DIFF **and** PIMP
N+Active = NDIFF **and** PWELL
P+Active = PDIFF **and** NWELL
ACTIVE = P+Active **or** N+Active
PTAP = PDIFF **and** PWELL
NTAP = NDIFF **and** NWELL
TAP = PTAP **or** NTAP
GATE = POLY **and** ACTIVE
NGATE = POLY **and** NACTIVE
PGATE = POLY **and** PACTIVE

Chanel width

Chanel length

Figure 6. Chanel

Table 1. DIFF Rules

Rule #	Rule description	μm	Mark
DIFF.W.1	Minimum width	0.12	a
DIFF.S.1	Minimum spacing	0.14	b
DIFF.S.2	Minimum spacing in DIFF_25	0.18	c
DIFF.E.1	Source/drain active to well edge (min enclosure by well)	0.24	d
DIFF.E.2	Substrate/well contact diff to well edge (min enclosure by well)	0.2	e
DIFF.R.1	DIFF w/o IMP is not allowed		
DIFF.A.1	Minimum area	0.08^2	f

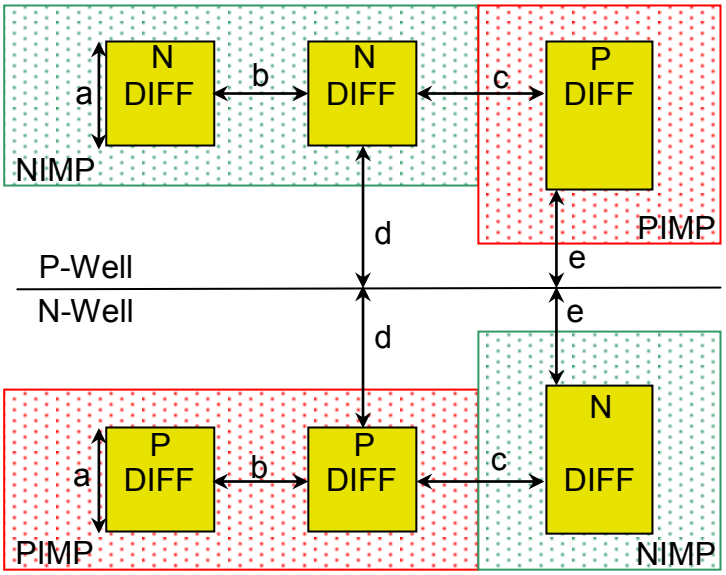


Figure 7. DIFF

Table 2. DIFF_25 Rules

Rule #	Rule description	μm	Mark
DIFF_25.W.1	Minimum width	0.66	a
DIFF_25.S.1	Minimum Spacing	0.66	b
DIFF_25.S.2	Minimum space to external DIFF	0.3	c
DIFF_25.E.1	Minimum DIFF enclosure	0.3	d

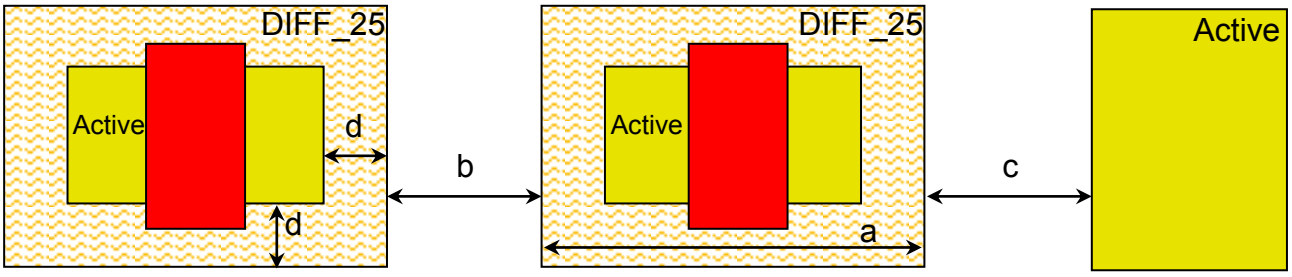


Figure 8. DIFF_25

Table 3. PO Rules

Rule #	Rule description	μm	Mark
PO.W.1	Minimum width	0.1	a
PO.W.2	Minimum poly width in a thick oxide gate	0.3	b
PO.S.1	Minimum spacing over field	0.18	c
PO.S.2	Minimum spacing over active	0.2	d
PO.EX.1	Minimum gate extension of active (end cap)	0.18	e
PO.EX.2	Minimum active extension of gate	0.16	f
PO.S.3	Minimum field poly to DIFF	0.05	g
PO.G.1	45 degree and 90 degree bent gate are not allowed		

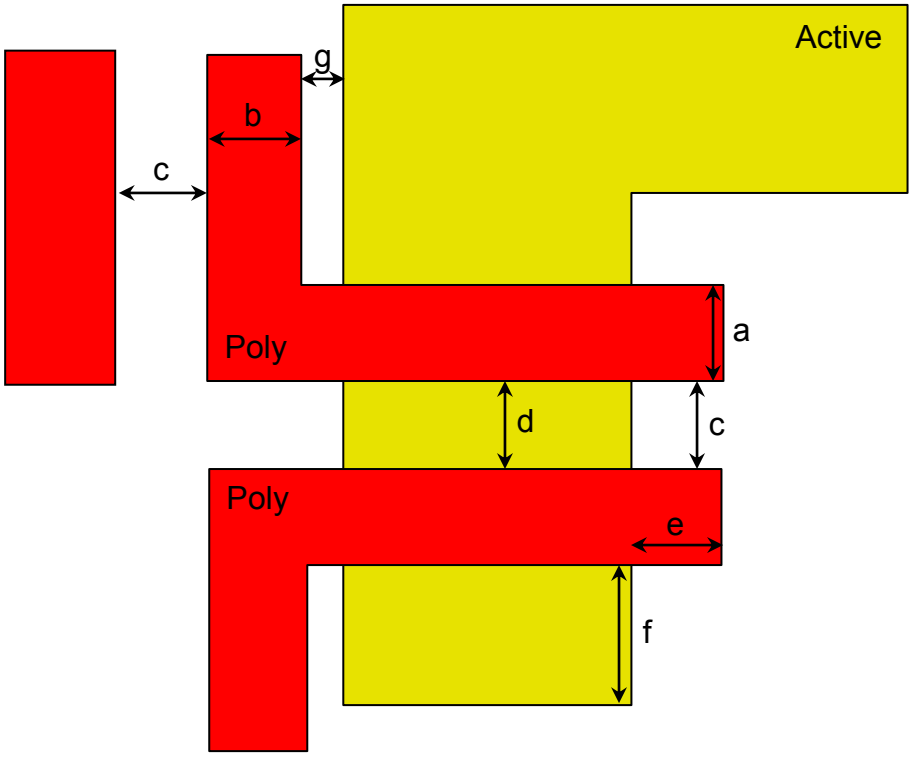


Figure 9. PO

Table 4. CO Rules

Rule #	Rule description	μm	Mark
CO.W.1	Exact contact size	0.13	a
CO.S.1	Minimum contact spacing	0.13	b
CO.S.2	(Contact inside DIFF) space to gate	0.12	c
CO.S.3	(Contact inside Poly) space to Active	0.12	d
CO.E.1	Minimum enclosure by poly	0.04	e
CO.E.2	Minimum enclosure by DIFF	0.04	f
CO.E.3	Minimum enclosure by poly at least two apposite sides	0.05	g
CO.E.4	Minimum enclosure by DIFF at least two apposite sides	0.05	h
CO.E.5	Minimum butted diffusion IMP enclosure of S/D contact	0.06	i
CO.E.6	Minimum enclosure of any contact (CO outside M1 is not allowed)	0.005	j
CO.E.7	Minimum enclosure of contact at end of line	0.05	k

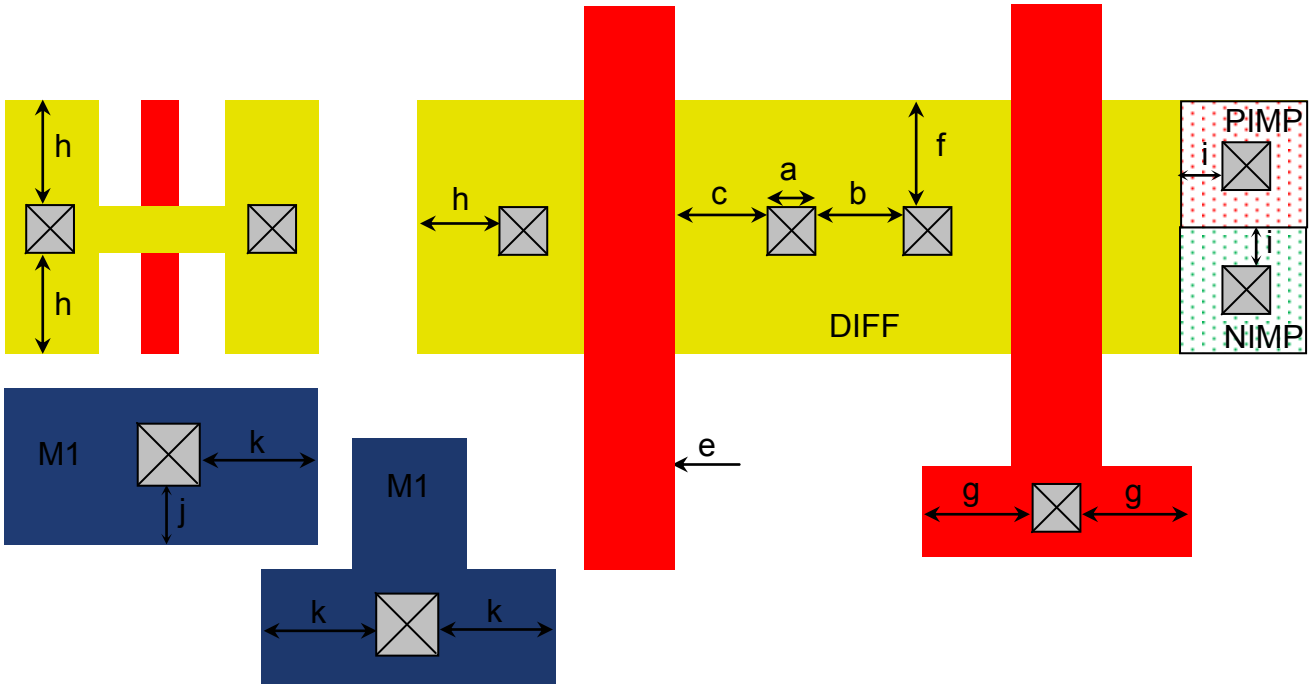


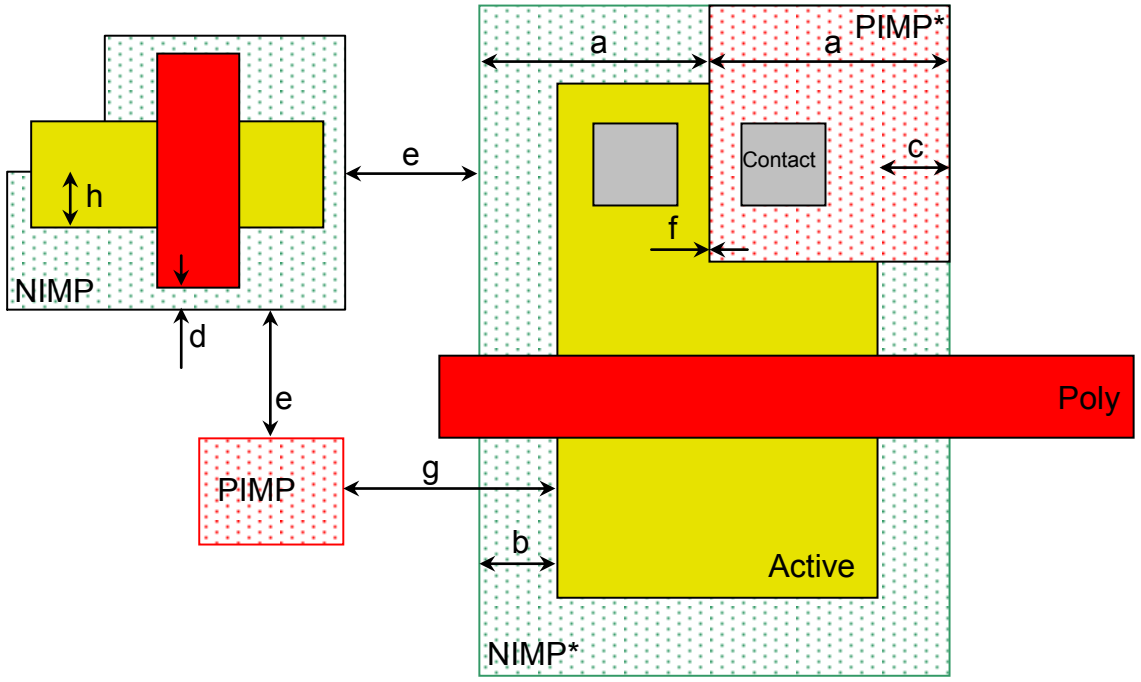
Figure 10. CO

Table 5. PIMP Rules

Rule #	Rule description	μm	Mark
PIMP.W.1	Minimum width	0.24	a
PIMP.E.1	Enclosure of P+Active	0.14	b
PIMP.E.2	Enclosure of PTAP	0.04	c
PIMP.E.3	Poly enclosure		d
PIMP.S.1	Minimum space	0.24	e
PIMP.S.2	Minimum space to butted N+Active	0	f
PIMP.S.3	Minimum space to N+Active in PWELL	0.14	g
PIMP.O.1	Minimum active overlap	0.14	h

Table 6. NIMP Rules

Rule #	Rule description	μm	Mark
NIMP.W.1	Minimum width	0.24	a
NIMP.E.1	Enclosure of N+Active	0.14	b
NIMP.E.2	Enclosure of NTAP	0.04	c
NIMP.E.3	Poly enclosure		d
NIMP.S.1	Minimum space	0.24	e
NIMP.S.2	Minimum space to butted P+Active	0	f
NIMP.S.3	Minimum space to P+Active in NWELL	0.14	g
NIMP.O.1	Minimum active overlap	0.14	h



* The same rules apply to N+_inplant

Figure 11. PIMP, NIMP

Table 7. HVTIMP Rules

Rule #	Rule description	μm	Mark
HVTIMP.W.1	Minimum width	0.24	a
HVTIMP.S.1	Minimum spacing	0.24	b
HVTIMP.E.1	Minimum enclosure	0.14	c

Table 8. LVTIMP Rules

Rule #	Rule description	μm	Mark
LVTIMP.W.1	Minimum width	0.24	a
LVTIMP.S.1	Minimum spacing	0.24	b
LVTIMP.E.1	Minimum enclosure	0.14	c

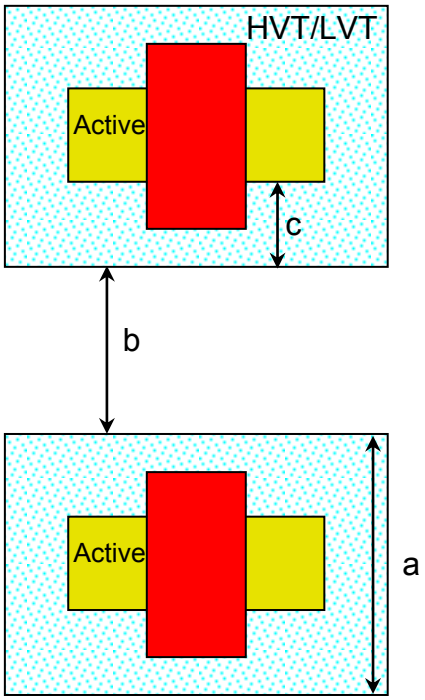


Figure 12. HVTIMP, LVTIMP

Table 9. NWELL Rules

Rule #	Rule description	μm	Mark
NWELL.W.1	Minimum width	0.65	a
NWELL.S.1	Minimum spacing between wells at same potential	0.65	b
NWELL.S.2	Minimum spacing between wells at different potential	1.2	c

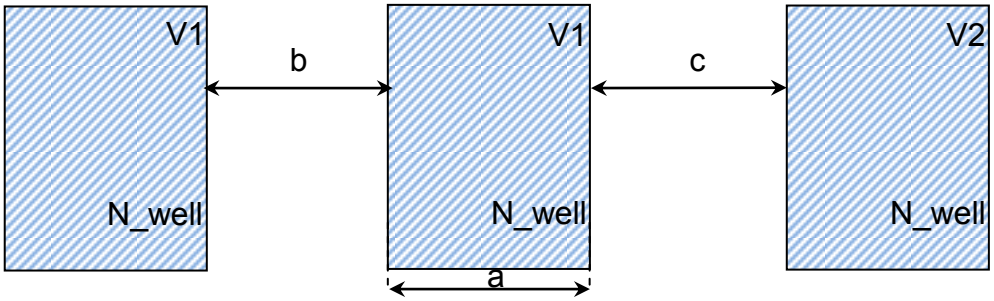


Figure 13. NWELL

Table 10. DNW Rules

Rule #	Rule description	μm	Mark
DNW.W.1	Minimum width	3.5	a
DNW.S.1	Minimum spacing, Deep_N_Well to Deep_N_Well	5	b
DNW.S.2	Minimum spacing, Deep_N_Well to unrelated N_Well	3.5	c
DNW.S.3	Minimum spacing, external N+Active to Deep_N_Well	2	d
DNW.S.4	Minimum spacing, P+Active in N_Well to its Deep_N_Well	1	e
DNW.E.1	Minimum enclosure, N+Active by isolated P-well	0.7	f
DNW.E.2	Minimum enclosure, N_Well beyond Deep_N_Well edge	1.5	g
DNW.O.1	Minimum overlap, N_Well over Deep_N_Well edge	0.5	h

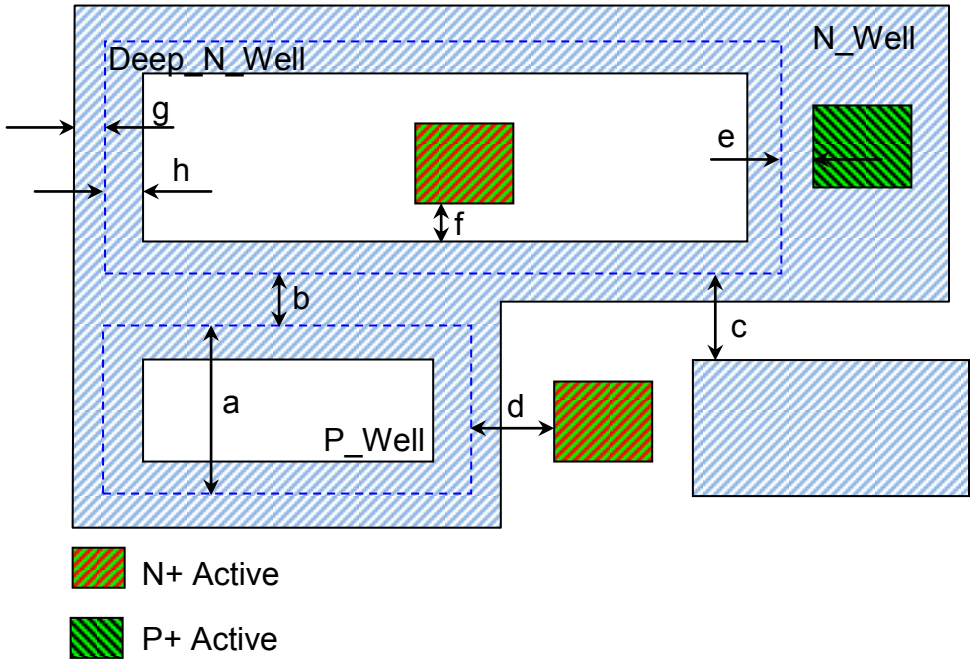


Figure 14. DNW

Table 11. M1 Rules

Rule #	Rule description	μm	Mark
M1.W.1	Minimum width	0.14	a
M1.S.1	Minimum spacing	0.14	b
M1.S.2	Minimum spacing when either metal line is wider than 5 μm	0.25	c
M1.A.1	Minimum area	0.14^2	d

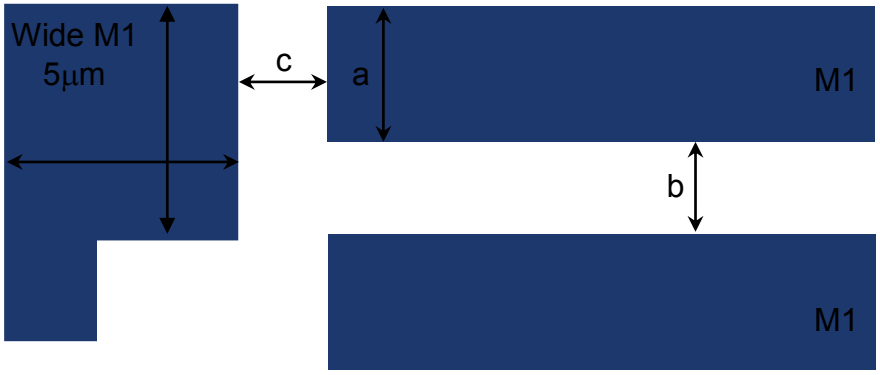


Figure 15. M1

Table 12. MX Rules, where X=2...T-1

Rule #	Rule description	μm	Mark
MX.W.1	Minimum width	0.16	a
MX.S.1	Minimum spacing	0.16	b
MX.S.2	Minimum spacing when either metal line is wider than 5 μ_m	1.5	c

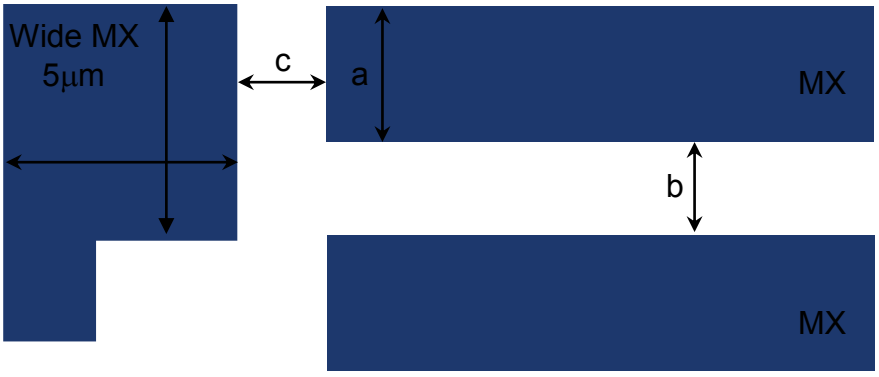


Figure 16. MX

Table 13. VIAX Rules, where X=1..T-2

Rule #	Rule description	μm	Mark
VIAX.W.1	Exact size	0.14	a
VIAX.S.1	Minimum viaX spacing	0.24	b
VIAX.E.1	Minimum viaX enclosure by MX and MX+1	0.005	c
VIAX.E.2	Minimum viaX enclosure by MX and MX+1 at end of line	0.05	d

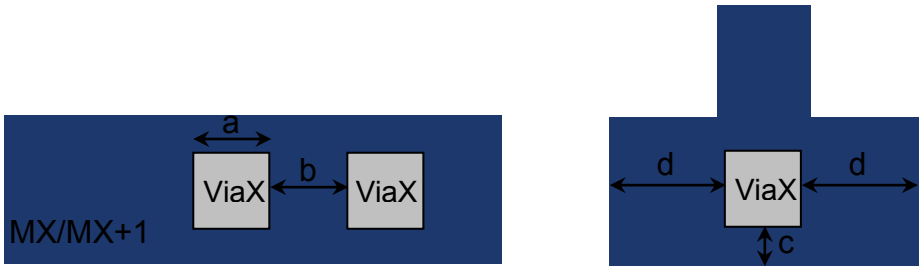


Figure 17. VIAX

Table 14. VIAT Rules

Rule #	Rule description	μm	Mark
VIAT.W.1	Exact size	0.36	a
VIAT.S.1	Minimum viaX spacing	0.34	b
VIAT.E.1	Minimum VIAT enclosure by MT and MT-1	0.05	c
VIAT.E.2	Minimum VIAT enclosure by MT and MT-1 at end of line	0.08	d

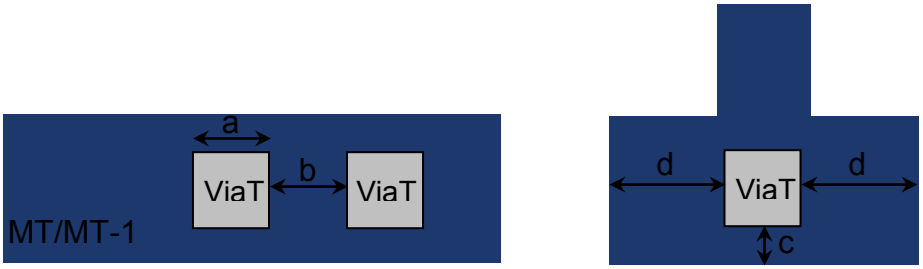


Figure 18. VIAT

Table 15. SBLK Rules

Rule #	Rule description	μm	Mark
SBLK.W.1	Minimum SBLK width	0.44	a
SBLK.S.1	Minimum SBLK spacing	0.44	b
SBLK.S.2	Minimum spacing, SBLK to contact (no contacts allowed inside SBLK)	0.24	c
SBLK.S.3	Minimum spacing, SBLK to external diff	0.24	d
SBLK.S.4	Minimum spacing, SBLK to external poly	0.3	e
SBLK.S.5	Minimum spacing of poly resistors (in a single SBLK region)	0.3	f
SBLK.S.6	Minimum spacing, SBLK to poly (in a single active region)	0.4	g
SBLK.W.2	Minimum poly width in unsalicided resistor	0.39	h
SBLK.O.1	Minimum SBLK extension of poly or active	0.24	i
SBLK.O.2	Minimum poly extension of SBLK	0.24	j
SBLK.C.1	Resistor is poly inside SBLK: poly ends stick out for contacts the entire resistor must be outside well and over field		

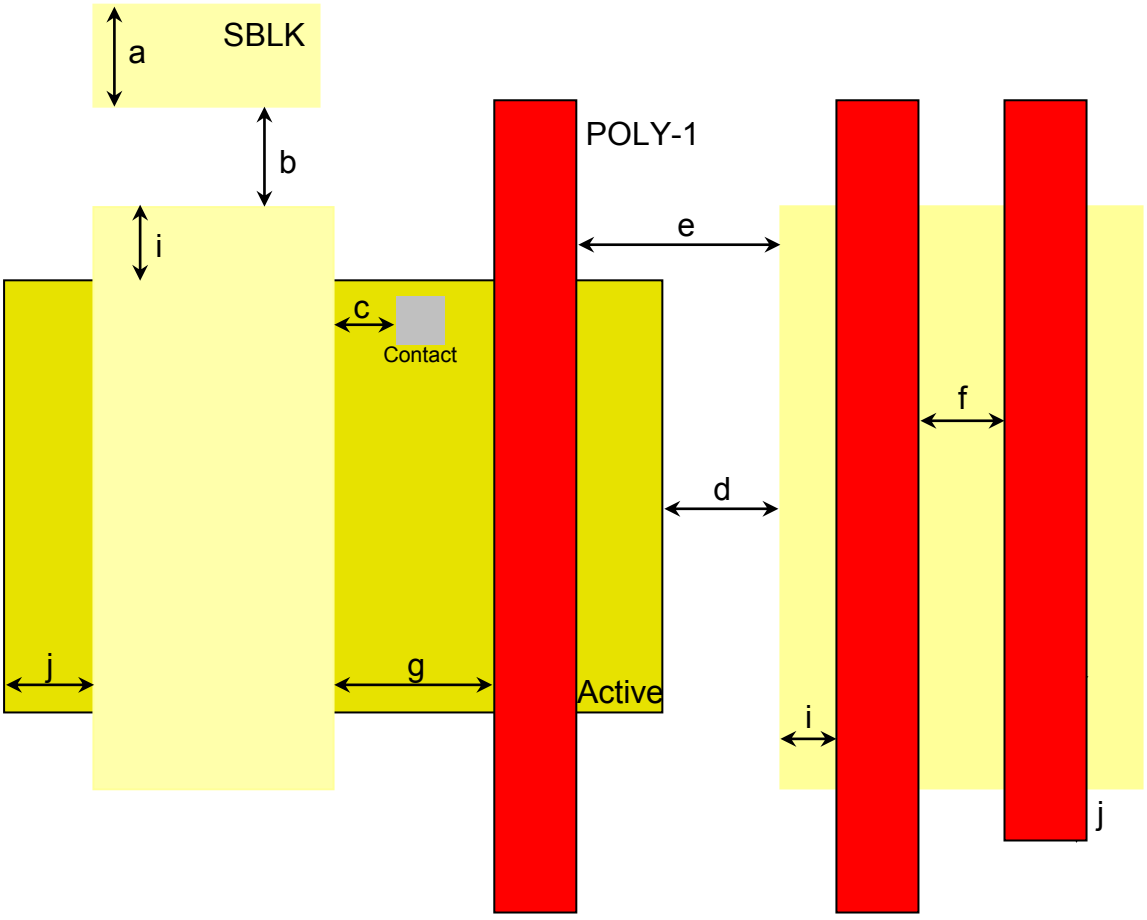
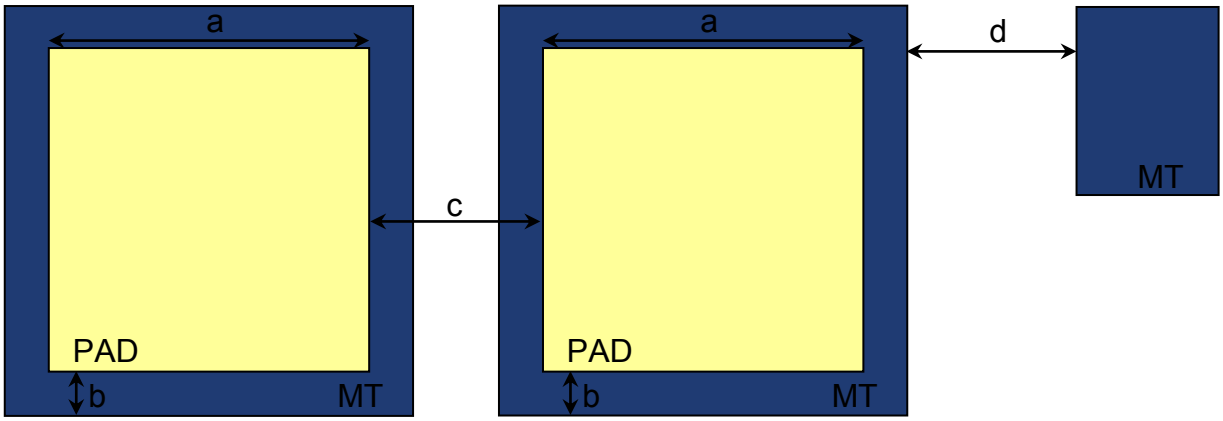


Figure 19. SBLK

Table 16. PAD Rules

Rule #	Rule description	μm	Mark
PAD.W.1	Minimum bonding passivation opening	60	a
PAD.E.1	Pad metal enclose of passivation	2	b
PAD.S.1	Minimum space	10	c
PAD.S.2	Minimum pad metal spacing to unrelated metal	3	d



* “Pad” metal is illustrated as MT (topmost metal layer)

Figure 20. PAD