

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4515B **MSI**

1-of-16 decoder/demultiplexer with
input latches

Product specification
File under Integrated Circuits, IC04

January 1995

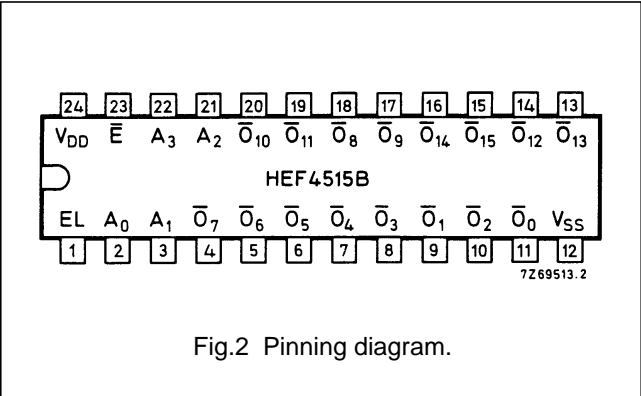
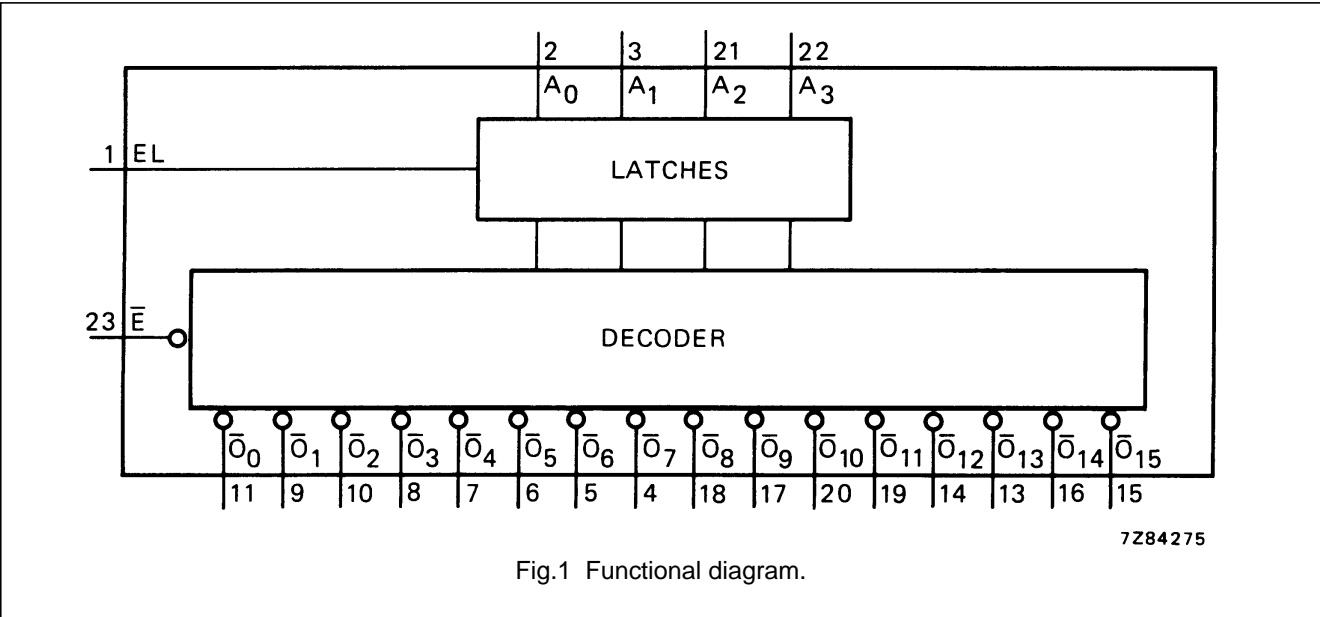
1-of-16 decoder/demultiplexer with input latches

HEF4515B
MSI

DESCRIPTION

The HEF4515B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input (\overline{E}). The 16 outputs (\overline{O}_0 to \overline{O}_{15}) are mutually exclusive active LOW. When EL is HIGH, the selected output is determined by the data on A_n . When EL goes LOW, the last data

present at A_n are stored in the latches and the outputs remain stable. When \overline{E} is LOW, the selected output, determined by the contents of the latch, is LOW. At \overline{E} HIGH, all outputs are HIGH. The enable input (\overline{E}) does not affect the state of the latch. When the HEF4515B is used as a demultiplexer, \overline{E} is the data input and A_0 to A_3 are the address inputs.



PINNING

- A_0 to A_3
- address inputs
- \overline{E}
- enable input (active LOW)
- EL
- latch enable input
- \overline{O}_0 to \overline{O}_{15}
- outputs (active LOW)

- HEF4515BP(N): 24-lead DIL; plastic (SOT101-1)
- HEF4515BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
- HEF4515BT(D): 24-lead SO; plastic (SOT137-1)
- (): Package Designator North America

APPLICATION INFORMATION

Some examples of applications for the HEF4515B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

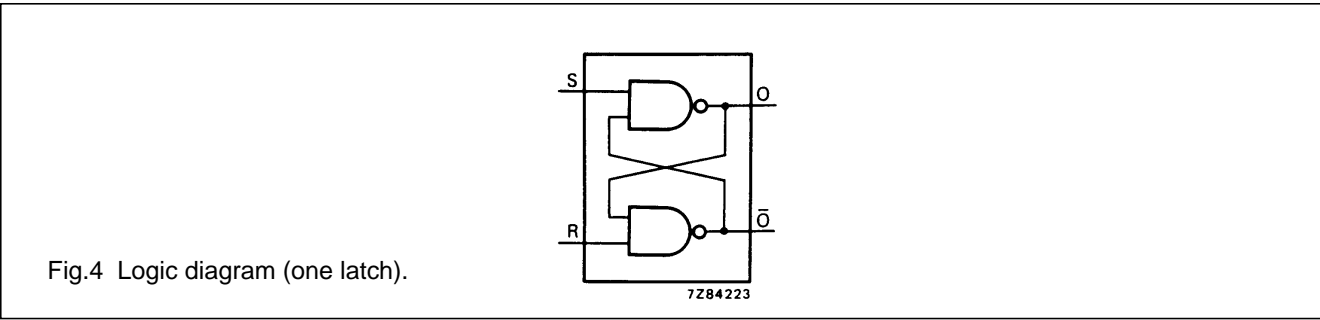
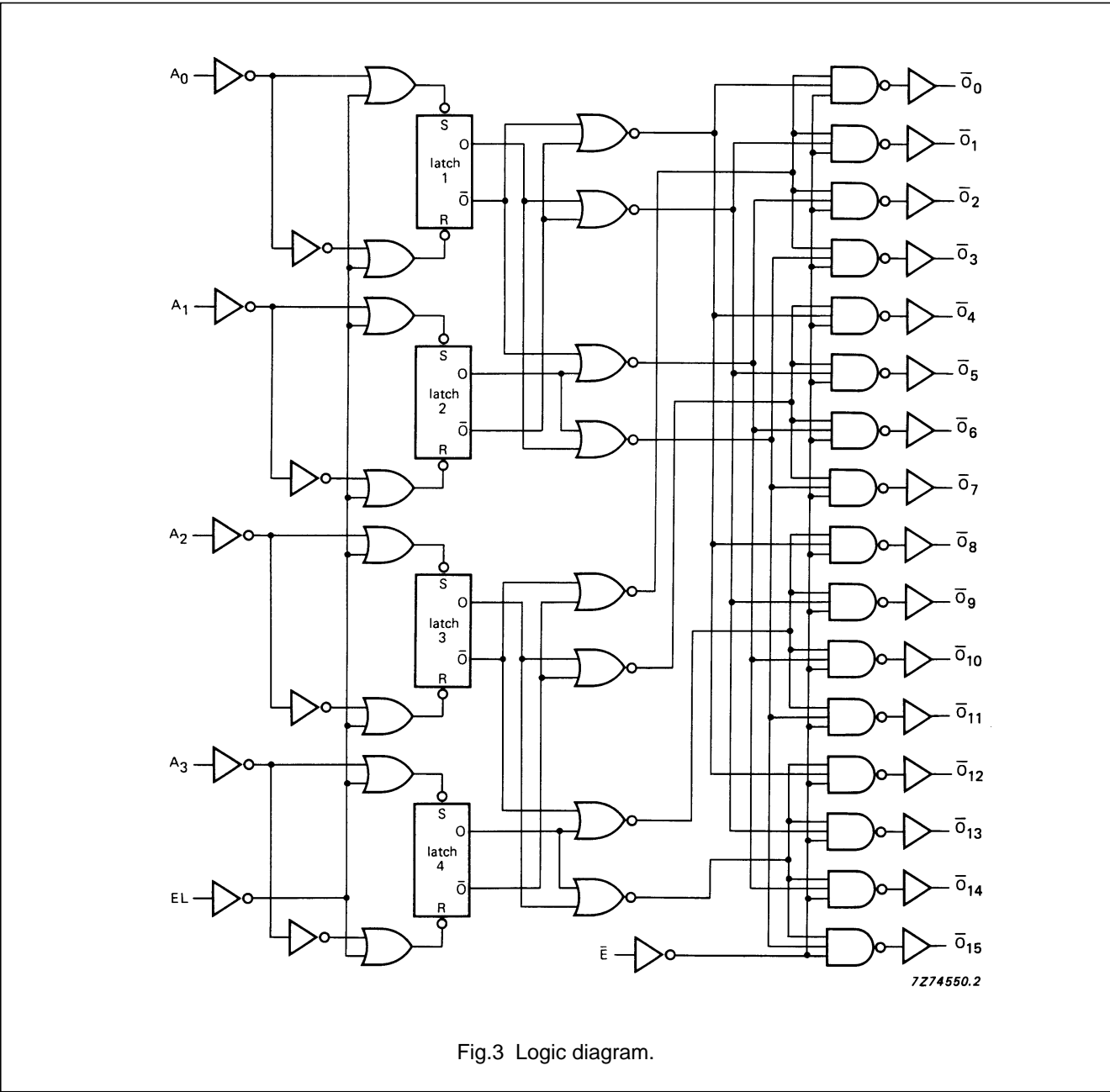
FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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TRUTH TABLE

INPUTS					OUTPUTS															
\overline{E}	A_0	A_1	A_2	A_3	\overline{O}_0	\overline{O}_1	\overline{O}_2	\overline{O}_3	\overline{O}_4	\overline{O}_5	\overline{O}_6	\overline{O}_7	\overline{O}_8	\overline{O}_9	\overline{O}_{10}	\overline{O}_{11}	\overline{O}_{12}	\overline{O}_{13}	\overline{O}_{14}	\overline{O}_{15}
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

Notes

1. EL = HIGH; H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage); X = state is immaterial

AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $A_n, EL \rightarrow \bar{O}_n$ HIGH to LOW LOW to HIGH $\bar{E} \rightarrow \bar{O}_n$ HIGH to LOW LOW to HIGH	5	t_{PHL}	260	520	ns	$233\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		95	190	ns	$84\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		65	130	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5	t_{PLH}	270	550	ns	$243\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		95	190	ns	$84\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		65	130	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5	t_{PHL}	175	350	ns	$148\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		65	130	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5	t_{PLH}	200	400	ns	$173\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$

1-of-16 decoder/demultiplexer with input latches

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW	5	t_{THL}		90	180 ns	40 ns + (1,0 ns/pF) C_L
	10			35	65 ns	14 ns + (0,42 ns/pF) C_L
	15			25	50 ns	11 ns + (0,28 ns/pF) C_L
	5	t_{TLH}		85	170 ns	35 ns + (1,0 ns/pf) C_L
	10			35	70 ns	14 ns + (0,42 ns/pF) C_L
	15			25	50 ns	11 ns + (0,28 ns/pF) C_L
Set-up time $A_n \rightarrow \text{EL}$	5	t_{su}	120	60	ns	see also waveforms Fig.5
	10		40	20	ns	
	15		30	15	ns	
Hold time $A_n \rightarrow \text{EL}$	5	t_{hold}	0	60	ns	
	10		0	20	ns	
	15		0	15	ns	
Minimum EL pulse width; HIGH	5	t_{WELH}	120	60	ns	
	10		40	20	ns	
	15		30	15	ns	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1100 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$16\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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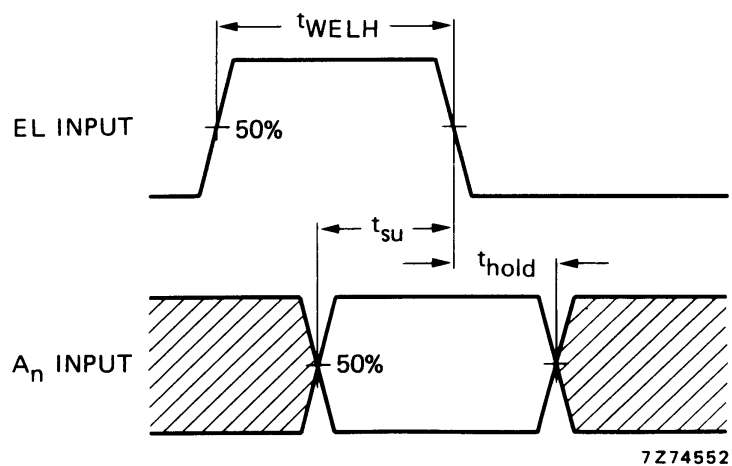
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Fig.5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.

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