

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOC莫斯 HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOC莫斯 HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4543B** **MSI** BCD to 7-segment latch/decoder/driver

Product specification  
File under Integrated Circuits, IC04

January 1995

**BCD to 7-segment latch/decoder/driver****HEF4543B  
MSI****DESCRIPTION**

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs ( $D_A$  to  $D_D$ ), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs ( $O_a$  to  $O_g$ ).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

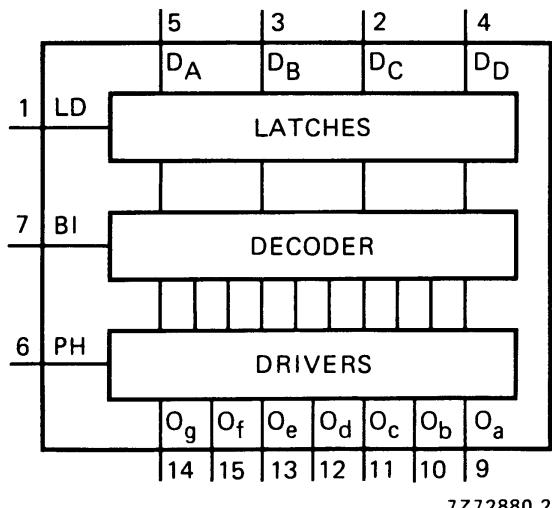


Fig.1 Functional diagram.

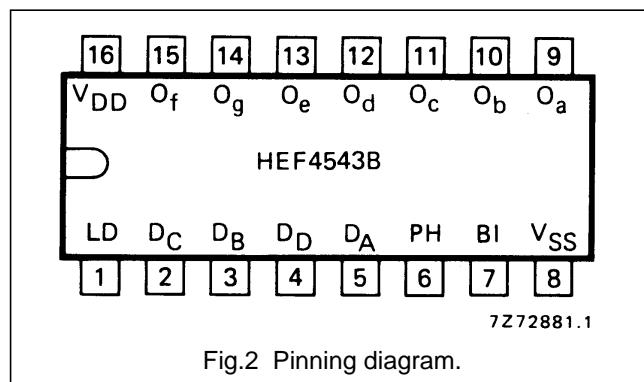


Fig.2 Pinning diagram.

HEF4543BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4543BD(F): 16-lead DIL; ceramic (cerdip) ( SOT74)

HEF4543BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

**PINNING**

$D_A$ to $D_D$	address (data) inputs
PH	phase input (active HIGH)
BI	blanking input (active HIGH)
LD	latch disable input (active HIGH)
$O_a$ to $O_g$	segment outputs

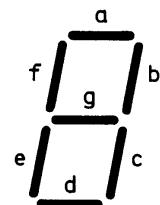


Fig.3 Segment designation.

**FAMILY DATA,  $I_{DD}$  LIMITS category MSI**

See Family Specifications

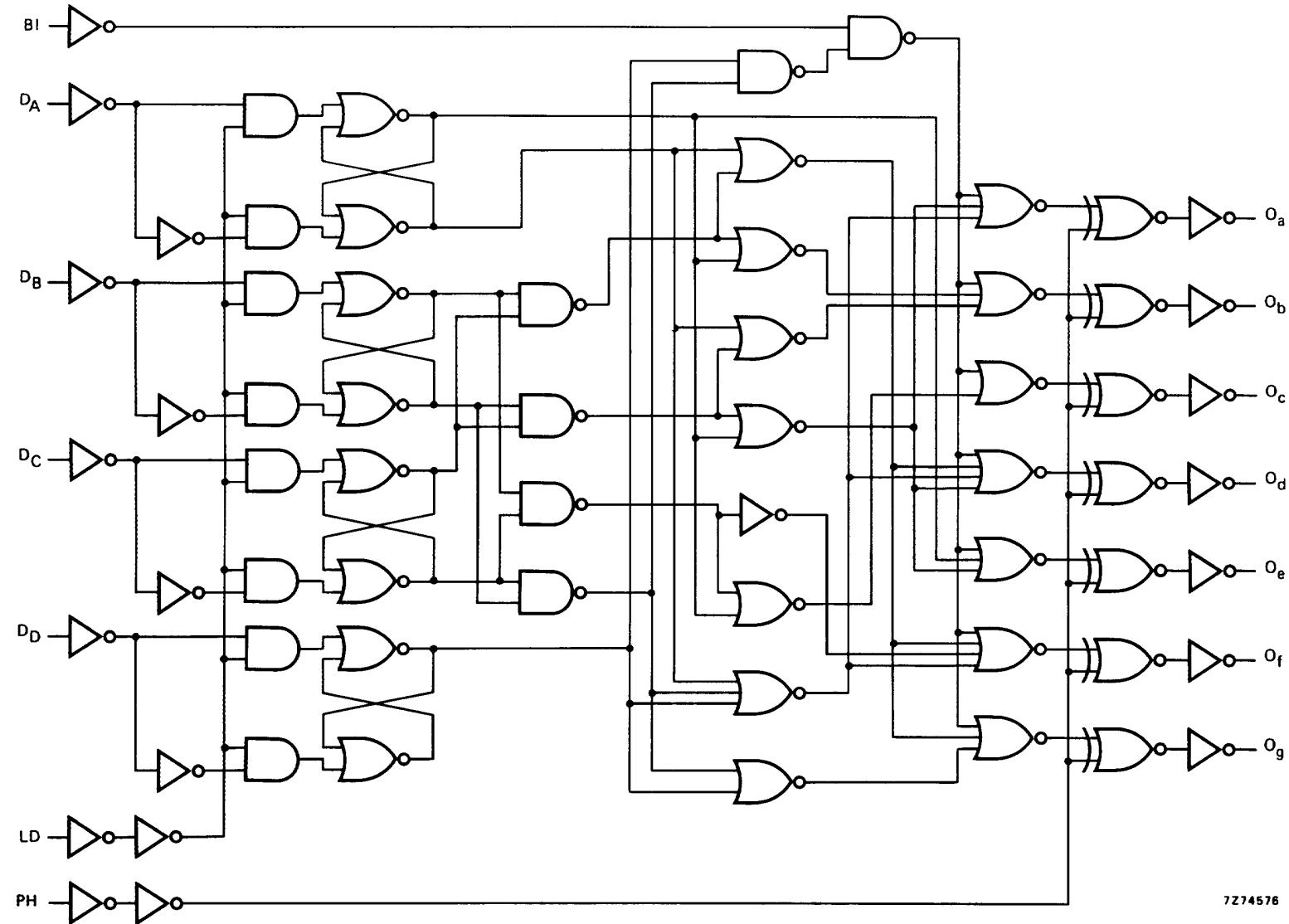


Fig.4 Logic diagram.

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## FUNCTION TABLE

INPUTS						OUTPUTS								
LD	BI	PH <sup>(4)</sup>	D <sub>D</sub>	D <sub>C</sub>	D <sub>B</sub>	D <sub>A</sub>	O <sub>a</sub>	O <sub>b</sub>	O <sub>c</sub>	O <sub>d</sub>	O <sub>e</sub>	O <sub>f</sub>	O <sub>g</sub>	DISPLAY
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X	(5)							(5)
as above	H	as above			inverse of above							as above		

## Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. For liquid crystal displays, apply a square-wave to PH.  
For common cathode LED displays, select PH = LOW.  
For common anode LED displays, select PH = HIGH.
5. Depends upon the BCD-code previously applied when LD = HIGH.

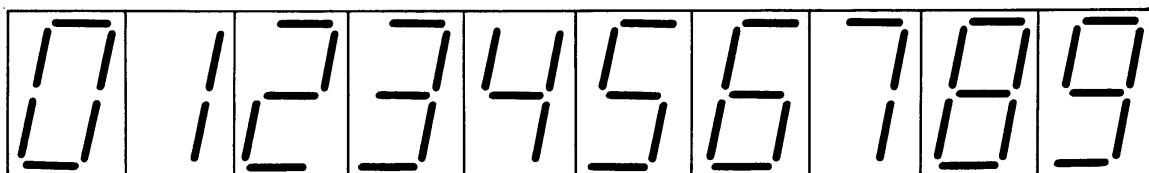


Fig.5 Display.

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## AC CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25^\circ\text{C}$ ;  $C_L = 50 \text{ pF}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays	D <sub>n</sub> → O <sub>n</sub> HIGH to LOW	t <sub>PHL</sub>	5	180	360	ns
			10	75	150	ns
			15	55	110	ns
	LOW to HIGH	t <sub>PLH</sub>	5	180	360	ns
			10	75	150	ns
			15	55	110	ns
	LD → O <sub>n</sub> HIGH to LOW	t <sub>PHL</sub>	5	170	340	ns
			10	80	160	ns
			15	60	120	ns
	LOW to HIGH	t <sub>PLH</sub>	5	190	380	ns
			10	80	160	ns
			15	60	120	ns
	BI → O <sub>n</sub> HIGH to LOW	t <sub>PHL</sub>	5	145	290	ns
			10	65	130	ns
			15	45	90	ns
	LOW to HIGH	t <sub>PLH</sub>	5	125	250	ns
			10	55	110	ns
			15	40	80	ns
Output transition times	HIGH to LOW	t <sub>THL</sub>	5	60	120	ns
			10	30	60	ns
			15	20	40	ns
	LOW to HIGH	t <sub>TLH</sub>	5	60	120	ns
			10	30	60	ns
			15	20	40	ns
	Minimum LD pulse width; HIGH	t <sub>WLDH</sub>	5	60	30	ns
			10	30	15	ns
			15	20	10	ns
Set-up time	D <sub>n</sub> → LD	t <sub>su</sub>	5	40	20	ns
			10	20	5	ns
			15	15	0	ns
	Hold time D <sub>n</sub> → LD	t <sub>hold</sub>	5	0	-15	ns
			10	15	0	ns
			15	20	5	ns

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	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$2\ 200 f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$10\ 400 f_i + \sum (f_o C_L) \times V_{DD}^2$	$f_i$ = input freq. (MHz)
	15	$33\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	$f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

## APPLICATION INFORMATION

Some examples of applications for the HEF4543B are:

- Driving LCD displays.
- Driving LED displays.
- Driving fluorescent displays.
- Driving incandescent displays.
- Driving gas discharge displays.

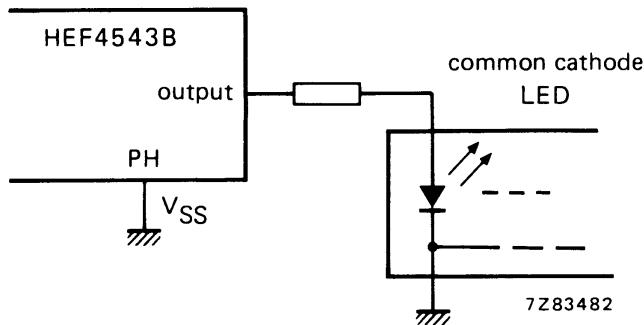


Fig.6 Connection to common cathode LED display readout.

## BCD to 7-segment latch/decoder/driver

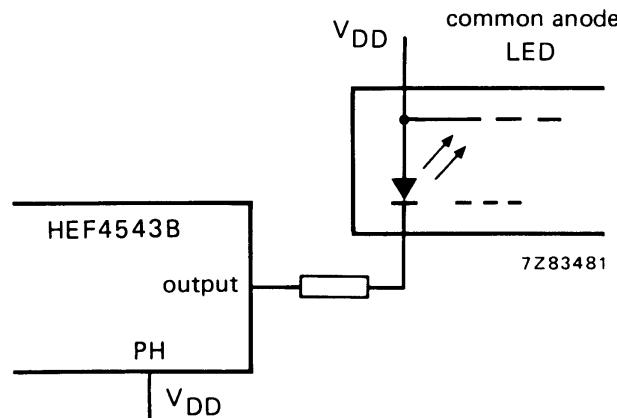
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Fig.7 Connection to common anode LED display readout.

Note to Figs 6 and 7: bipolar transistors may be added for gain where  $V_{DD} \leq 10$  V or  $I_{out} \geq 10$  mA.

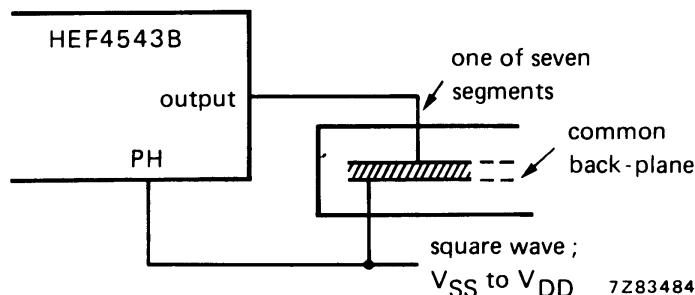


Fig.8 Connection to liquid crystal (LCD) display readout.

## BCD to 7-segment latch/decoder/driver

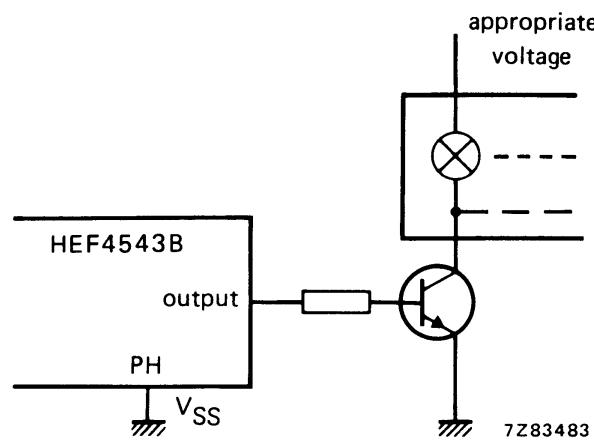
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Fig.9 Connection to incandescent display readout.

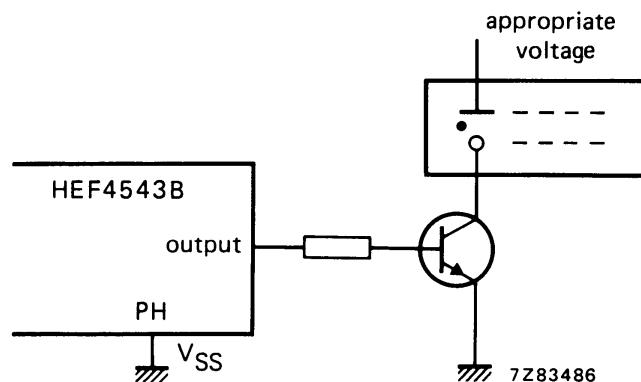


Fig.10 Connection to gas discharge display readout.

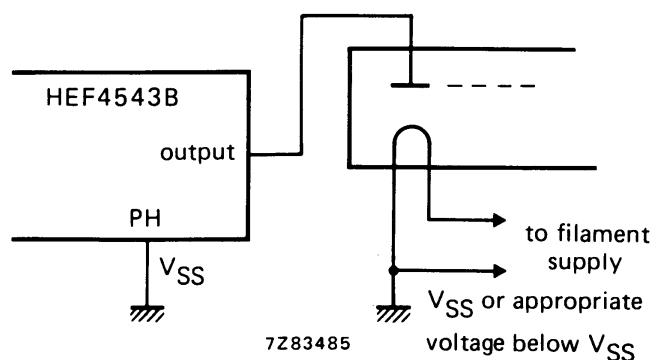


Fig.11 Connection to fluorescent display readout.