

# 74HC151; 74HCT151

## 8-input multiplexer

Rev. 5 — 26 January 2015

Product data sheet

## 1. General description

The 74HC151; 74HCT151 are 8-bit multiplexers with eight binary inputs ( $I_0$  to  $I_7$ ), three select inputs ( $S_0$  to  $S_2$ ) and an enable input ( $\bar{E}$ ). One of the eight binary inputs is selected by the select inputs and routed to the complementary outputs ( $Y$  and  $\bar{Y}$ ). A HIGH on  $\bar{E}$  forces the output  $Y$  LOW and output  $\bar{Y}$  HIGH. Inputs also include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Specified in compliance with JEDEC standard no. 7A
- Input levels:
  - ◆ For 74HC151: CMOS level
  - ◆ For 74HCT151: TTL level
- Low-power dissipation
- Non-inverting data path
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC151N	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT151N				
74HC151D	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT151D				
74HC151DB	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT151DB				
74HC151PW	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT151PW				



#### 4. Functional diagram

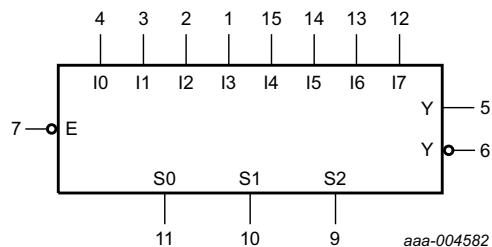


Fig 1. Logic symbol

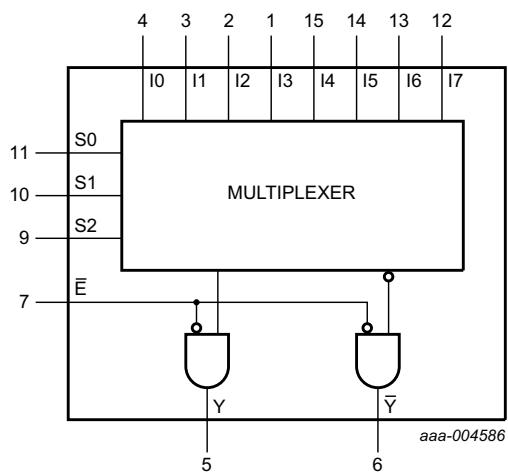


Fig 2. Functional diagram

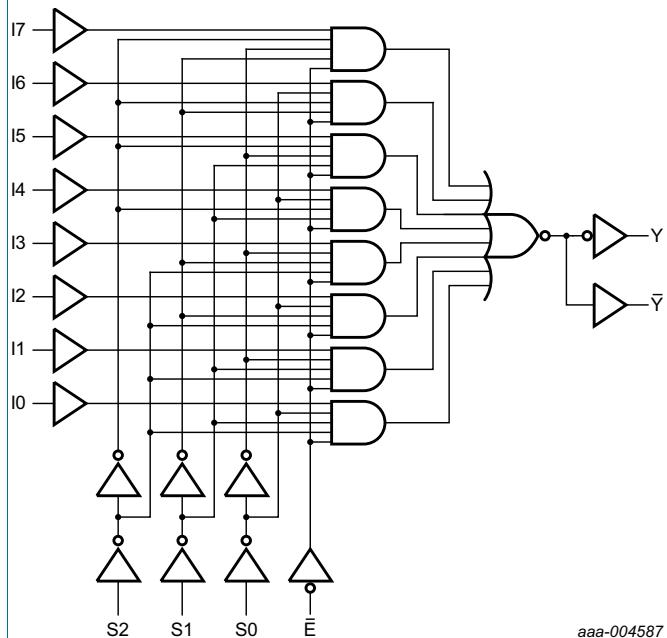


Fig 3. Logic diagram

## 5. Pinning information

### 5.1 Pinning

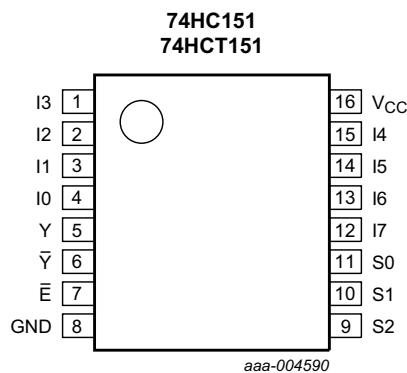


Fig 4. Pin configuration DIP16, SO16 and (T)SSOP16

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
I0 to I7	4, 3, 2, 1, 15, 14, 13, 12	data inputs
Y	5	multiplexer output
Ȳ	6	complementary multiplexer output
Ē	7	enable input (active LOW)
GND	8	ground (0 V)
S0, S1, S2	11, 10, 9	common data select inputs
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

**Table 3. Function table<sup>[1]</sup>**

Input														Output	
$\bar{E}$	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	$\bar{Y}$	Y		
H	X	X	X	X	X	X	X	X	X	X	X	H	L		
L	L	L	L	L	X	X	X	X	X	X	X	H	L		
L	L	L	L	H	X	X	X	X	X	X	X	L	H		
L	L	L	H	X	L	X	X	X	X	X	X	H	L		
L	L	L	H	X	H	X	X	X	X	X	X	L	H		
L	L	H	L	X	X	L	X	X	X	X	X	H	L		
L	L	H	L	X	X	H	X	X	X	X	X	L	H		
L	L	H	H	X	X	X	L	X	X	X	X	H	L		
L	L	H	H	X	X	X	H	X	X	X	X	L	H		
L	H	L	L	X	X	X	X	L	X	X	X	H	L		
L	H	L	L	X	X	X	X	H	X	X	X	L	H		
L	H	L	H	X	X	X	X	X	L	X	X	H	L		
L	H	L	H	X	X	X	X	X	H	X	X	L	H		
L	H	H	L	X	X	X	X	X	X	L	X	H	L		
L	H	H	L	X	X	X	X	X	X	H	X	L	H		
L	H	H	H	X	X	X	X	X	X	X	X	H	L		
L	H	H	H	X	X	X	X	X	X	X	X	H	L		

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	$\pm 20$	mA
$I_o$	output current	$V_O = -0.5 \text{ V}$ to $(V_{CC} + 0.5 \text{ V})$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	$\pm 50$	mA
$I_{GND}$	ground current		-	-50	mA
$T_{stg}$	storage temperature		-65	+150	°C

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
	DIP16 package		[1]	-	750 mW
	SO16 package		[2]	-	500 mW
	(T)SSOP16 package		[3]	-	500 mW

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.[3] For SSOP16 and TSSOP16 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC151			74HCT151			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = 25^{\circ}\text{C}$			$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC151</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$ ; $V_{CC} = 6.0\text{ V}$	-	-	8.0	-	80	-	160	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-					pF

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT151</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		per input pin; In inputs	-	45	162	-	203	-	221	µA
		per input pin; Ē input	-	30	108	-	135	-	147	µA
		per input pin; Sn input	-	150	540	-	675	-	735	µA
C <sub>I</sub>	input capacitance		-	3.5	-					pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{amb} = 25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_{amb} = -40^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC151</b>										
$t_{pd}$	propagation delay	In to Y; see <a href="#">Figure 5</a> [1]								
		$V_{CC} = 2.0 \text{ V}$	-	52	170	-	215	-	255	ns
		$V_{CC} = 4.5 \text{ V}$	-	19	34	-	43	-	51	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	15	29	-	37	-	43	ns
		In to $\bar{Y}$ ; see <a href="#">Figure 5</a> [1]								
		$V_{CC} = 2.0 \text{ V}$	-	58	185	-	230	-	280	ns
		$V_{CC} = 4.5 \text{ V}$	-	21	37	-	46	-	56	ns
	Sn to Y; see <a href="#">Figure 6</a> [1]	$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	17	31	-	39	-	48	ns
		$V_{CC} = 2.0 \text{ V}$	-	61	185	-	230	-	280	ns
		$V_{CC} = 4.5 \text{ V}$	-	22	37	-	46	-	56	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	18	31	-	39	-	48	ns
		Sn to $\bar{Y}$ ; see <a href="#">Figure 6</a> [1]								
		$V_{CC} = 2.0 \text{ V}$	-	61	205	-	255	-	310	ns
	$\bar{E}$ to Y; see <a href="#">Figure 6</a>	$V_{CC} = 4.5 \text{ V}$	-	22	41	-	51	-	62	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	18	35	-	43	-	53	ns
		$V_{CC} = 2.0 \text{ V}$	-	41	125	-	155	-	190	ns
		$V_{CC} = 4.5 \text{ V}$	-	15	25	-	31	-	38	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	12	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	12	21	-	26	-	32	ns
		$\bar{E}$ to $\bar{Y}$ ; see <a href="#">Figure 6</a>								
$t_t$	transition time	$Y, \bar{Y}$ ; see <a href="#">Figure 5</a> [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns

**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{amb} = 25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_{amb} = -40^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ [3] $V_I = \text{GND to } V_{CC}$	-	40	-	-	-	-	-	pF
<b>74HCT151</b>										
$t_{pd}$	propagation delay	In to Y; see <a href="#">Figure 5</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	22	38	-	48	-	57	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
		In to $\bar{Y}$ ; see <a href="#">Figure 5</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	22	38	-	48	-	57	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
		Sn to Y; see <a href="#">Figure 6</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	23	41	-	51	-	62	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	20	-	-	-	-	-	ns
		Sn to $\bar{Y}$ ; see <a href="#">Figure 6</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	25	43	-	54	-	65	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	20	-	-	-	-	-	ns
		$\bar{E}$ to Y; see <a href="#">Figure 6</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	16	29	-	36	-	44	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	13	-	-	-	-	-	ns
		$\bar{E}$ to $\bar{Y}$ ; see <a href="#">Figure 6</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	21	36	-	45	-	54	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	18	-	-	-	-	-	ns
$t_t$	transition time	Y, $\bar{Y}$ ; see <a href="#">Figure 5</a> [2]								
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ [3] $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$	-	40	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

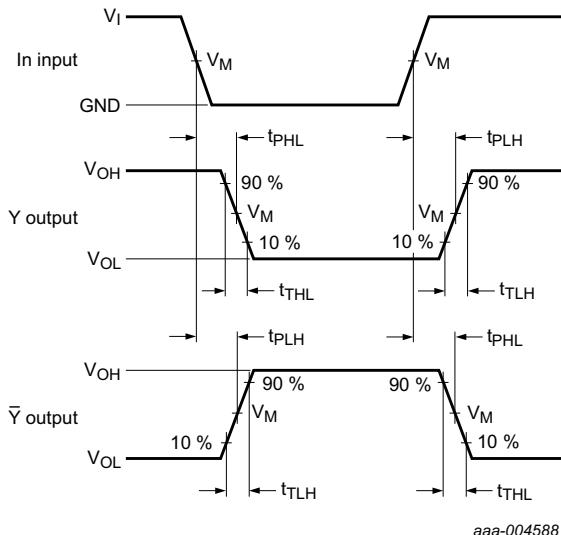
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

$$\sum(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$$

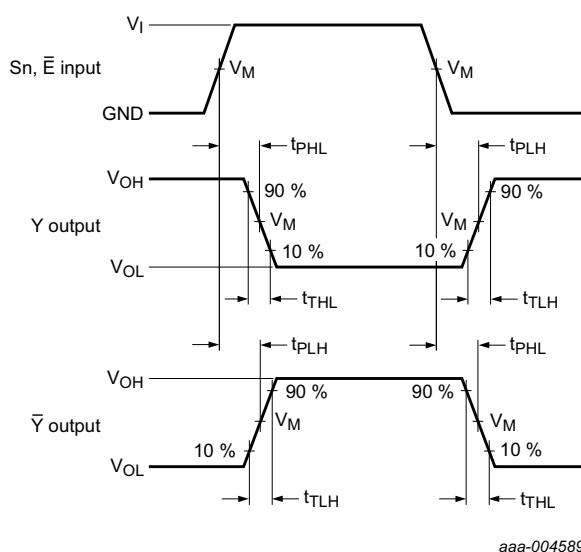
## 11. Waveforms



Measurement points are given in [Table 8](#).

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 5. Propagation delay input (In) to output (Y, Ȳ) and the output (Y, Ȳ) transition time**



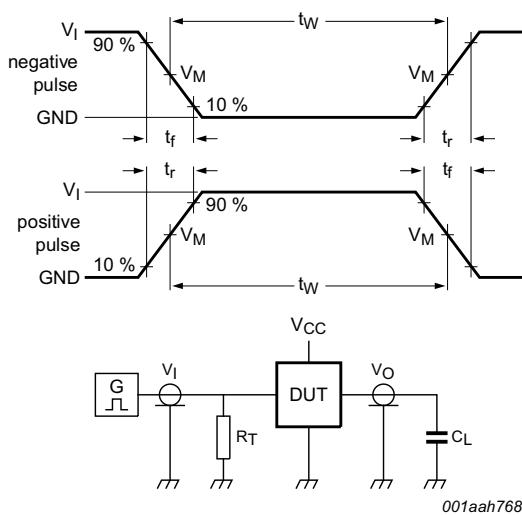
Measurement points are given in [Table 8](#).

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (Sn, E) to output (Y, Ȳ) and output (Y, Ȳ) transitions time**

Table 8. Measurement points

Type	Input	Output
	$V_M$	$V_M$
74HC151	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT151	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	$V_I$	$t_r, t_f$		
74HC151	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT151	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

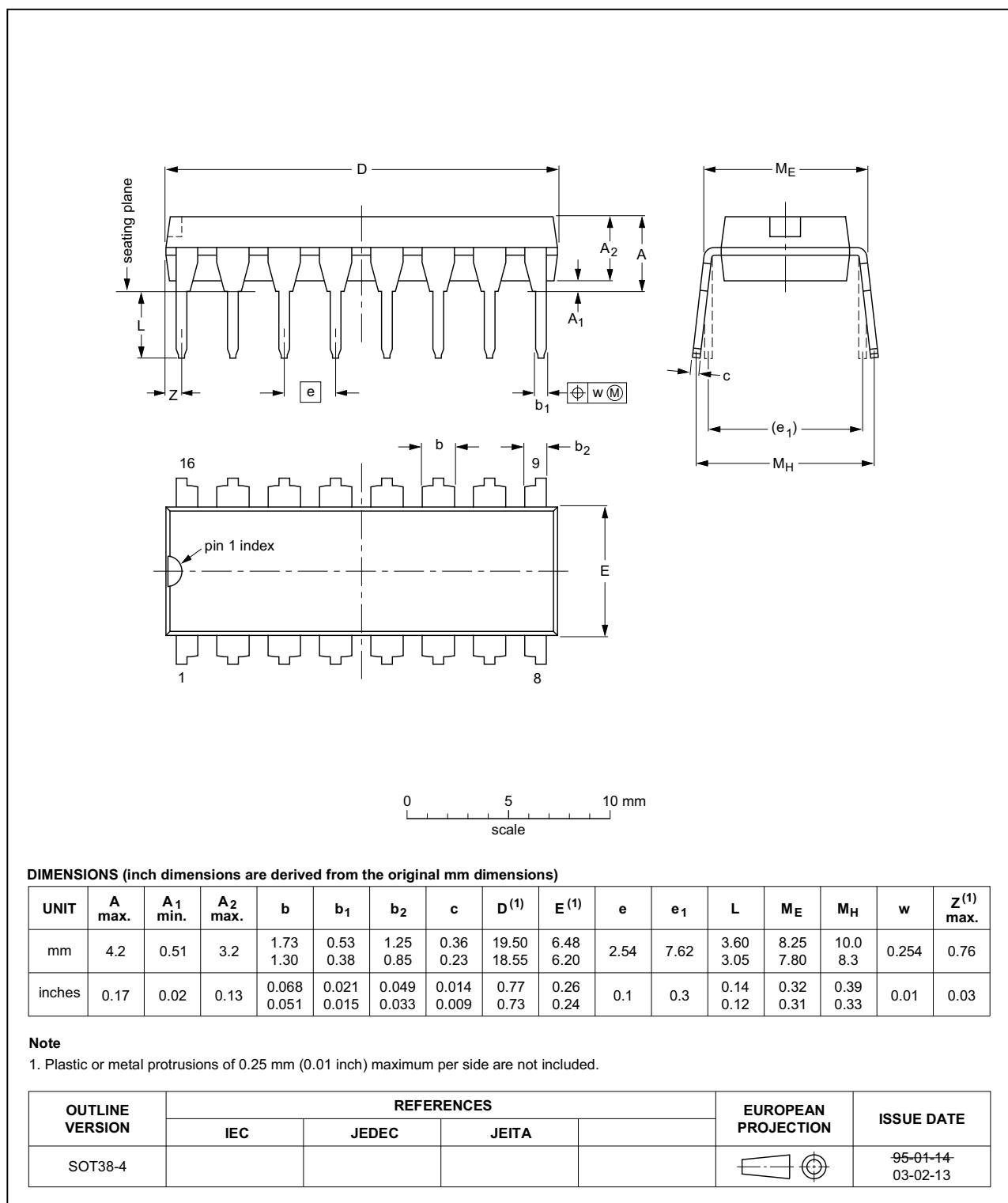


Fig 8. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

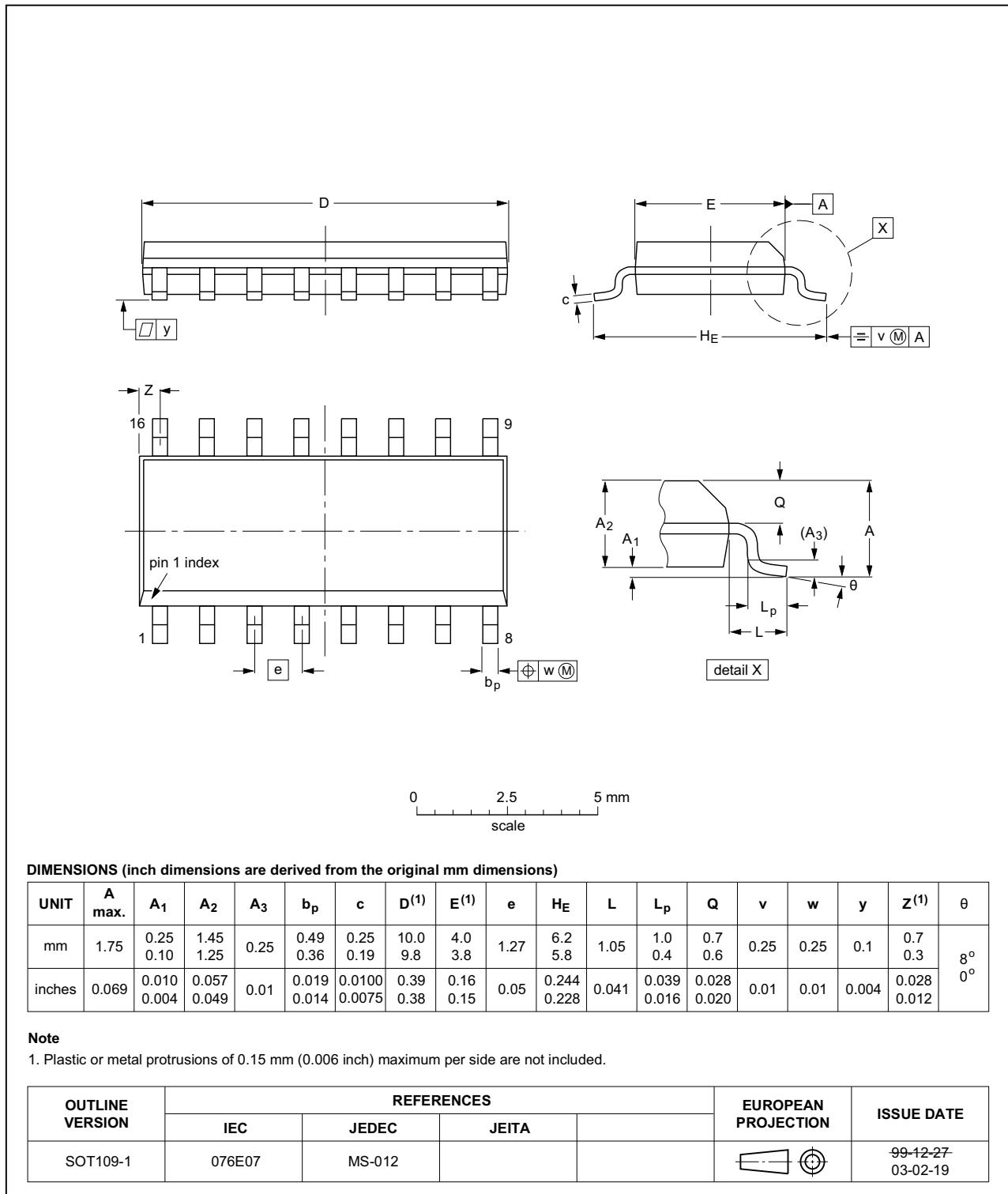


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

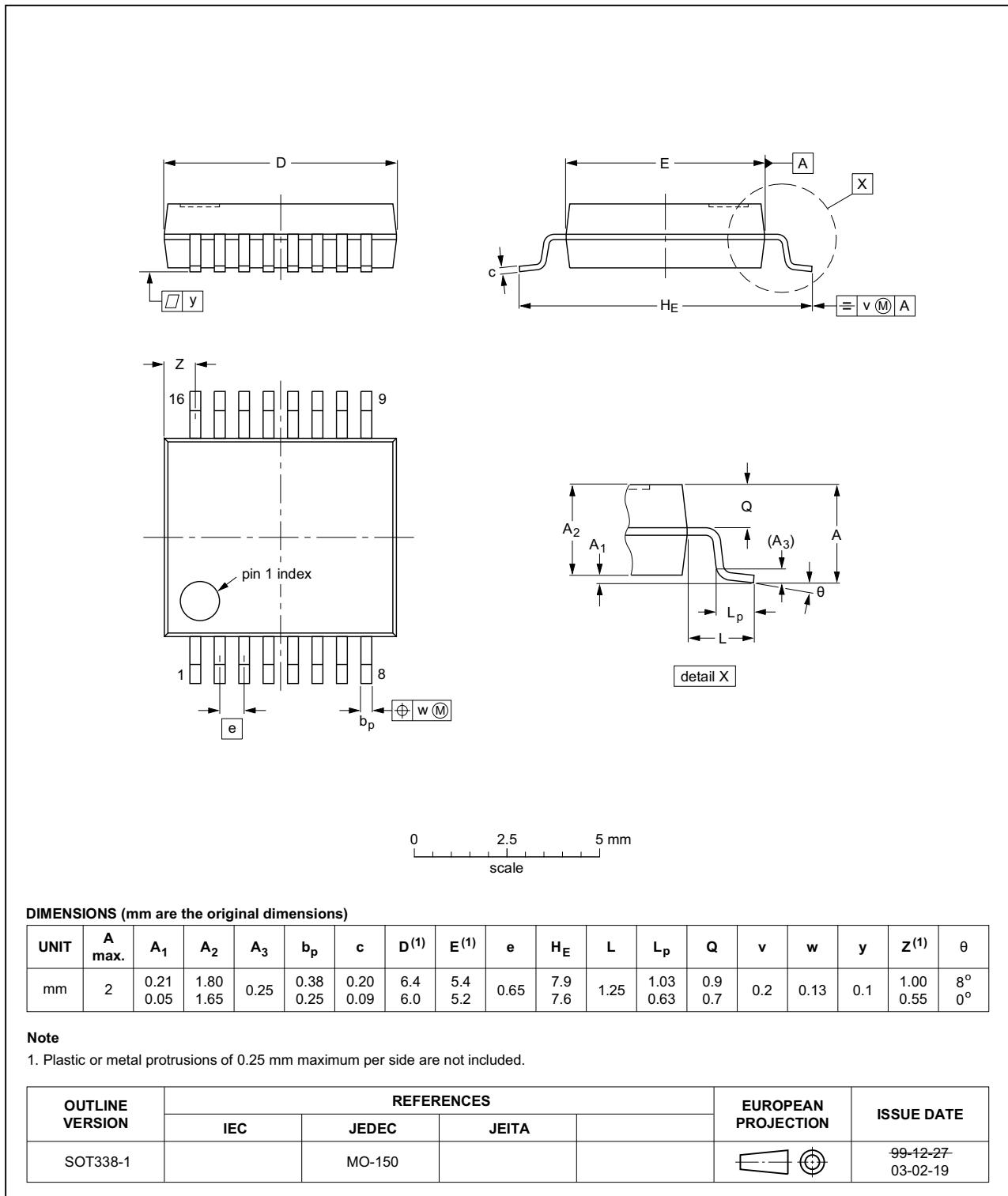


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

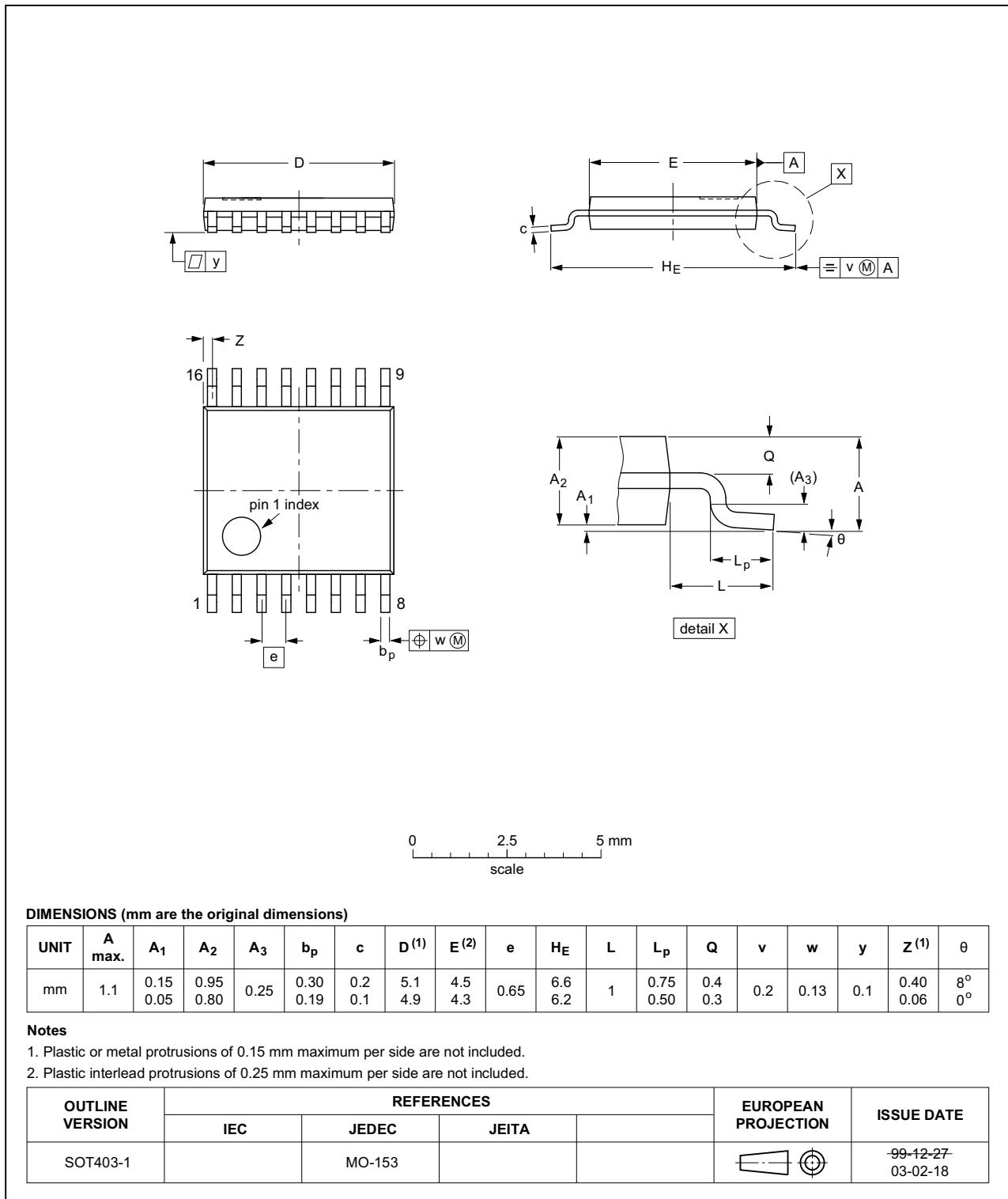


Fig 11. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT151 v.5	20150126	Product data sheet	-	74HC_HCT151 v.4
Modifications:	• <a href="#">Table 7</a> : Power dissipation capacitance condition for 74HCT151 is corrected.			
74HC_HCT151 v.4	20130211	Product data sheet	-	74HC_HCT151 v.3
Modifications:	• New descriptive title (errata).			
74HC_HCT151 v.3	20120919	Product data sheet	-	74HC_HCT151_CNV v.2
74HC_HCT151_CNV v.2	19970827	Product specification	-	

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 17. Contents

<b>1</b>	<b>General description</b>	<b>1</b>
<b>2</b>	<b>Features and benefits</b>	<b>1</b>
<b>3</b>	<b>Ordering information</b>	<b>1</b>
<b>4</b>	<b>Functional diagram</b>	<b>2</b>
<b>5</b>	<b>Pinning information</b>	<b>3</b>
5.1	Pinning	3
5.2	Pin description	3
<b>6</b>	<b>Functional description</b>	<b>4</b>
<b>7</b>	<b>Limiting values</b>	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b>	<b>5</b>
<b>9</b>	<b>Static characteristics</b>	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b>	<b>8</b>
<b>11</b>	<b>Waveforms</b>	<b>10</b>
<b>12</b>	<b>Package outline</b>	<b>12</b>
<b>13</b>	<b>Abbreviations</b>	<b>16</b>
<b>14</b>	<b>Revision history</b>	<b>16</b>
<b>15</b>	<b>Legal information</b>	<b>17</b>
15.1	Data sheet status	17
15.2	Definitions	17
15.3	Disclaimers	17
15.4	Trademarks	18
<b>16</b>	<b>Contact information</b>	<b>18</b>
<b>17</b>	<b>Contents</b>	<b>19</b>
<b>18</b>	<b>Contents</b>	<b>19</b>

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