

CDx4HC373 Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- 2-V to 6-V V_{CC} operation
- Wide operating temperature range of -55°C to 125°C
- Balanced propagation delays and transition times
- Standard outputs drive up to 15 LS-TTL loads
- Significant power reduction compared to LS-TTL Logic ICs

2 Description

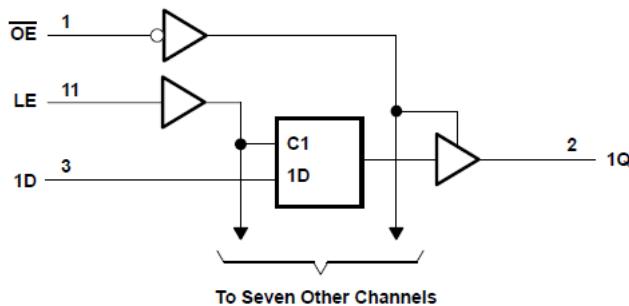
The 'HC373 devices are octal transparent D-type latches designed for 2-V to 6-V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
CD74HC373M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC373E	PDIP (20)	25.40 mm × 6.35 mm
CD54HC373F	CDIP (20)	26.92 mm × 6.92 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (positive logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

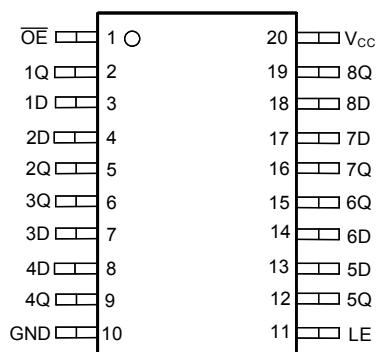
Changes from Revision B (January 2022) to Revision C (May 2022)	Page
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- Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6....**4**

Changes from Revision A (April 2003) to Revision B (January 2022)	Page
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- Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....**1**

4 Pin Configuration and Functions



**J, N, or DW package
20-Pin CDIP, PDIP, or SOIC
Top View**

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}		± 20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}		± 20	mA
I _O	Continuous output drain current per output	V _O = 0 to V _{CC}		± 35	mA
I _O	Continuous output source or sink current per output	V _O = 0 to V _{CC}		± 25	mA
	Continuous current through V _{CC} or GND			± 50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 6 V	4.2		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 4.5 V		1.35	
		V _{CC} = 6 V		1.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V		1000	ns
		V _{CC} = 4.5 V		500	
		V _{CC} = 6 V		400	
T _A	Operating free-air temperature		-55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	UNIT
		20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	109.1	84.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	76	72.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	77.6	65.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	51.5	55.3	°C/W
Ψ _{JB}	Junction-to-top characterization parameter	77.1	65.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	2 V	1.9	1.9	1.9	1.9	1.9	V
			4.5 V	4.4	4.4	4.4	4.4	4.4	
			6 V	5.9	5.9	5.9	5.9	5.9	
		I _{OH} = -6 mA	4.5 V	3.98	3.7	3.7	3.84	3.84	
		I _{OH} = -7.8 mA	6 V	5.48	5.2	5.2	5.34	5.34	
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V	0.1	0.1	0.1	0.1	0.1	V
			4.5 V	0.1	0.1	0.1	0.1	0.1	
			6 V	0.1	0.1	0.1	0.1	0.1	
		I _{OL} = 6 mA	4.5 V	0.26	0.4	0.4	0.33	0.33	
		I _{OL} = 7.8 mA	6 V	0.26	0.4	0.4	0.33	0.33	
I _I	V _I = V _{CC} or 0	6 V	±0.1	±1	±1	±1	±1	±1	µA
I _{OZ}	V _O = V _{CC} or 0	6 V	±0.5	±10	±10	±10	±5	±5	µA
I _{CC}	V _I = V _{CC} or 0 I _O = 0	6 V	8	160	160	160	80	80	µA
C _i			10	10	10	10	10	10	pF
C _o			20	20	20	20	20	20	pF

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

		V _{CC}	T _A = 25°C		T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	2 V	80	120	100	100	100	100	ns
		4.5 V	16	24	20	20	20	20	
		6 V	14	20	17	17	17	17	
t _{su}	Setup time, data before LE↓	2 V	50	75	65	65	65	65	ns
		4.5 V	10	15	13	13	13	13	
		6 V	9	13	11	11	11	11	
t _h	Hold time, data after LE↓	2 V	5	5	5	5	5	5	ns
		4.5 V	5	5	5	5	5	5	
		6 V	5	5	5	5	5	5	

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

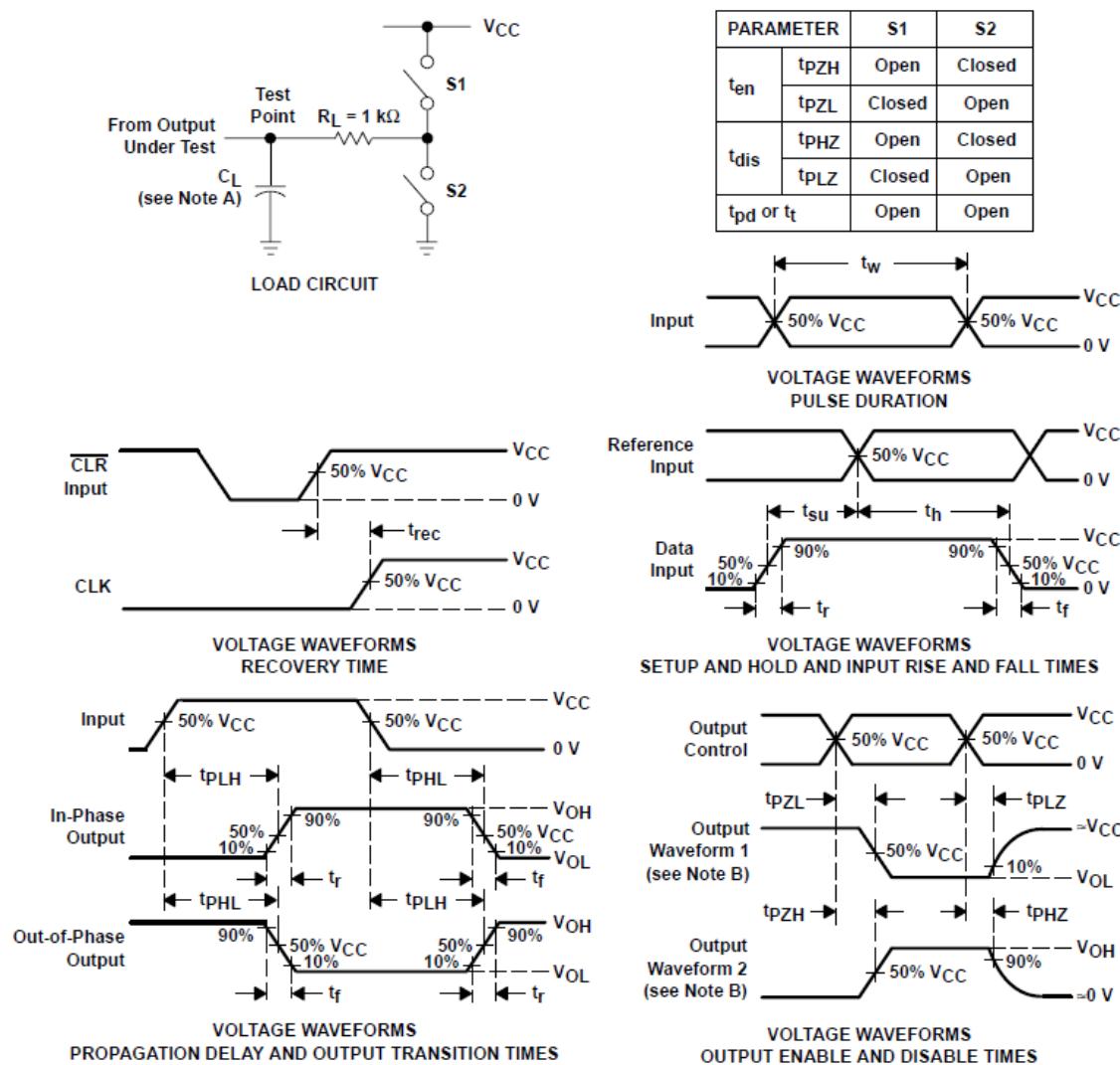
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C		T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q	C _L = 50 pF	2 V	150		225		190		ns
				4.5 V		30		45		38	
				6 V		26		38		33	
	LE	Q	C _L = 50 pF	2 V		175		265		220	
				4.5 V		35		53		44	
				6 V		30		45		37	
t _{en}	OE	Q	C _L = 50 pF	2 V	150		225		190		ns
				4.5 V		30		45		38	
				6 V		26		38		33	
t _{dis}	OE	Q	C _L = 50 pF	2 V	150		225		190		ns
				4.5 V		30		45		38	
				6 V		26		38		33	
t _t		Q	C _L = 50 pF	2 V	60		90		75		ns
				4.5 V		12		18		15	
				6 V		10		15		13	

5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance	51	pF

6 Parameter Measurement Information



- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
- For clock inputs, f_{max} measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The 'HC373 devices are octal transparent D-type latches designed for 2-V to 6-V V_{CC} operation.

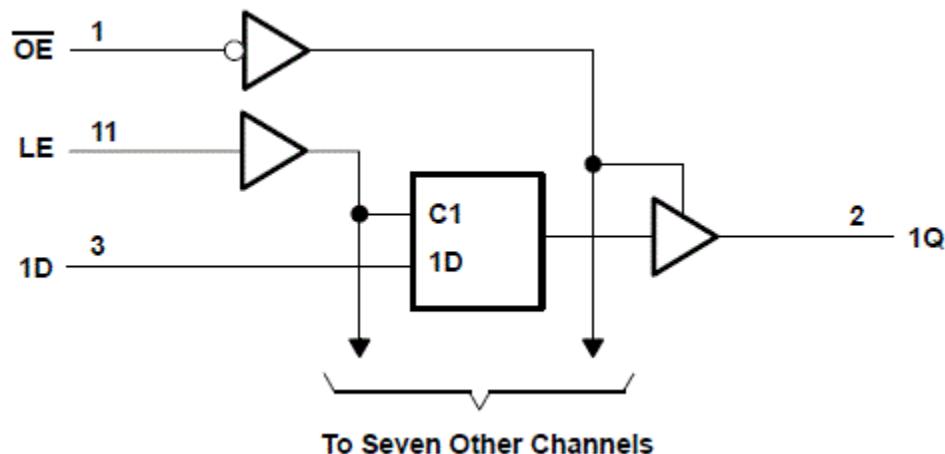
When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table(each latch)

INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC373F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC373F	Samples
CD54HC373F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407201RA CD54HC373F3A	Samples
CD74HC373E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC373E	Samples
CD74HC373EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC373E	Samples
CD74HC373M	OBsolete	SOIC	DW	20	TBD		Call TI	Call TI	-55 to 125	HC373M	
CD74HC373M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC373M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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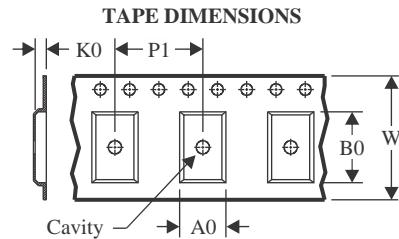
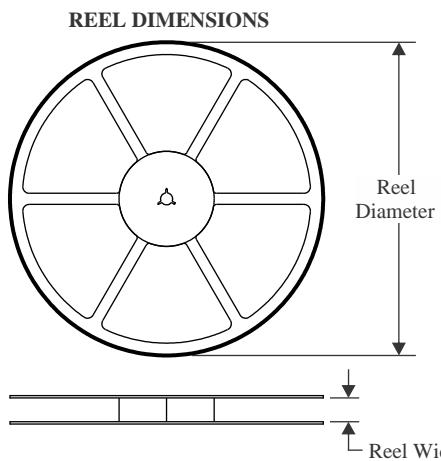
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC373, CD74HC373 :

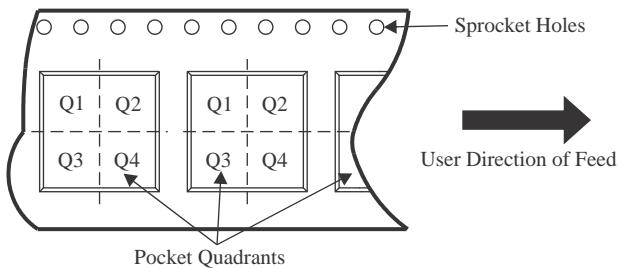
- Catalog : [CD74HC373](#)
- Military : [CD54HC373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

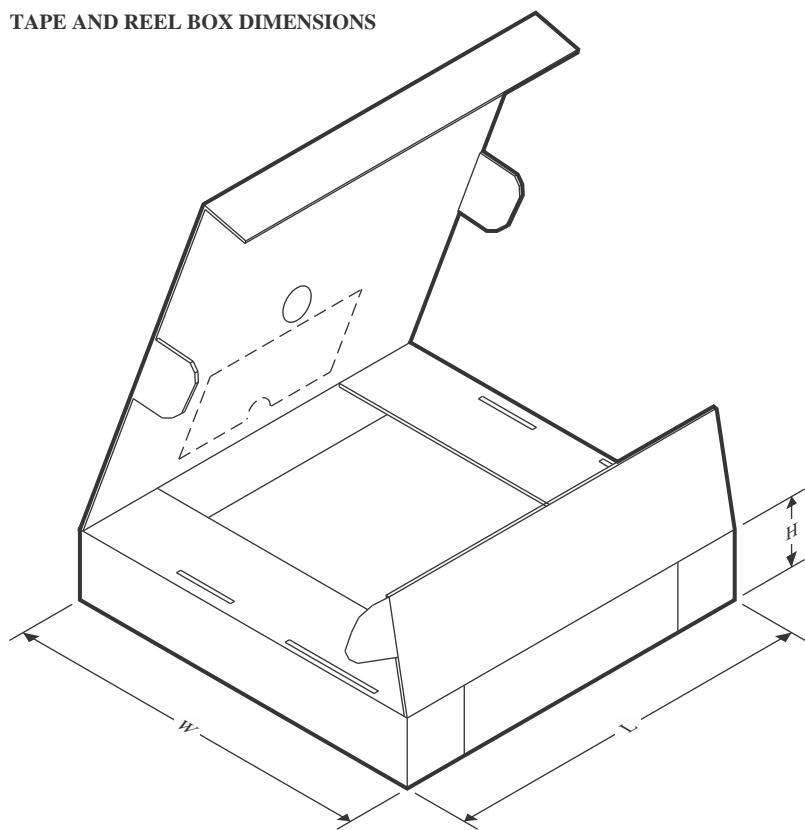
TAPE AND REEL INFORMATION

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

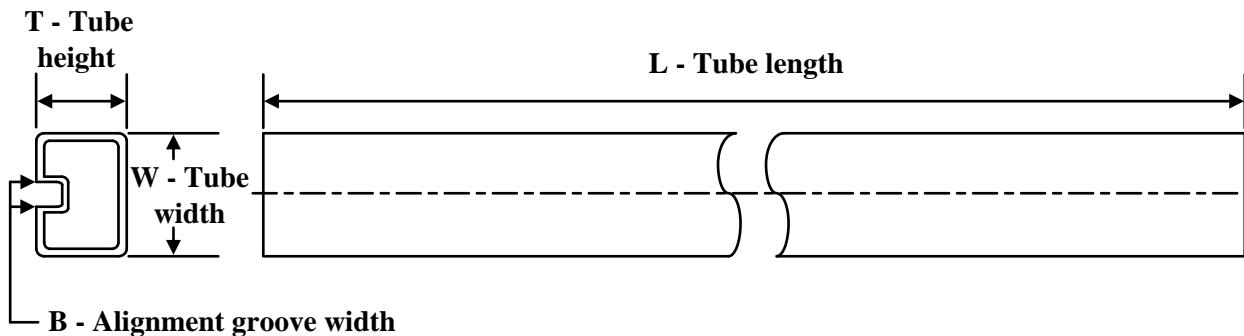
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC373M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC373M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC373M96	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE


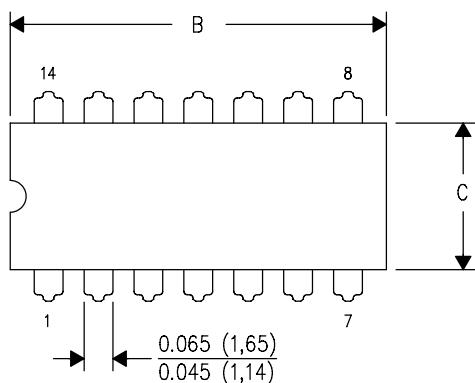
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD74HC373E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC373EE4	N	PDIP	20	20	506	13.97	11230	4.32

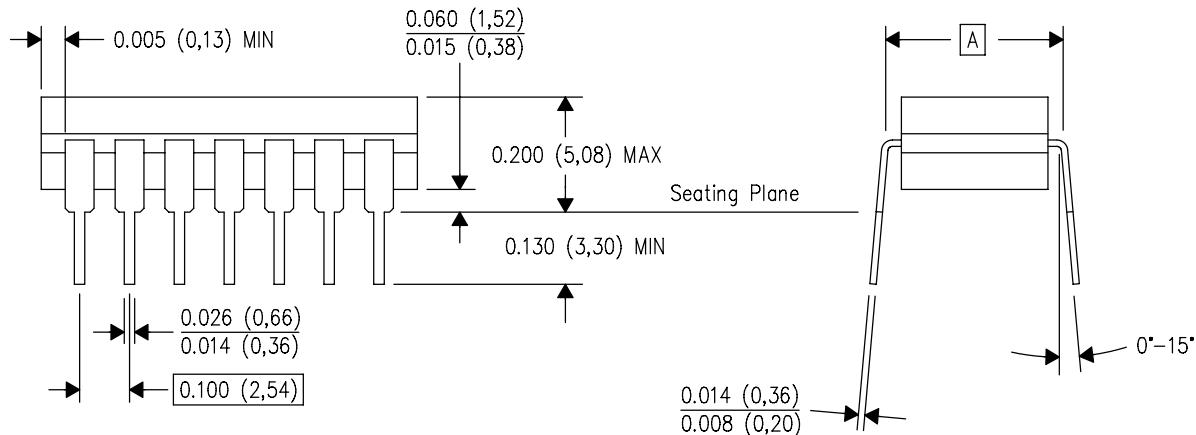
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



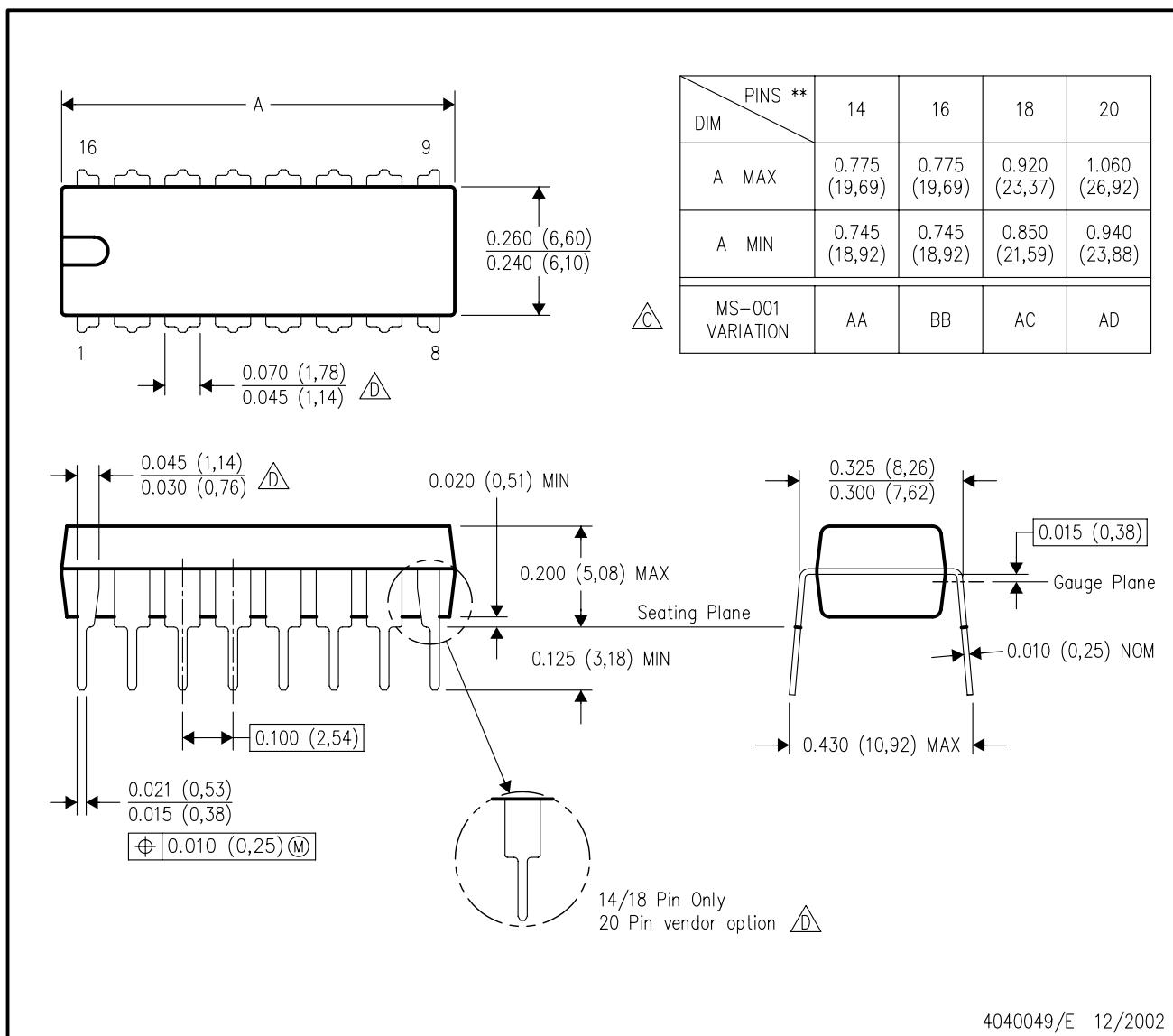
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



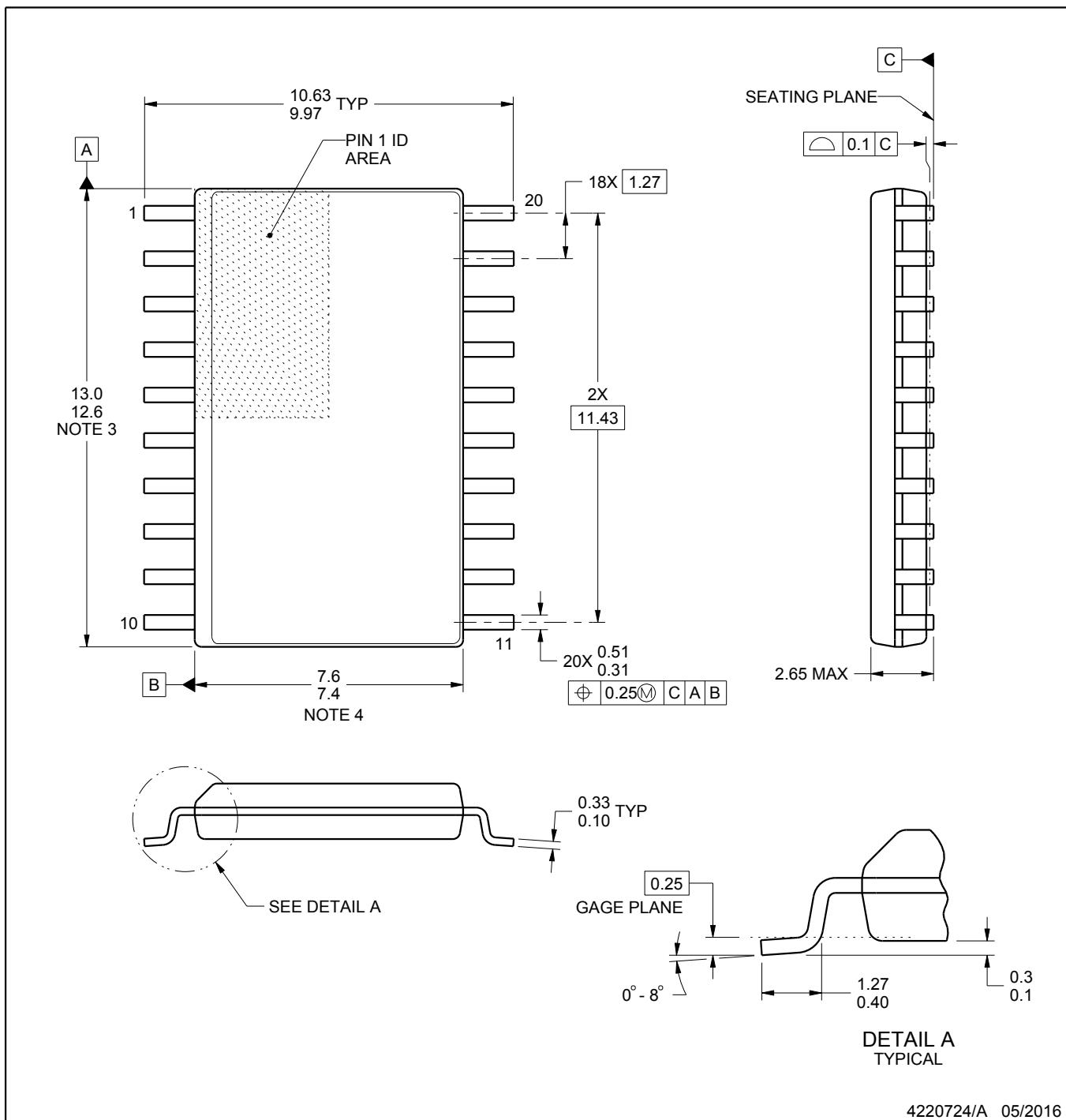
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

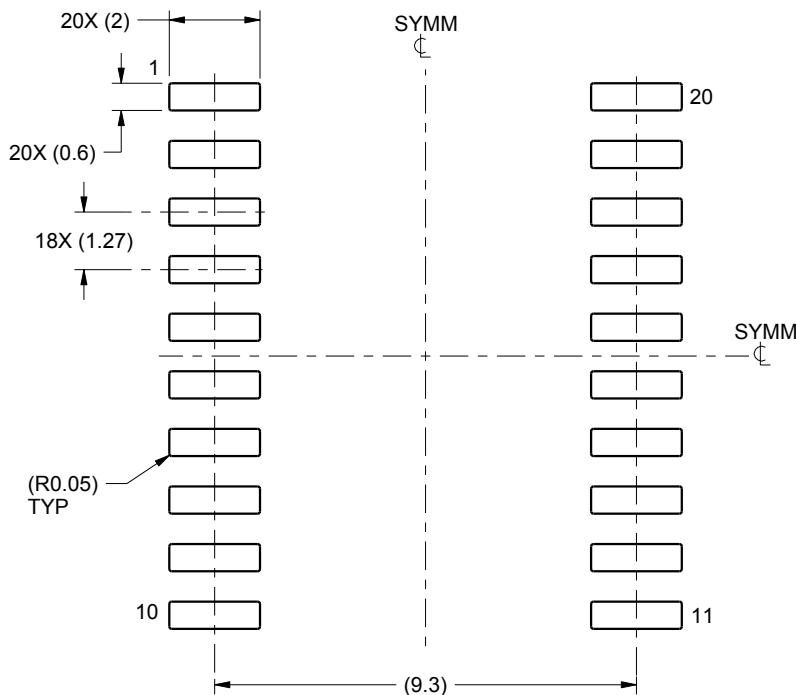
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

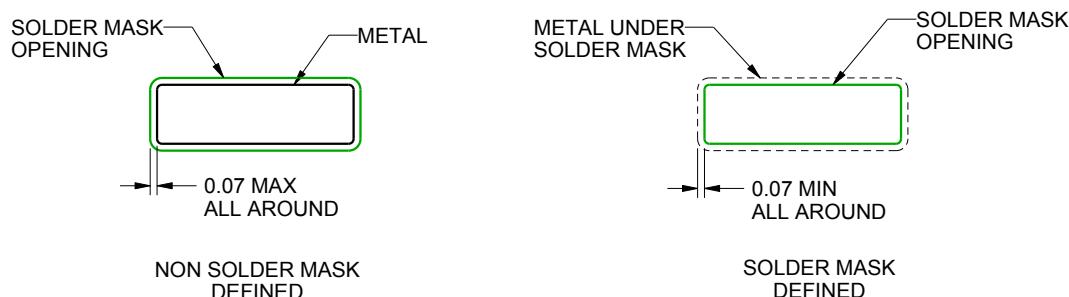
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

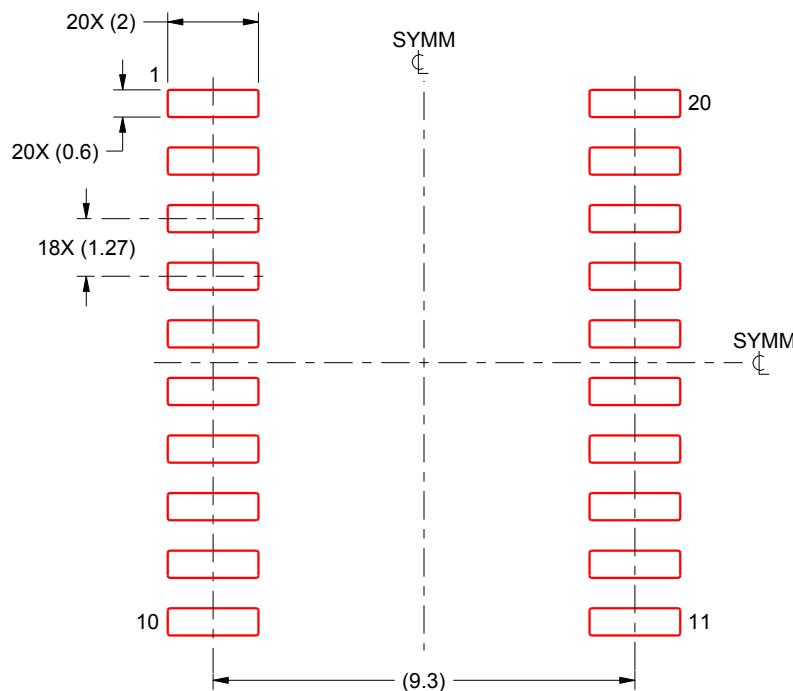
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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