

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4512B** **MSI**

8-input multiplexer with 3-state output

Product specification  
File under Integrated Circuits, IC04

January 1995

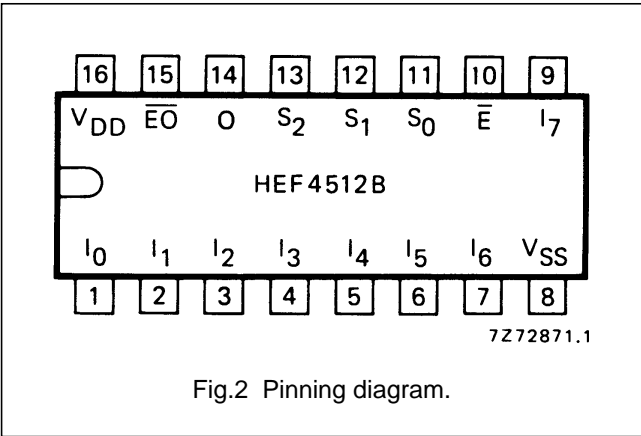
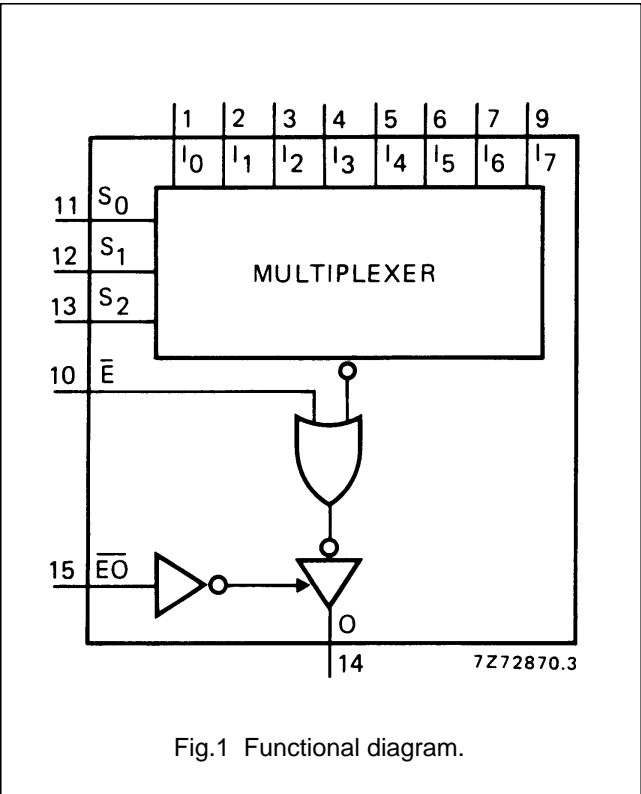
8-input multiplexer with 3-state output

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DESCRIPTION

The HEF4512B is an 8-input multiplexer with 8 binary inputs ( $I_0$  to  $I_7$ ), an enable input ( $\overline{E}$ ) and an output enable input ( $\overline{EO}$ ). One of eight binary inputs is selected by select inputs  $S_0$ ,  $S_1$  and  $S_2$ , and is routed to the output  $O$ . A HIGH on  $\overline{EO}$  causes  $O$  to assume a high impedance OFF-state, regardless of other input conditions. This allows the output

to interface directly with bus oriented systems (3-state). When the active LOW enable ( $\overline{E}$ ) is HIGH, it forces the output LOW provided  $\overline{EO}$  is LOW. By proper manipulation of the inputs, the device can provide any logic functions of four variables. It cannot be used to multiplex analogue signals.



- HEF4512BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4512BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4512BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

PINNING

- $S_0, S_1, S_2$  select inputs
- $\overline{EO}$  output enable (active LOW)
- $\overline{E}$  enable (active LOW)
- $I_0$  to  $I_7$  multiplexer inputs
- $O$  multiplexer output

FAMILY DATA,  $I_{DD}$  LIMITS category MSI

See Family Specifications

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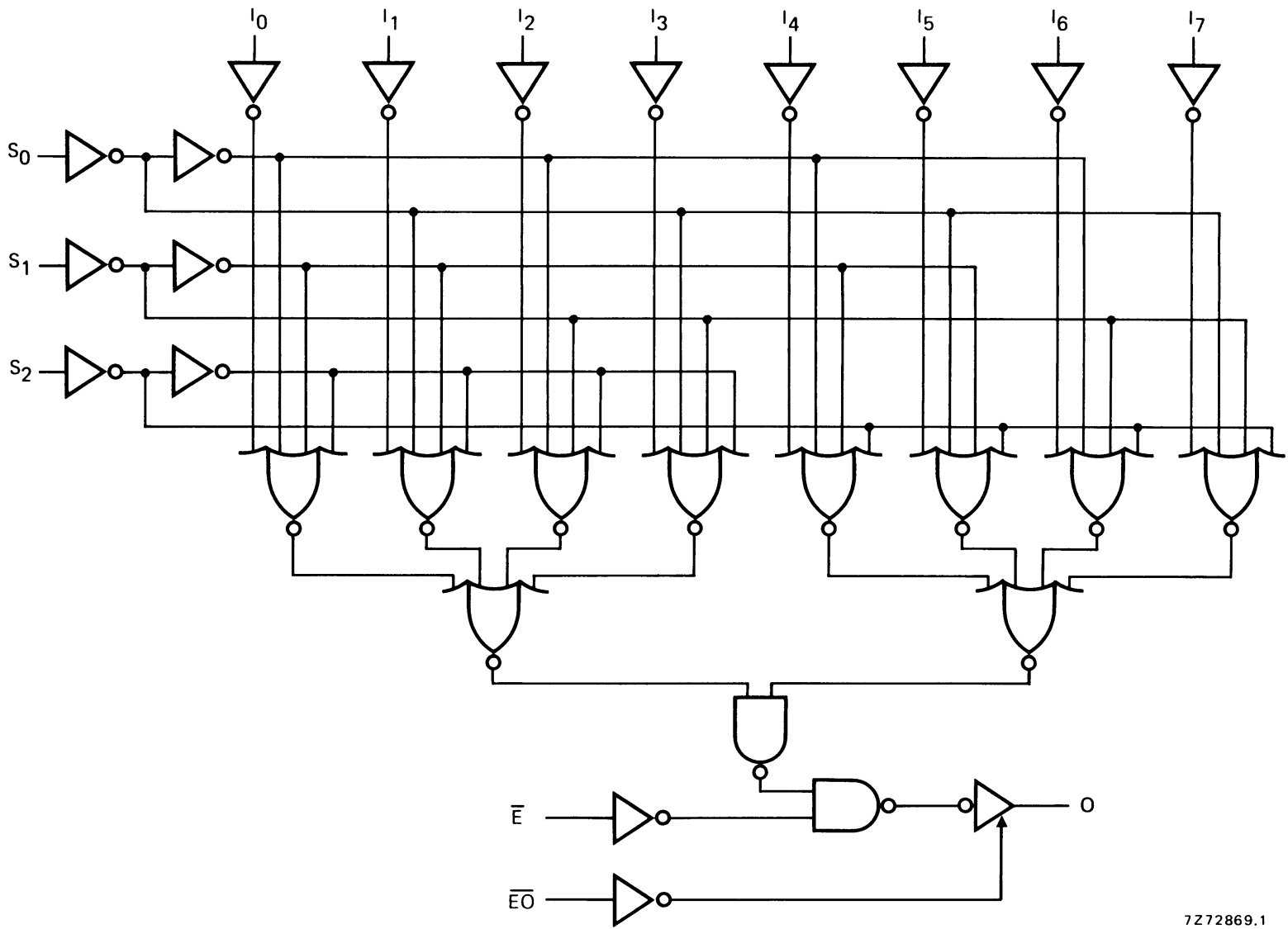


Fig.3 Logic diagram.

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## TRUTH TABLE

INPUTS													OUTPUT
$\overline{EO}$	$\overline{E}$	$S_2$	$S_1$	$S_0$	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$	O
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

## Notes

1. H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
Z = high impedance OFF-state

## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5 10 15	$500 f_i + \sum (f_o C_L) \times V_{DD}^2$ $2100 f_i + \sum (f_o C_L) \times V_{DD}^2$ $5800 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

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## AC CHARACTERISTICS

 $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O$	5		100	200	ns	73 ns + (0,55 ns/pF) $C_L$
HIGH to LOW	10	$t_{PHL}$	40	80	ns	29 ns + (0,23 ns/pF) $C_L$
	15		30	60	ns	22 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$	100	200	ns	73 ns + (0,55 ns/pF) $C_L$
	10		40	80	ns	29 ns + (0,23 ns/pF) $C_L$
	15		30	60	ns	22 ns + (0,16 ns/pF) $C_L$
$S_n \rightarrow O$	5		140	280	ns	113 ns + (0,55 ns/pF) $C_L$
HIGH to LOW	10	$t_{PHL}$	55	110	ns	44 ns + (0,23 ns/pF) $C_L$
	15		40	80	ns	32 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$	150	300	ns	123 ns + (0,55 ns/pF) $C_L$
	10		60	120	ns	49 ns + (0,23 ns/pF) $C_L$
	15		40	80	ns	32 ns + (0,16 ns/pF) $C_L$
$\bar{E} \rightarrow O$	5		60	120	ns	33 ns + (0,55 ns/pF) $C_L$
HIGH to LOW	10	$t_{PHL}$	25	50	ns	14 ns + (0,23 ns/pF) $C_L$
	15		20	40	ns	12 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$	55	110	ns	28 ns + (0,55 ns/pF) $C_L$
	10		25	50	ns	14 ns + (0,23 ns/pF) $C_L$
	15		20	40	ns	12 ns + (0,16 ns/pF) $C_L$
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
HIGH to LOW	10	$t_{THL}$	30	60	ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$
LOW to HIGH	5	$t_{TLH}$	60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$
3-state propagation delays						
Output disable times						
$\bar{E}O \rightarrow O$	5		35	70	ns	
HIGH	10	$t_{PHZ}$	20	40	ns	
	15		15	30	ns	
LOW	5	$t_{PLZ}$	35	70	ns	
	10		15	30	ns	
	15		10	20	ns	
Output enable times						
$\bar{E}O \rightarrow O$	5		35	70	ns	
HIGH	10	$t_{PZH}$	15	30	ns	
	15		10	20	ns	

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	V <sub>DD</sub> V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
LOW	5	t <sub>PZL</sub>	35	70	ns	
	10		20	40	ns	
	15		15	30	ns	

**APPLICATION INFORMATION**

Some examples of applications for the HEF4512B are:

- Signal gating
- Digital multiplexing
- Number sequence generation

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TRUTH TABLE for Fig. 4

A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	INPUT CONN. TO OUTPUT
L	L	L	L	L	0
L	L	L	L	H	1
L	L	L	H	L	2
L	L	L	H	H	3
L	L	H	L	L	4
L	L	H	L	H	5
L	L	H	H	L	6
L	L	H	H	H	7
L	H	L	L	L	8
L	H	L	L	H	9
L	H	L	H	L	10
L	H	L	H	H	11
L	H	H	L	L	12
L	H	H	L	H	13
L	H	H	H	L	14
L	H	H	H	H	15
H	L	L	L	L	16
H	L	L	L	H	17
H	L	L	H	L	18
H	L	L	H	H	19
H	L	H	L	L	20
H	L	H	L	H	21
H	L	H	H	L	22
H	L	H	H	H	23
H	H	L	L	L	24
H	H	L	L	H	25
H	H	L	H	L	26
H	H	L	H	H	27
H	H	H	L	L	28
H	H	H	L	H	29
H	H	H	H	L	30
H	H	H	H	H	31

