

### FEATURES

- Microprocessor Compatible (6800, 8085, Z80, Etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- Endpoint Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch Free (No Protection Schottky Required)

### APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

### GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

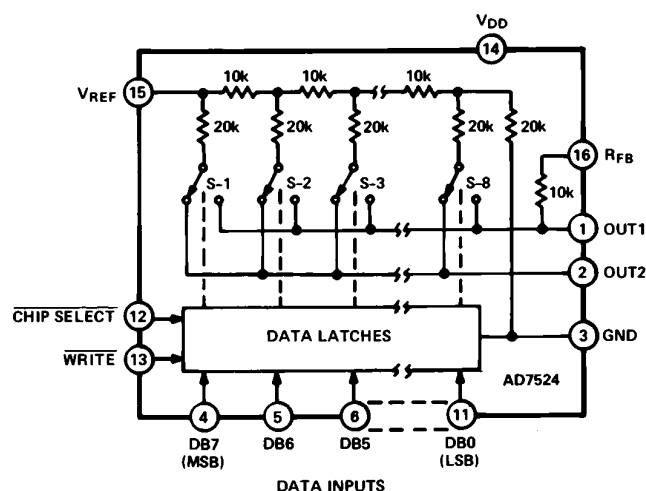
Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5 V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5 V to +15 V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

### FUNCTIONAL BLOCK DIAGRAM



### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Nonlinearity (V <sub>DD</sub> = +15 V)	Package Option <sup>2</sup>
AD7524JN	-40°C to +85°C	±1/2 LSB	N-16
AD7524KN	-40°C to +85°C	±1/4 LSB	N-16
AD7524LN	-40°C to +85°C	±1/8 LSB	N-16
AD7524JP	-40°C to +85°C	±1/2 LSB	P-20A
AD7524KP	-40°C to +85°C	±1/4 LSB	P-20A
AD7524LP	-40°C to +85°C	±1/8 LSB	P-20A
AD7524JR	-40°C to +85°C	±1/2 LSB	R-16A
AD7524AQ	-40°C to +85°C	±1/2 LSB	Q-16
AD7524BQ	-40°C to +85°C	±1/4 LSB	Q-16
AD7524CQ	-40°C to +85°C	±1/8 LSB	Q-16
AD7524SQ	-55°C to +125°C	±1/2 LSB	Q-16
AD7524TQ	-55°C to +125°C	±1/4 LSB	Q-16
AD7524UQ	-55°C to +125°C	±1/8 LSB	Q-16
AD7524SE	-55°C to +125°C	±1/2 LSB	E-20A
AD7524TE	-55°C to +125°C	±1/4 LSB	E-20A
AD7524UE	-55°C to +125°C	±1/8 LSB	E-20A

### NOTES

<sup>1</sup>To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.

<sup>2</sup>E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

### REV. B

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# AD7524–SPECIFICATIONS ( $V_{REF} = +10\text{ V}$ , $V_{OUT1} = V_{OUT2} = 0\text{ V}$ , unless otherwise noted)

Parameter	Limit, T <sub>A</sub> = +25°C		Limit, T <sub>MIN</sub> , T <sub>MAX</sub> <sup>1</sup>		Units	Test Conditions/Comments
	V <sub>DD</sub> = +5 V	V <sub>DD</sub> = +15 V	V <sub>DD</sub> = 5 V	V <sub>DD</sub> = +15 V		
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	Gain TC Measured from +25°C to T <sub>MIN</sub> or from +25°C to T <sub>MAX</sub> ΔV <sub>DD</sub> = ±10%
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	Guaranteed	Guaranteed	Guaranteed	Guaranteed		
Gain Error <sup>2</sup>	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC <sup>3</sup>	±40	±10	±40	±10	ppm/°C	
DC Supply Rejection, <sup>3</sup> ΔGain/ΔV <sub>DD</sub>	0.08 0.002	0.02 0.001	0.16 0.01	0.04 0.005	% FSR/% max % FSR/% typ	
Output Leakage Current						
I <sub>OUT1</sub> (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0 V; $\overline{\text{WR}}$ , $\overline{\text{CS}}$ = 0 V; V <sub>REF</sub> = ±10 V DB0–DB7 = V <sub>DD</sub> ; $\overline{\text{WR}}$ , $\overline{\text{CS}}$ = 0 V; V <sub>REF</sub> = ±10 V
I <sub>OUT2</sub> (Pin 2)	±50	±50	±400	±200	nA max	
DYNAMIC PERFORMANCE						
Output Current Settling Time <sup>3</sup> (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100 Ω, C <sub>EXT</sub> = 13 pF; $\overline{\text{WR}}$ , $\overline{\text{CS}}$ = 0 V; DB0–DB7 = 0 V to V <sub>DD</sub> to 0 V.
AC Feedthrough <sup>3</sup>						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V <sub>REF</sub> = ±10 V, 100 kHz Sine Wave; DB0–DB7 = 0 V; $\overline{\text{WR}}$ , $\overline{\text{CS}}$ = 0 V
at OUT2	0.25	0.25	0.5	0.5	% FSR max	
REFERENCE INPUT						
R <sub>IN</sub> (Pin 15 to GND) <sup>4</sup>	5 20	5 20	5 20	5 20	kΩ min kΩ max	
ANALOG OUTPUTS						
Output Capacitance <sup>3</sup>						
C <sub>OUT1</sub> (Pin 1)	120	120	120	120	pF max	DB0–DB7 = V <sub>DD</sub> ; $\overline{\text{WR}}$ , $\overline{\text{CS}}$ = 0 V
C <sub>OUT2</sub> (Pin 2)	30	30	30	30	pF max	
C <sub>OUT1</sub> (Pin 1)	30	30	30	30	pF max	DB0–DB7 = 0 V; $\overline{\text{WR}}$ , $\overline{\text{CS}}$ = 0 V
C <sub>OUT2</sub> (Pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement						
V <sub>IH</sub>	+2.4	+13.5	+2.4	+13.5	V min	V <sub>IN</sub> = 0 V or V <sub>DD</sub>
Input LOW Voltage Requirement						
V <sub>IL</sub>	+0.8	+1.5	+0.5	+1.5	V max	
Input Current						
I <sub>IN</sub>	±1	±1	±10	±10	μA max	
Input Capacitance <sup>3</sup>						
DB0–DB7	5	5	5	5	pF max	V <sub>IN</sub> = 0 V V <sub>IN</sub> = 0 V
$\overline{\text{WR}}$ , $\overline{\text{CS}}$	20	20	20	20	pF max	
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time <sup>5</sup>						See Timing Diagram t <sub>WR</sub> = t <sub>CS</sub>
t <sub>CS</sub>						
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time						t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0
t <sub>CH</sub>						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t <sub>WR</sub>						
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time						
t <sub>DS</sub>						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time						
t <sub>DH</sub>						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I <sub>DD</sub>	1 100	2 100	2 500	2 500	mA max μA max	All Digital Inputs V <sub>IL</sub> or V <sub>IH</sub> All Digital Inputs 0 V or V <sub>DD</sub>

## NOTES

<sup>1</sup>Temperature ranges as follows: J, K, L versions:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
A, B, C versions:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
S, T, U versions:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

<sup>2</sup>Gain error is measured using internal feedback resistor. Full-Scale Range (FSR) =  $V_{REF}$ .

<sup>3</sup>Guaranteed not tested.

<sup>4</sup>DAC thin-film resistor temperature coefficient is approximately  $-300\text{ ppm}/^\circ\text{C}$ .

<sup>5</sup>AC parameter, sample tested @  $+25^\circ\text{C}$  to ensure conformance to specification.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS\***(T<sub>A</sub> = +25°C, unless otherwise noted)

V <sub>DD</sub> to GND	−0.3 V, +17 V
V <sub>RFB</sub> to GND	±25 V
V <sub>REF</sub> to GND	±25 V
Digital Input Voltage to GND	−0.3 V to V <sub>DD</sub> +0.3 V
OUT1, OUT2 to GND	−0.3 V to V <sub>DD</sub> +0.3 V

\*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Power Dissipation (Any Package)**

To +75°C	450 mW
Derates above 75°C by	6 mW/°C
<b>Operating Temperature</b>	
Commercial (J, K, L)	−40°C to +85°C
Industrial (A, B, C)	−40°C to +85°C
Extended (S, T, U)	−55°C to +125°C
<b>Storage Temperature</b>	−65°C to +150°C
<b>Lead Temperature (Soldering, 10 secs)</b>	+300°C

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7524 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**TERMINOLOGY**

**RELATIVE ACCURACY:** A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V<sub>REF</sub> range.

**RESOLUTION:** Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2<sup>−n</sup>) (V<sub>REF</sub>). A bipolar converter of n bits has a resolution of [2<sup>−(n−1)</sup>] [V<sub>REF</sub>]. Resolution in no way implies linearity.

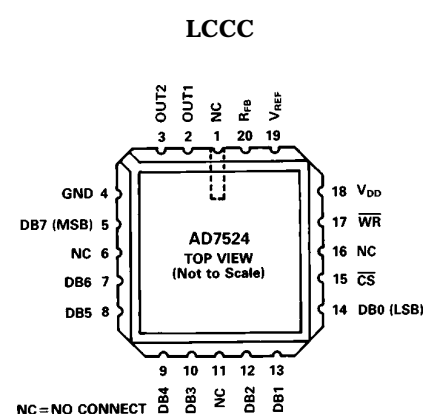
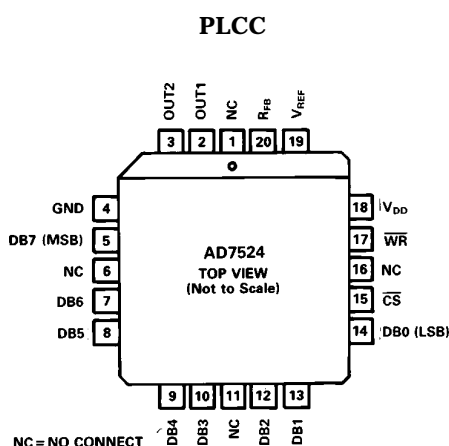
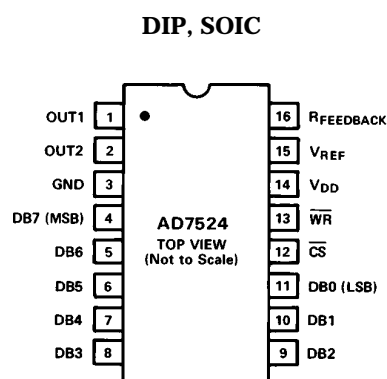
**GAIN ERROR:** Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured

with all 1s in the DAC after offset error has been adjusted out and is expressed in LSBs. Gain Error is adjustable to zero with an external potentiometer.

**FEEDTHROUGH ERROR:** Error caused by capacitive coupling from V<sub>REF</sub> to output with all switches OFF.

**OUTPUT CAPACITANCE:** Capacity from OUT1 and OUT2 terminals to ground.

**OUTPUT LEAKAGE CURRENT:** Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

**PIN CONFIGURATIONS**

AD7524

CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

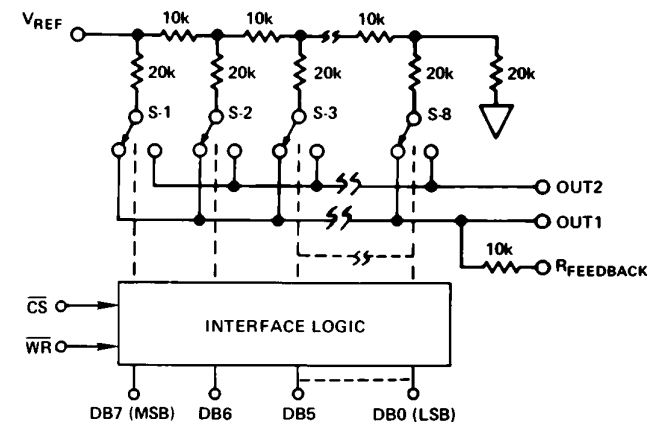


Figure 1. Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source  $I_{LEAKAGE}$  is composed of surface and junction leakages to the substrate

while the  $\frac{1}{256}$  current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The “ON” capacitance of the output N-channel switches is 120 pF, as shown on the OUT2 terminal. The “OFF” switch capacitance is 30 pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the “ON” switches are now on terminal OUT1, hence the 120 pF appears at that terminal.

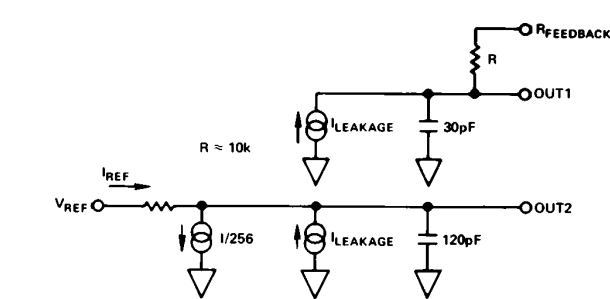


Figure 2. AD7524 DAC Equivalent Circuit—All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the  $\overline{CS}$  and  $\overline{WR}$  inputs.

WRITE MODE

When  $\overline{CS}$  and  $\overline{WR}$  are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

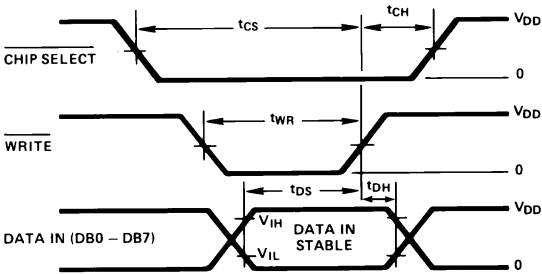
When either  $\overline{CS}$  or  $\overline{WR}$  is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to  $\overline{WR}$  or  $\overline{CS}$  assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0–DB7) inputs.
H	X	Hold	Data bus (DB0–DB7) is Locked Out:
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



- NOTES:
1. All input signal rise and fall times measured from 10% to 90% of  $V_{DD}$ .  $V_{DD} = +5V$ ,  $t_r = t_f = 20ns$ ;  $V_{DD} = +15V$ ,  $t_r = t_f = 40ns$ .
  2. Timing Measurement Reference level is  $\frac{V_{IH} + V_{IL}}{2}$ .
  3.  $t_{DS} + t_{DH}$  is approximately constant at 145ns min at  $+25^\circ C$ ;  $V_{DD} = +5V$  and  $t_{WR} = 170ns$  min. The AD7524 is specified for a minimum  $t_{DH}$  of 10ns, however, in applications where  $t_{DH} > 10ns$ ,  $t_{DS}$  may be reduced accordingly up to the limit  $t_{DS} = 65ns$ ,  $t_{DH} = 80ns$ .

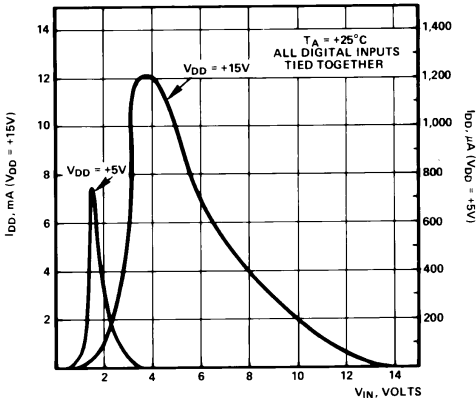


Figure 3. Supply Current vs. Logic Level  
Typical plots of supply current,  $I_{DD}$ , versus logic input voltage,  $V_{IN}$ , for  $V_{DD} = +5V$  and  $V_{DD} = +15V$  are shown above.

## ANALOG CIRCUIT CONNECTIONS

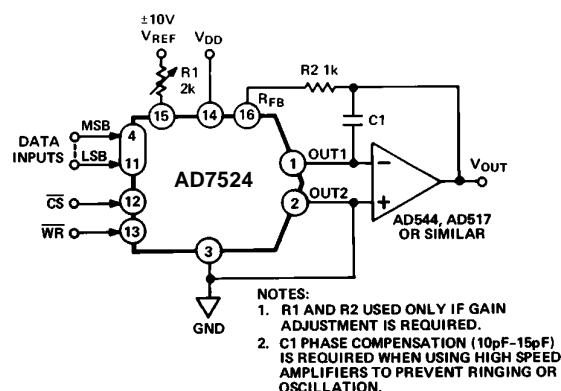


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

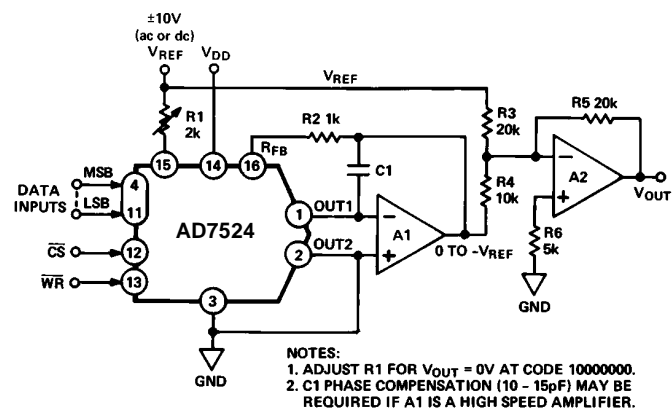


Figure 5. Bipolar (4-Quadrant) Operation

Table I. Unipolar Binary Code Table

Digital Input MSB    LSB	Analog Output
1111 1111	$-V_{REF}$ (255/256)
1000 0001	$-V_{REF}$ (129/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0111 1111	$-V_{REF}$ (127/256)
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

Note: 1 LSB =  $(2^{-8})(V_{REF}) = 1/256 (V_{REF})$

Table II. Bipolar (Offset Binary) Code Table

Digital Input MSB    LSB	Analog Output
1111 1111	$+V_{REF}$ (127/128)
1000 0001	$+V_{REF}$ (1/128)
1000 0000	0
0111 1111	$-V_{REF}$ (1/128)
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Note: 1 LSB =  $(2^{-7})(V_{REF}) = 1/128 (V_{REF})$

## MICROPROCESSOR INTERFACE

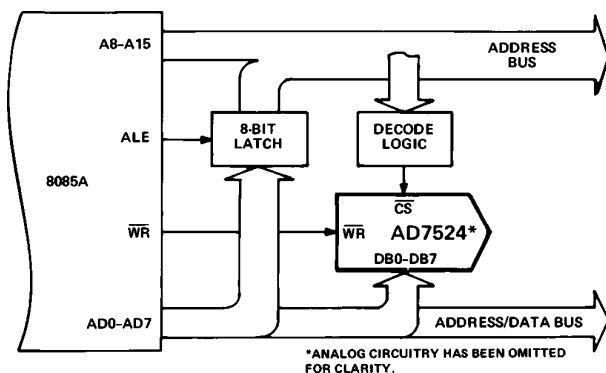


Figure 6. AD7524/8085A Interface

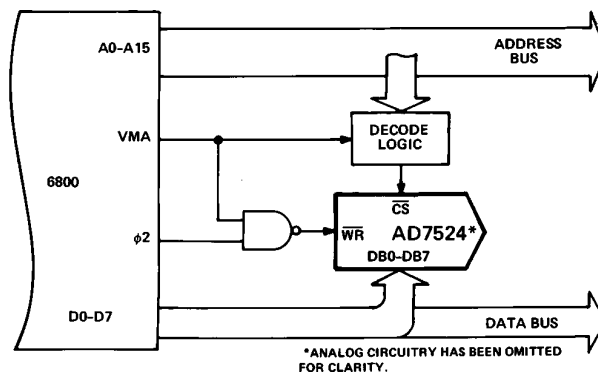


Figure 7. AD7524/MC6800 Interface

## POWER GENERATION

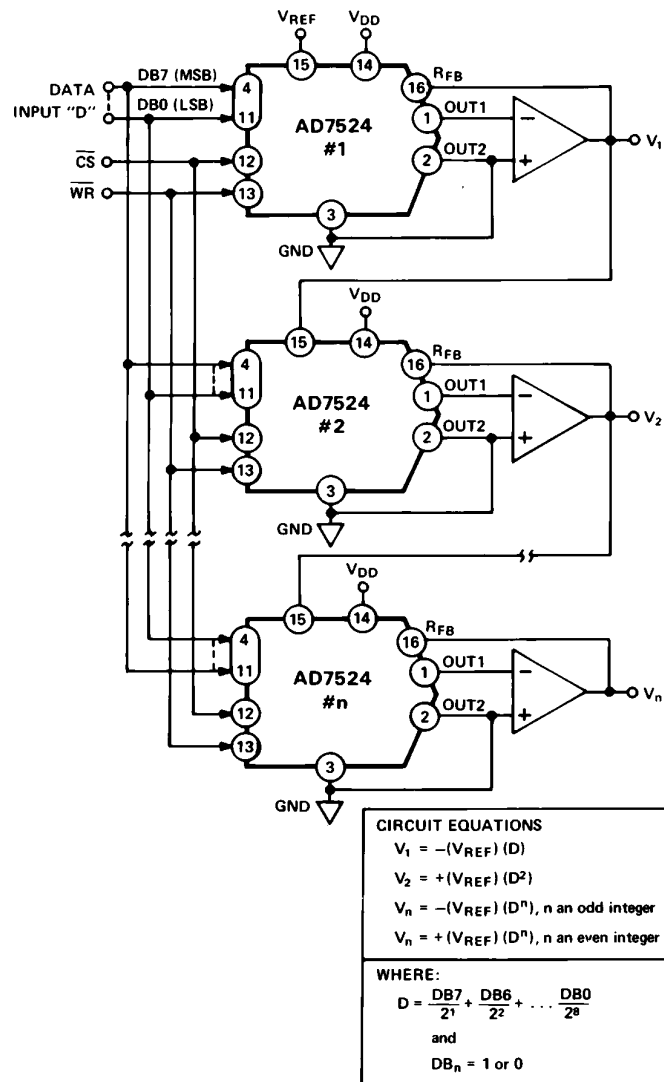
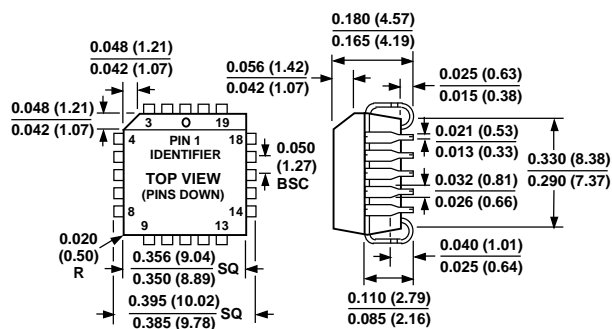


Figure 8.

Dimensions shown in inches and (mm).

### 20-Lead Plastic Leadless Chip Carrier (PLCC) (P-20A)



### 16-Lead Cerdip (Q-16)

