

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOC莫斯 HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOC莫斯 HE4000B Logic Package Outlines/Information HEF, HEC

HEF4030B **gates** Quadruple exclusive-OR gate

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple exclusive-OR gate**HEF4030B
gates****DESCRIPTION**

The HEF4030B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

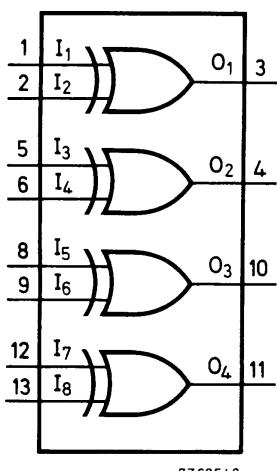


Fig.1 Functional diagram.

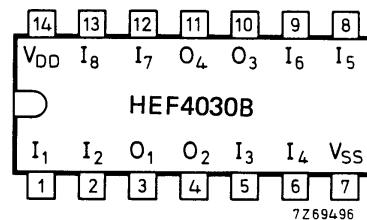


Fig.2 Pinning diagram.

HEF4030BP(N): 14-lead DIL; plastic
(SOT27-1)

HEF4030BD(F): 14-lead DIL; ceramic (cerdip)
(SOT73)

HEF4030BT(D): 14-lead SO; plastic
(SOT108-1)

(): Package Designator North America

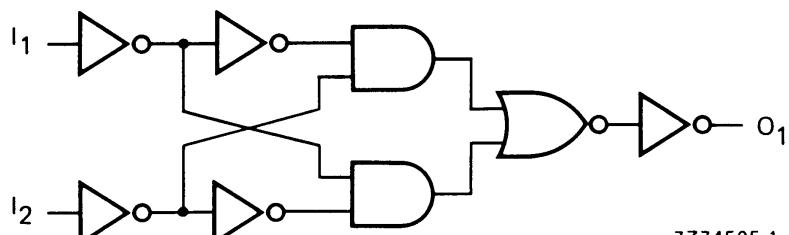


Fig.2 Logic diagram (one gate).

TRUTH TABLE

I ₁	I ₂	O ₁
L	L	L
H	L	H
L	H	H
H	H	L

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Quadruple exclusive-OR gate

HEF4030B
gates**AC CHARACTERISTICS** $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	85	175	ns
	10		35	75	ns
	15		30	55	ns
	5	t_{PLH}	75	150	ns
	10		30	65	ns
	15		25	50	ns
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns
	10		30	60	ns
	15		20	40	ns
	5	t_{TLH}	60	120	ns
	10		30	60	ns
	15		20	40	ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	$1\ 100 f_i + \sum(f_o CL) \times V_{DD}^2$ $4\ 900 f_i + \sum(f_o CL) \times V_{DD}^2$ $14\ 400 f_i + \sum(f_o CL) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) CL = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)