8.1

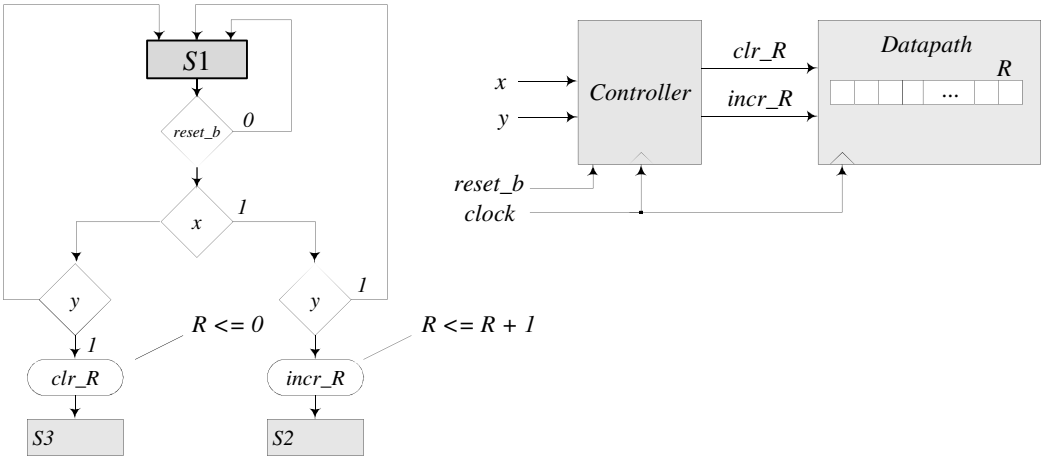
(a) The transfer and increment occur concurrently, i.e., at the same clock edge. After the transfer, R2 holds the contents that were in R1 before the clock edge, and R2 holds its previous value incremented by 1.

(b) Decrement the content of R3 by one.

(c) If (T_1 = 1), transfer content of R1 to R0.

If (T_1 = 0 and T_2 = 1), transfer content of R2 to R0.

8.2



8.5

The operations specified in a flowchart are executed sequentially, one at a time. The operations specified in an ASM chart are executed concurrently for each ASM block. Thus, the operations listed within a state box, the operations specified by a conditional box, and the transfer to the next state in each ASM block are executed at the same clock edge. For example, in Fig. 8.5 with Start = 1 and Flag = 1, signal Flush_R is asserted. At the clock edge the state moves to S_2, and register R is flushed.

An ASM chart describes the state transitions and output signals generated by a finite state machine in response to its input signals. An ASMD chart is an ASM chart that has been annotated to indicate the register operations that are executed by the machine in response to the control signals (outputs) generated by the state machine.

8.7

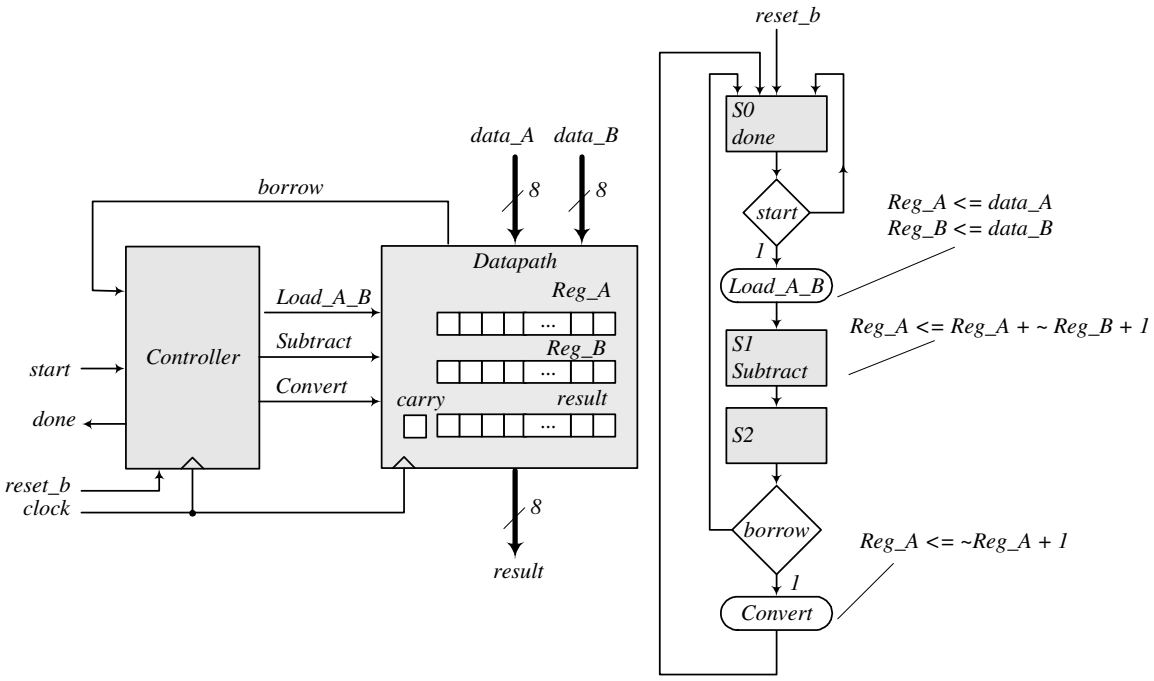
RTL notation:

*S*0: Initial state: if (start = 1) then (*RA* ← data_*A*, *RB* ← data_*B*, go to *S*1).

*S*1: {Carry, *RA}* ← *RA* + (2's complement of *RB*), go to *S*2.

*S*2: If (borrow = 0) go to *S*0. If (borrow = 1) then *RA* ← (2's complement of *RA*), go to *S*0.

Block diagram and ASMD chart:



8.8

RTL notation:

*S*0: if (start = 1) *AR* ← input data, *BR* ← input data, go to *S*1.

*S*1: if (AR [15]) = 1 (sign bit negative) then *CR* ← *AR*(shifted right, sign extension).

else if (positive non-zero) then (Overflow ← *BR*([15] ⊕ [14]), *CR* ← *BR*(shifted left)

else if (*AR* = 0) then (CR ← 0).