National Chiao Tung University
Computer Science Department

INTRODUCTION TO ELECTRIC AND ELECTRONIC CIRCUITS

Assignment [3] : Laplace Transforms & CMOS Logic Circuits

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Issuing date:	Tuesday, January 8, 2013
Submission due date:	Tuesday, January 22, 2013

Homework Reading

- Zao & Peng, "EE Circuit Notes", 2008. Sect. 3.5 – 3.7; pp. 30 – 41
- Strum & Ward, "Electric Circuits and Networks", 1985. Ch. 3,4 & 5; pp. 95 – 167

Part 1. Conceptual Questions **30%**

1.1 Please define the following concepts with respect to a linear time-invariant system:

- *Impulse Response* $h(t)$ 3%
- *Transfer Function* in Laplace domain $H(s)$ 3%
- *Frequency Response Function* $H(\omega)$ 3%

Please specify the relations between $h(t), H(s)$ and $H(\omega)$. 8%

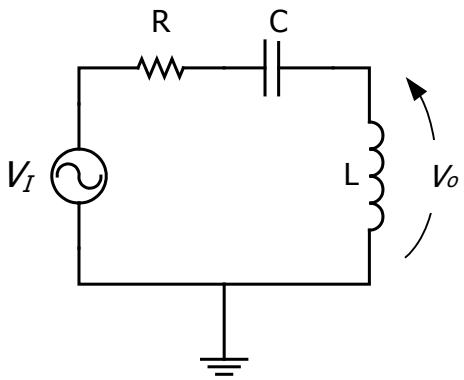
1.2 Please define the concept of *impedance* $Z(s)$ of a device in Laplace domain 3%

1.3 Please use Laplace transform to derive the formulae of the KVL (voltage based) & KCL (current based) equivalent circuits of a capacitor. 10%
Note: please refer to Section 3.6 of EE Circuit Notes for details.

Part 2. Analytical Questions, Laplace Transforms **40&**

2.1 Given the *serial RLC circuit* with input voltage source $V_I(s)$ and output voltage $V_O(s)$, please derive the following expressions assuming *zero* initial conditions:

- *System Equation* in Laplace (s) domain 10%
- *System Transfer Function* $H(s)$ 5%



Now, assume that the electric components take the following two sets of values.

- Set #1: $R = 100\Omega, L = 1mH, C = 1nF$
- Set #2: $R = 1K\Omega, L = 1mH, C = 1nF$

Compute the parameter values and output functions of the circuit corresponding to the two sets of component values:

- *System Poles* $\{s_p, s_p'\}$ and *Zeros* $\{s_z, s_z'\}$ 5%
- *Frequent Response* $H(j\omega)$ 5%
- *Impulse Response* $h(t)$ 10%
- *Sinusoidal (Steady State) Response* $v_{Oss}(t)$ towards the input $v_I(t) = \cos(10^6 \times t)$ 5%

Part 3. Analytical Questions, CMOS Logic

Please complete the following marked questions on the next electronically scanned pages:

- 16.49 – All Parts
- 16.54 – Parts (a) & (b)
- 16.55 – Parts (a) & (b)
- 16.59 – Parts (a)

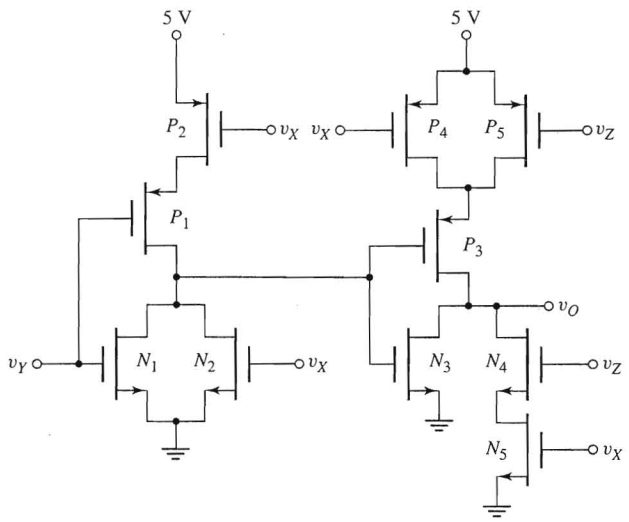


Figure P16.49

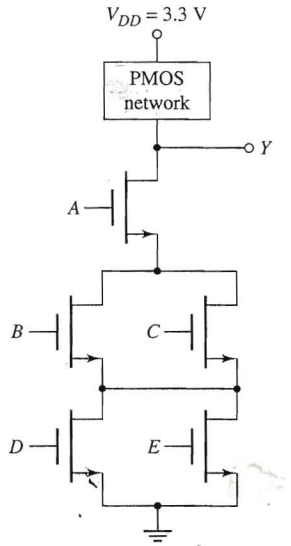


Figure P16.54

determine the relationship between $(W/L)_p$ and $(W/L)_n$ such that $v_I = 2.5$ V when all transistors are biased in the saturation region. (c) Using the results of part (b) and assuming $v_A = v_B = 5$ V, determine v_C such that both N_3 and P_3 are biased in the saturation region. (State any assumptions you make.)

16.49 Consider the circuit in Figure P16.49. (a) The inputs v_X, v_Y, and v_Z listed in the following table are either a logic 0 or a logic 1. These inputs are the outputs from similar-type CMOS logic circuits. The input logic conditions listed are sequential in time. State whether the transistors listed are "on" or "off," and determine the output voltage. (b) What logic function does this circuit implement?

Logic "0" = +0V
Logic "1" = +5V

v_X	v_Y	v_Z	N_1	N_2	N_3	N_4	N_5	v_O
1	0	1						
0	0	1						
1	1	0						
1	1	1						

16.50 Consider a four-input CMOS NOR logic gate. Determine the W/L ratios of the transistors to provide for symmetrical switching based on the CMOS inverter design with $(W/L)_n = 2$ and $(W/L)_p = 4$. (b) If the load capacitance of the NOR gate doubles, determine the required W/L ratios to provide the same switching speed as the logic gate in part (a).

16.51 Repeat Problem 16.50 for a four-input CMOS NAND logic gate.

16.52 Repeat Problem 16.50 for a three-input CMOS NOR logic gate.

16.53 Repeat Problems 16.50 for a three-input CMOS NAND logic gate.

16.54 Figure P16.54 is a classic CMOS logic gate. (a) What is the logic function performed by the circuit? (b) Design the PMOS network. (c) Determine the transistor W/L ratios to provide symmetrical switching times equal to the basic CMOS inverter with $(W/L)_n = 2$ and $(W/L)_p = 4$.

16.55 Figure P16.55 is a classic CMOS logic gate. (a) What is the logic function performed by the circuit? (b) Design the PMOS network. (c) Determine the transistor W/L ratios to provide symmetrical switching times at twice the switching speed as the basic CMOS inverter with $(W/L)_n = 2$ and $(W/L)_p = 4$.

16.56 Figure P16.56 is a classic CMOS logic gate. (a) What is the logic function performed by the circuit? (b) Design the NMOS network. (c) Determine the transistor W/L ratios to provide symmetrical switching times equal to the basic CMOS inverter with $(W/L)_n = 2$ and $(W/L)_p = 4$.

16.57 Figure P16.57 is a classic CMOS logic gate. (a) What is the logic function performed by the circuit? (b) Design the NMOS network. (c) Determine the transistor W/L ratios to provide symmetrical switching times at twice the switching speed of the basic CMOS inverter with $(W/L)_n = 2$ and $(W/L)_p = 4$.

D16.58 (a) Given inputs A, B, and C, design a CMOS circuit to implement the logic function $Y = ABC + \overline{ABC}$. (b) For $k'_n = 2k'_p$ and assuming a minimum width-to-length ratio of unity, size the transistors in the design to provide equal switching characteristics.

D16.59 (a) Given inputs A, B, C, and D, design a CMOS circuit to implement the logic function $Y = \overline{(A + B)C + D}$. (b) Repeat part (b) of Problem 16.58 for this circuit.

16.60 Determine the logic function implemented by the circuit in Figure P16.60.

16.61 Consider a five-input CMOS NAND logic gate. Design the width-to-length ratios of the transistors for symmetrical switching characteristics of the NMOS and PMOS portions of the circuit and such that the switching times are the same as the basic CMOS inverter with $(W/L)_n = 2$ and $(W/L)_p = 4$.

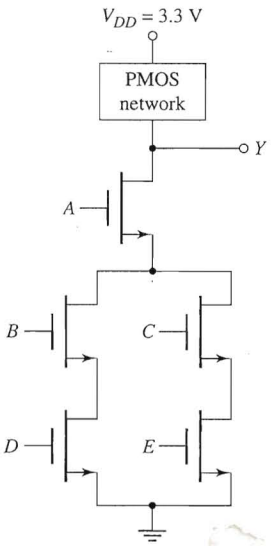


Figure P16.55

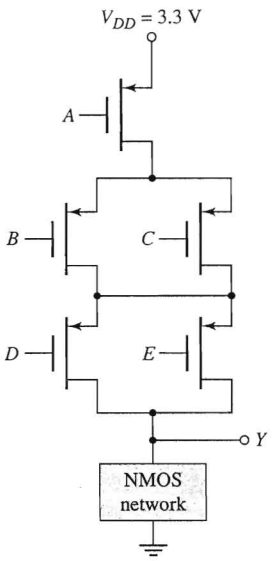


Figure P16.56

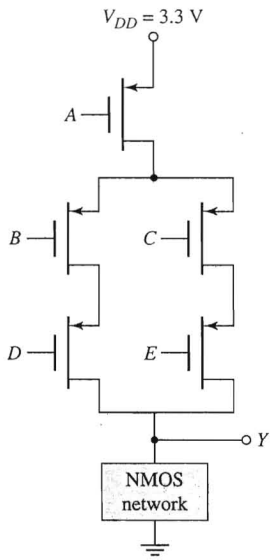


Figure P16.57

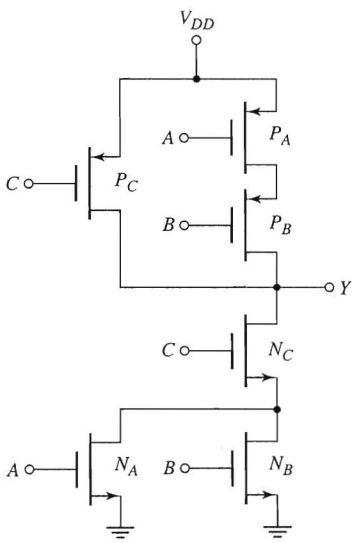


Figure P16.60

Section 16.5 Clocked CMOS Logic Circuits

16.62 (a) Figure P16.62 shows a clocked CMOS logic circuit. Make a table showing the state of each transistor ("on" or "off"), and determine the output

voltages v_{O1} and v_{O2} for the input logic states listed in the following table. Assume the input conditions are sequential in time from state 1 to state 6. (b) What logic function does the circuit implement?

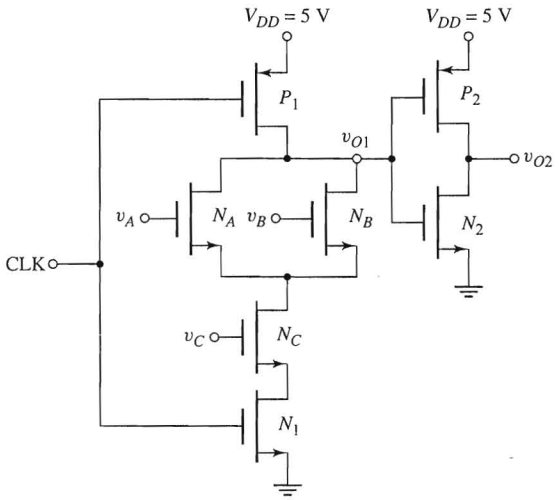


Figure P16.62

State	CLK	v_A	v_B	v_C
1	0	0	0	0
2	1	1	0	0
3	0	0	0	0
4	1	0	0	1
5	0	0	0	0
6	1	0	1	1

16.63 (a) For the circuit in Figure P16.63, make a table showing the state of each transistor ("on" or "off"), and determine the output voltages v_{O1}, v_{O2}, and v_{O3} for the input logic states listed in the following table. Assume the input conditions are sequential in time from state 1 to state 6. (b) What logic function does the circuit implement?

State	CLK	v_X	v_Y	v_Z
1	0	0	0	0
2	1	1	1	1
3	0	0	0	0
4	1	0	1	1
5	0	0	0	0
6	1	1	0	1

D16.64 Sketch a clocked CMOS domino logic circuit that realizes the function $Y = ABC + \bar{A}\bar{B}\bar{C}$. Assume that both the variable and its complement are available as input signals.

D16.65 Sketch a clocked CMOS domino logic circuit that realizes the function $Y = (A + B)C + D$.

D16.66 Sketch a clocked CMOS domino logic circuit that realizes the function $Y = (A + B)(C + D)(E + F)$.