CSEE ELECTRONICS (II) LECTURE NOTES

MOSFET LOGIC

Logic Circuit Design

John K. Zao

2010/05/07 (Monday)

P.1

ALL CMOS Logic Circuits can be divided into TWO PARTS:

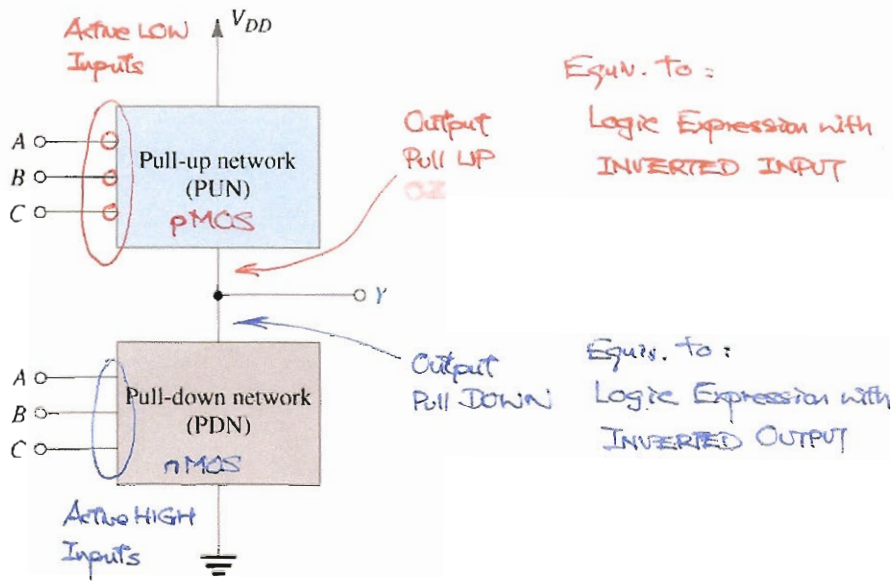


Figure 10.8 Representation of a three-input CMOS logic gate. The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

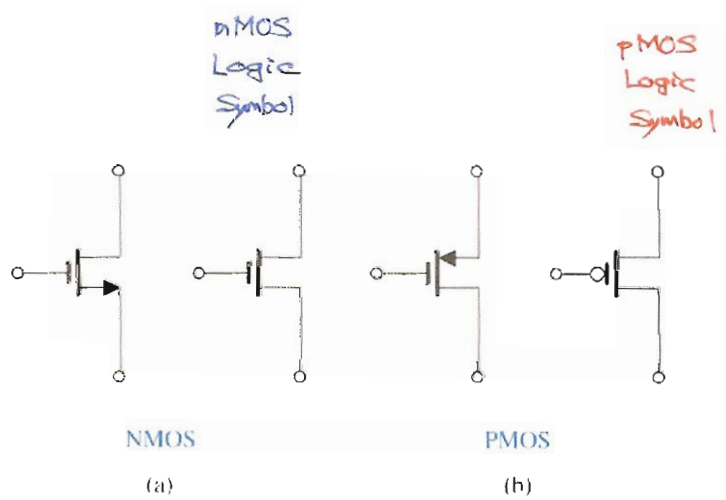
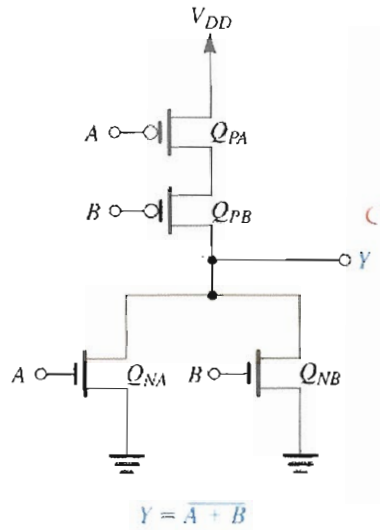


Figure 10.11 Usual and alternative circuit symbols for MOSFETs.

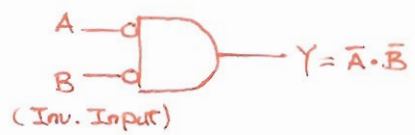
CSEE ELECTRONICS (II), LECTURE NOTES
MOSFET Logic
Logic Circuit Design

John K. Zao
2010/05/07 (Monday)
P.2

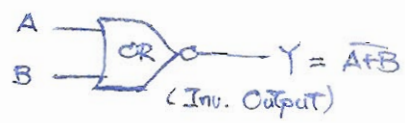
AND ⇔ Serial Connection



$Y = \bar{A} \cdot \bar{B}$



$\bar{Y} = A + B$



OR ⇔ Parallel Connection

Figure 10.12 A two-input CMOS NOR gate.

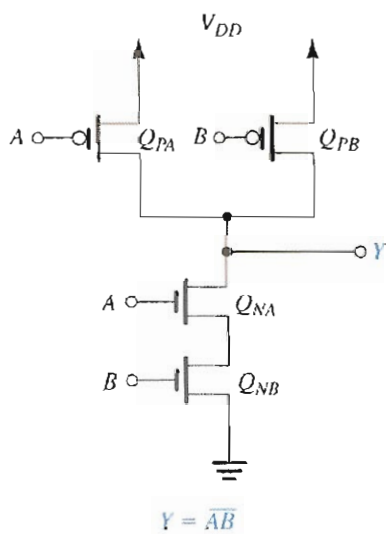


Figure 10.13 A two-input CMOS NAND gate.

Example : nMOS Pull-Down Networks

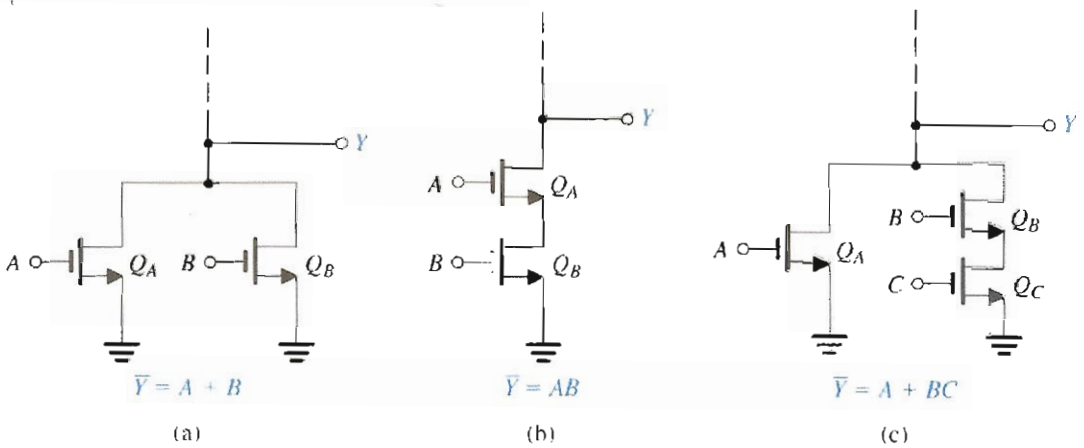


Figure 10.9 Examples of pull-down networks.

Example : pMOS Pull-Up Networks

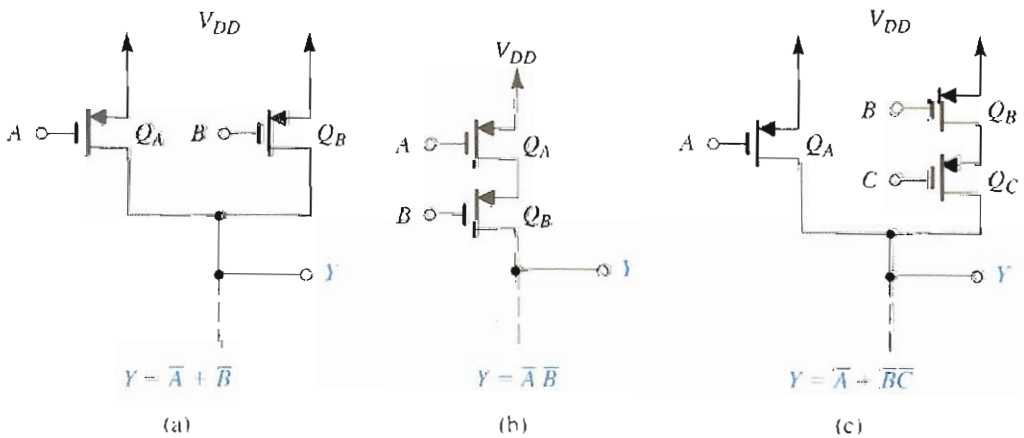


Figure 10.10 Examples of pull-up networks.