

MOSFET as a switch

Resistor-Transistor (MOS) Logic, Inverter

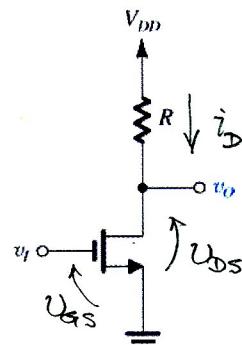


Figure P4.41

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86

Complementary MOS (CMOS) Logic, Inverter

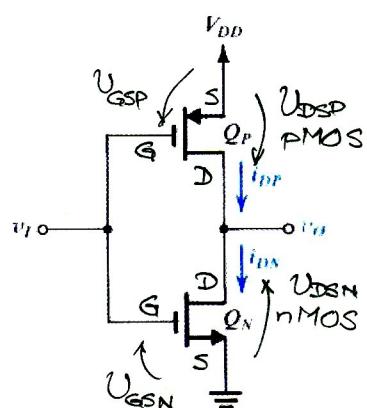


Figure 4.53 The CMOS inverter.

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67

P.2

Resistor-Transistor (MOS) Logic, Switching Operation

MOSFET Output i-V Characteristics vs. Resistive Load Line

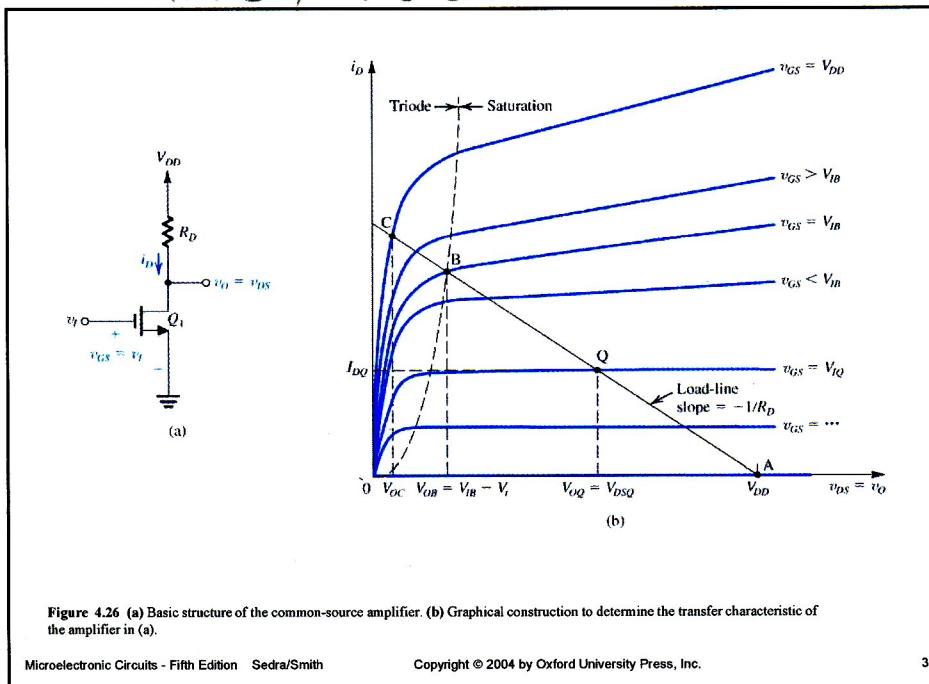


Figure 4.26 (a) Basic structure of the common-source amplifier. (b) Graphical construction to determine the transfer characteristic of the amplifier in (a).

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31

RTL (MOS) Transfer Characteristics.

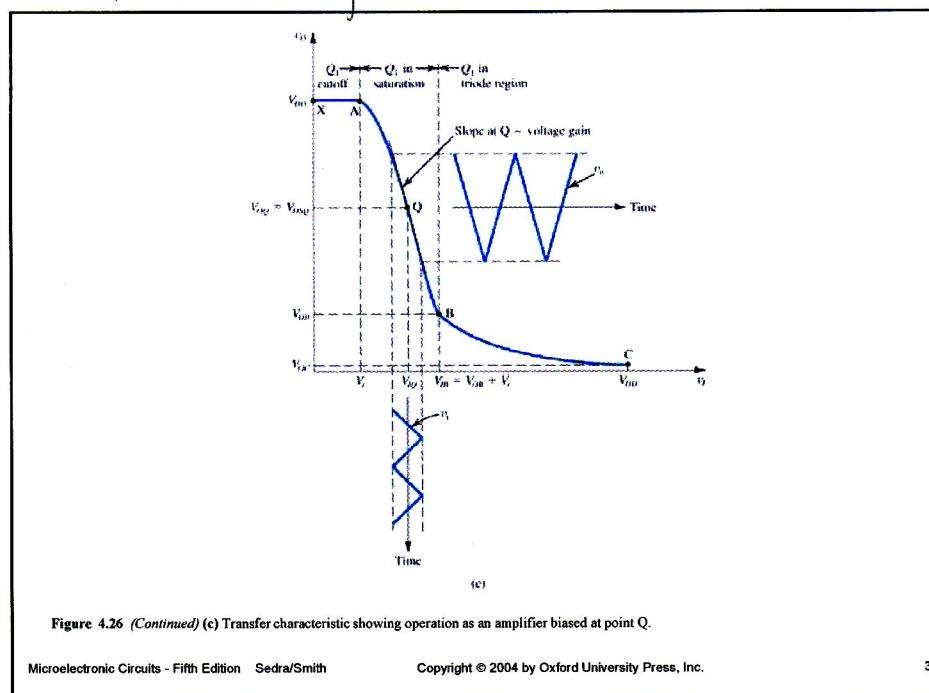


Figure 4.26 (Continued) (c) Transfer characteristic showing operation as an amplifier biased at point Q.

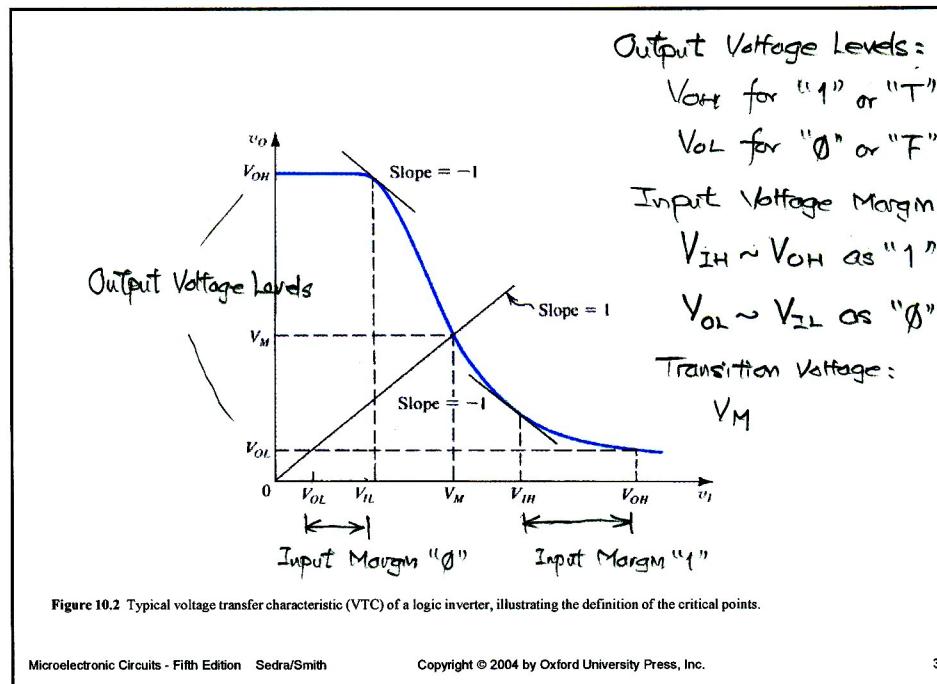
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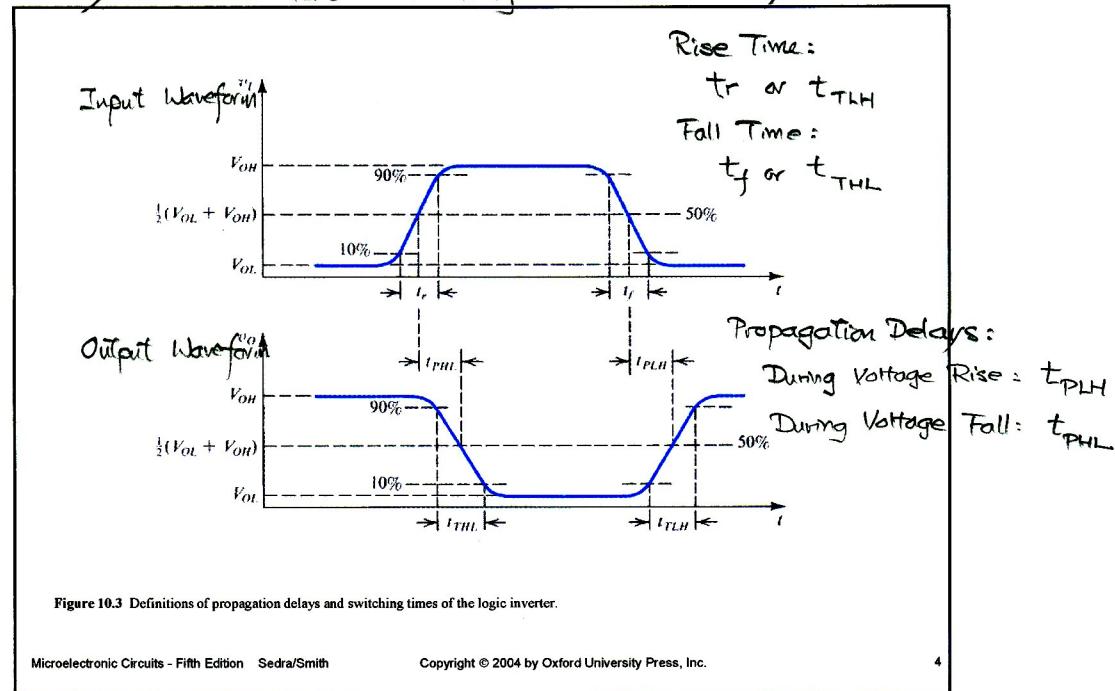
32

Operational Specification of Logic Circuits

Static Parameters



Dynamic Parameters (Switching Characteristics)



Complementary MOSFET (CMOS) Logic Circuit

Basic CMOS Inverter : Circuit & Concept of Operation

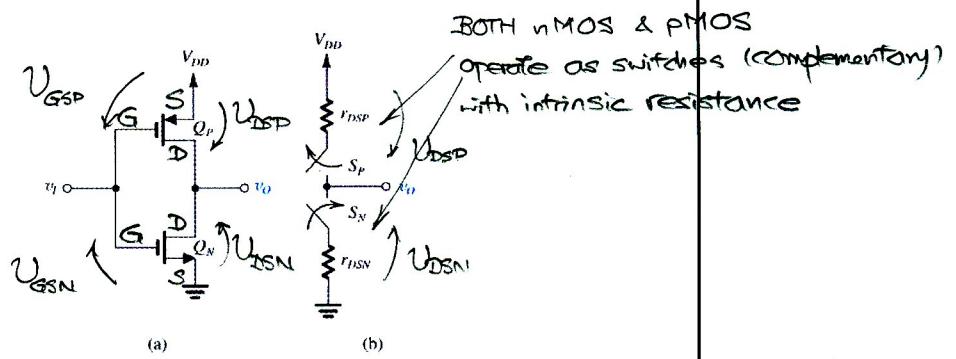


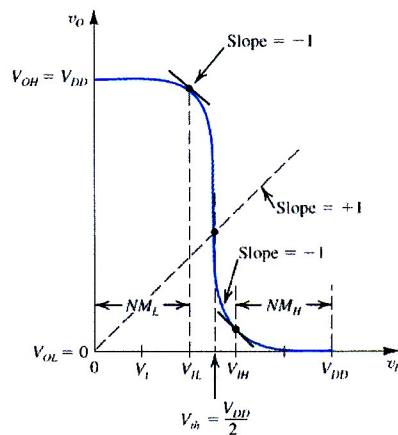
Figure 10.4 (a) The CMOS inverter and (b) its representation as a pair of switches operated in a complementary fashion.

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5

Basic CMOS Inverter : Transfer Characteristics

Figure 10.5 The voltage transfer characteristic (VTC) of the CMOS inverter when Q_N and Q_P are matched.

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6

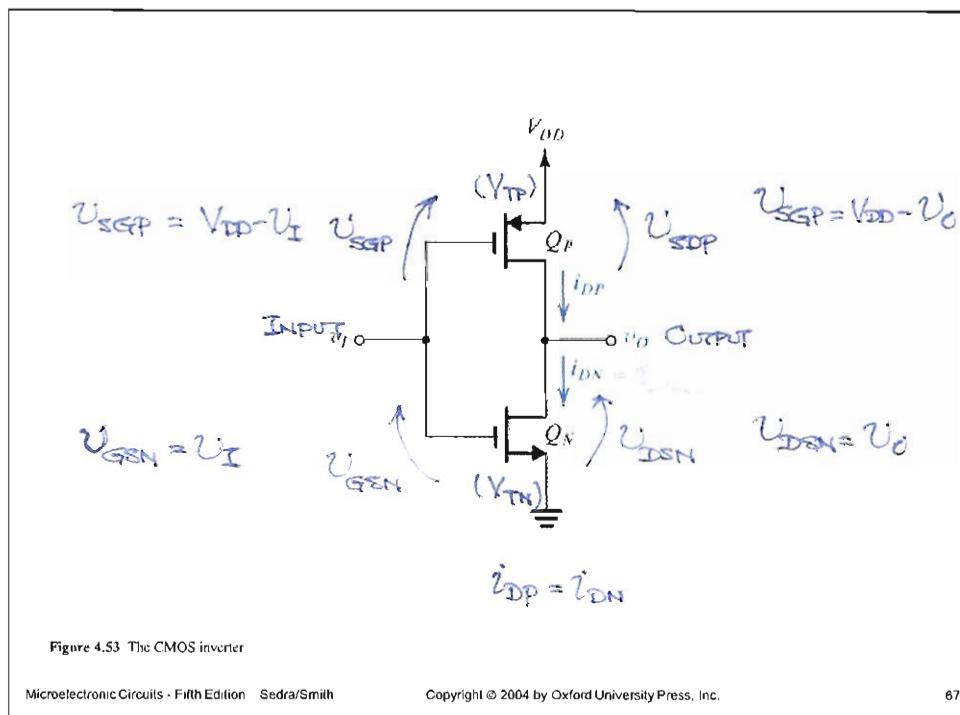


Figure 4.53 The CMOS inverter

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67

OPERATION REGIONS

- ① nMOS OFF
PMOS Triode
- ② nMOS Saturation
PMOS Triode
- ③ nMOS Saturation
PMOS Saturation
- ④ nMOS Triode
PMOS Saturation
- ⑤ nMOS Triode
PMOS OFF

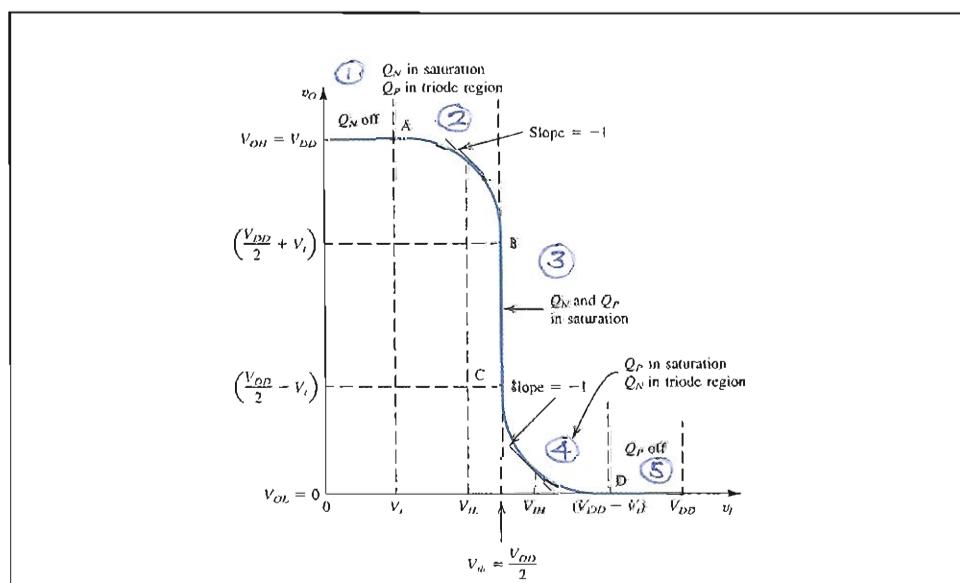


Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

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70

nMOS Operation Modes

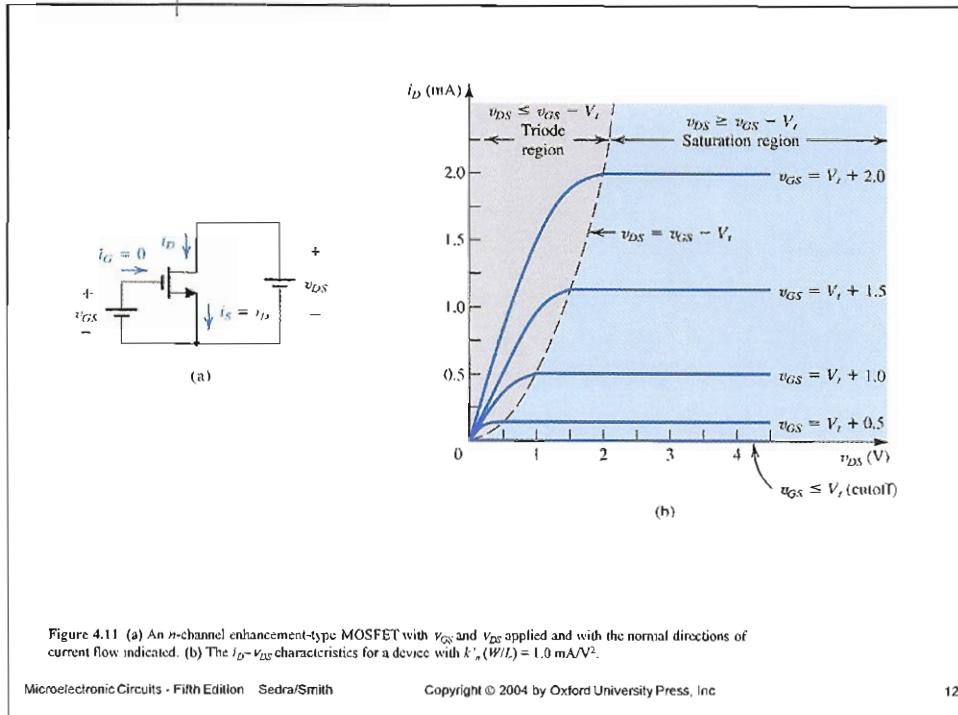


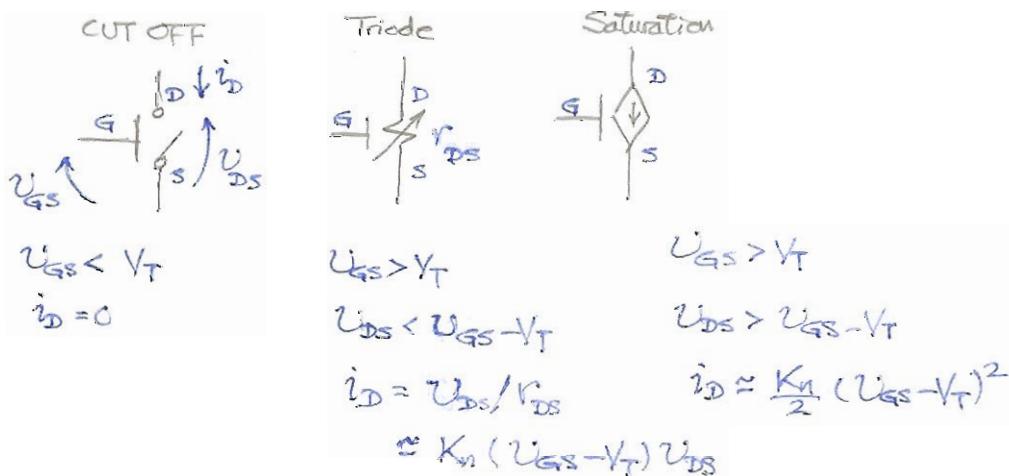
Figure 4.11 (a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. (b) The i_D - v_{DS} characteristics for a device with $k'_n (W/L) = 1.0 \text{ mA/V}^2$.

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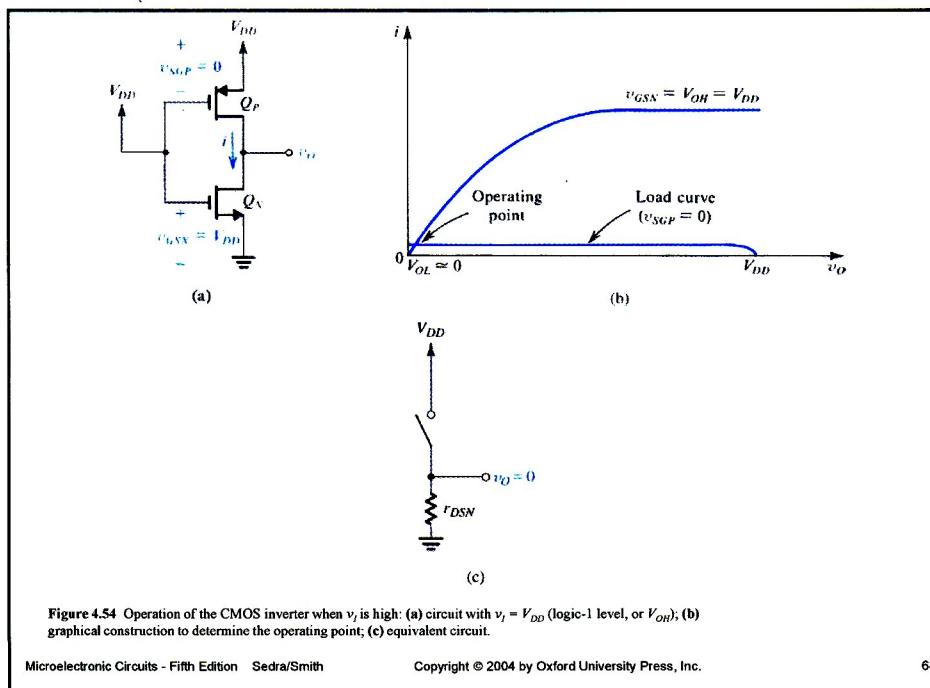
12

Large Signal Equivalent Circuits:



CMOS Switching Operation

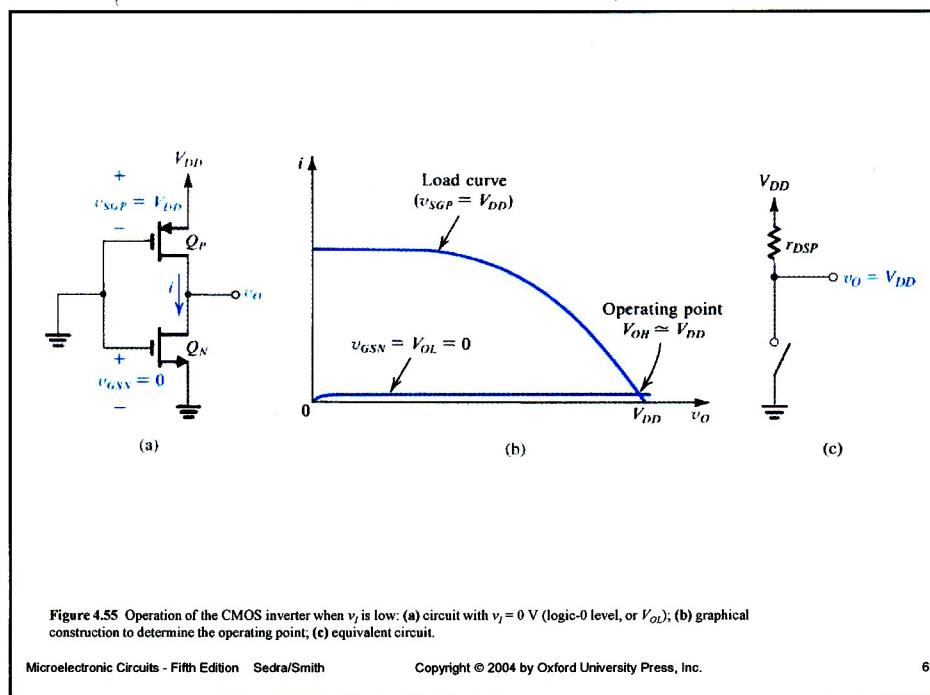
P5

Input = "1" $V_{GSN} = V_{DD}$ Figure 4.54 Operation of the CMOS inverter when v_i is high: (a) circuit with $v_i = V_{DD}$ (logic-1 level, or V_{OH}); (b) graphical construction to determine the operating point; (c) equivalent circuit.

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68

Input = "0" $V_{GSN} = \text{Ground (0V)}$ Figure 4.55 Operation of the CMOS inverter when v_i is low: (a) circuit with $v_i = 0$ V (logic-0 level, or V_{OL}); (b) graphical construction to determine the operating point; (c) equivalent circuit.

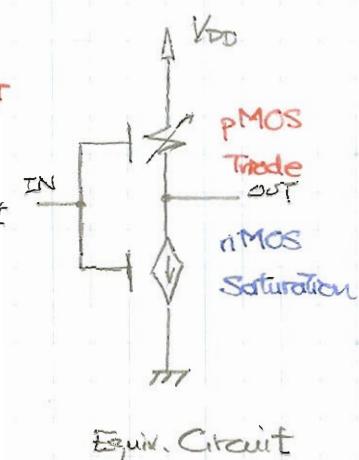
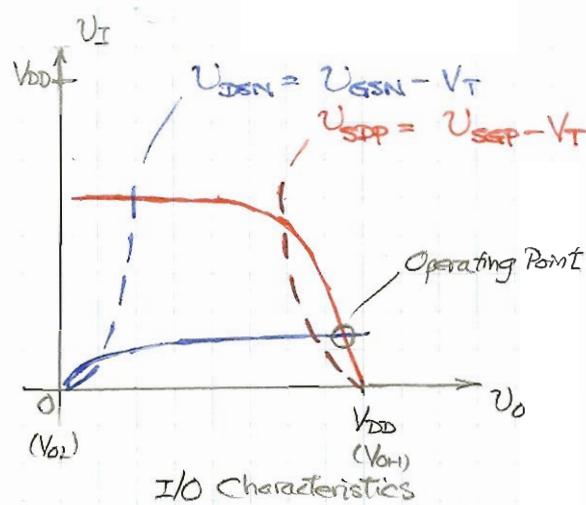
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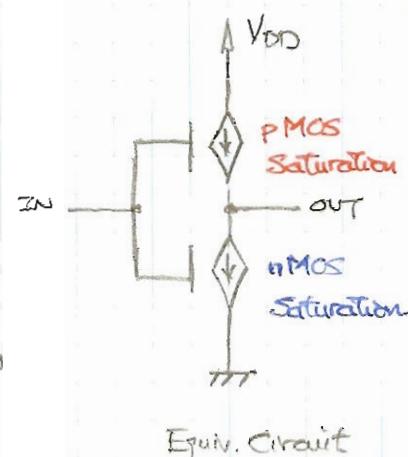
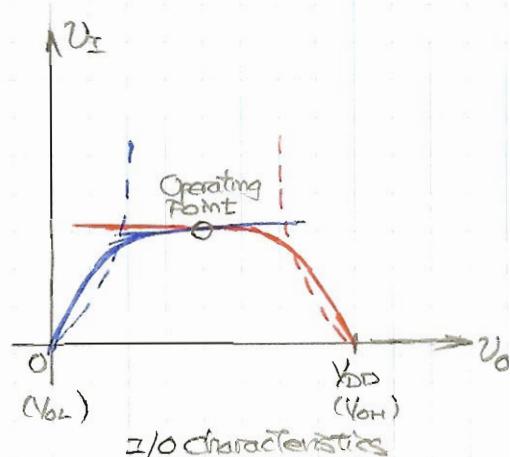
69

Region ②

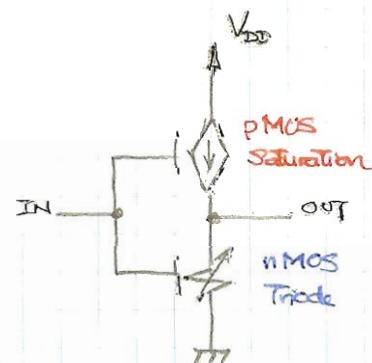
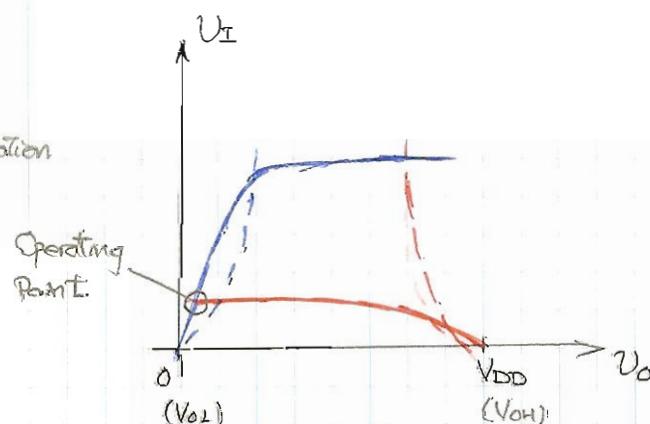
nMOS Saturation
pMOS Triode

Region ③

nMOS Saturation
pMOS Saturation

Region ④

nMOS Triode
pMOS Saturation



Static Switching characteristics

Determination of Input/Output Noise Margins (V_{IL} , V_{IH})

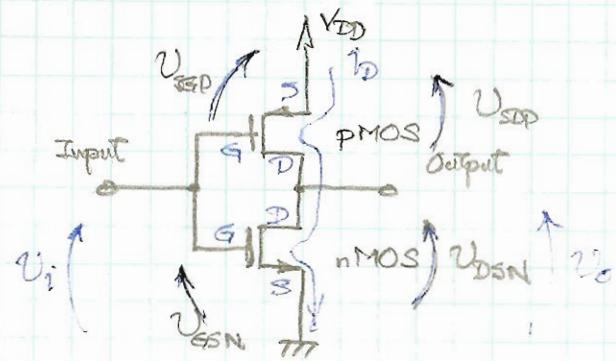
<Defn> Input/Output Noise Margins of Digital Logic Circuits are bounded by their Low/High Output Voltages and the input voltages at which the slope of input-output transfer characteristics equals to -1.

At $V_I = V_{IL}$,

CMOS is in Operation Region (2).

- ▷ nMOS is in Saturation Mode
- ▷ pMOS is in Triode Mode

Hence,



$$(\text{Saturation}) \quad i_{DSN} = \frac{K_n}{2} (V_{GSN} - V_T)^2 \quad \text{with } V_{GSN} = V_i \quad (1)$$

$$(\text{Triode}) \quad i_{SDP} = K_p \left[(V_{GSP} - V_T) V_{SDP} - \frac{V_{SDP}^2}{2} \right] \quad \text{with } V_{GSP} = V_{DD} - V_i \quad (2)$$

$$V_{SDP} = V_{DD} - V_o$$

Now, with $i_D = i_{DSN} = i_{SDP}$, and subs. input & output voltages into Eqs (1)&(2)

Also, assume $K_n = K_p = K$

Then,

$$\frac{K}{2} (V_i - V_T)^2 = K \left[(V_{DD} - V_i - V_T)(V_{DD} - V_o) - \frac{(V_{DD} - V_o)^2}{2} \right] \quad (3)$$

$$\Rightarrow (V_i - V_T)^2 = (V_{DD} - 2V_i + V_o - V_T)(V_{DD} - V_o)$$

Differentiate both side by V_i

$$\text{LHS: } \frac{\partial}{\partial V_i} (V_i - V_T)^2 = 2(V_i - V_T)$$

$$\text{RHS: } \frac{\partial}{\partial V_i} (V_{DD} - 2V_i + V_o - V_T)(V_{DD} - V_o)$$

$$= \left(\frac{\partial V_o}{\partial V_i} - 2 \right) (V_{DD} - V_o) + (V_{DD} - 2V_i + V_o - V_T) \left(-\frac{\partial V_o}{\partial V_i} \right)$$

Equating LHS & RHS, we get:

$$2(V_I - V_T) = (V_{DD} - V_o) \frac{\partial V_o}{\partial V_I} - 2(V_{DD} - V_o) - \frac{\partial V_o}{\partial V_I} (V_{DD} - 2V_I + V_o - V_T)$$

At $V_I = V_{IL}$, $\frac{\partial V_o}{\partial V_I} = -1$ by definition.

Thus,

$$\begin{aligned} 2(V_{IL} - V_T) &= -(V_{DD} - V_o) - 2(V_{DD} - V_o) + (V_{DD} - 2V_{IL} + V_o - V_T) \\ &= -3V_{DD} + 3V_o + V_{DD} - 2V_{IL} + V_o - V_T \end{aligned}$$

$$\begin{aligned} 4V_{IL} &= -2V_{DD} + 2V_T - V_T + 4V_o \\ &= 4V_o - 2V_{DD} + V_T. \end{aligned}$$

$$\Rightarrow 4V_o = 4V_{IL} + 2V_{DD} - V_T$$

$$\Rightarrow V_o = V_{IL} - \frac{V_{DD}}{2} - \frac{V_T}{4}.$$

Subs. V_o back to Eqn (3), we obtain:

$$\& V_I = V_{IL}$$

$$\boxed{V_{IL} = \frac{1}{8}(3V_{DD} + 2V_T)}.$$

Similar derivation gives:

$$\boxed{V_{IH} = \frac{1}{8}(5V_{DD} - 2V_T).}$$

I/O characteristics (Voltage)

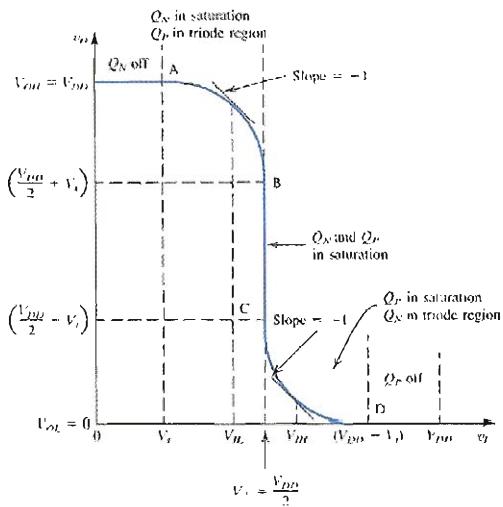


Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

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70

Current ($I_{DSN} = I_{SDP}$) DISSIPATION

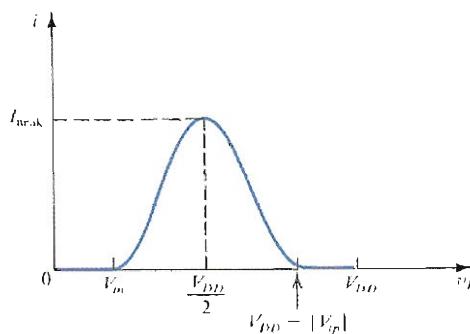


Figure 4.58 The current in the CMOS inverter versus the input voltage.

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72

Course of Finite Rise/Fall Time & Propagation Delays

Intrinsic & Lead Capacitance

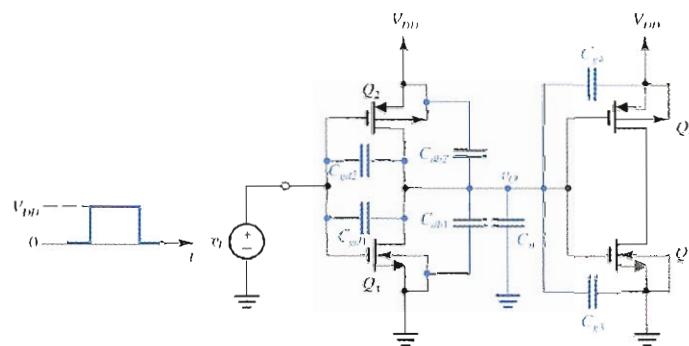


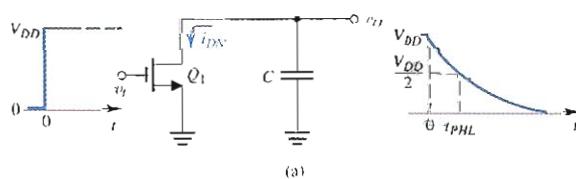
Figure 10.6 Circuit for analyzing the propagation delay of the inverter formed by Q_1 and Q_2 , which is driving an identical inverter formed by Q_3 and Q_4 .

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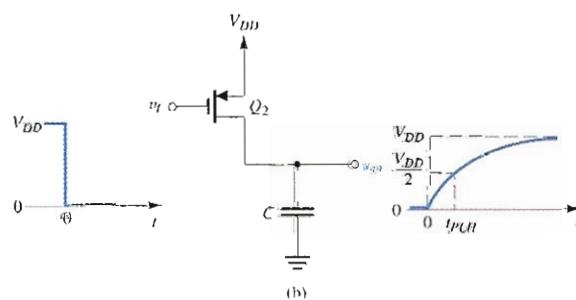
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7

Effects of Intrinsic & Lead Capacitance



(a)



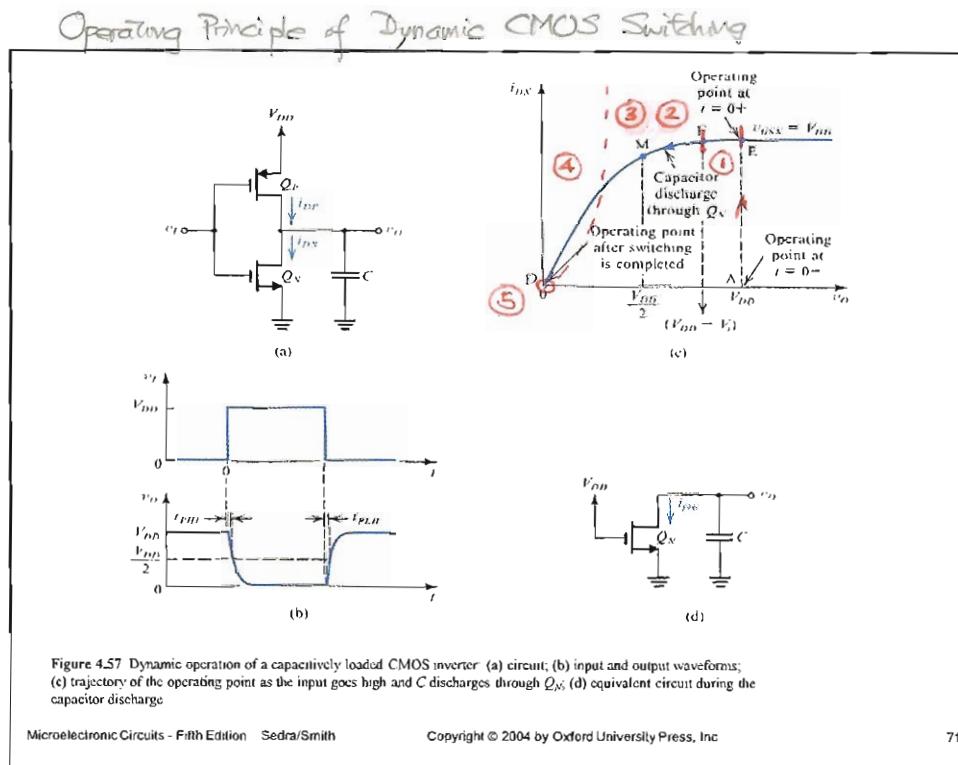
(b)

Figure 10.7 Equivalent circuits for determining the propagation delays (a) $t_{P_{HL}}$ and (b) $t_{P_{LH}}$ of the inverter

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8



Operation Regions

- ① pMOS Triode
nMOS Saturation
 - ② pMOS Triode
nMOS saturation
 - ③ pMOS Saturation
nMOS Saturation
 - ④ pMOS Saturation
nMOS Triode
 - ⑤ pMOS OFF
nMOS Triode
- Active (Current)
Pull Down (by nMOS)
- Passive (Resistive)
Pull Down (by nMOS)

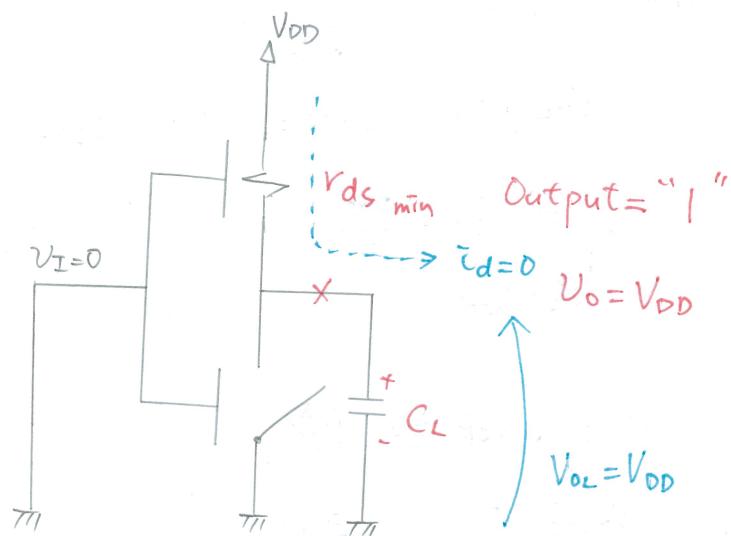
State ①

$$V_I < V_T$$

nMOS off

pMOS Triode

(stable)



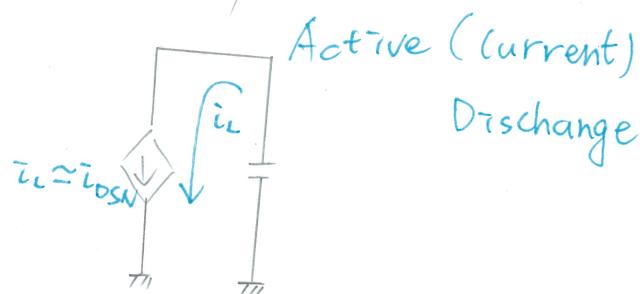
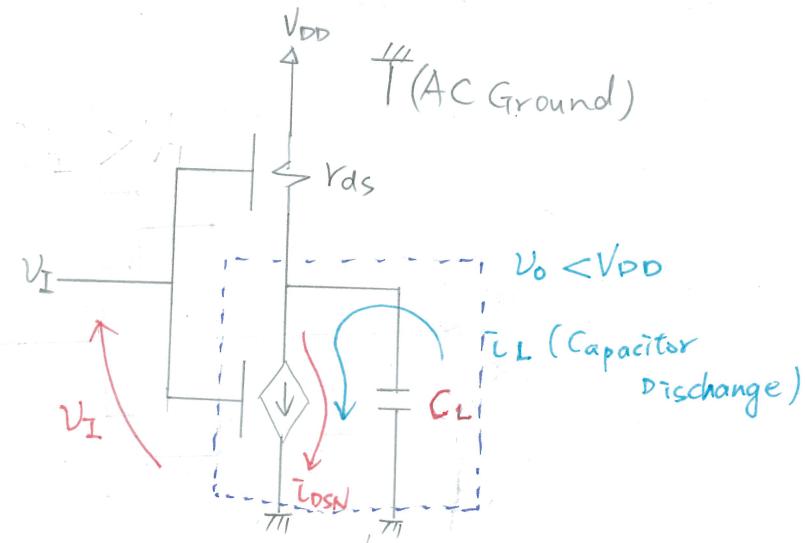
State ②

$$\frac{V_{DD}}{2} > V_I > V_T$$

nMOS Sat.

pMOS Triode

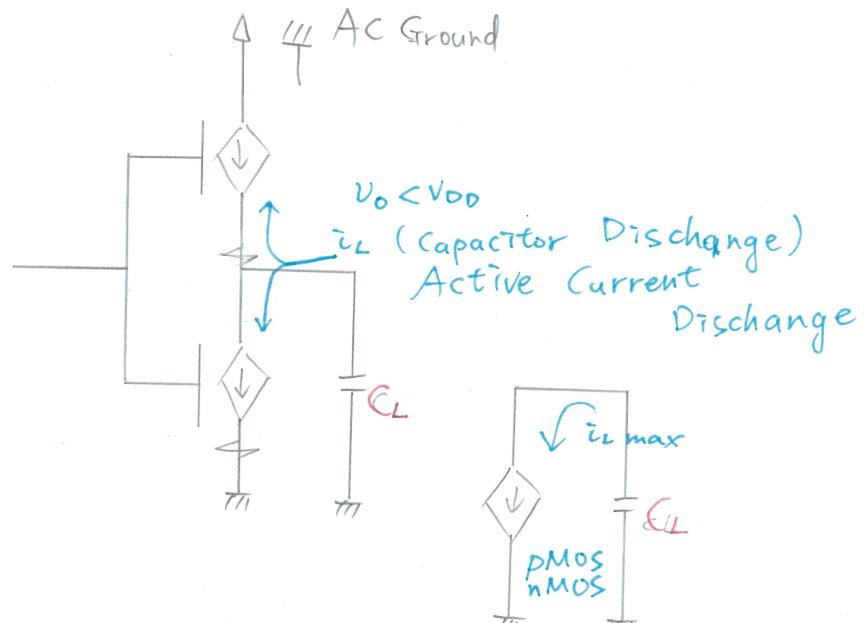
(Transition)



State ③

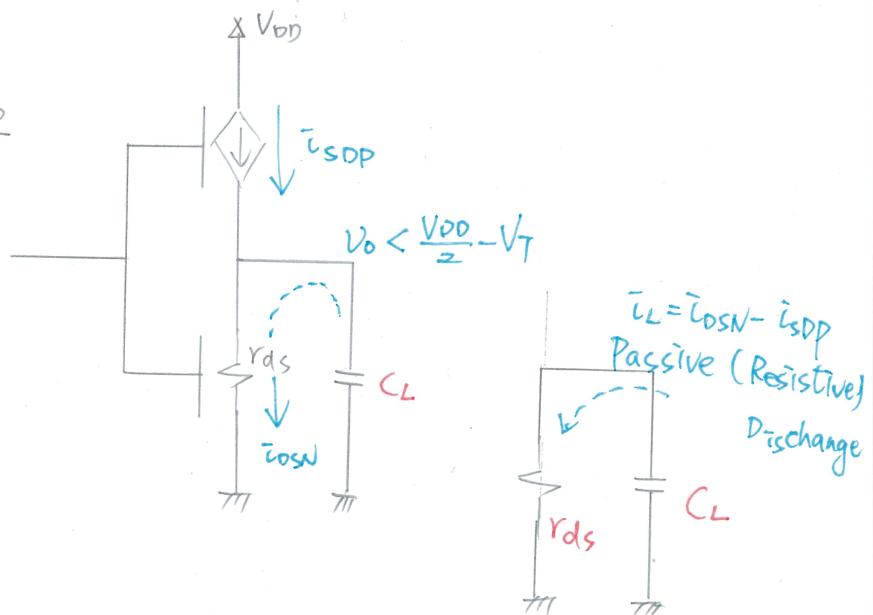
$$V_I \approx \frac{V_{DD}}{2}$$

n MOS Sat.
p MOS Sat



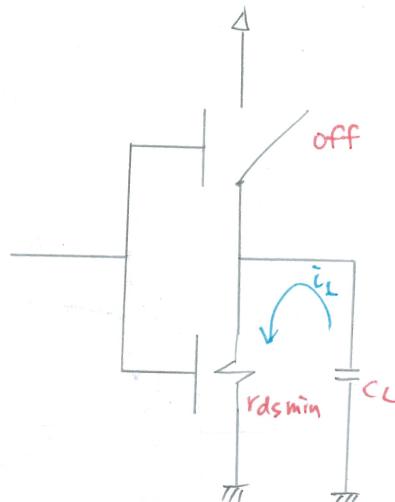
State ④

$$V_{DD} - V_T > V_I > \frac{V_{DD}}{2}$$



State 5

$$V_I > V_{DD} - V_T$$



$$V_o < \frac{V_{DD}}{2} - V_T$$

Passive
(Resistive)
Discharge

