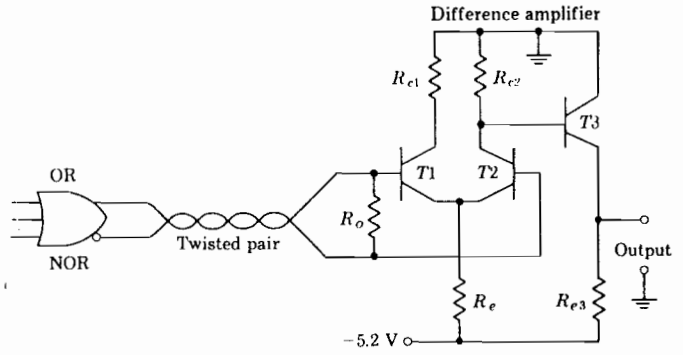

FIGURE 7.13-8
Twisted-pair transmission in ECL.

Whatever the change in voltage at one output, the change at the other output is equal and opposite. We take advantage of this feature as indicated in Fig. 7.13-8. The *difference* in output between OR and NOR output is transmitted over a twisted pair of wires to a *difference* amplifier. This difference voltage is nominally twice as large in amplitude as the signal available from the OR or the NOR output separately. The difference amplifier is normally made available by manufacturers for the present purpose and is generally referred to as a *receiver*. The twisting of the transmission wires keeps the wires together and also regularly reverses their relative positions. Hence, any signal path which might have induced in it a signal from one of the wires in the pair may well be expected to have an equal and opposite signal induced by the other wire. Hence, crosstalk from the twisted pair to other signal paths may be expected to be minimal. Similarly, crosstalk of other signals to the twisted pair will be introduced into the difference amplifier as a *common-mode* signal and hence will largely be restrained from appearing at the single-ended output. Of course, as appears, the twisted pair must be matched at its receiving end. A twisted pair may be used for transmission over many feet and may be used to distribute commonly used signals (such as clock waveforms) to many points. Generally, at each point when the signal is to be picked off the pair, a receiver will be required.

REFERENCE

1 Blood, W. R., Jr.: "MECL System Design Handbook," Motorola Semiconductor Products, Inc, Phoenix, Ariz., October 1971.

8

MOS GATES

MOS devices, as well as bipolar junction transistors (BJT), find application in logic gates. In this chapter we discuss the operation of PMOS (*p*-channel), NMOS (*n*-channel), and CMOS (complementary-symmetry) gates. CMOS is rapidly becoming the most favored because of its lower power dissipation, shorter propagation delay, and shorter rise and fall times.

8.1 ANALYTIC EQUATIONS FOR MOSFETS

Within a MOSFET, by definition, the charge carriers move away from the *source* and towards the *drain*. Therefore, in an *n*-channel device, where the carriers are negative, the conventional direction of current flow within the device is from drain to source. Thus the drain is positive with respect to the source, i.e., V_{DS} is positive as is also the current I_{DS}. Typical characteristics of *n*-channel MOSFETS are shown in Fig. 8.1-1. In Fig. 8.1-1*a* and *b* the MOSFET characteristics refer to an *enhancement* device. In such a device there is no channel between source and drain at $V_{GS} = 0$ V. No drain-to-source current I_{DS} flows until the gate-to-source voltage exceeds a threshold voltage V_T. This threshold

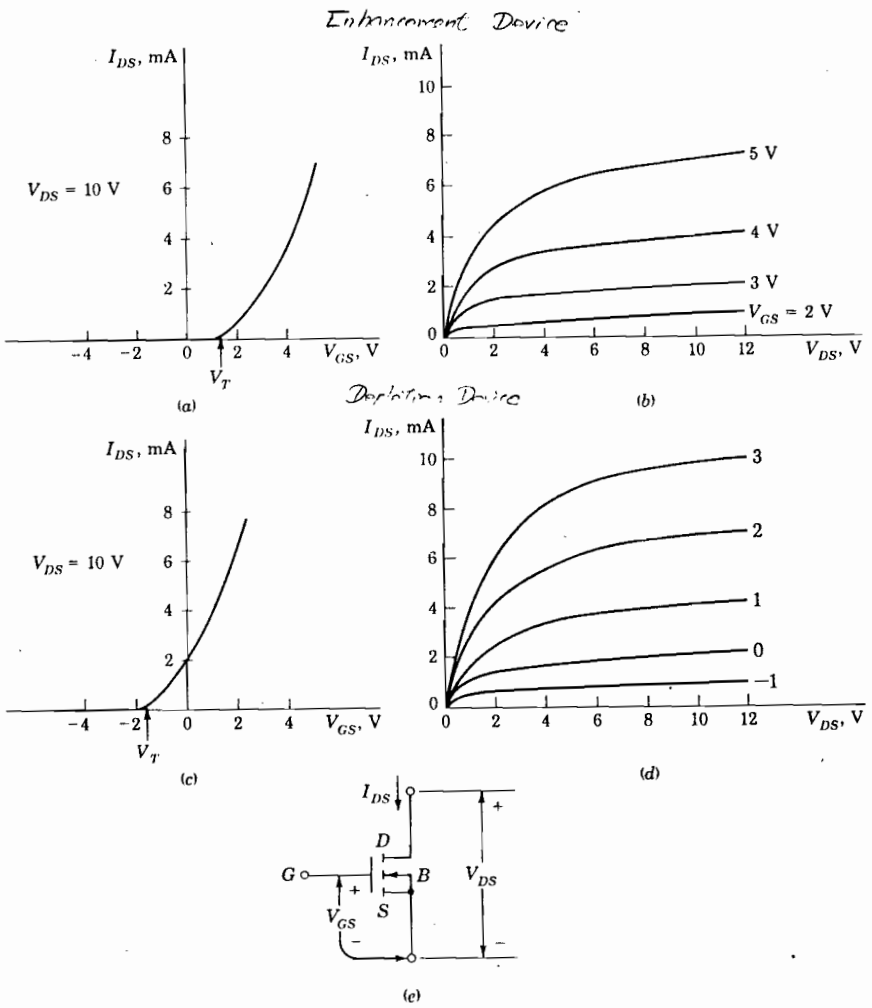

FIGURE 8.1-1
MOSFET characteristics. (*a* and *b*) Enhancement type. (*c* and *d*) Depletion type. (*e*) Defining voltages and currents. The device symbol represents an *n*-channel enhancement-type transistor.

voltage is of polarity which is the same as the polarity normally applied to the drain. Thus in an *n*-channel device, where V_{DS} is positive, so also is V_T, and a channel forms when $V_{GS} > V_T$.

In a *p*-channel device, where the carriers are positive, it is V_{SD} and I_{SD} (rather than V_{DS} and I_{DS}) which are positive. Furthermore, a channel forms to allow current I_{SD} to flow, when the source-to-gate voltage V_{SG} (rather than V_{GS}) exceeds a positive threshold voltage V_T, that is, when $V_{SG} > V_T$. We are using

the symbol V_T with two meanings. In an *n*-channel device V_T is defined as a particular value of V_{GS}, while in a *p*-channel device V_T represents a particular value of V_{SG}. Where any confusion may result we shall use instead the symbols $V_T(n)$ and $V_T(p)$. The symbolism we are employing avoids inconvenient negative signs and absolute-value signs.

In Fig. 8.1-1*c* and *d* typical characteristics are shown (again for an *n*-channel device) for a *depletion* transistor. Here a channel exists when $V_{GS} = 0$, and the threshold voltage V_T is negative. Strictly, such an *n*-channel transistor operates in the depletion mode when V_{GS} is negative and in the enhancement mode when V_{GS} is positive. It is customary nonetheless to refer to such a device simply as a depletion MOSFET. Both enhancement and depletion transistors are used in logic gates.

Either transistor type (enhancement or depletion) may operate in the non-saturation region (also referred to as the *triode* region in fond memory of the days of vacuum tubes) or in the saturation region. In the triode region there is a continuous channel between source and drain, and I_{DS} varies "lincarly" with V_{DS} for fixed V_{GS}. At the source, the channel depth is nominally proportional to the extent to which the gate-to-source voltage V_{GS} exceeds the threshold voltage V_T and is thus proportional to $V_{GS} - V_T$. For fixed V_{GS} the channel depth is fixed. At the drain, the channel depth is proportional to the extent to which the gate-to-drain voltage V_{GD} exceeds V_T. Hence at the drain the channel depth is proportional to $V_{GD} - V_T = V_{GS} - V_{DS} - V_T$. The channel is pinched off at the drain when $V_{GD} - V_T \leq 0$ or when

$$V_{DS} \geq V_{GS} - V_T \tag{8.1-1}$$

When $V_{DS} \geq V_{GS} - V_T$, the transistor is in *saturation*. That is, because of the channel pinch-off, the current I_{DS} remains nearly constant, increasing only very slightly with increasing V_{DS}.

Just as we found it convenient to have analytic expressions for bipolar transistors (Ebers-Moll equations), so too is it useful to have analytic expressions for the MOSFET. In the triode region it is found that for an *n*-channel device

$$I_{DS} = k[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \qquad 0 \leq V_{DS} \leq V_{GS} - V_T \tag{8.1-2}$$

In the saturation region

$$I_{DS} = k(V_{GS} - V_T)^2 \qquad 0 \leq V_{GS} - V_T \leq V_{DS} \tag{8.1-3}$$

The constant k is given by

$$k = \frac{\mu\varepsilon}{2t}\frac{W}{L} \tag{8.1-4}$$

where μ = mobility of carriers in channel (electrons in *n*-channel devices)
ε = dielectric constant of oxide insulating layer
t = thickness of oxide under gate
W = channel width
L = channel length

Typically, for n-channel devices $\mu\varepsilon/2t \approx 12\ \mu A/V^2$ and for p-channel devices is smaller by about a factor of 3. The width-to-length ratio W/L may range from 0.1 for a load transistor to as high as 20 or 40 for a driver device. (See Sec. 1.13)

In a p-channel transistor, operating in the triode region the equations for the device current are more conveniently written in the form

$$I_{SD} = k[2(V_{SG} - V_T)V_{SD} - V_{SD}^2] \qquad 0 \le V_{SD} \le V_{SG} - V_T \tag{8.1-5}$$

In the saturation region

$$I_{SD} = k(V_{SG} - V_T)^2 \qquad 0 \le V_{SG} - V_T \le V_{SD} \tag{8.1-6}$$

These equations, like Eqs. (8.1-2) and (8.1-3), are approximations and do not include all effects which have an influence on device current; however, they are entirely adequate for our purposes of exploring the operation of FET logic gates.

8.2 TEMPERATURE EFFECTS

Equations (8.1-2), (8.1-3), (8.1-5), and (8.1-6) for the current I_{DS} (and I_{SD}) are affected by the temperature because both V_T, the threshold voltage, and the parameter k are temperature-sensitive. The temperature dependence of V_T is given approximately by

$$\frac{dV_T}{dT} \approx -2.5\ \text{mV/°C} \tag{8.2-1}$$

The temperature sensitivity of k results almost entirely from the temperature sensitivity of μ [see Eq. (8.1-4)], the carrier mobility. The mobility decreases approximately inversely with the absolute temperature and hence so also does k. When there is a temperature increase, I_{DS} (or I_{SD}) increases because of the lowering of the magnitude of V_T and decreases because of the decreased carrier mobility. In a typical case we find that the effect of μ may be fivefold greater than the effect of V_T. The overall result is that generally the overall effect of a temperature increase is a decrease of current. In this respect the MOSFET differs from the bipolar transistor, where an increase in temperature increases the current both because the current gain h_{FE} increases and because the junction voltages decrease.

8.3 THE MOS INVERTER

As discussed in Chap. 1, the basic MOS switching-circuit configuration is an inverter which consists of a MOSFET switch driver driving a load which is itself a MOSFET device rather than a passive resistor. The driver is invariably an enhancement device since it is a great convenience that the driver be OFF when the gate voltage is at or near ground. When the driver is turned ON, it

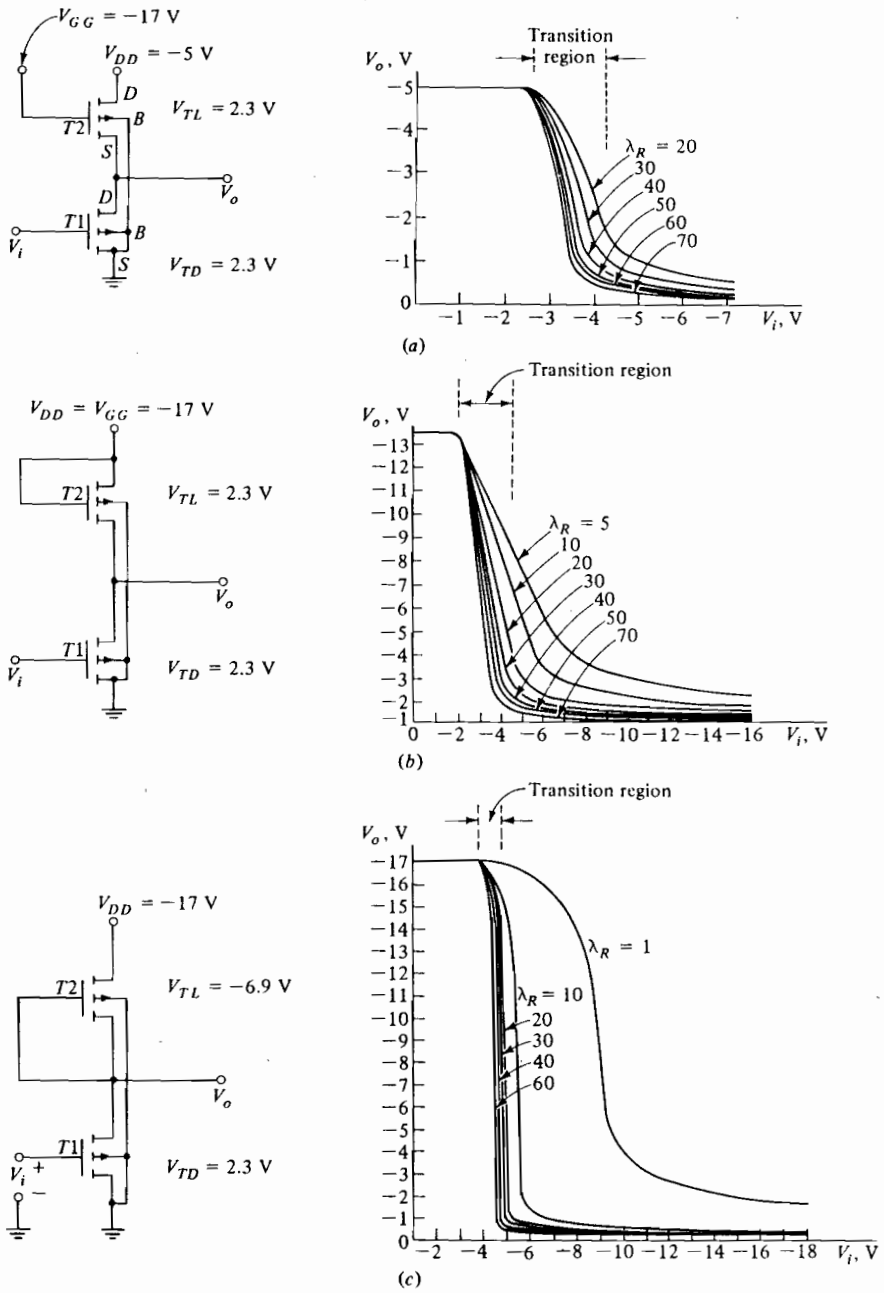

FIGURE 8.3-1
Input-output characteristics. (From "MOS/LSI Design and Applications," W. N. Carr, and J. P. Mize, McGraw-Hill, chap. 4, 1972).

invariably finds itself in the triode region. Such is the case since the gate voltage (furnished by another driving gate) will be at or near the supply voltage and the drain-to-source voltage will be at minimum magnitude. The load, on the other hand, may be an enhancement device or a depletion device and may operate in the triode or saturation region.

In Fig. 8.3-1 we display calculated input-output characteristics of PMOS inverters for three typical cases. In Fig. 8.3-1*a* both transistors are of the enhancement type, and both load and driver transistors have a threshold voltage $V_T = 2.3$ V. Since the transistors are *p*-channel devices, we apply the criterion given in Eq. (8.1-6) to determine whether we are in the triode or saturation region. Thus, to be in the triode region we require that $V_{SD} \leq V_{SG} - V_T$. This condition can be written as

$$V_{DG} \geq V_T \tag{8.3-1}$$

Since $V_{DG} = V_D - V_G = -5 - (-17) = 12$ V is greater than $V_T = 2.3$ V, the load transistor is biased to operate in the triode region. In Fig. 8.3-1*b* the driven transistor remains as in Fig. 8-3-1*a*, but in this case the load transistor operates in the *saturation* region (the proof of this statement is left to the problems). In Fig. 8.3-1*c* the load transistor is a depletion device with a negative threshold voltage $V_T = -6.9$ V. The biasing of the load places it in the triode region when $V_o \leq -10.1$ V and in saturation when $V_o > -10.1$ V.

As we have discussed in Sec. 1.14 (see Fig. 1.14-1), we should expect the form of the input-output characteristic to depend principally on the parameter λ_R, defined by

$$\lambda_R \equiv \frac{\lambda_D}{\lambda_L} \equiv \frac{(W/L)_D}{(W/L)_L} \tag{8.3-2}$$

where $(W/L)_D$ = width-to-length ratio of channel in driver transistor
$(W/L)_L$ = width-to-length ratio for load

We noted that as λ_R increases, the transition of the output between its high and low levels becomes sharper. These expectations are confirmed in Fig. 8.3-1. In the calculations leading to the plots in Fig. 8.3-1 the effect of substrate bias is taken into account. Note also that the inverter using a depletion-mode MOSFET load has the steepest transition region.

8.4 THE CMOS INVERTER

The CMOS inverter is shown in Fig. 8.4-1*a*. The drains of a *p*-channel and an *n*-channel transistor are joined, and a supply voltage V_{SS} is applied from source to source. The output is taken at the common drain. The input V_i swings nominally through the range of V_{SS}. In the CMOS inverter shown, since we have grounded the source of the *n*-channel device, V_{SS} must be a positive voltage and V_i swings between ground and V_{SS}.

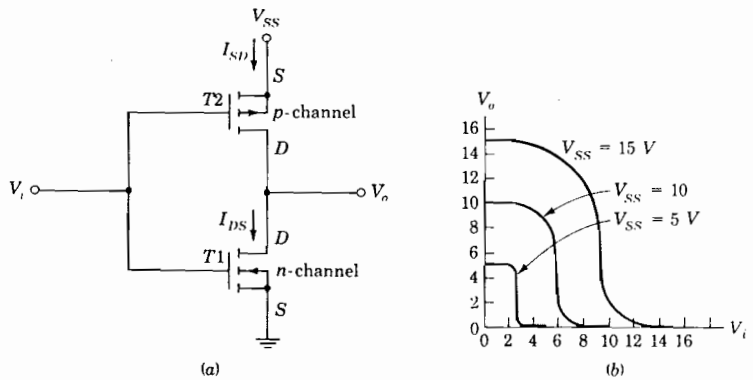

FIGURE 8.4-1
(*a*) A CMOS inverter and (*b*) its transfer characteristic.

Because of the complete symmetry of the circuit it seems intuitively clear that we shall want the two transistors to be reasonably alike. Therefore customarily it is arranged that the parameter k in Eqs. (8.1-2), (8.1-3), (8.1-5), and (8.1-6) are the same for the two transistors. The mobility of carriers in the *p*-channel device is smaller than the mobility in the *n*-channel device by a factor of 2 or 3. Hence to make the k's equal, the ratio W/L for the *p*-channel must be correspondingly larger by a factor of 2 or 3 than W/L for the *n*-channel device [see Eq. (8.1-4)]. However, even with such an adjustment of the W/L ratio the CMOS inverter is not necessarily entirely symmetrical since the threshold voltages of the *p*-channel and *n*-channel devices generally turn out to be somewhat different.

Usually CMOS gates are designed to operate with supply voltages in the range 5 to 15 V. Typical transfer characteristics are shown in Fig. 8.4-1*b*. For the device to which Fig. 8.4-1*b* applies, the magnitude of the threshold voltage is about 2 V for each of the transistors. Observe the abruptness of the transition and that the total swing in voltage is equal to V_{SS}. In the MOS inverters such a situation prevails only when we arrange that the *ratio* λ_R of the λ's be very large. In the present CMOS case, however, this situation prevails rather independently of the value of λ_R. Hence the CMOS inverter is often referred to as a *ratioless* inverter.

8.5 CALCULATION OF CMOS-INVERTER TRANSFER CHARACTERISTIC

It is instructive to use the device current equations to calculate the transfer characteristic of a CMOS inverter in a typical case. Referring to Fig. 8.4-1, we have that for $V_i \leq V_T(n)$, $T1$ is OFF, $T2$ is ON, and $V_o = V_{SS}$. Similarly for

$V_i \geq V_{SS} - V_T(p)$, $T2$ is OFF, $T1$ is ON, and $V_o = 0$ V. Further, $T1$ is saturated when $V_{DS1} \geq V_{GS1} - V_T$, i.e.,

$$V_T(n) \leq V_i \leq V_o + V_T(n) \tag{8.5-1}$$

while $T2$ is saturated when $V_{SD2} \geq V_{SG2} - V_T$, i.e.,

$$V_o - V_T(p) \leq V_i \leq V_{SS} - V_T(p) \tag{8.5-2}$$

Thus, if, say, $V_T(n) = V_T(p) = 2$ V and $V_{SS} = 10$ V, we would have $T1$ saturated when $2 \leq V_i \leq V_o + 2$ and $T2$ saturated when $V_o - 2 \leq V_i \leq 8$. Or, to put the matter otherwise, $T1$ would be saturated when

$$V_o \geq V_i - 2 \tag{8.5-3}$$

and $T2$ would be saturated when

$$V_o \leq V_i + 2 \tag{8.5-4}$$

The currents I_{SD} and I_{DS} indicated in Fig. 8.4-1*a* are always equal. Accordingly, when $T1$ is in saturation and $T2$ is not, we have, using Eqs. (8.1-3) and (8.1-5),

$$k_n[V_i - V_T(n)]^2 = k_p\{2[V_{SS} - V_i - V_T(p)](V_{SS} - V_o) - (V_{SS} - V_o)^2\} \tag{8.5-5}$$

Here we have taken account of the fact that for the p-channel transistor $V_{SG} = V_{SS} - V_i$ and $V_{SD} = V_{SS} - V_o$. Similarly we find that when $T2$ is in saturation and $T1$ is not, we have

$$k_p[V_{SS} - V_i - V_T(p)]^2 = k_n\{2[V_i - V_T(n)]V_o - V_o^2\} \tag{8.5-6}$$

Finally, when both transistors are in saturation, we find that

$$k_n[V_i - V_T(n)]^2 = k_p[V_{SS} - V_i - V_T(p)]^2 \tag{8.5-7}$$

Using Eqs. (8.5-5) to (8.5-7), we have plotted in Fig. 8.5-1 the input-output characteristic of a CMOS inverter for $V_T(n) = V_T(p) = 2$ V, $V_{SS} = 10$ V, and $k_p/k_n = 1$. Above the line $V_o = V_i - 2$ [Eq. (8.5-3)] $T1$ is in saturation. Below the line $V_o = V_i + 2$ [Eq. (8.5-4)] $T2$ is in saturation. In the region between the two lines both transistors are in saturation.

Note that the simultaneous saturation of both transistors defines a unique voltage V_i(sat), calculated from Eq. (8.5-7) to be

$$V_i(\text{sat}) = \frac{\sqrt{k_p/k_n}[V_{SS} - V_T(p)] + V_T(n)}{1 + \sqrt{k_p/k_n}} \tag{8.5-8}$$

In Fig. 8.5-1 with $k_p/k_n = 1$, $V_T(p) = V_T(n)$, V_i(sat) = 5 V. This voltage, at which there occurs an abrupt transition in output voltage is midway between 0 and V_{SS} because we have selected $k_p = k_n$. If k_p were not equal to k_n, then even if $V_T(n)$ were equal to $V_T(p)$, complete symmetry would not prevail. In any event we find from Eqs. (8.5-1) and (8.5-2) that the magnitude of the abrupt transition is given by

$$\Delta V_o = V_T(n) + V_T(p) \tag{8.5-9}$$

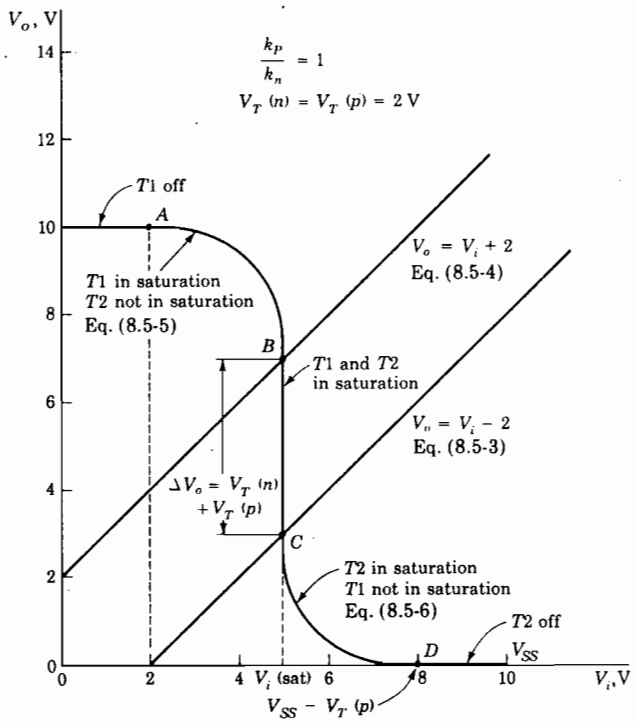

FIGURE 8.5-1
Transfer function of a CMOS inverter, $k_p/k_n = 1$.

The infinite slope displayed in Fig. 8.5-1 results from our assumption that in the saturation region the device current is absolutely independent of drain-to-source voltage, i.e., that the device is a constant current source. Such, of course, is not precisely so, and hence the transition from B to C in a physical situation would be sharp but not absolutely abrupt.

8.6 MOS GATES

Assuming that positive logic is intended, the NMOS circuit of Fig. 8.6-1 is a two-input NAND gate. The supply voltages V_{DD} and V_{GG} and the threshold voltage V_T are all positive. Logic **0** is represented by a voltage less than the threshold voltage and logic **1** by a voltage above the threshold voltage. The truth table given in Fig. 8.6-1 is readily verified. When either V_1 or V_2 or both are below threshold, only TL conducts. In this case V_o is $V_{GG} - V_T$ or V_{DD}, whichever is lower. When both V_1 and V_2 are above threshold, both $T1$ and $T2$ conduct.