MOSbius-Style Class D Amplifier

XDAC

Xavier, Devlin, Angel, Christopher

General Specifications

As a lab device, we'd like students to be able to power a pair of headphones from the output of our chip. By listening to their amplifier configuration, students can tie their mathematical understanding of frequency response to what they hear.

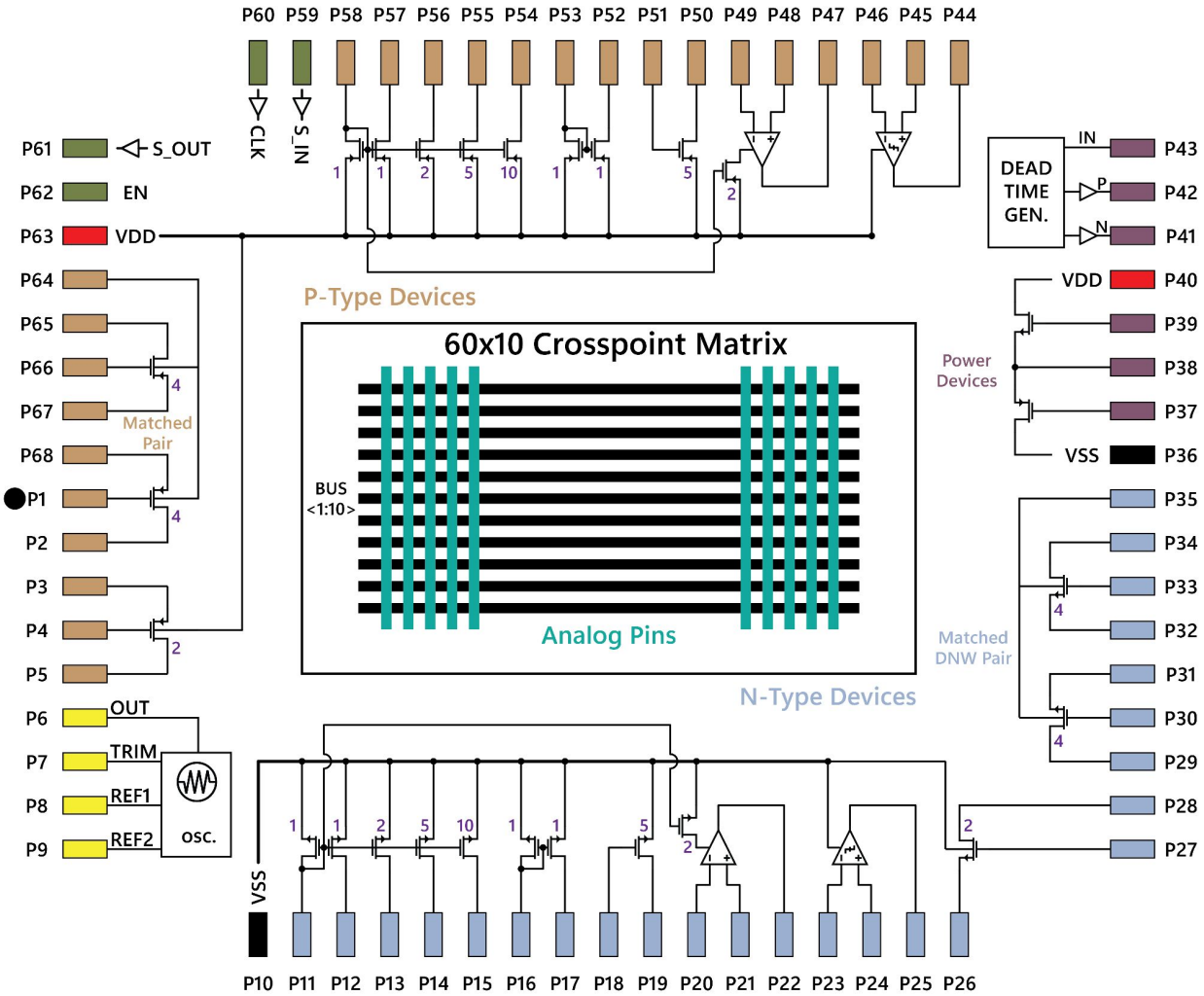
	Target	Motivation
Output Power	100mW	Typical max power for headphone jack. Real loads should take far less, around 40mW.
Sine-Wave Peak Differential Output Swing	Min. 1.4Vpp	Calculated from sound-pressure level of +110dB into typical 32-Ohm headphone load. Value should be easy to hit in Class-D operation.
VDD	3.3V	Standard LV Voltage transistor in gf180mcuD
Sawtooth Frequency	Programmable to max 200kHz	Manipulating the modulation frequency should be an interesting exercise.

General Specifications

Other modes of operation (e.g. Class AB) should be possible with our chip, as should a front-end audio amplifier for a basic microphone.

Equivalent P and N-type devices should be made available so that different configurations can be tested. For example, N vs. P input diff pair for an OTA.

Following the original MOSBIUS project, we decided to target the same PLCC68 packaging.


P60 P59 P58 P57 P56 P55 P54 P53 P52 P51 P50 P49 P48 P47 P46 P45 P44
CLK
S_IN
P61 S_OUT
P62 EN
P63 VDD
P64
P65
P66
P67
P68
P1
P2
P3
P4
P5
P6 OUT
P7 TRIM
P8 REF1
P9 REF2
OSC.
P-Type Devices
60x10 Crosspoint Matrix
BUS <1:10>
Analog Pins
N-Type Devices
Matched Pair
DEAD TIME GEN.
IN
P
N
P43
P42
P41
VDD P40
P39
P38
P37
VSS P36
Power Devices
P35
P34
P33
P32
P31
P30
P29
P28
P27
Matched DNW Pair
VSS
P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 P20 P21 P22 P23 P24 P25 P26

Open Points of Discussion

Should voltage references for relaxation oscillator be made available to general switch matrix? Oscillator performance may be degraded by crosstalk in the matrix.

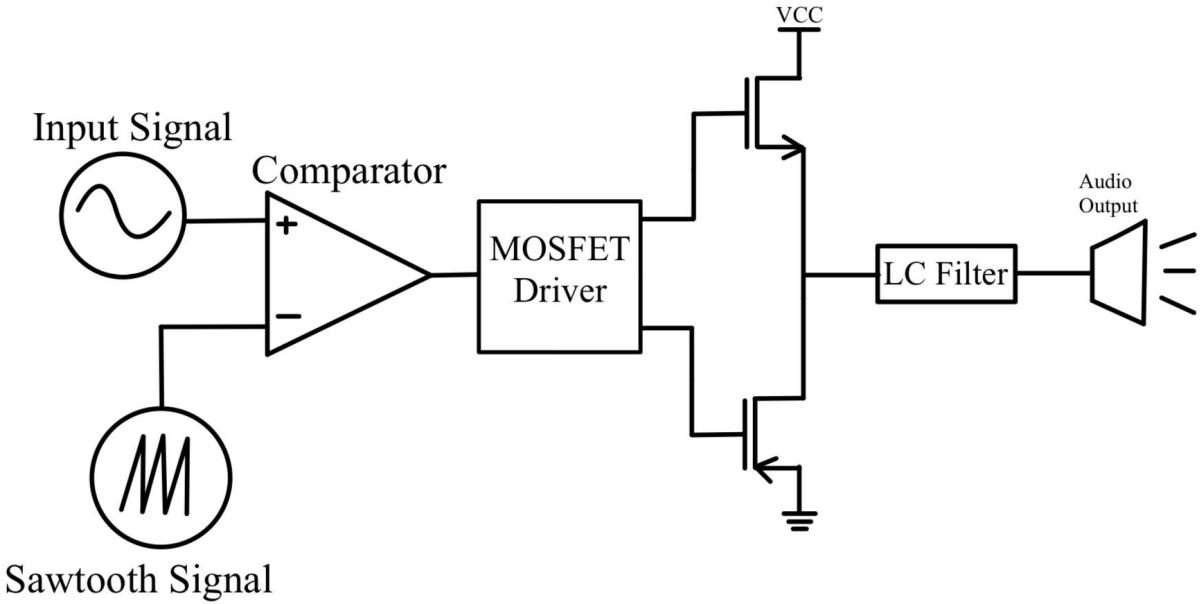
Included S_OUT (Serial Out) intended to cascade multiple MOSbius-style chips over one command interface.

Note we have one DNW NMOS pair, which appears to be available in the d-variant of gf180mcu we are using.

Whether we should support internal connections between the power pads (2X VDD, VSS, respectively).

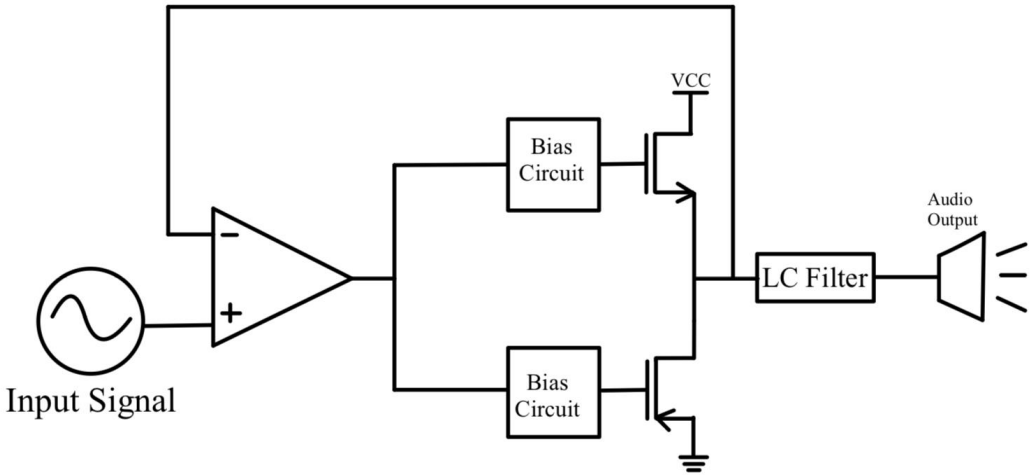
Proposed Application Circuits (1)

Class D: Amplifier



Proposed Application Circuits (2)

Class AB: Operation



More General Applications

Many of the original MOSbius labs on the website are still possible with our proposed chip:

- Current mirrors
- Differential pair AC and DC characterizations
- 5T-OTA

Additionally, the included N and P comparators could be used by users to create their own triangle-wave oscillators, learn about hysteresis, etc.

Members + Work Allocation

Output Stage + Gate Driver, Comparator, Deadtime Circuit

Christopher Amankwaa

Oscillator, OTAs, Current Sources, Current Mirrors

Xavier Lee

Crosspoint Matrix, Shift Register Interface

Angel Romero + Devlin Glover

Project Schedule

Week	Christopher	Xavier (Presenter)	Devlin	Angel
29 (7/12 - 18)	Basic FET constraints: gm/id Comparator	Device Params Current Mirrors Current Ref.	Look into analog switch design, start designing digital blocks (NAND, NOT, work up to DFF)	Look into K-layout in python, also start designing digital blocks
30 (7/19 - 25)	Designs: Output driver + Deadtime	Design: OTA, Triangle Oscillator	Research matrix design & begin designing analog switch network	Research digital elements for matrix (non-overlapping clock elements, etc) & begin serial register design
31 **(7/26 - 8/1)** **Schem. Review**	Collaboration + Cross-Check Finish block sims	Collaboration + Cross-Check Finish block sims	Continue analog switch network design	Continue Serial register design
32 **(8/2 - 8/9)** **Block Sim Review**	Tie up loose ends Begin top-level integration simulations	Coordinate w/ digital Begin top-level integration simulations	Finish overall matrix design and begin integration	Integration of overall digital design
33 **(8/10 - 8/17)** **Go / NoGo**	Finish integration simulations + presentation of work	Finish integration simulations + prepare presentation of work	Finish integration of matrix design	Finish integration of matrix design

	Week	Christopher	Xavier	Devlin	Angel
	34: (8/18-8/25)	NMOS, PMOS, Gate Driver layout	Layout current mirrors, reference	Digital element layout	Automate switch matrix layout
Xavier Starts Grad School	35: (8/26-9/2)	Comparator, Deadtime, Layout	OTA, Oscillator Layout	Complete ^	Complete ^
	36: (9/3-9/10) Block Layout Review	Top-Level Integration	Top-Level Integration	Top-Level Integration	Top-Level Integration
	37: (9/17-9/24) Top Layout Review	Top-Level Integration	Top-Level Integration	Top-Level Integration	Top-Level Integration
Devlin Starts Grad School	38: (9/25-10/2)	Top-Level Integration	Top-Level Integration	Top-Level Integration	Top-Level Integration
	39: (10/3-10/10) Final Review	Top-Level Integration	Top-Level Integration	Top-Level Integration	Top-Level Integration