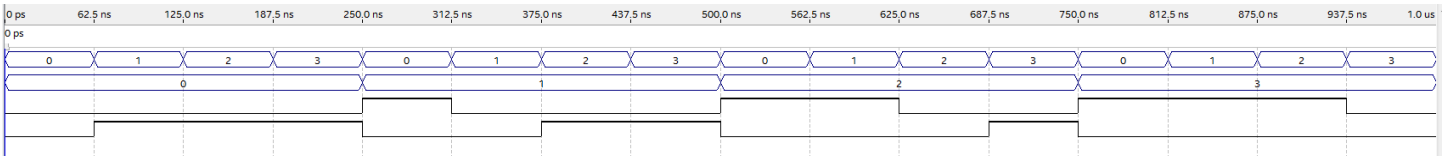
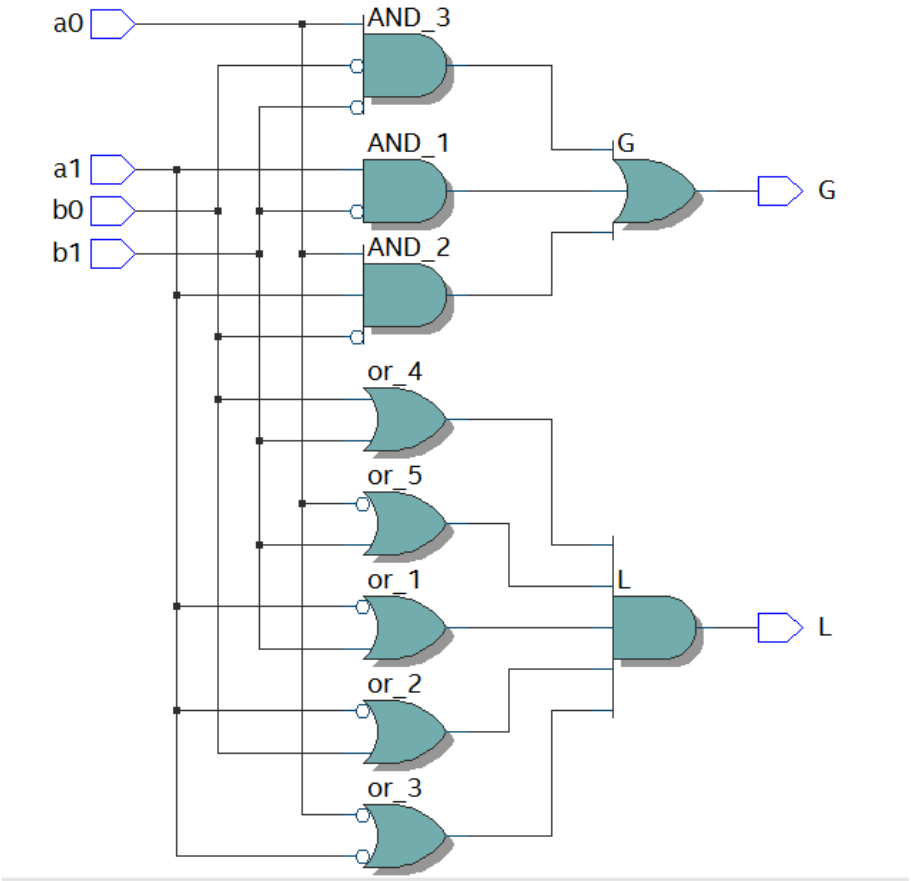
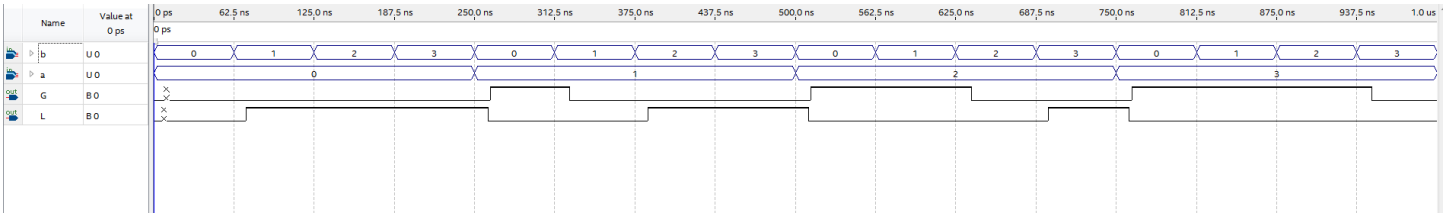
```vhdl
library ieee;                  --library clause
use ieee.std_logic_1164.all;  --use clause

entity compare_2bit is --start entity declaration statement

--start of port clause
   port(signal a1: in std_logic;    --signal_name : signal_mode data_type
        signal a0: in std_logic;    --signal_name : signal_mode data_type
        signal b1: in std_logic;    --signal_name : signal_mode data_type
        signal b0: in std_logic;    --signal_name : signal_mode data_type

        signal L: out std_logic;
        signal G: out std_logic
       );                          --end of port clause

end entity compare_2bit; --end entity declaration statement

architecture dataflow of compare_2bit is --start of architecture declaration statement
                                         --describes what the entity does
                                         --declaration potion of the architecture

-------------------------------------------------------------------------------------------------------

signal sig_a0 : std_logic;          --declare internal signal sig_a0
                                    --represents input of a0


signal not_sig_a0 : std_logic;         --declare internal signal not_sig_a0
                                       --represents output(s) of any NOT gate


signal sig_a1 : std_logic;             --declare internal signal sig_a1
                                       --represents input of a1


signal not_sig_a1 : std_logic;         --declare internal signal not_sig_a1
                                       --represents output(s) of any NOT gate


signal sig_b0 : std_logic;             --declare internal signal sig_b0
                                       --represents input of b0


signal not_sig_b0 : std_logic;         --declare internal signal not_sig_b0
                                       --represents output(s) of any NOT gate


signal sig_b1 : std_logic;             --declare internal signal sig_b1
                                       --represents input of b1

signal not_sig_b1 : std_logic;         --declare internal signal not_sig_b1
                                       --represents output(s) of any NOT gate
```

```vhdl
-------------------------------------------------------------------------------------------
--declare internal signal AND_1-3
--represents output(s) of any AND gates for SOP

signal AND_1    : std_logic;
signal AND_2    : std_logic;
signal AND_3    : std_logic;

-------------------------------------------------------------------------------------------
--declare internal signal or_1-5
--represents output(s) of any OR gates for POS

signal or_1     : std_logic;
signal or_2     : std_logic;
signal or_3     : std_logic;
signal or_4     : std_logic;
signal or_5     : std_logic;
-------------------------------------------------------------------------------------------

begin    --implementation potion of the architecture

      --Signal Initialization/assignment
      sig_a0 <=  a0;
      sig_b0 <=  b0;
      not_sig_a0 <= not a0;
      not_sig_b0 <= not b0;

      sig_a1 <=  a1;
      sig_b1 <=  b1;
      not_sig_a1 <= not a1;
      not_sig_b1 <= not b1;
-------------------------------------------------------------------------------------------

      --To model the 2-level logic networks corresponding to the SOP of G
      AND_1 <= sig_a1 AND not_sig_b1;
      AND_2 <= not_sig_b0 AND sig_a1 AND sig_a0;
      AND_3 <= not_sig_b0 AND sig_a0 AND not_sig_b1;

      G <= AND_1 OR AND_2 OR AND_3;
-------------------------------------------------------------------------------------------

      --to model the 2-level logic networks corresponding to the POS of L
      or_1 <= sig_b1 OR not_sig_a1;
      or_2 <= not_sig_a1 OR sig_b0;
      or_3 <= not_sig_a1 OR not_sig_a0;
      or_4 <= sig_b1 OR sig_b0;
      or_5 <= not_sig_a0 OR sig_b1;

      L    <= or_1 AND or_2 AND or_3 AND or_4 AND or_5;


   end architecture dataflow;
```






```
        ************************************************************************
        Running Quartus Prime Analysis & Synthesis
        Command: quartus_map --read_settings_files=on --write_settings_files=off lab1 -c compare_2bit
 18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
 20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
 12021 Found 2 design units, including 1 entities, in source file compare_2bit.vhd
 12127 Elaborating entity "compare_2bit" for the top level hierarchy
286030 Timing-Driven Synthesis is running
 16010 Generating hard_block partition "hard_block:auto_generated_inst"
 21057 Implemented 8 device resources after synthesis - the final resource count might be different
        Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
        ************************************************************************
        Running Quartus Prime Fitter
        Command: quartus_fit --read_settings_files=off --write_settings_files=off lab1 -c compare_2bit
        qfit2_default_script.tcl version: #1
        Project  = lab1
        Revision = compare_2bit
 18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
 20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
119006 Selected device EP4CE115F29C7 for design "compare_2bit"
 21077 Low junction temperature is 0 degrees C
 21077 High junction temperature is 85 degrees C
171003 Fitter is performing an Auto Fit compilation, which may decrease Fitter effort to reduce compilation time
176444 Device migration not selected. If you intend to use device migration later, you may need to change the pin assignments as they may be incompatible with other devices
169124 Fitter converted 5 user pins into dedicated programming pins
 15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details
332012 Synopsys Design Constraints File file not found: 'compare_2bit.sdc'. A Synopsys Design Constraints File is required by the TimeQuest Timing Analyzer to get proper timing constraints. Without it, the Compiler will not pr
332144 No user constrained base clocks found in the design
332096 The command derive_clocks did not find any clocks to derive.  No clocks were created or changed.
332068 No clocks defined in design.
332143 No user constrained clock uncertainty found in the design. Calling "derive_clock_uncertainty"
```


Name
Value at
0 ps
0 ps
62,5 ns
125,0 ns
187,5 ns
250,0 ns
312,5 ns
375,0 ns
437,5 ns
500,0 ns
562,5 ns
625,0 ns
687,5 ns
750,0 ns
812,5 ns
875,0 ns
937,5 ns
1,0 us
b
U 0
a
U 0
G
B 0
L
B 0