XAVIER ROUTH

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EDUCATION

University Of Illinois, Urbana-Champaign   **Urbana-Champaign, IL**
Computer Engineering, B.S. Candidate, 3.87 GPA (Dean's List 3/4 Semesters)   *Expected **December 2024***
James Scholar Honors Program, HKN ECE Honors Society

Relevant Courses: Data Structures, Analog Signal Processing, Algorithms and Models of Computation, Digital Systems Laboratory (FPGAs), Applied Parallel Programming (CUDA)
Current: Compiler Construction, Computer Systems Engineering, Cryptography, Programming Languages

PROFESSIONAL EXPERIENCE

UIUC LLVM Group, under **Professor Vikram Adve**, Undergraduate Researcher   **Champaign, IL**
HPVM Project   *May 2023 - Present*
- Ported several hyperdimensional computing (HDC) GPU and FPGA applications to a custom language, Hetero-C++, to be used as benchmarks for the HPVM project.
- Wrote a C++ library to support HDC operations for CPU targets within the HPVM framework.
- Helped develop LLVM passes to lower HDC intrinsics to LLVM IR, including custom memory management and tiling.

SCaN - NASA Glenn Research Center, Engineering Intern   **Cleveland, OH**
Ground Station Control Software   *June - Aug. 2022*
- Developed software to monitor and control operation of the S-Band Ground Station.
- Interfaced with various hardware devices via serial commands, SCPI, and functions defined in DLLs.
- Two separate GUIs developed using Python and PyQt5. Monitored signal power levels and weather conditions.
- Set up TCP Socket connection to communicate remotely across computers hosting different sensors.

ACADEMIC AND PERSONAL PROJECTS

C to LC-3 Compiler
- Wrote a non optimizing C compiler that targets LC-3 Assembly. First implemented in C, then rewritten in Rust.
- Includes custom memory management to avoid usage of dynamic memory.
- Integrated compiler with Compiler Explorer to allow better understanding of LC-3 calling conventions and the implementation of C concepts in LC-3.
- Supported by course staff and actively used by students taking ECE 220.

NES Hardware Emulator
- Designed a semi-cycle accurate NES emulator which runs on a DE10-Lite FPGA board using SystemVerilog.
- Used Intel's Platform Designer to configure a basic NIOS II based SoC design to handle USB input via SPI and program the NES design with game roms.
- Design was centered around a 6502 CPU core that interacted with system components via a memory mapped bus.
- Required re-designing various asynchronous components of the original system to work on an FPGA.
- Able to play Donkey Kong, Super Mario Bros, and more.

FPGA SLC-3 Processor
- Implemented a simplified version of the LC-3 architecture onto an FPGA using SystemVerilog and ModelSim.
- Allows for input from on-board switches and buttons at program runtime via memory-mapped IO.

CUDA Convolutional Neural Network
- Implemented the forward propagation stage of the LeNet-5 CNN architecture using CUDA and Nsight Compute.
- Used various techniques including tiling, kernel fusion, and streaming to optimize memory bandwidth.
- Placed in the top 15 of final competition submissions, out of around 200 students.

TECHNICAL SKILLS

Programming Languages:
Python, PyQt5, NumPy, x86 Assembly, C, C++, CUDA, SystemVerilog, LLVM, Rust, OCaml

Workflow:
Git, Quartus Prime, ModelSim, WSL 2, Docker, CMake, Make, Bash, Linux,

INTERESTS

FPGAs, Computer Architecture, Game Engines, Embedded Systems, Hardware Acceleration, Compilers, Logic synthesis, Data-Oriented Design

INVOLVEMENT / LEADERSHIP

ACM SIGARCH and SIGPLAN
HKN Review Sessions and Community Outreach