XAVIER ROUTH

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EDUCATION

University Of Illinois Urbana-Champaign, **Urbana-Champaign, IL**
Computer Engineering, B.S. Candidate, 3.88 GPA (Deans List 2/3 Semesters) *Expected **December 2024***
James Scholar (Honors Program), HKN ECE Honors Society

Relevant Courses: Computer Systems & Programming, Data Structures, Analog Signal Processing, Linear Algebra, Differential Equations, Algorithms and Models of Computation, Digital Systems Laboratory, Applied Parallel Programming, Discrete Structures

PROFESSIONAL EXPERIENCE

SCaN - NASA Glenn Research Center, Engineering Intern **Cleveland, OH**
Ground Station Control Software *June-Aug. 2022*

- Developed software to monitor and control operation of the S-Band Ground Station.
- Interfaced with various hardware devices via serial commands, SCPI, and functions defined in DLLs.
- Two separate GUIs developed using Python and PyQt5. Monitored signal power levels and weather conditions.
- Set up TCP Socket connection to communicate remotely across computers hosting different sensors.

ACADEMIC AND PERSONAL PROJECTS

FPGA NES Hardware Emulator
Designed a semi-cycle accurate NES emulator on a DE10-Lite FPGA board. Used Intel's Platform Designer to configure a basic NIOS II based SoC design to handle USB input via SPI and program the NES with game roms. Design was based on the original NES, centered around a 6502 CPU core that interacted with various system components via a memory mapped bus. Required re-designing various asynchronous components of the original system to work on an FPGA. Implemented using SystemVerilog and Quartus Prime for the final project of Digital Systems Laboratory.

FPGA SLC-3 Processor
Implemented a simplified version of the LC-3 architecture onto an FPGA using SystemVerilog. Fully programmable 16-bit processor with 14 different instructions. Simulated using ModelSim. Follows the traditional von Neumann design of a processor. Allows for input from on-board switches and buttons at program runtime via memory-mapped IO.

CUDA Convolutional Neural Network
Implemented the forward propagation stage of the LeNet-5 CNN architecture using CUDA. Used parallel programming techniques such as tiling to optimize memory bandwidth. Was able to achieve a 10000x speedup over a non-parallel implementation. Profiled using NVIDIA Nsight Compute.

Generalized Minimax Search Algorithm
Implemented Minimax / Negamax search with Alpha-Beta pruning, Iterative Deepening, and Transposition Table memoization optimizations. Applied search to various custom implementations of 2-player games including Tic Tac Toe, Dots and Boxes, and Connect Four. Programmed in C++.

Data Structures Academic Projects
Multiple MPs throughout the Fall 22 Semester. Maze generated using disjoint sets, solved using a BFS traversal. Class scheduler algorithm using greedy implementation of graph coloring. Photo mosaic generator using K-dimensional trees and nearest neighbor search. Final project consisting of a graph based chess engine evaluation function.

LLVM LC-3 Backend
Currently working on implementing an LLVM backend for the LC-3 instruction set architecture. Will eventually be integrated with Compiler Explorer to allow better understanding of the compilation process among students learning LC-3.

TECHNICAL SKILLS

Programming Languages:
Python, PyQt5, NumPy, LC-3 Assembly, C, C++, CUDA, SystemVerilog, LLVM

Workflow:
VSCode, Git, Quartus Prime, ModelSim, Excel, Word, WSL 2, Docker, CMake, Make,

INTERESTS

Machine Learning, FPGAs, Computer Architecture, Game Engine Design, Embedded Programming, Parallel Programming, Compiler Design, Logic Synthesis

INVOLVEMENT / LEADERSHIP

ACM SIGARCH and SIGPLAN
HKN Review Sessions / Community Outreach