



Learn Git and GitHub without any code!


Using the Hello World guide, you'll start a branch, write comments, and open a pull request.

Read the guide

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 **Code**

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xbarto0c 3.cv ...

now  History

..



Komparator

3 days ago



images

3 minutes ago



mux_2bit_4to1

3 minutes ago



project_1

3 minutes ago



readme.md

now

readme.md



1.Connection of 16 LEDs and switches to the Nexys A7 board:

Pin name:	Pin name on the board :
LED0	H17
LED1	K15
LED2	J13
LED3	N14
LED4	R18
LED5	V17
LED6	U17
LED7	U16
LED8	V16
LED9	T15
LED10	U14
LED11	T16
LED12	V15
LED13	V14
LED14	V12
LED15	V11
SW0	J15
SW1	L16
SW2	M13
SW3	R15
SW4	R17
SW5	T18
SW6	U18
SW7	R13
SW8	T8

Pin name:	Pin name on the board :
SW9	U8
SW10	R16
SW11	T13
SW12	H6
SW13	U12
SW14	U11
SW15	V10

2.Two-bit wide 4-to-1 multiplexer

Multiplexer architecture code:

```
architecture Behavioral of mux_2bit_4to1 is
begin

    f_o  <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;
end architecture Behavioral;
```

Multiplexer stimulus process code:

```
p_stimulus : process
begin
    -- Report a note at the beginning of stimulus process
    report "Stimulus process started" severity note;

    -- First test values
    s_a <= "00"; s_b <= "01"; s_c <= "11"; s_d <= "10";
    s_sel <= "00"; wait for 100 ns;

    s_a <= "00"; s_b <= "01"; s_c <= "11"; s_d <= "10";
    s_sel <= "10"; wait for 100 ns;
```

```

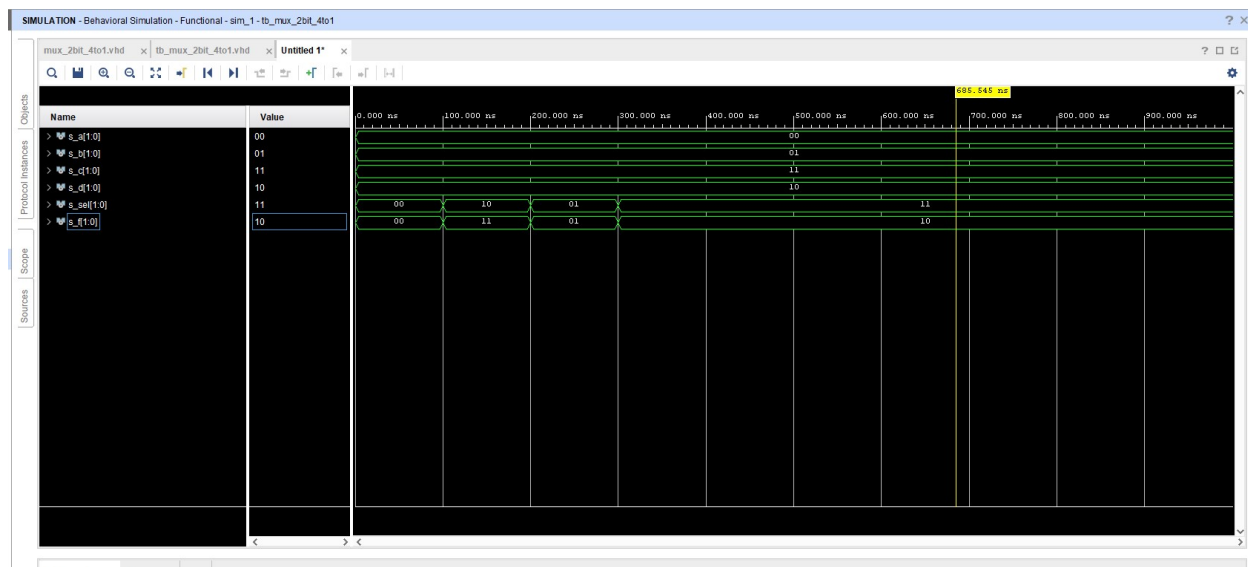
s_a <= "00"; s_b <= "01"; s_c <= "11"; s_d <= "10";
s_sel <= "01"; wait for 100 ns;

s_a <= "00"; s_b <= "01"; s_c <= "11"; s_d <= "10";
s_sel <= "11"; wait for 100 ns;

report "Stimulus process finished" severity note;
wait;
end process p_stimulus;

```

Multiplexer simulation screenshot:

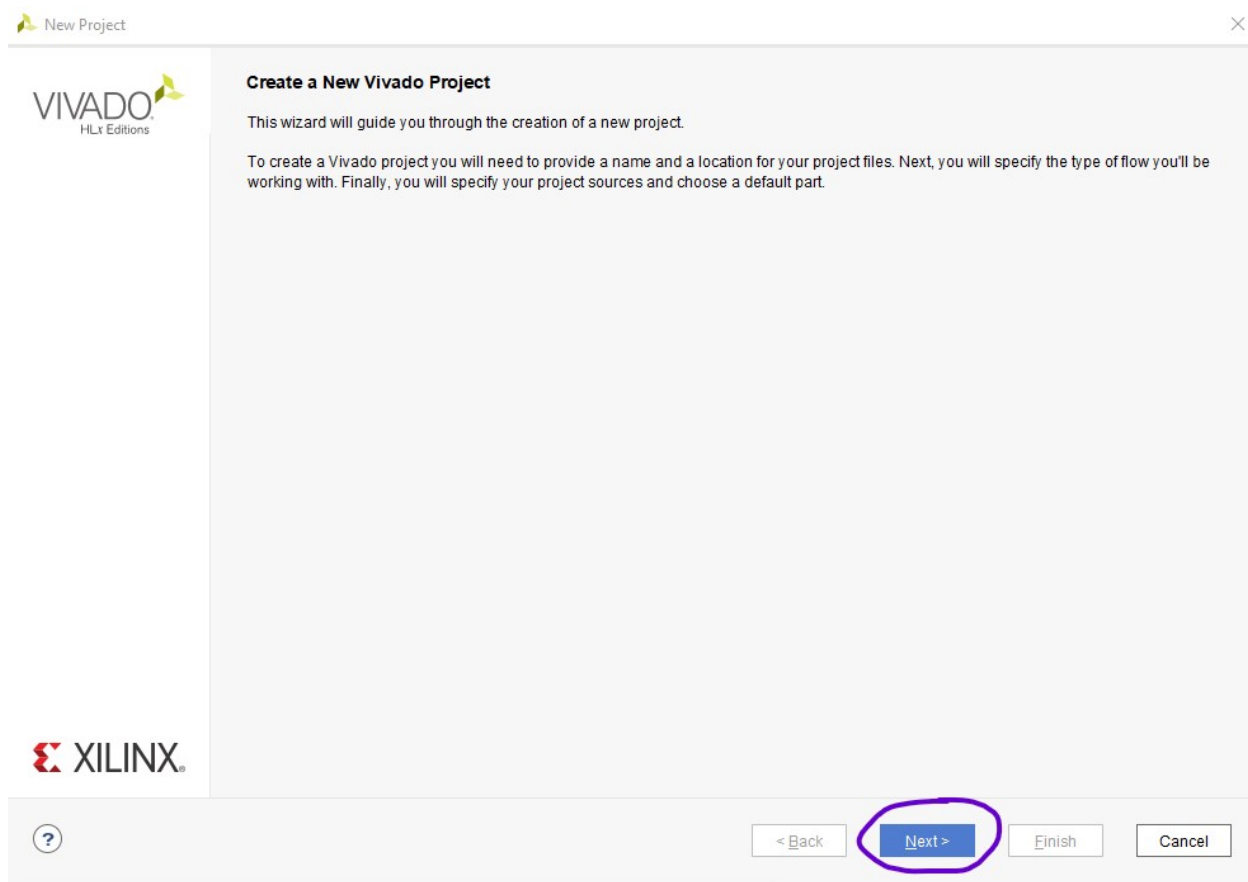


3. Vivado basics tutorial:

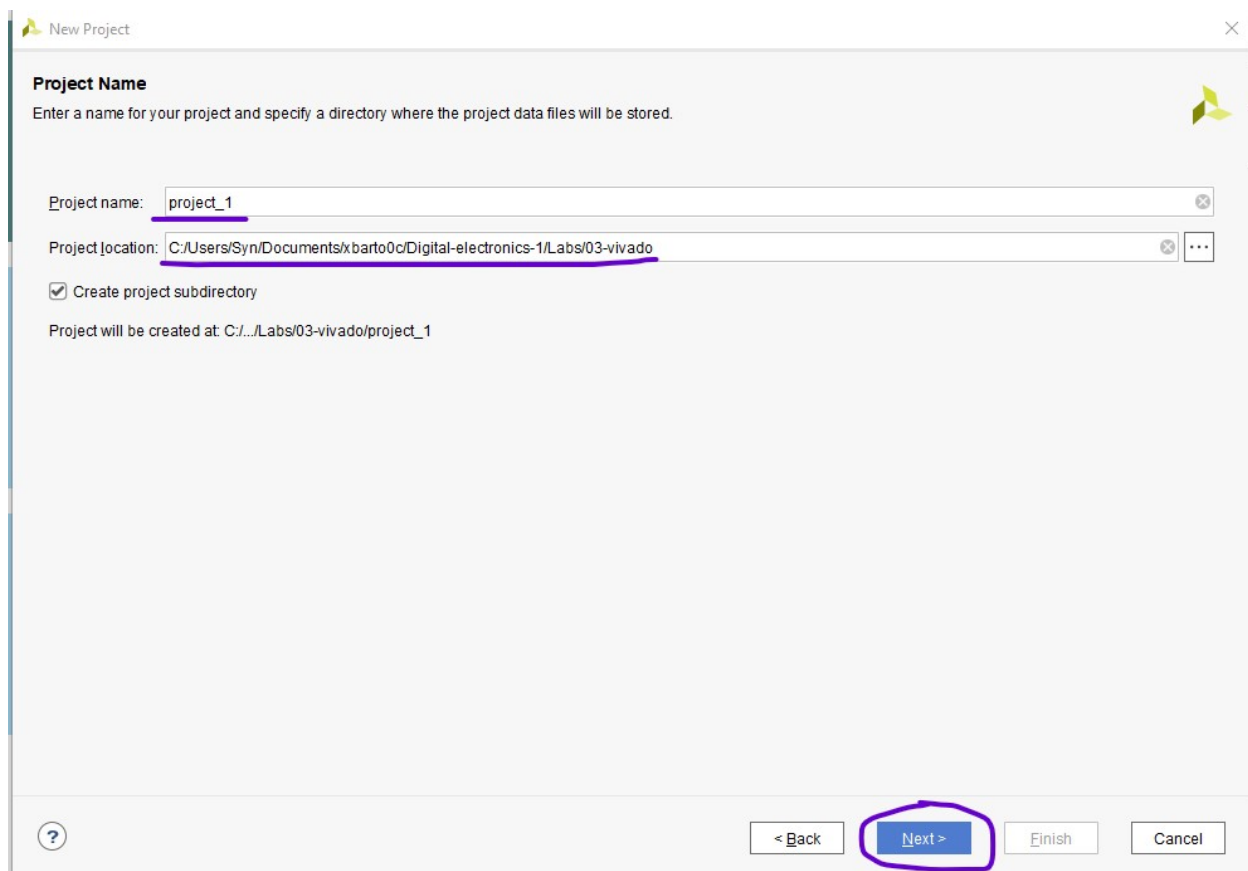
Creating project:



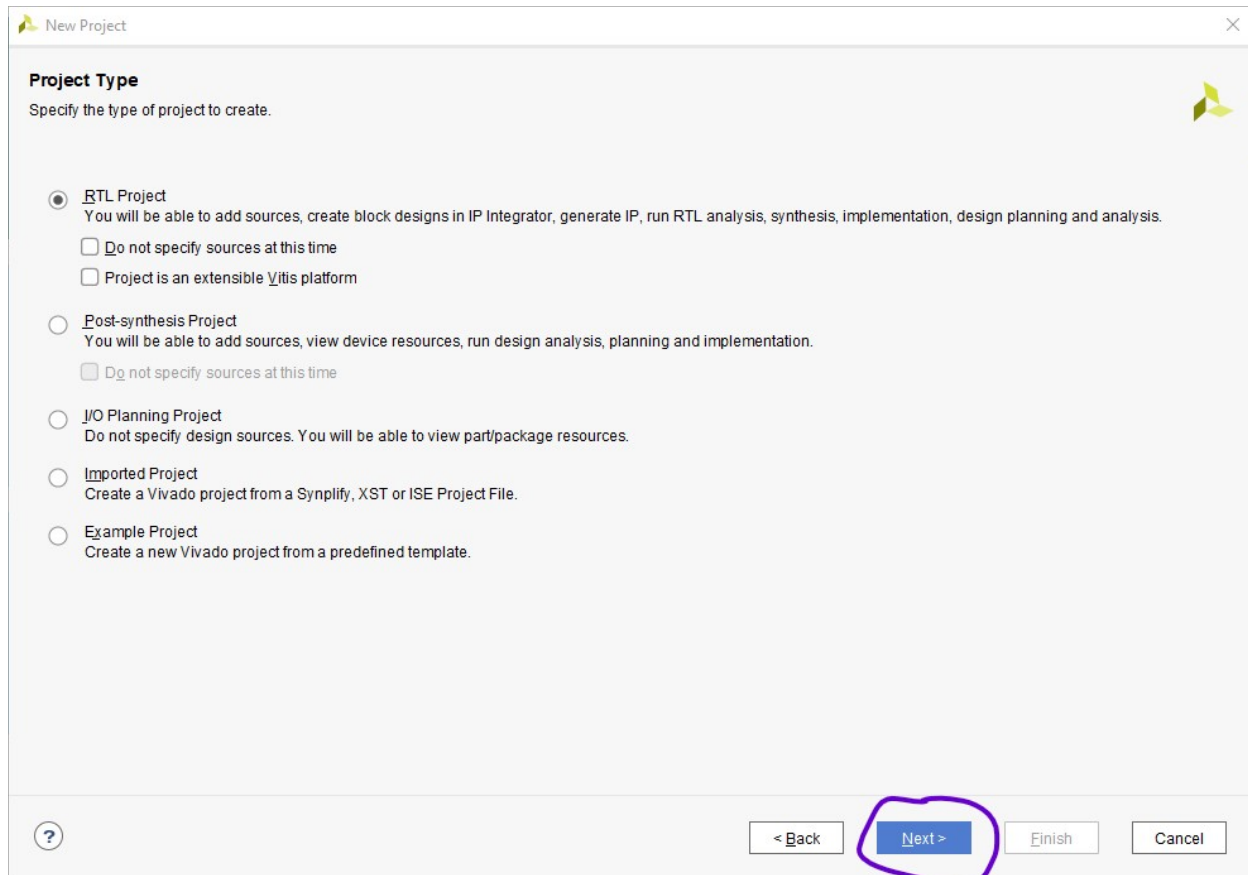
Create project:



Create project:



Create project:



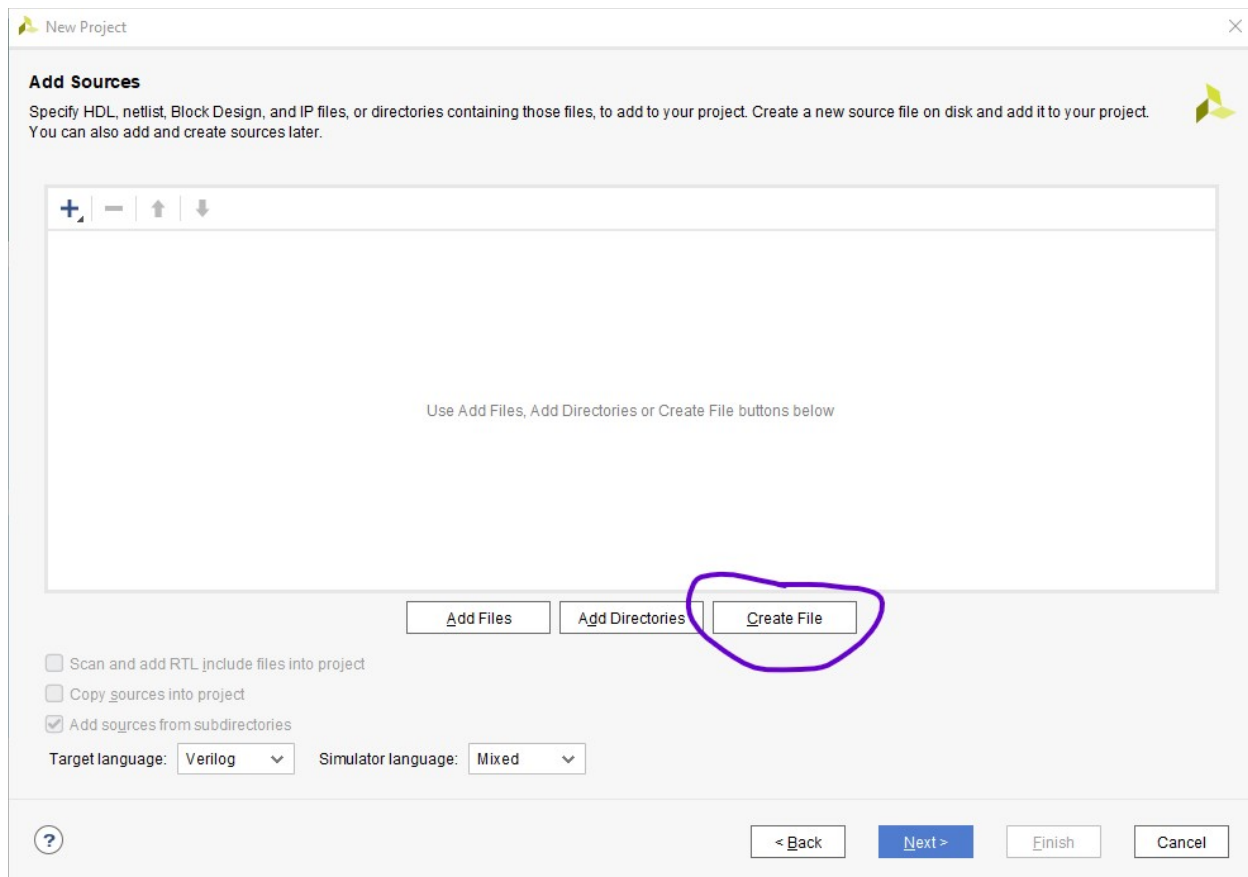
New Project

Project Type
Specify the type of project to create.

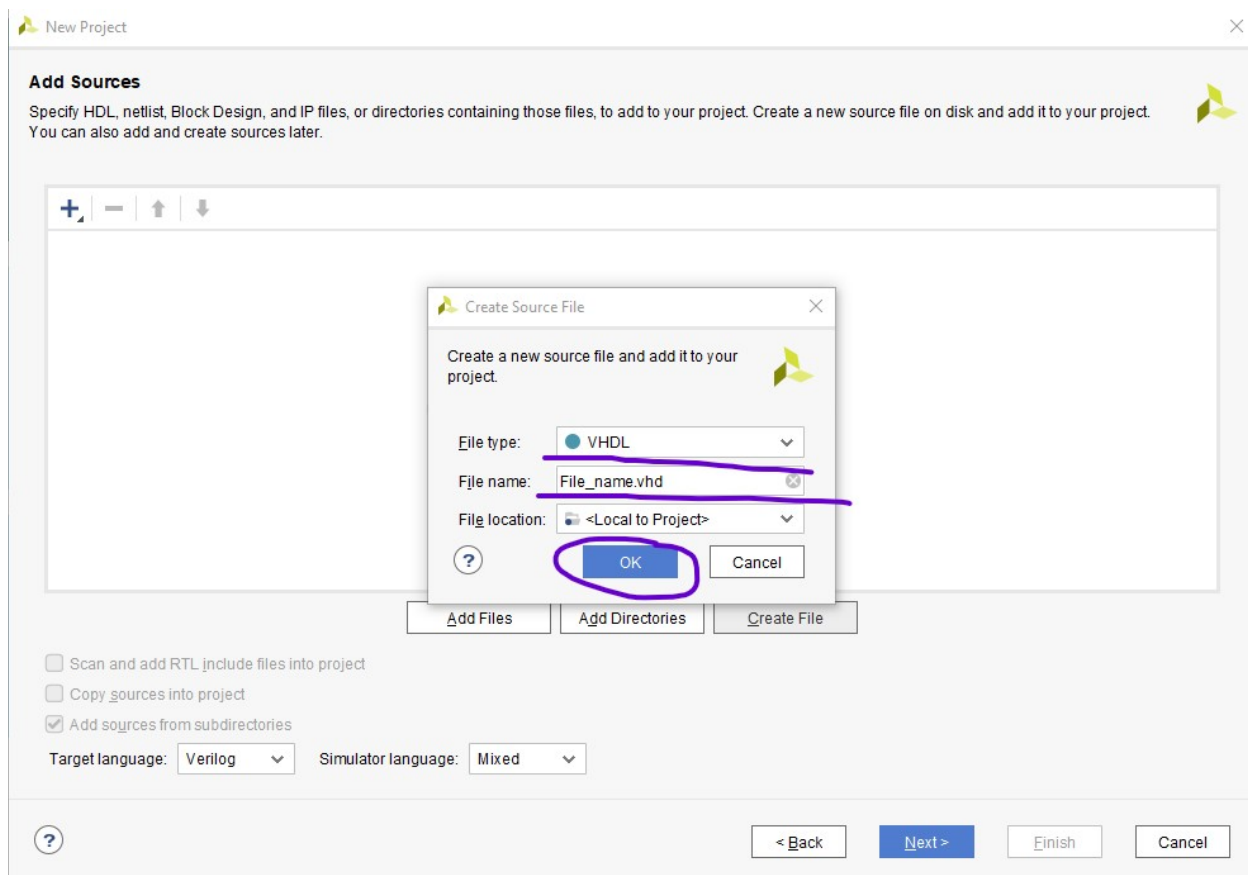
- ☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 - ☐ Do not specify sources at this time
 - ☐ Project is an extensible Vitis platform
- ☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
 - ☐ Do not specify sources at this time
- ☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- ☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- ☐ **Example Project**
Create a new Vivado project from a predefined template.

? < Back **Next >** Finish Cancel


Create project:



Create project:








Create project:

 New Project ×

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

	Index	Name	Library	HDL Source For	Location
	1	File_name.vhd	xil_defaultlib	Synthesis & Simulation	<Local to Project>

Add FilesAdd DirectoriesCreate File

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

Target language: Verilog Simulator language: Mixed

?

< BackNext >FinishCancel

Create project:

New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

☐ Copy constraints files into project

Create project:

New Project

Default Part

Choose a default Xilinx part or board for your project.


Category:
 Package:
 Temperature:

Family:
 Speed:
 Static power:

Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceiv
xc7k70tffbg676-2L	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg676-1	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg484-3	484	285	41000	82000	135	0	240	4	0
xc7k70tffbg484-2	484	285	41000	82000	135	0	240	4	0
xc7k70tffbg484-2L	484	285	41000	82000	135	0	240	4	0
xc7k70tffbg484-1	484	285	41000	82000	135	0	240	4	0
xc7k70tffbg676-3	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg676-2	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg676-2L	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg676-1	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg484-2L	484	285	41000	82000	135	0	240	4	0

Create project:

 New Project ✕

Default Part
Choose a default Xilinx part or board for your project.

Parts | **Boards**

[Reset All Filters](#)

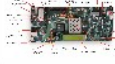

Vendor: All

Name: All


Board Rev: Latest

Install/Update Boards

Search:

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs
Nexys A7-50T		digilentinc.com	1.0	xc7a50tcs324-1L	324	D.0	210
Nexys4		digilentinc.com	1.1	xc7a100tcs324-1	324	B.1	210
Artix-7 AC701 Evaluation Platform Add Companion Card Connections		xilinx.com	1.4	xc7a200tfg676-2	676	1.1	400
Spartan-7 SP701 Evaluation Platform		xilinx.com	1.0	xc7s100fpga676-2	676	1.0	400

<>



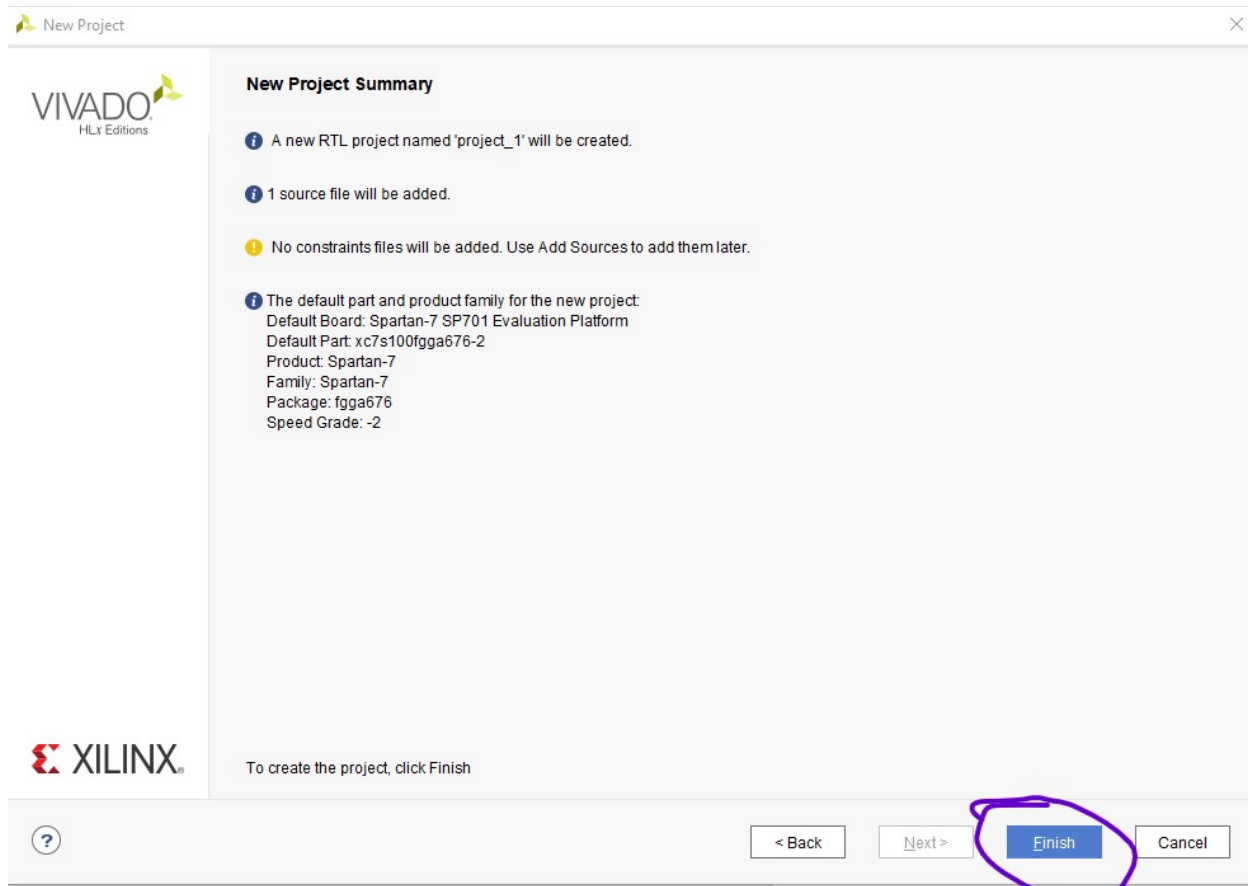
< Back

Next >

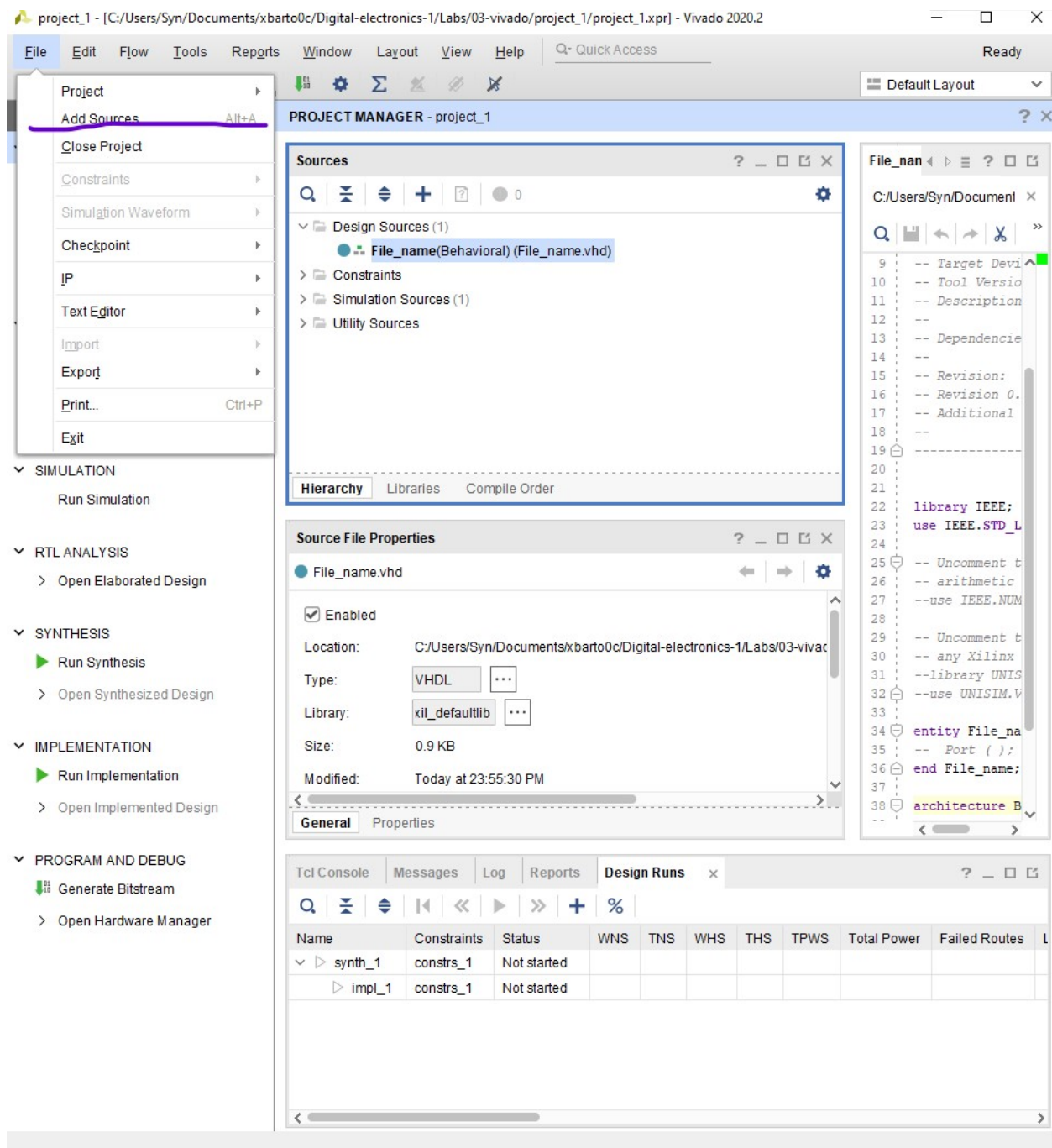
Finish

Cancel

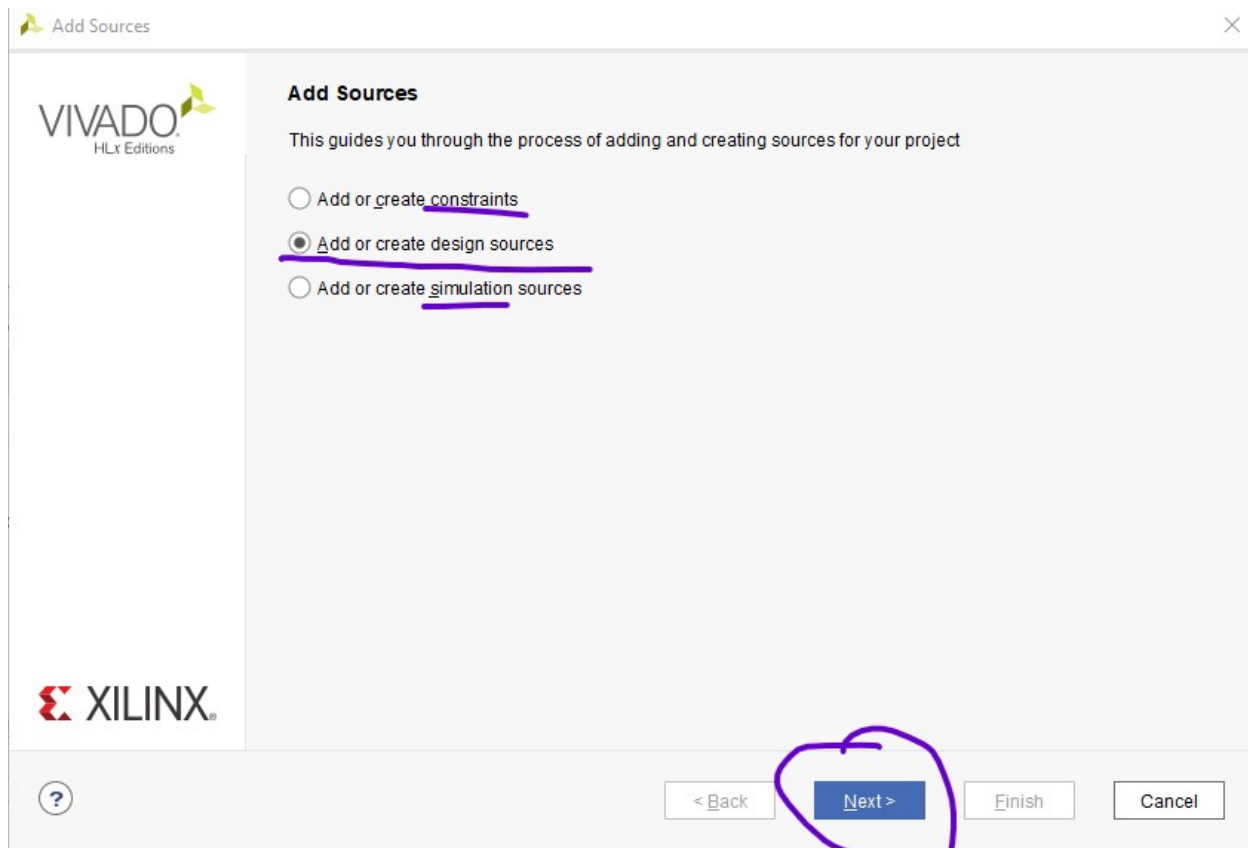
Create project:



Adding source file, testbench file or XDC file:



Adding source file, testbench file or XDC file:



Running simulation:

