Verification Plan

Team 5 Asynchronous FIFO

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ECE 593
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1 Table of Contents

2 Introduction

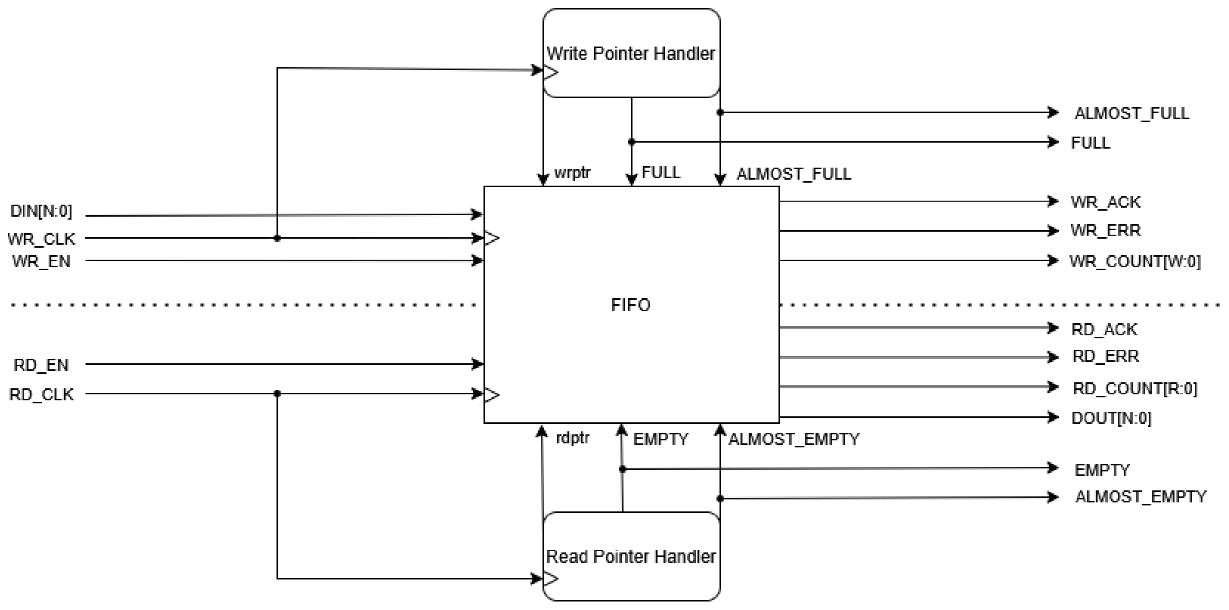
2.1 Team 5 Github Repository Link

https://github.com/xbicai/ECE593_Project

2.2 Objective of the verification plan

The Purpose of this document is to provide members of the project a guideline for how the asynchronous FIFO should function. By having a plan to follow, each member will be able to put in work that will help reach the end goal.

2.3 Top Level block diagram



2.4 Specifications for the design

Data can be safely passed from one asynchronous clock domain to another using FIFO. When two clock domains are asynchronous to one another, an asynchronous FIFO design occurs when data values are written from one clock domain to a FIFO buffer and read from the same FIFO buffer from another clock domain.

The next word to be written is always shown by the write pointer. The write pointer increases and the empty flag is cleared as soon as the first piece of data is written to the FIFO. The current FIFO word to be read is always shown by the read pointer. When the read and write pointers are equal, the FIFO is empty.

FIFO Depth Calculation:
Double the frequency of write and half of the read
120 MHz is the sender clock frequency.
Three idle cycles separate two consecutive writes, and the receiver clock frequency is 50 MHz.
There are two idle cycles in between two consecutive reads.
Given that the sender clock frequency is less than the receiver clock frequency, write burst = 1024.

Three clock cycles separate two consecutive writes, indicating that after writing one piece of data, the write module waits three clock cycles before starting the next write. This means that one piece of data is written every four clock cycles.
Writing one data item takes 4 * (1/120MHz) = 33.33 ns.
It took 34,129.92 = 34,129 ns to write the data in the burst.
One data item's reading time is equal to 3 * (1/50MHz) = 60 ns.
Thus, the read module will read one data item from the burst every 60 ns.
In 34,129 ns, the number of data pieces that can be read is 34,129/60 = 568.81 = 568 items. 1024 – 568 = 456 is the remaining number of bytes that must be kept in the FIFO.

3 Verification Requirements

3.1 Verification Levels

3.1.1 Hierarchy Level

This project will be verified at the **block level** since we want to verify the entire asynchronous FIFO module. Such parts include data correctness, proper clock timing, and flag handling (empty/full).

3.1.2 Controllability and Observability

Controllability will be good because the asynchronous FIFO's inputs will be directly controlled by the testbench. Observability will be good too, because the flags such as empty/full can be monitored directly by the testbench or QuestaSim.

3.1.3 List of Interfaces and Specification

4 UVM Verification

4.1 UVM Architecture

This project will follow the traditional UVM testbench architecture and component hierarchy. The testbench top will include the UVM test class, the virtual interface, and the DUT. The UVM test class will include the environment, the sequence items, and the test sequence classes. The environment class is where the coverage, scoreboard, and agent classes are instantiated, with the agent consisting of the sequencer, driver, and monitor. The sequencer will connect to the static sequences and send that information dynamically to the driver. The driver will interact with the virtual interface to provide the input stimulus to the DUT. The monitor will observe the virtual interface for any input stimulus from the driver and output response from the DUT and send that information to the scoreboard. The scoreboard is where that data is compiled and measured for correctness.

4.2 Verification Levels

4.2.1 Hierarchy Level

This project will be verified at the **block level** since we want to verify the entire asynchronous FIFO module. Such parts include data correctness, proper clock timing, and flag handling (empty/full).

4.2.2 Controllability and Observability

The sequence classes will allow us to make a variety of random and directed test stimulus that will be sent to the DUT via the other UVM components allowing us a good lever of controllability of the DUT. The scoreboard is what will provide us the observability of the DUTs actions allowing us to both via the input stimulus and the corresponding output stimulus from the DUT for comparison. Since we are taking a more of a gray box approach to the testbench, we are limited by the output ports of the DUT for observing functionality and not any internal values. Since the DUT is parameterized for data size and buffer depth, we do know those aspects of the DUT's characteristics.

5 Required Tools

5.1 List of required software and hardware toolsets needed.

- QuestaSim (ran on PSU servers)
- MobaXterm (or some other server remote access method) for PSU Server access.
- UVM SV library

6 Risks and Dependencies

6.1 Risks

- Asynchronous Clock Synchronization: Metastability in pointer synchronization across clock domains.
- Coverage Gaps: Missing corner cases (e.g., simultaneous read/write with maximum dept

6.2 Mitigation

- Use constrained-random tests to stress clock domain crossings.
- Implement comprehensive coverage metrics and review reports weekly.
- Schedule tool access and optimize testbench for simulation efficiency.

7 Functions to be Verified.

7.1 Functions from specification and implementation

7.1.1 List of functions that will be verified. Description of each function

Function	Description
Write Operation	Data is being written in correctly when **wen** high and **fifo_full** low
Read Operation	Data is being read out correctly when **ren** high and **fifo_empty** low
Reset	When **wrst_n_i** is asserted the write reg/signals are reset to initial state When **rrst_n_i** is asserted the read reg/signals are reset to initial state
Data Integrity	FIFO correctly outputs the same data in the same order it was put in
Full / Emply Flags	**fifo_full** is asserted when fifo is full **fifo_empty** is asserted when fifo is empty
Data width and memory depth	Supports data widths up to 256 bits Supports memory depths of up to 65,535

locations

7.1.2 List of functions that will not be verified / need to be implemented

Function	Why
Almost full / empty flags	Not implemented yet
Read / write requests are rejected without affecting FIFO state	Not implemented yet
Write / read acknowledge flags	Not implemented yet

7.1.3 List of critical functions and non-critical functions for tapeout

To keep it short for now, everything that is implemented so far is critical, and the unimplemented functions listed above are non-critical.

8 Tests and Methods (TEST CASES)

8.1.1 Testing methods to be used

The team will be using gray box testing over black or white box testing.

8.1.2 State the PROs and CONs for each and why you selected the method for this DUV.

	Pros	Cons
Black	• Quickly validate functionality • No need to understand internal signals	• Will miss internal bugs • Low controllability/observability of internal signals
Gray	• Have some knowledge of internal signals ○ Leads to better detection of internal bugs	• Still don't see every internal signal or structure, which means some bugs might be missed
White	• Highest controllability/observability	• High costs for maintenance (if one internal signal is changed, test might need a reflecting change)

The team decided on gray box testing because it provides the most balanced approach when it comes to controllability and observability. The most important signals and protocols can be tested along with their functionalities.

8.1.3 Testbench Architecture; Component used (list and describe Drivers, Monitors, scoreboards, checkers etc.)

- Generator: Generates DIN, WR_EN, RD_EN signals with randomized or specified values depending on operation mode.
- Driver: Drivers the DIN, WR_EN, RD_EN signals synchronized to WR_CLK and RD_CLK to theDUT via the virtual interface . Uses random DIN values.
- Monitor: Observes DOUT, FULL, EMPTY, ALMOST_FULL, ALMOST_EMPTY, WR_ACK, WR_ERR, RD_ACK, RD_ERR, WR_COUNT, RD_COUNT.
- Scoreboard: Tracks written data and compares with read data to verify integrity. Maintains expected FIFO state (e.g., occupancy). Automates comparison of actual vs. expected outputs using a reference, behavioral fifo buffer.

8.1.4 Verification Strategy

The team decided on **dynamic simulation** since it's suitable for verifying asynchronous behavior, flag updates, and handshake signals. Formal verification may be added for pointer synchronization.

8.1.5 What is your driving methodology?

The driving methodology will be a mix of directed tests and constrained random testing depending on the need of the tests.

- Directed Tests: Reset, basic write/read, fill/empty scenarios.
- Constrained Random: Random DIN, random delays between read/write operations.

8.1.6 What will be your checking methodology?

- From specification: Verify flags, handshake signals, and count vectors.
- Automated checkers compare actual vs. expected outputs.

8.1.7 Testcase Scenarios (Matrix)

8.1.7.1 Basic Tests

Number	Name	Test Description/ Features	Status
1.1.1	Standard write/read	Write 01234567 in Read 01234567 out	Not done
1.1.2	Random write/read stress test	Write many random bursts of data in, then confirm FIFO correctly reads these bursts out. Do this over a long period (write a lot, read a lot, write a lot...)	Not done
1.1.3	Fill	Write into FIFO until it's FULL, **fifo_full** should be asserted	Not done
1.1.4	Drain	Read from FIFO until it's EMPTY, **fifo_empty** should be asserted	Not done
1.1.5	Write when full	Write into FIFO when **fifo_full** is asserted; FIFO should block write	Not done
1.1.6	Read when empty	Write into the FIFO when **fifo_empty** is asserted; FIFO should block read	Not done

1.1.7	Reset	Reset when empty Reset when partially full Reset when full Make sure correct signals are reset in any instance	Not done
1.1.8	Random interval write/read	Set the timing between writes and reads to a random time, FIFO should still correctly raise FULL/EMPTY flags and have data integrity	Not done
1.1.9	Random data size write/read	Write randomly sized data into FIFO and read them out when full, check for data integrity	Not done

8.1.7.2 Complex Tests

Number	Name	Test Description/ Features	Status
1.2.1	Concurrent testing 1	Concurrent read and write Condition: **fifo_full** What should happen: Read is allowed, write is blocked, **fifo_full** is low after clock	Not done
1.2.2	Concurrent testing 2	Concurrent read and write Condition: **fifo_empty** What should happen: Read is blocked, write is allowed, **fifo_empty** is low after clock	Not done
1.2.3	Concurrent testing 3	Concurrent read and write Condition: **fifo_empty** and **fifo_full** What should happen: Read is blocked, write is blocked, **fifo_empty/fifo_full** is low after clock	Not done
1.2.4	Concurrent testing 4	Concurrent read and write after inserting a single test data into fifo Condition: no flags asserted What should happen: Read out the test data, write in new data	Not done

8.1.7.3 Regression Tests (Not at this point yet)

Test Name / Number	Test Description/Features
1.3.1	Tests that should always pass
1.3.2	

8.1.7.4 Any special or corner cases test cases

Number	Name	Test Description/ Features	Status
1.4.1	WR	Check input output of W->R->W->R many times	Not done

		fifo_empty should be asserted after every read if starting from an empty state.	
1.4.2	WWR	Check input output of W->W->R->W->W->R many times **fifo_full** should be asserted eventually	Not done
1.4.3	RRW	Check input output of R->R->W... many times First two reads will be blocked, then it will start allowing the first read and blocking the second, empty flag is asserted correctly	Not done

9 Coverage Requirements

9.1.1.1 Describe Code and Functional Coverage goals for the DUV

The goal for code coverage in this project is 100%, and 90% coverage for the Class-based testbench for Milestone 3 and 100% coverage for the UVM testbench. This will give us time to improve our set of test cases between the Class-based stage and the UVM stage of the verification project and adjust for any changes to the DUT that occur between those stages.

9.1.2 Covergroups

9.1.2.1 Coverpoint for AINIT and transition bins for 0->1 and 1->0

9.1.2.2 Coverpoint for Req_WR with bins for it being 0, 1, and it being 1 for concurrent cycles

9.1.2.3 Coverpoint for Req_RD with bins for it being 0, 1, and it being 1 for concurrent cycles

9.1.2.4 Coverpoint for data (Both in & out) where the data is all 0s, Low values, and high values, and all 1s (max value).

9.1.2.5 Coverpoint for Full, Almost Full, Empty, and Almost Empty Flags with bins for them being 0, 1, 0->1, 1->0.

9.1.3 Assertions

9.1.3.1 If Full flag is high, Almost Full is also high

9.1.3.2 If Empty flag is high, Almost Empty is also high

9.1.3.3 If Almost Full flag is low, Full is also low

9.1.3.4 If Almost Empty flag is low, Empty is also low

10 Roles and Responsibilities

Role	Main	Helper
RTL coding	Pavan	Suryateja, Kai
Testbench coding	Kai	Suryateja, Pavan, Gene
Design specification	Gene	

Verification plan	Gene, Suryateja	Kai

11 Schedule

Objective	Description	Date
Milestone 1	● Complete design specification ● Start initial verification plan ● Initial implementation of design ● Simple initial testbench	4/20/25
Milestone 2	● Develop class based testbench with completed interfaces ○ Has components: generator, driver, monitor, scoreboard, mailbox ○ Verify 20-50 random bursts of data ● Update verification plan	5/2/25
Milestone 3	● Finalize changes to RTL ● Complete class based testbench ○ Finish coverage here as well ● Add reports for code and functional coverage ● Update verification plan	5/22/25
Milestone 4	● Develop UVM TB ● Update verification plan to include UVM plan ● Utilize UVM_MESSAGE and UVM_LOGGING to create logs and reports about the data	5/22/25
Milestone 5	● Complete UVM architecture, environment, and testbench ● All test cases completed with coverage reflected ● Create RTL bug as a bug injection and verify ● Finalize all documents and presentation	5/27/25

12 References

- Xilinx Asynchronous FIFO V3.0 Design Specification.
- SystemVerilog IEEE 1800-2017 Standard.
- ECE-593 Course Materials, Winter 2025.