The Analysis of PIN CONTROL Subsystem

Nadya A. Mohamed and Xu Chen
ECE Department, Rice University

Abstract

In this report, we focus on a specific Linux subsystem - the PIN CONTROL subsystem, which is a centralized mechanism that can arrange and configure pins. We discuss the hardware background of the PIN CONTROL subsystem, the reason why it is necessary in Linux, and its three major functions. Finally, we perform our own analysis for this subsystem. We leverage cloc and cscope as analyzers, and observe several interesting facts about PIN CONTROL subsystem.

1. Introduction

Some of them have well-defined purposes. For example, they can be used to supply powers and clocks, to generate video output and to perform the memory control. While other pins do not have specific functions (i.e., GPIO). So the infrastructure of pins on a specific board essentially is quite complex.

2. Pins in Hardware

2.1 Overview

What is pin?

2.2 SoC Pins

What is pin?

2.3 Pad Cell

What is pin?

2.4 GPIO

How GPIO block is formed using I/O Cell.

3. PIN CONTROL Subsystem

As mentioned, given a system-on-chip (SOC), it has plenty of pins on it. To ensure that a SOC work can normally, all pins should be properly configured. However, managing such complex configuration is quite challenging since the correct pin configuration is board-specific, and lots of board-specific codes are required in the pin configuration.

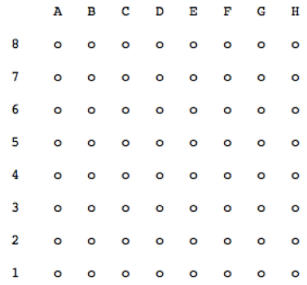


Figure 1: A single PGA chip

The PIN CONTROL subsystem, as a centralized mechanism, has three major functions that help address these challenges, pin enumerating, pin multiplexing (e.g., the way to reuse a single pin or a single group of pins for different purposes), and pin configuration.

3.1 Pin Enumerating

In the top-level interface, an important function of PIN CONTROL subsystem is enumerating, which means that it can enumerate all controllable pins that a specific processor provides. In the example of a PGA chip board seen from the underneath, as shown in the Fig. 1, we observe that PIN CONTROL subsystem is able to register a pin controller and name all pins by associating them with integers. These integers are called pin numbers. Fig. 2 displays a typical industrial standard to name all controllable pins in a given board. Specifically, the pins A8, B8, C8 are named as 0, 1, 2 in the beginning, and the pins F1, G1, H1 are denoted as 61, 62, 63 in the end.

It is important to note that this naming strategy is only a typical example. Other naming principles are also allowed. The association between pins and pin numbers can be regarded as a bridge that connects the hardware and software, hence making further analysis from the perspective of software much easier.

In addition, controllers usually deal with groups of pins when performing functions, instead of a single pin. There-

ISBN [to be supplied]. . . $15.00

```
#include <linux/pinctrl/pinctrl.h>

const struct pinctrl_pin_desc foo_pins[] = {
      PINCTRL_PIN(0, "A8"),
      PINCTRL_PIN(1, "B8"),
      PINCTRL_PIN(2, "C8"),
      ...
      PINCTRL_PIN(61, "F1"),
      PINCTRL_PIN(62, "G1"),
      PINCTRL_PIN(63, "H1"),
};

static struct pinctrl_desc foo_desc = {
        .name = "foo",
        .pins = foo_pins,
        .npins = ARRAY_SIZE(foo_pins),
        .owner = THIS_MODULE,
};

int __init foo_probe(void)
{
        int error;

        struct pinctrl_dev *pctl;

        error = pinctrl_register_and_init(&foo_desc, <PARENT>, NULL, &pctl);
        if (error)
                return error;

        return pinctrl_enable(pctl);
}
```

Figure 2: Enumerating pins

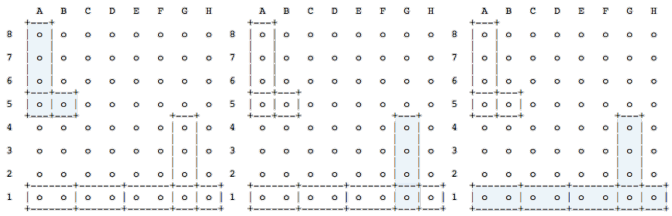
fore, a mechanism that can enumerate and retrieve "groups of pins" is highly desirable. These groups of pins are defined as the pin groups, which often correspond to a specific function. For example, we can have one groups of pins 0, 8, 16, 24 (i.e., pin numbers) dealing with SPI interface, and the other groups of pins 24, 25 dealing with I2C interface. Once the pin groups are clearly defined, then the function in PINCTRL code get_group_count will be able to determine the total number of legal selectors needed for other functions to retrieve the names and pins of each pin group.

3.2 PINMUX

Given the system-on-chip, there are multiple ways to utilize its pins. However, a common situation users might encounter is that some pins need to be reused for different tasks. To this end, a mechanism that can regulate the way to reuse pins for multiple mutually exclusive functions becomes necessary. PIN CONTROL subsystem has the PINMUX functionality, which helps the reuse of pins.

Fig. 3 shows a example of how the PINMUX mechanism works for a single chip. This example again utilizes a single PGA chip seen from the underneath. When this chip is used, some pins will be taken by feeding power to the chip. They might be connected to VCC or GND. Another groups of pins will be occupied by large ports, such as the external memory interface. After then, the remaining pins on the board will be subject to pin multiplexing (i.e., PINMUX).

In the case where the pins A8, A7, A6, A5 are used to deal with the SPI port, and the pins A5, B5 are exploited to deal with I2C port, we observe that the A5 pin is actually "shared" by two ports. Due to this sharing, SPI and I2C ports could not be used at the same time. However, PINMUX settings enable the SPI logic to be routed out on the pins G4, G3, G2, G1, such that the conflict at A5 can be eliminated, and the SPI, I2C ports then can be exploited simultaneously. Similarly, while a 8-bit MMC bus is being used, the routed SPI port then will not be allowed to be utilized at the same time. PINMUX settings control all these processes.



(a) Pins for SPI and I2C (b) Routed pins for SPI (c) SPI and MMC (8-bit)

Figure 3: Example of PINMUX use

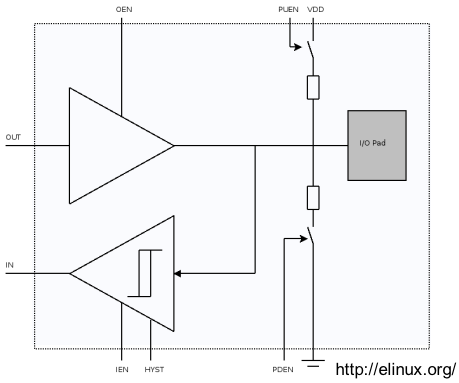


Figure 4: The illustration of pin configuration

3.3 Pin Configuration

The last function of the PINCTRL subsystem is pin configuration. The key idea of pin configuration is that pins can be software-configured since pins also have electronic properties.

Specifically, as shown in the Fig. 4, once the switch in the upper of this circuit is closed, an input pin will be attached to VDD to provide power. We also notice that there is a pull-up resistor, which ensures that the input signal will be maintained at a stable level even when pins are disconnected, or when output pins are connected to a high impedance. The lower part of this circuit contains a pull-down resistor, which serves a similar purpose, keeping the signal at low level when the pin is unconnected. Pin configuration codes integrated in the PINCTRL subsystem is able to help set all these electronic operations of pins (i.e., hardware operation) from the software perspective.

4. PINCTRL Subsystem Analysis

4.1 Line of Codes (LOC) Analysis

To start with, we first discuss our findings in the lines of code (LOC) analysis. Fig. 5 displays the number of code lines, comment lines, and the number of blank lines in the PINCTRL codes designed for multiple hardware in Linux 4.11 version, the latest version we study. We pick up the several hardware examples that PINCTRL code can work for,

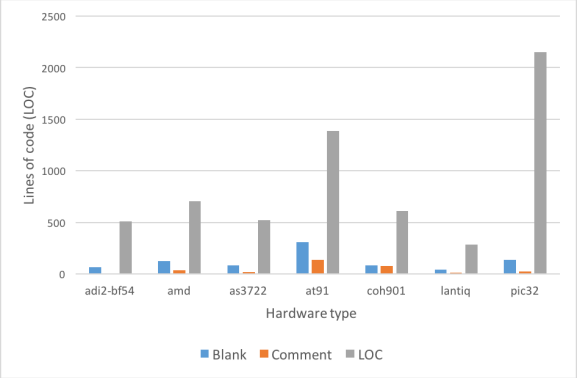
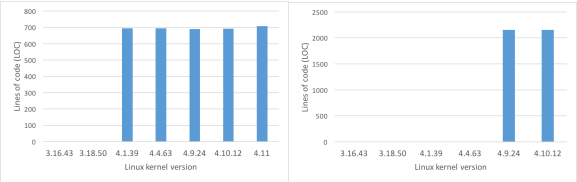


Figure 5: LOC of PINCTRL for various hardware v.4.11



(a) PINCTRL for hardware amd (b) PINCTRL for hardware pic32

Figure 6: LOC revolution of PINCTRL for two hardware

including ADI GPIO2 controller on bf54x processor (i.e., adi2-bf54), GPIO driver for AMD (amd), the power management unit AS3722 (as3722), Atmel AT91SAM SoC (at91), ST-Ericsson U300 Series (coh901), Lantiq SOC (lantiq), and PIC32 pin controller driver (pic32). In Fig. 5, we observe that most PINCTRL codes do have much shorter comment lines compared to effective lines of code (LOC). We envision that it is partly since the documentation is concrete enough such that only a few of comment lines are in need to highlight the hardware-specific requirements.

As shown in Fig. 6, we also study the temporal development of the LOC in PINCTRL codes. According to the official document [?], the overall PINCTRL subsystem was added to the Linux kernel from the version 3.13. The codes designed for GPIO driver of AMD, and PIC32 pin controller driver, were not developed until the version 4.1.39 and 4.9.24, respectively. But after they were introduced, these two codes only experienced minor modifications in the past few versions.

Then we focus on the version-by-version difference of LOC in PINCTRL codes for different hardware. As shown in Fig. 7, we note that adi2-bf54 and lantiq experience no change at all starting from their released dates. That means codes designed for them are robust. However, PINCTRL codes designed for Atmel AT91SAM SoC have been extended a lot from 3.16 to 3.18, and then are shrinked from the version 4.1.39 to 4.9.24.

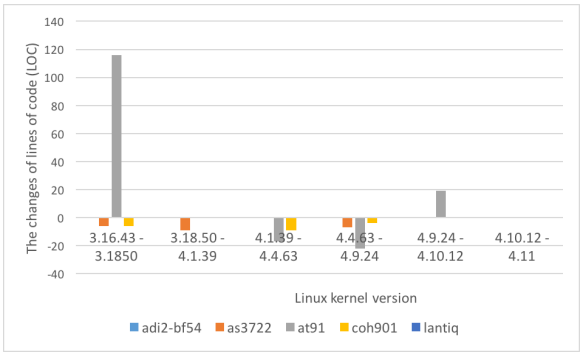


Figure 7: LOC difference across different versions

In conclusion, starting from the Linux kernel version 3.13 where the PINCTRL codes were initially introduced

4.2 Author Database Analysis

4.3 Function Use Analysis

4.4 Methods, Tools, and Procedures

In LOC analysis, we leverage the tool **cloc** [?]. This toolkit can display the lines of code (LOC) for all the files in a single folder in different categories (e.g., C, C++, HTML, XML, etc.)

5. Conclusion

In this report, we study the PINCTRL subsystem extensively by examining its background information (i.e., hardware) and its three major functions. We then perform our own analysis for the codes of PINCTRL subsystem, using cloc and cscope tools. Our analysis involves lines of code (LOC) in multiple hardware, and xxx