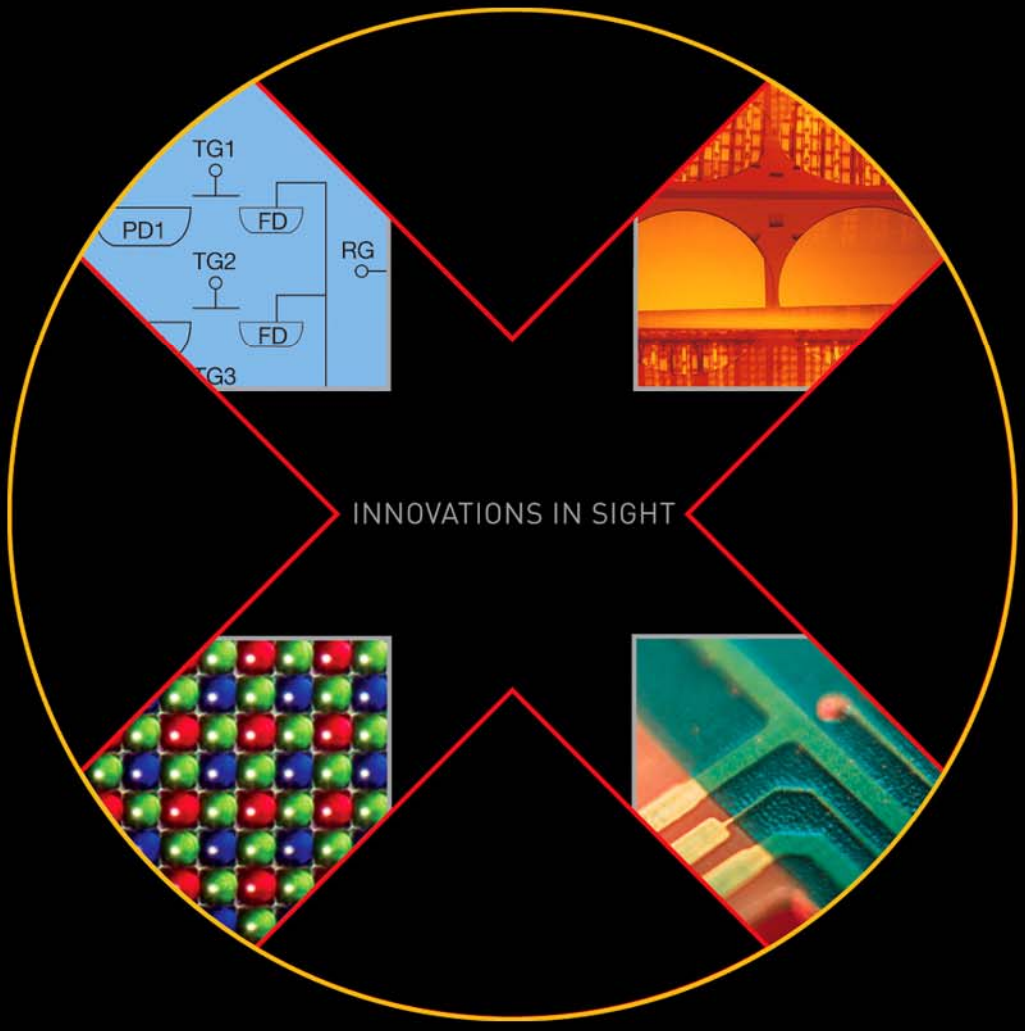
DEVICE PERFORMANCE SPECIFICATION

Revision 1.0 MTD/PS-1070

May 7, 2009



KODAK KAC-00401 IMAGE SENSOR

768 (H) X 488 (V) WVGA CMOS RAW IMAGE SENSOR

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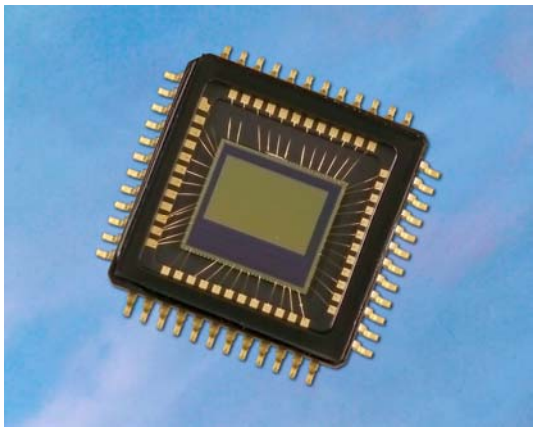
SUMMARY SPECIFICATION

KODAK KAC-00401 IMAGE SENSOR

1/3" WVGA RAW CMOS IMAGE SENSOR



DESCRIPTION

The KAC-00401 is a high performance, low power, automotive grade image sensor capable of capturing motion and still images. Included on-chip is a video gain amplifier, 12-bit A/D converter, and fixed pattern noise elimination circuits. Also integrated are programmable smart timing and control circuits, which allow maximum flexibility in adjusting gain, frame rate, integration time, and active window size. In addition, the dynamic range of the sensor can be extended >100dB through a high dynamic range response curve.

FEATURES

- WVGA resolution for wider field of view
- Monochrome or Bayer RGB available
- Low noise architecture for increased SNR
- Enhanced near-IR performance
- Extended Dynamic Range via three breakpoint programmable response curve
- Partial Line Integration for superior exposure control under high-light conditions
- High frame rate – 60 fps @ full resolution
- Simple I^2C compatible serial interface
- Operating temperature range up to +105°C
- Automotive grade 48-pin PQFP

APPLICATIONS

- Automotive Imaging
- Machine Vision

Parameter	Value
Optical Format	1/3-inch
Active Array	768(H) x 488(V)
Imaging Area	5.15mm(H) x 3.27mm(V)
Pixel Size	6.7µm x 6.7µm
Quantum Efficiency	Monochrome: 60% @ 550nm
Sensitivity	Monochrome: 4.5 V/lux-sec
Dynamic Range	Linear: 60dB Extended: >100dB
Dark Current	0.9nA/cm2
Read Noise	4.3 LSBs
Frame Rate	60 fps @ 768H x 488V
Readout Rate	6-24 MSPS
Data Format	12-bit parallel Bayer RAW
Scan Mode	Progressive scan
Shutter Modes	Continuous and single frame rolling shutter
Programmable Gain	Fine: 5.7x, 0.075x steps Coarse: 2.35x, 0.19x steps
Power Supply	I/O: 3.3V ±10% Analog: 3.3V ±5% Digital: 1.8V ±5%
Power Consumption	Total: 191mW Analog + I/O: 184mW Digital: 7mW
Temperature Range	Operating: -40°C to 105°C
Package	48-pin PQFP

All parameters above are specified at T = 20°C

ORDERING INFORMATION

Catalog Number	Product Name	Description
4H2104	KEK-4H2104-KAC-00401	CDU Evaluation Kit – Complete System
4H2105	KEH-4H2105-KAC-00401	CDU Evaluation Kit – Headboard only
4H2094	KAC-00401-MBC-LB-A1 Trays	Monochrome, Telecentric Microlens, PQFP Package in Tray, Clear Cover Glass, Standard Grade
4H2095	KAC-00401-CBC-LB-A0 Trays	Bayer RGB, Telecentric Microlens, PQFP Package in Tray, Clear Cover Glass, Standard Grade

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Please address all inquiries and purchase orders to:

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Rochester, New York 14650-2010

Phone: (585) 722-4385
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E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

FUNCTIONAL DIAGRAMS

OVERALL CHIP BLOCK DIAGRAM

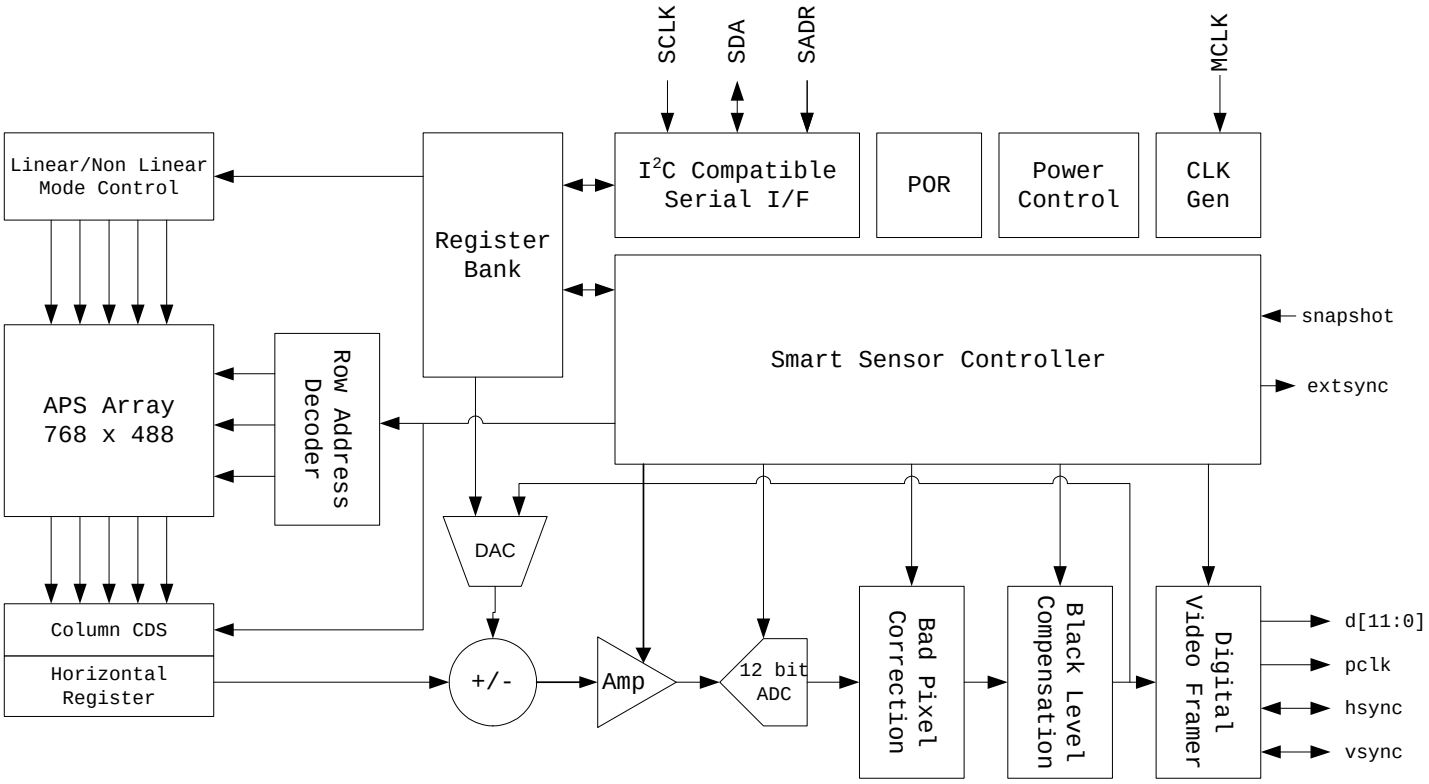


Figure 1: Block Diagram

CONNECTION DIAGRAM

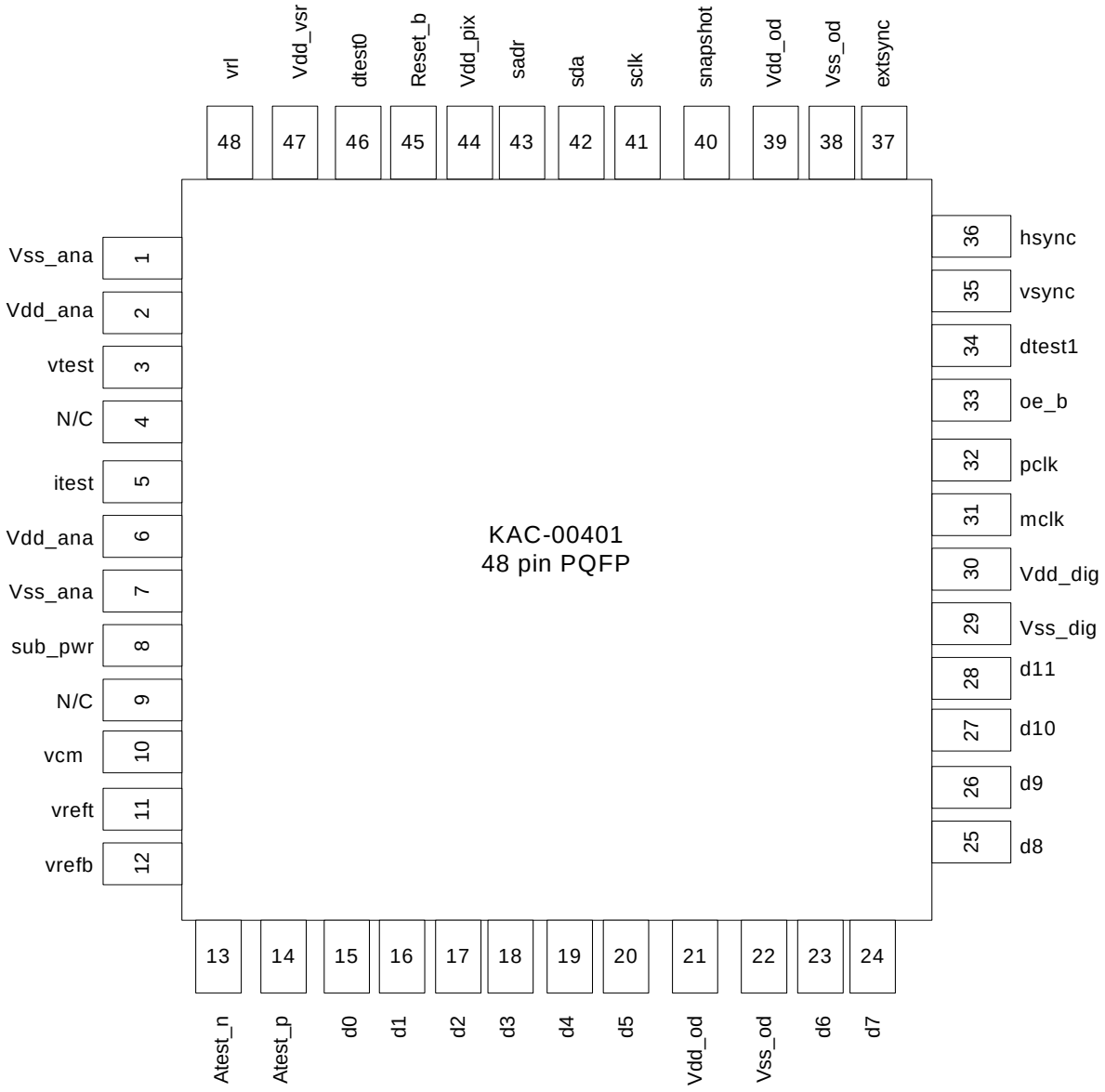


Figure 2: KAC-00401 Pin Diagram for PQFP Package

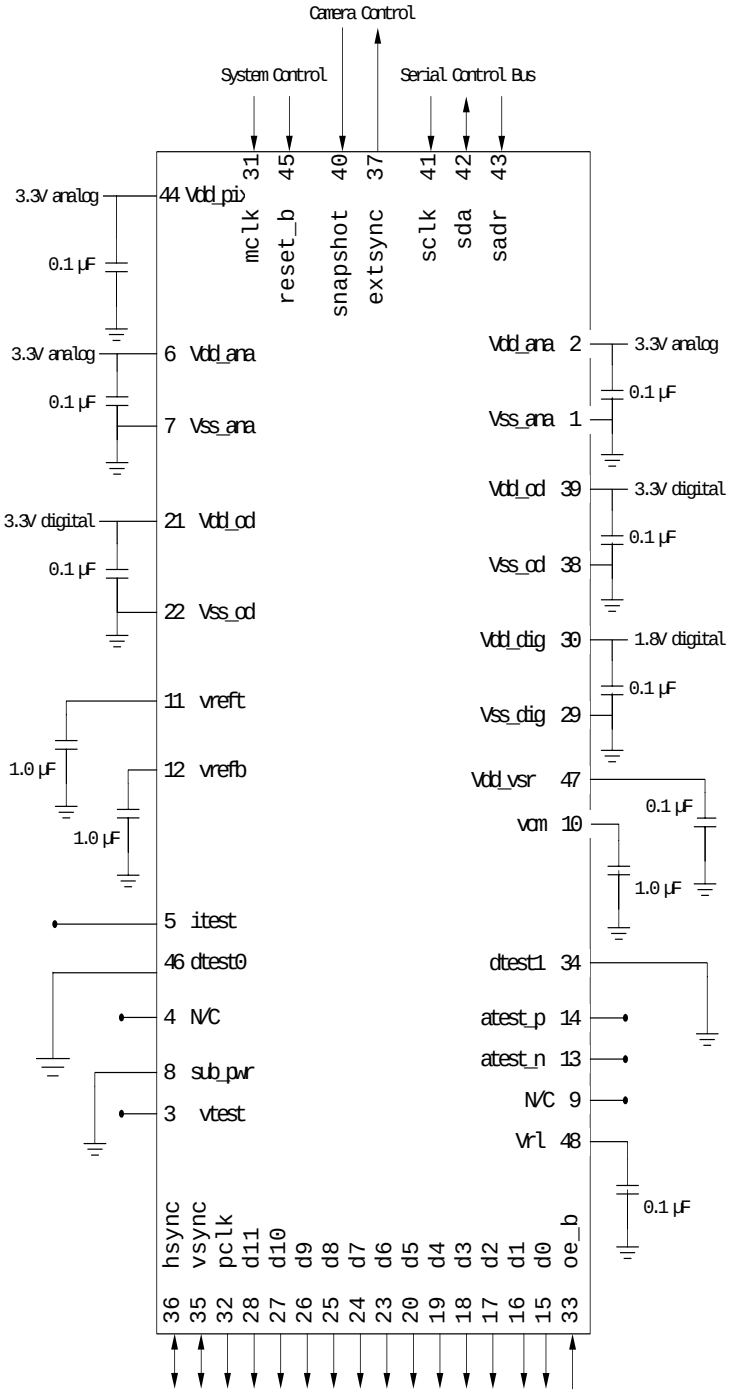


Figure 3: Typical Application Circuit Diagram

PIN DESCRIPTION

PQFP Pin	Name	Description	Type	Power	Value
1	vss_ana	Ground supply for analog circuits	G	A	0 V
2	vdd_ana	3.3 volt supply for the analog circuits	P	A	3.3V
3	Vtest	Reserved for production testing. This pin should not be connected.	O	D	
4	N/C	No Connect	I	A	
5	Itest	Reserved for production testing. This pin should not be connected.	I	A	
6	vdd_ana	3.3 volt supply for analog circuits	P	A	3.3V
7	vss_ana	Ground supply for analog circuits	G	A	0V
8	sub_pwr	Substrate power connection. This pin should be tied to ground	G	A	0V
9	N/C	No Connect	O	D	
10	Vcm	Common mode reference voltage. This pin should be bypassed with a 1.0 µF capacitor.	O	A	
11	Vreft	ADC top reference output. This pin should be bypassed with a 1.0 µF capacitor	O	A	
12	Vrefb	ADC bottom reference output. This pin should be bypassed with a 1.0 µF capacitor	O	A	
13	atest_n	Reserved for production testing. This pin should not be connected.	I/O	A	
14	atest_p	Reserved for production testing. This pin should not be connected.	I/O	A	
15	d0	Digital output, Bit 0 of 11. This output can be put into tri-state mode.	O	D	
16	d1	Digital output, Bit 1 of 11. This output can be put into tri-state mode.	O	D	
17	d2	Digital output, Bit 2 of 11. This output can be put into tri-state mode.	O	D	
18	d3	Digital output, Bit 3 of 11. This output can be put into tri-state mode.	O	D	
19	d4	Digital output, Bit 4 of 11. This output can be put into tri-state mode.	O	D	
20	d5	Digital output, Bit 5 of 11. This output can be put into tri-state mode.	O	D	
21	vdd_od	3.3 volt supply for the digital IO buffers. This pin should be bypassed with a 0.1 µF capacitor to ground.	P	D	3.3V
22	vss_od	Ground supply for I/O circuits	G	D	0V
23	d6	Digital output, Bit 6 of 11. This output can be put into tri-state mode.	O	D	
24	d7	Digital output, Bit 7 of 11. This output can be put into tri-state mode.	O	D	
25	d8	Digital output, Bit 8 of 11. This output can be put into tri-state mode.	O	D	
26	d9	Digital output, Bit 9 of 11. This output can be put into tri-state mode.	O	D	
27	d10	Digital output, Bit 10 of 11. This output can be put into tri-state mode.	O	D	
28	d11	Digital output, Bit 11 of 11. This output can be put into tri-state mode.	O	D	
29	vss_dig	Ground supply for digital circuits	G	D	
30	vdd_dig	1.8 volt supply for digital circuits. This pin should be bypassed with 0.1 µF capacitor to ground.	P	D	1.8V
31	Mclk	Digital input. The sensor's master clock input	I	D	
32	Pclk	Digital output. The pixel clock	O	D	
33	oe_b	Digital input with pulldown resistor. When forced to a logic 1 the sensor's digital video port d[11:0], vsync, hsync and pclk will be tri-stated.	I	D	
34	dtest1	Reserved for production testing. This pin should be tied to ground.	I	D	
35	Vsync	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, (the default), this pin is an output and is the vertical synchronization pulse. When the sensor's digital video port is configured to be a slave, this pin is an input and is the frame trigger.	I/O	D	
36	Hsync	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, (the default), this pin is an output and is the horizontal synchronization pulse. When the sensor's digital video port is configured to be a slave, this pin is an input and is the row trigger	I/O	D	
37	Extsync	Digital output. Used to synchronize external events in snapshot mode.	O	D	
38	vss_od	Ground supply for the digital IO buffer. This pin should be connected to ground	G	D	0V
39	vdd_od	3.3 volt supply for the digital IO buffers. This pin should be bypassed with a 0.1 µF capacitor to ground.	P	D	3.3V
40	snapshot	Digital input with pulldown resistor used to activate (trigger) a snapshot sequence.	I	D	
41	Sclk	I2C compatible serial interface clock	I	D	
42	Sda	I2C compatible serial interface data bus. The output stage of this pin is an open drain driver.	I/O	D	
43	Sadr	Digital Input with pulldown resistor, to program different slave addresses in an I^2C compatible system.	I	D	
44	vdd_pix	3.3 volt supply for the pixel array.	P	A	3.3V

PQFP Pin	Name	Description	Type	Power	Value
45	reset_b	Digital Input with pull up resistor. When forced to a logic 0 the sensor is reset to its default power up state. The resetb signal is internally synchronized to mclk, which must be running for a reset to occur.	I	D	
46	dtest0	Reserved for production testing. This pin should be tied to ground.	I	D	
47	vdd_vsr	4.4V Charge pump output voltage, bypass to ground with a 0.1 µF capacitor	O	A	
48	Vrl	Anti blooming pin. This pin should be bypassed to ground with a 0.1 µF capacitor	O	A	

P = VDD, G = VSS, I = Input, O = Output, D = Digital, A = Analog

RATINGS AND SEPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Any Positive Supply Voltage except Vdigita	3.6V
Vdigital Supply Voltage	2.0V
Voltage on any input or output pin except Vdigital	-0.5V to 3.6
Input voltage on Vdigital	2.0V
Input current at any pin	25mA
ESD Susceptibility Human Body Model Machine Model	 2000V 200V
Package Input Current	50mA
Package Power Dissipations @ TA	2.5W
Soldering Temperature	240° C
Storage Temperature	-40° C to 125° C

Note: Human body model is 100pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 200 pF discharged through 0 Ω.

OPERATING RATINGS

Parameter	Value
Operating Temperature Range	-40° C ≤ T ≤ +105° C
All vdd_od Supply Voltages All vdd_ana Supply Voltages	+3.0V to +3.6V +3.15 to +3.5V
All vdd_dig Supply Voltages	+1.7V to +1.9V

DC AND LOGIC LEVEL SPECIFICATIONS

The following specifications apply for V_{analog} = 3.3V, V_{od} = 3.3V, $V_{digital}$ = 1.8V, Mclk = 16.5Mhz. **Boldface limits apply for TA = T_{min} to T_{max}**: all other limits TA = 25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Units
sclk, sda, sadr Digital Input/Output Characteristics						
VIH	Logical "1" Input Voltage		Vdd_od*0.7		Vdd_od	V
VIL	Logical "0" Input Voltage				Vdd_od*0.3	V
VOL	Logical "0" Output Voltage	vdd_od = 3.3V, Iout = 3.0mA			0.4	V
V_{hys}	Hysteresis (sclk pin only)	vdd_od = 3.3V, Iout = 3.0mA	vdd_od*0.5			V
I_{leak}	Input Leakage Current			-1		µA
mclk, snapshot, pdwn, reset_b, hsync, oe_b Digital Input Characteristics						
VIH	Logical "1" Input Voltage	Vdd_od = 3.0V	Vdd_od*0.7		Vdd_od	V
VIL	Logical "0" Input Voltage	Vdd_io = 3.6V			Vdd_od*0.3	V
IIH	Logical "1" Input Current	VIH = vdd_dig		0.1		µA
IIL	Logical "0" Input Current	VIL = vss_dig		0.1		µA

d0 - d11, pclk, hsync, vsync, extsync Digital Output Characteristics						
VOH	Logical "1" Output Voltage	vdd_od = 3.3V, Iout = 1.6mA	Vdd_od – 0.4			V
VOL	Logical "0" Output Voltage	vdd_od = 3.3V, Iout = 1.6mA			0.4	V
IOZ	Tri-State Output Current	VOUT = vss_od VOUT = vdd_od		-0.1 0.1		µA
Power Supply Characteristics						
I_a	Analog Supply			41		mA
I_d	Digital Supply			3.7		mA
I_{io}	IO Supply			15.0		mA

POWER DISSIPATIONS SPECIFICATIONS

The following specifications apply for V_{analog} = 3.3V, V_{od} = 3.3V, $V_{digital}$ = 1.8V, Mclk = 16.5 MHz, Hclk = 16.5 MHz, frame rate = 34.15 frames/sec. **Boldface limits apply for TA = T_{min} to T_{max}**: all other limits TA = 25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Units
P_{dwn}	Power Down	no clock running		0.33		mW

VIDEO AMPLIFIER SPECIFICATIONS

The following specifications apply for V_{analog} = 3.3V, V_{od} = 3.3V, $V_{digital}$ = 1.8V. **Boldface limits apply for TA = T_{min} to T_{max}**: all other limits TA = 25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Units
G_{gain}	Maximum Coarse gain	7 linear steps		2.35		x
F_{gain}	Maximum Fine gain	64 linear steps		5.7		x

AC ELECTRICAL SPECIFICATIONS

The following specifications apply for V_{analog} = 3.3V, V_{od} = 3.3V, $V_{digital}$ = 1.8V. **Boldface limits apply for TA = T_{min} to T_{max}**: all other limits TA = 25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Units
F_{mclk}	Input clock frequency		12		48	MHz
	Clock duty cycle	@ Fmclk Max	45/55		55/45	min/max
T_{rc},T_{fc}	Clock input rise and fall time			3		ns
F_{hclk}	Internal system clock frequency		6		24	MHz
F_{CPclk}	Charge pump clock frequency		12		24	MHz
T_{reset}	Reset pulse width		1			µs

CMOS ACTIVE PIXEL ARRAY SPECIFICATIONS

Parameter	Value
Number of pixels (row, column)	
Total	768H x 512V pixels
Active	768H x 488V pixels
1/3" optic	750H x 480V pixels
Array size (x,y Dimensions)	
Total	5.156 x 3.4304 mm
Active	5.156 x 3.2696 mm
1/3" optic	5.025 x 3.2696 mm
Pixel Pitch	6.7 µm

IMAGE SENSOR SPECIFICATIONS (LINEAR MODE)

Parameter	Description	Min	Typical	Max	Units
Optical Sensitivity[1]	Measured at the input of the A/D		4.5		Volts/(lux*sec)
Dark Signal	The pixel output signal due to dark current.		0.039		Volt/sec
Read Noise	The RMS temporal noise of the pixel output signal in the dark averaged over all pixels in the array		4.3		LSBs
Dynamic Range	The ratio of the saturation pixel output signal and the read noise expressed in dB.		59.5		dB
SNR (also see figure)	Signal to Noise Ratio, expressed in dB, is defined as $\frac{Pixel_{mean} - Pixel_{dark}}{Frame_{std}}$ Where **$Pixel_{mean}$** is the average of all pixels at 70% saturation and TBD fps, **$Pixel_{dark}$** is the average of all pixels in the dark after black level compensation, and **$Frame_{std}$** is the spatial standard deviation of all pixels in the frame.		36		dB
FPN	Fixed Pattern Noise: the RMS spatial noise in the dark excluding the effect of read noise.		0.66		%
PRNU	Photo Response Non Uniformity: the RMS variation of pixel senstivities as a percentatge of the average optical sensitivity.		1.2		%

[1]The optical sensitivity at the A/D output, in units of LSBs/(lux*sec), can be calculated using 4096/(vrefp – vrefn) *Optical sensitivity

IMAGE SENSOR SPECIFICATIONS (HIGH DYNAMIC RANGE MODE)

Parameter	Description	Min	Typical	Max	Units
Dark Signal	The pixel output signal due to dark current.		0.039		Volt/sec
Read Noise	The RMS temporal noise of the pixel output signal in the dark averaged over all pixels in the array		4.3		LSBs
FPN	Fixed Pattern Noise: the RMS spatial noise in the dark excluding the effect of read noise.		0.66		%

[1]The optical sensitivity at the A/D output, in units of LSBs/(lux*sec), can be calculated using 4096/(vrefp – vrefn) *Optical sensitivity

SENSOR RESPONSE CURVES

QUANTUM EFFICIENCY

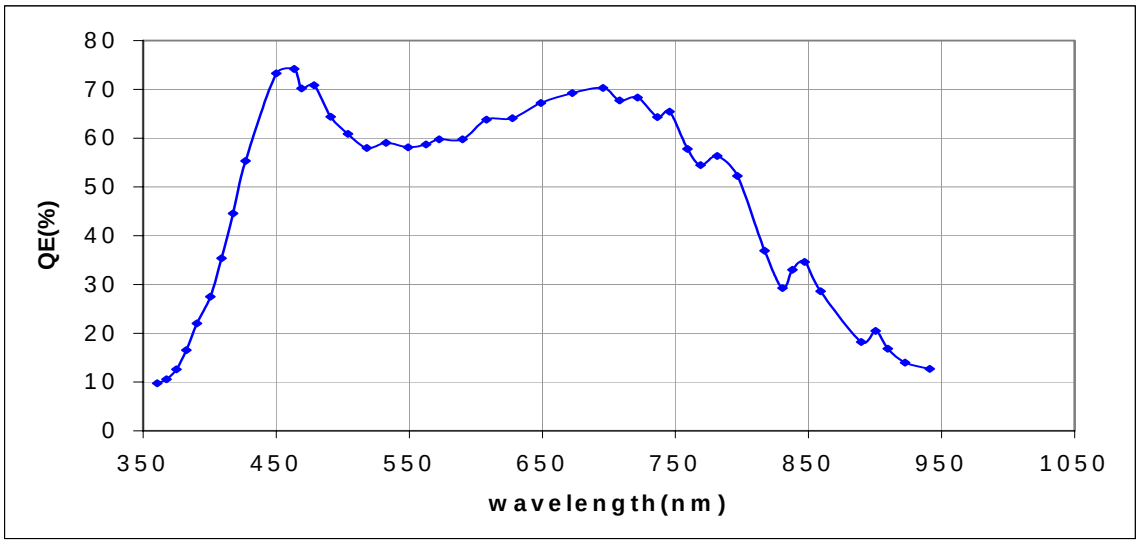


Figure 4: QE response for monochrome KAC-00401

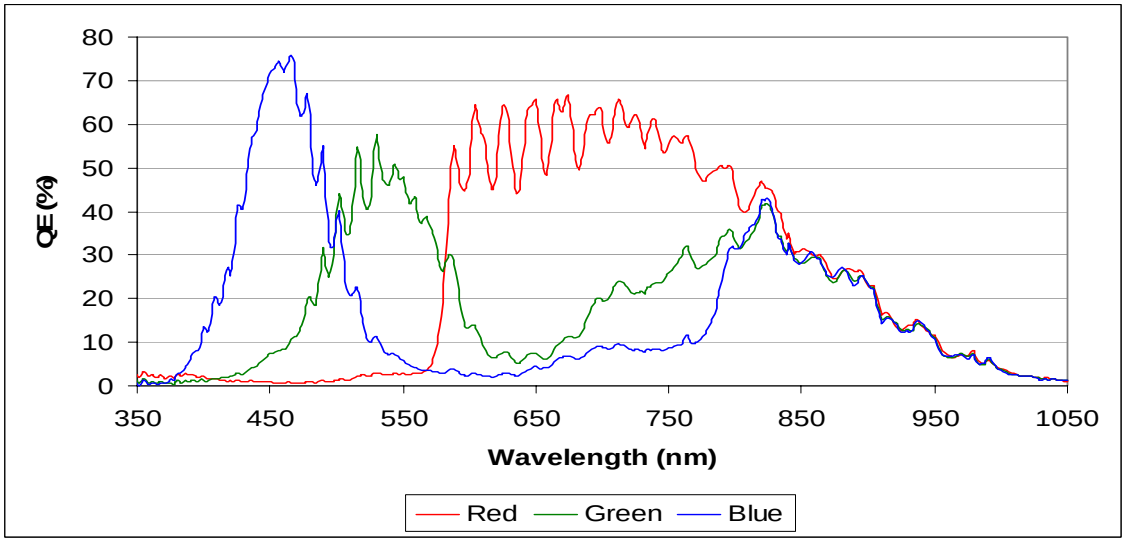


Figure 5: QE response for color KAC-00401

FUNCTIONAL DESCRIPTION

OVERVIEW

The KAC-00401 contains a CMOS active array consisting of 768 columns by 488 rows. 8 additional rows of optically shielded (black) pixels are provided at the bottom of the array as shown in Figure 6.

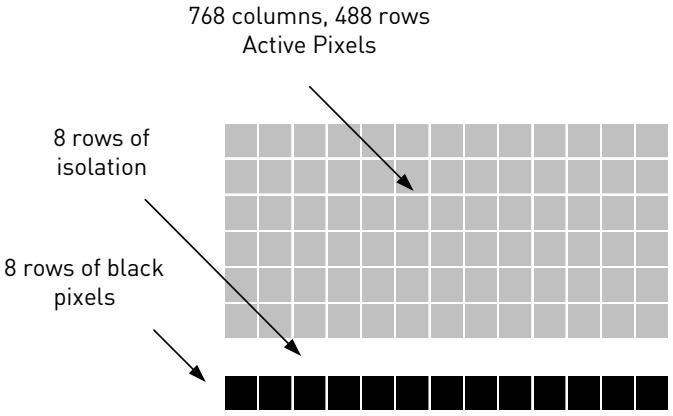


Figure 6: CMOS APS region of the KAC-00401

At the beginning of a given integration time the on-board timing and control circuit will reset every pixel in the array one row at a time as shown in Figure 7. Note that all pixels in the same row are simultaneously reset.

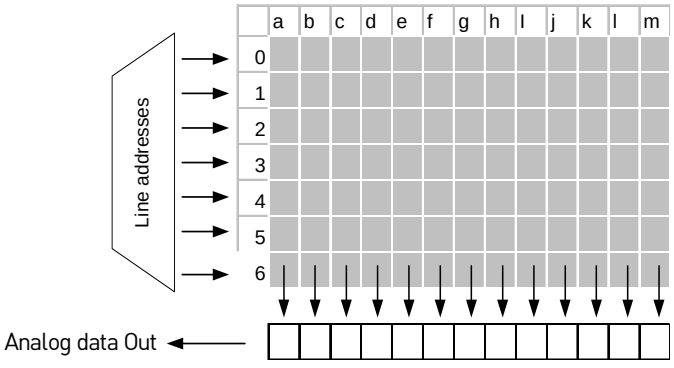


Figure 7: CMOS APS Row and Column addressing scheme

At the end of the integration time, the timing and control circuit will address each row and simultaneously transfer the integrated value of the pixel to a correlated double sampling circuit and then to a shift register as shown in Figure 7. Once the correlated double sampled signals have been loaded into the shift register, the timing and control circuit will shift them out one pixel at a time.

The analog pixel signal is then fed into an analog gain channel, as shown in Figure 8, where two programmable amplifiers (PGA and FGA) provide the necessary gain so that the signal level of the pixel can be adjusted.

After gain adjustment the analog value of each pixel is converted to a 12 bit digital data as shown in Figure 8.

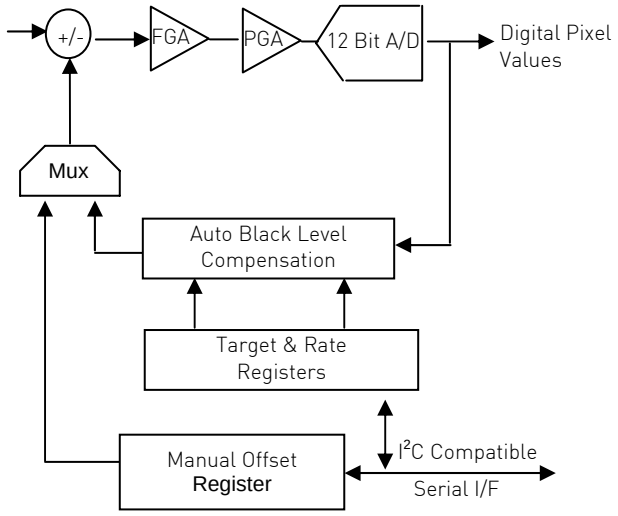


Figure 8: Analog Signal Conditioning and Conversion to Digital

The black level of each pixel together with the full analog signal path offset is automatically compensated as shown in Figure 8. This can be manually overridden.

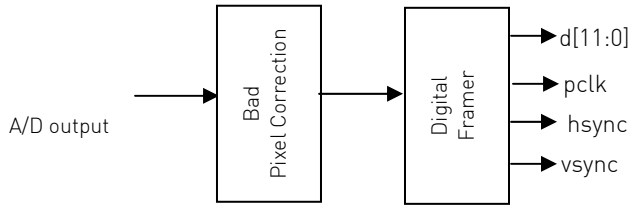


Figure 9: Digital Pixel Processing

The pixel data is processed next by the bad pixel correction circuit and finally framed and output on the digital video bus as shown in Figure 9.

CONFIGURATION

Program and Control Interfaces

The programming, control and status monitoring of the KAC-00401 is achieved through a two-wire I2C compatible serial bus. A device address pin is provided allowing two different device addresses to be selected for the serial interface as shown in Figure 10.

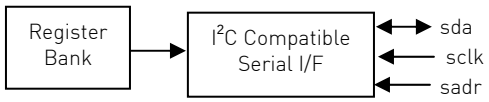


Figure 10: Control Interface to the KAC-00401

Snapshot control and status pins are provided to facilitate single frame capture (see Figure 11).

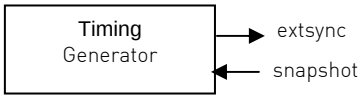


Figure 11: Snapshot and External Event Trigger Signals

Double Buffered Registers

All programmable registers that affect image resolution, quality, and exposure are double buffered. The double-buffered registers are: horizontal and vertical resolution, video gain, integration time, row delay, frame delay, breakpoint levels and breakpoint slopes.

Double buffering prevents "broken" frames such that new values for the above mentioned parameters take effect only at the start of a new frame, after the "update" bit has been set. This mechanism enables the user to change a bigger series of parameters (where the I2C writes may extend over several frames), without affecting the image during parameter change. Changes in the gain, row or frame delay registers become effective immediately (at the start of a frame and after the update bit was set), the integration time and all parameters affecting the HDR mode show a latency of one frame due to the nature of the rolling reset architecture. The "update" mechanism can be disabled; in that case changes to parameters go into effect immediately at the start of the new frame.

Windowing

The integrated timing and control circuit allows any size window in any position within the active resolution. The window read out is called the "*Scan Window*".

Four coordinates (start row address, start column address, end row address, and end column address) need to be programmed to define the size and location of the "*Scan Window*" to be read out (see Figure 12).

A *Display window* must be specified in order to tell the scan engine which are the lines interested in the read out; these rows are programmed in the Display Window Row registers and should be smaller than the *Scan Window* so that there is not blooming from rows that are not reset.

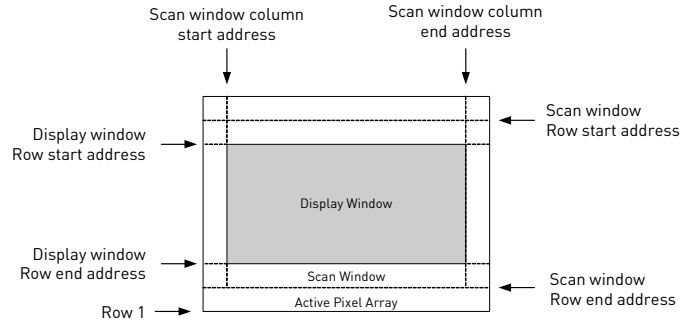


Figure 12: Windowing

Notes:

- By default the "Scan Window" is optically centered with a size of 750 columns by 480 rows as shown in Figure 13. (This yields a 1/3" optical format)
- The "Scan Window" registers are double buffered.

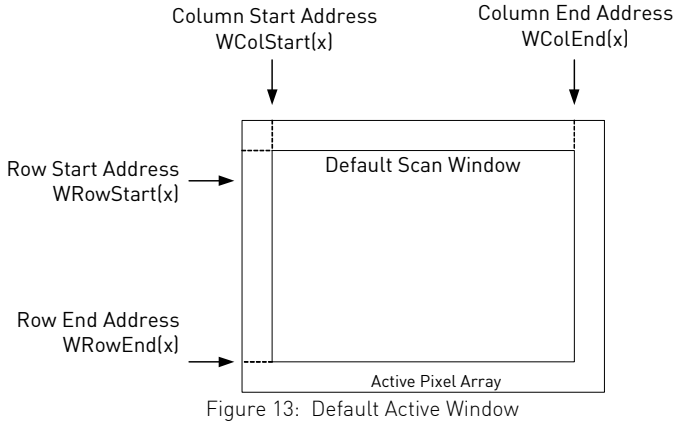


Figure 13: Default Active Window

Digital Array Readout

The pixels in the array are read out in progressive scan. In progressive scan, every pixel of every row in the defined "Display Window" is consecutively read out, one pixel at a time.

The scan direction can be programmed as follows:

Default Scan Direction

The default scan direction is to consecutively read out, one pixel at a time, starting with the leftmost pixel in the bottom row. Hence, for the example shown in Figure 14, the read out order will be a10, b10...n10 then a9, b9...n9 and so on until pixel n0 is read out. See Figure 14.

Reverse Vertical Scan Direction

The vertical scan direction can be reversed by setting the VScanDir bit in the SCANCONFIG register to a logic 0, while setting the HScanDir bit in the SCANCONFIG register to a logic 1. In this case for the example shown in Figure 14, the read out order will be a0, b0, ...n0 then a1, b1,...,n1 and so on until pixel n10 is read out.

Reverse Horizontal Scan Direction

The horizontal scan direction can be reversed by setting the "HScanDir" bit in the SCANCONFIG register to a logic 0, while setting the "VScanDir" bit in the SCANCONFIG register to a logic 1. In this case for the example shown in Figure 14, the read out order will be n10, m10,...,a10 then n0,m0,...a0 and so on until pixel a0 is read out.

Reversing the Horizontal and Vertical Scan Direction

The horizontal and vertical scan direction can be reversed by setting both the "HScanDir" bit in the SCANCONFIG and the "VScanDir" bit in the SCANCONFIG register to a logic 0. In this case for the example shown in Figure 14, the read out order will be n0, m0...a0 then n1, m1...a1 and so on until pixel a10 is read out.

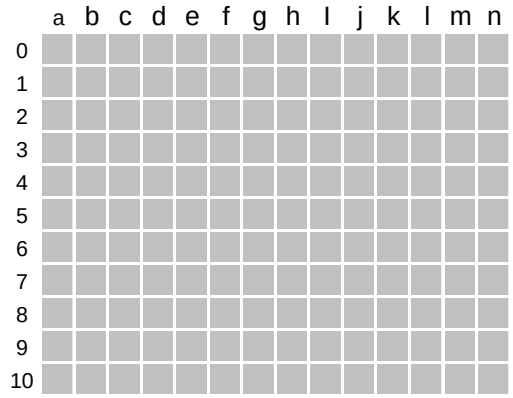


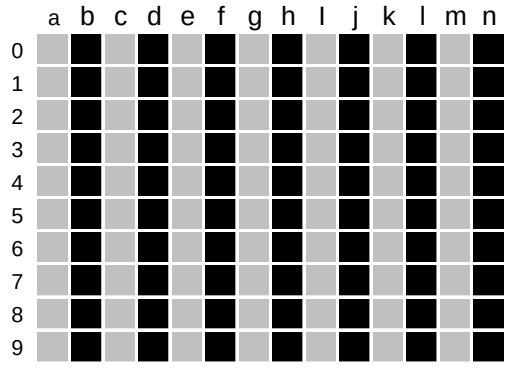
Figure 14: Progressive Scan Read Out

SUB-SAMPLING MODES

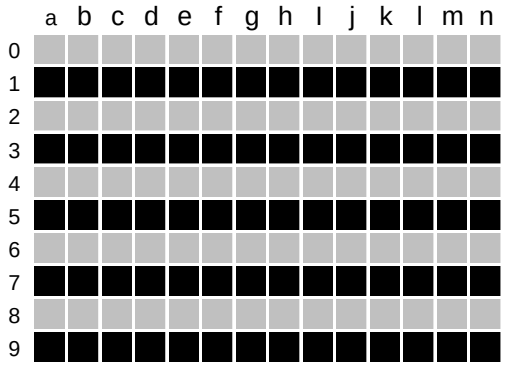
2:1 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the "Display Window" vertically, horizontally, or both, with an aspect ratio of 2:1 as illustrated in Figure 15.

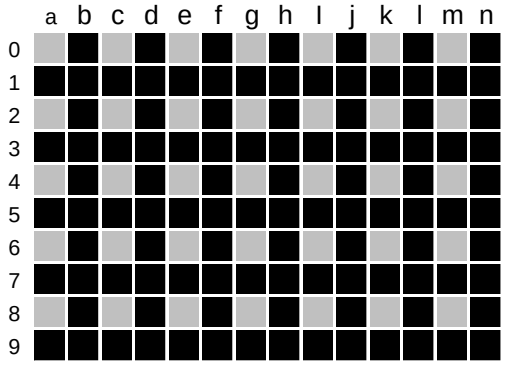
Register Bit	SCANCONFIG		
	Color	*Vsub*	*Hsub*
Vertical	0	1	0
Horizontal	0	0	1
Both	0	1	1



a) Horizontal Sub-Sampling



b) Vertical Sub-Sampling



c) Horizontal and Vertical Sub-Sampling

Read Out Not Read Out

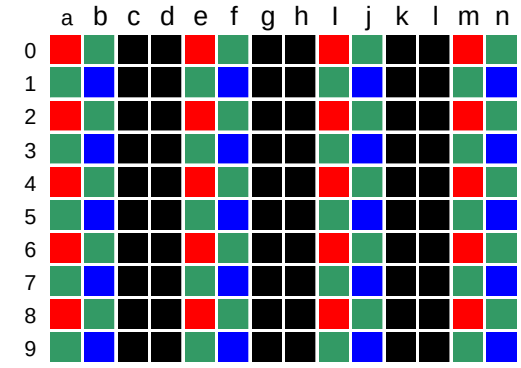
Figure 15: Example of 2:1 Sub-Sampling

The pixel read out will depend on the programmed order as described in the Digital Array Readout section.

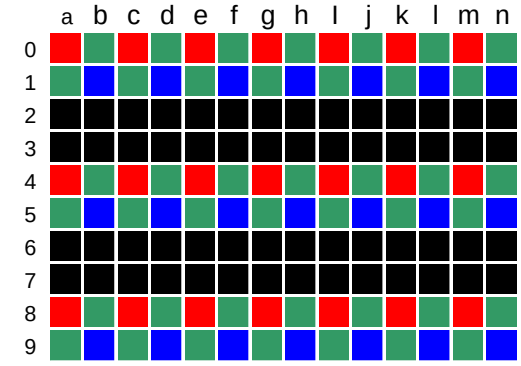
4:2 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the "Display Window" vertically, horizontally, or both, with an aspect ratio of 4:2 as illustrated in Figure 16.

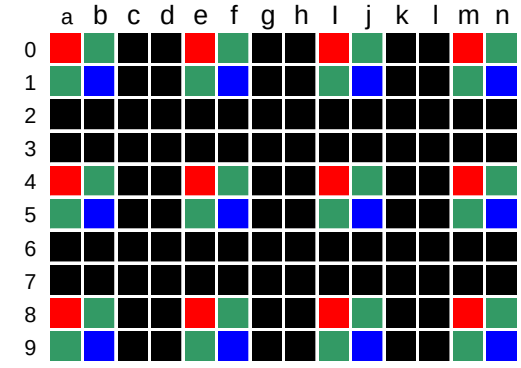
Register Bit	SCANCONFIG		
	Color	*Vsub*	*Hsub*
Vertical	1	1	0
Horizontal	1	0	1
Both	1	1	1



a) Horizontal Sub-Sampling



b) Vertical Sub-Sampling



c) Horizontal and Vertical Sub-Sampling

Green Pixel Red Pixel Blue Pixel Not Read Out

Figure 16: Example of 4:2 Sub-Sampling

The pixel read out will depend on the programmed order as described in the Digital Array Readout section.

FRAME RATE AND EXPOSURE CONTROL

Introduction

The frame time is defined as the time it takes to reset every pixel in the array, integrate the incident light, convert it to digital data and presents the data on the digital video port. This is not a concurrent process and is characterized in a series of events each requiring a certain amount of time as shown in Figure 17.

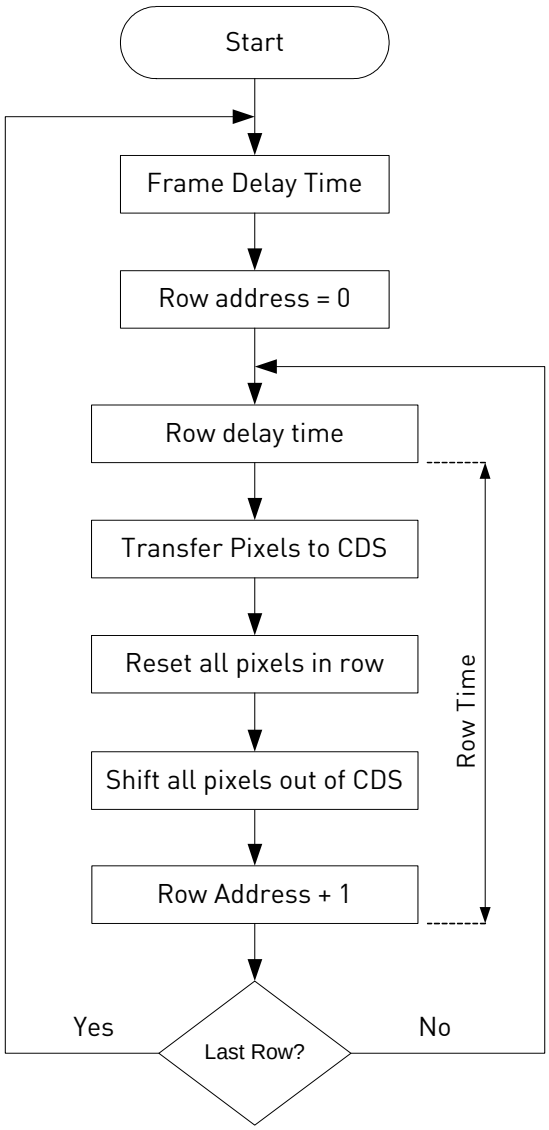


Figure 17: Frame Readout Flow Diagram

The following factors affect frame rate, exposure time, and signal level:

- Frequency of Hclk
- Size of the "Scan Window"
- Sub-sampling mode
- Programmed row delay
- Programmed frame delay

The following factors affect signal level only:

- Analog gain

The following factor affects exposure and signal level:

- Integration time

Analog Gain

Two programmable analog gain amplifiers are provided (PGA and FGA), allowing the level of the in-coming pixels to be gained from unity to a maximum of 13.4x (including PGA and FGA). The PGA has a maximum gain of 2.35x in 8 steps. The FGA gain has a maximum gain of 5.7x in 64 steps. For color sensors the PGA can be used for color balancing in the analog domain.

FGA Gain = 1 + 0.075 x (FGA Register setting)

PGA Gain = 1 + 0.19 x (PGA Register setting)

The analog gain is programmed using the PGA and FGA registers via the I2C compatible serial interface.

Clock Generation

The KAC-00401 contains a clock generation module (Figure 18) that will create three clocks as follows:

- Hclk: the horizontal clock. This is an internal system clock and can be programmed to be the input clock (Mclk) or Mclk divided by 1 or any even number between 2 and 8. All exposure times are in multiples of this clock

  To set the frequency of this clock HclkGen bits in the VCLKGEN register should be programmed.

- Pclk: the pixel clock. This is the external pixel clock that appears at the digital video port. By default Pclk is free running and its frequency is always equal to Hclk (see Figure 18).

Pclk can be programmed to the following modes:

  - o Data Ready Mode, where Pclk clock will go active every time a valid pixel appears

on the data out bus by setting the PixClkPol bit in the VMODE1 register.

- Reverse Polarity Mode, where the polarity of Pclk is negated by programming the PixClkPol bit in the VMODE1 register
- Reverse Active Edge Mode, where the active edge upon which pixel data is clocked out on is reversed. Programming the PixDatEdge bit in the VMODE1 register does this.

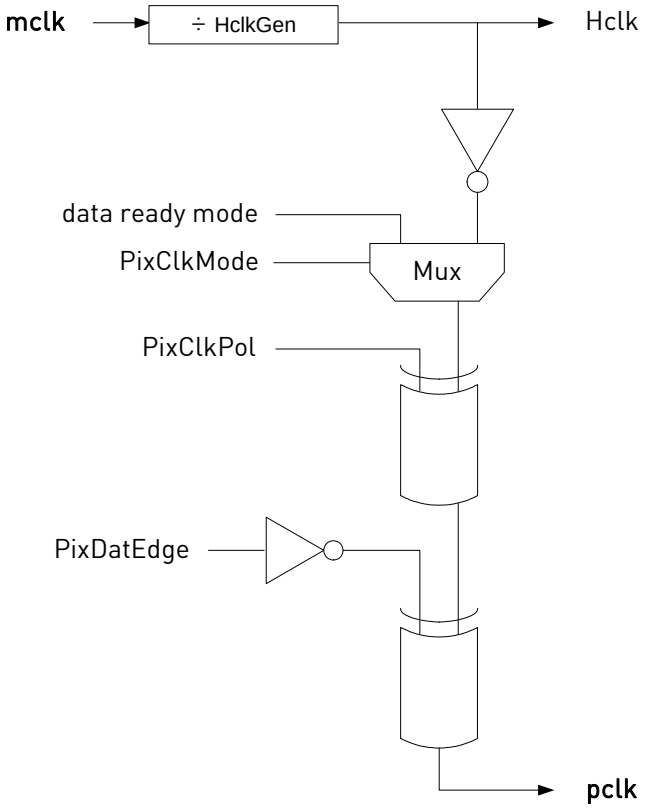


Figure 18: Clock Generation Module

Full Frame Integration

Full frame integration is when each pixel in the array integrates light incident on it for the duration of a frame (see Figure 19).

The number of pixels processed per row is given by:

$$Npix = WEndCol - WStartCol + 1$$

Where:

WEndCol: is the "Scan Window" column end address as programmed in registers WCOLE and WCOLLSB.

WStartCol: is the "Scan Window" column start address as programmed in registers WCOLS and WCOLLSB?

The number of Hclk clock cycles required to process and shift out one row of pixels is given by:

$$RNHclk = Ropcycle + (Npix * MHfactor) + Rdelay$$

Where:

Ropcycle: is a fixed integer value of 206 representing the Row Operation Cycle Time in multiples of Hclk clock cycles. It is the time required to carry out all fixed row operations outlined in Figure 17.

Npix: is the number of pixels in a row.

MHfactor: is 1 when horizontal sub-sampling is disabled and 0.5 when horizontal sub-sampling is enabled.

Rdelay: a programmable value between 0 and 8191 representing the Row Delay Time in multiples of Hclk. This parameter allows the Row Operation cycle time to be extended. The Rdelay value is programmed in the RDELAYH and RDELAYL registers.

The number of rows in the active window is given by:

$$Nrows = (WEndRow - WStartRow + 1) * MVfactor$$

Where:

WEndRow: is the "Scan Window" row end address as programmed in registers WROWE and WROWLSB.

WStartRow: is the "Scan Window" row start address as programmed in registers WROWS and WROWLSB.

MVfactor: is 1 when vertical sub-sampling is disabled and 0.5 when vertical sub-sampling is enabled.

The number of Hclk clocks required to process a full frame is given by:

$$FNHclk = [Nrows + Fdelay + 8] * RNHclk$$

Where:

Nrows: is the number of rows in the "Scan Window".

Fdelay: a programmable value between 0 and 16383 representing the Inter Frame Delay in multiples of RNHclk. This parameter allows the frame time to be extended. (See the Frame Delay High and Frame Delay Low registers.) The Fdelay value is programmed in the FDELAYH and FDELAYL registers.

The frame rate is given by:

Frame Rate = Hclk Period/FNHclk

Partial Frame Integration

In some cases it is desirable to reduce the time during which the pixels in the array are allowed to integrate incident light without changing the frame rate.

This is know as Partial Frame Integration and can be achieved by resetting pixels in a given row ahead of the row being selected for readout as shown in Figure 19. Partial Frame Integration takes affect one frame after the start of the frame after the update bit was set (one frame latency when updating partial frame integration). The number of Hclk clocks required to process a partial frame is given by:

FPHclk = RNHclk * Itime

Where:

RNHclk: the number of Hclk clock cycles required to process and shift out one row of pixels.

Itime: a programmable value between 0 and 32767 representing the number of rows ahead of the current row to be reset. The Itime value is programmed in the ITIMEH and ITIMEL registers.

NOTE: Itime should not be greater than the number of scan rows plus the frame delay. For example if the number of scan rows is equal to 10 and the frame delay is 5 then the maximum Itime would be 15 (which would be equivalent to full frame integration). If Itime is set to 16 then integration time will wrap around and will behave as if Itime was equal to 1.

Partial Line Integration

In some cases it may be desirable to reduce the time during which the pixels in the array are allowed to integrate the incident light below the minimum of one row allowed by the partial frame integration. This feature is called partial line integration, and is achieved by reducing the time between reset of a row and the readout of that row.

In normal operational mode, without applying the partial line reset mechanism, the reset for partial frame integration and the resets that generate the breakpoints in the HDR mode all occur within the horizontal blanking period, one after another.

Programming a partial line integration register (also a partial line slope in HDR mode) to a value other than zero will delay that reset by shifting it into the CDS shift out period, towards the Row readout by the programmed value, thus reducing the integration time.

As the value increases in partial line integration register the amount of time the pixel integrates light is reduced.

For more information please refer to the KAC-00401 piecewise linear application note.

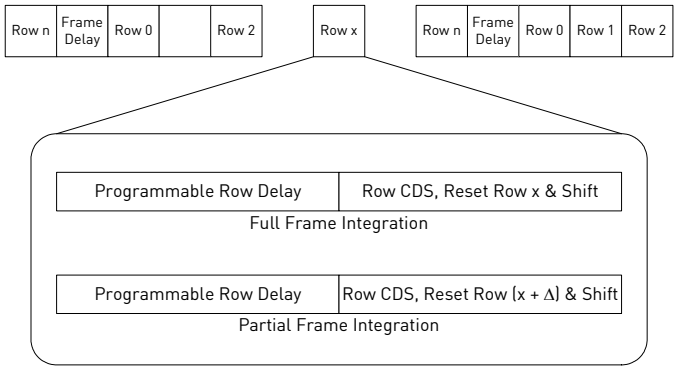


Figure 19: Partial and Full Frame Integration

MODIFICATION OF LINEAR RESPONSE CURVE

The electro-optic transfer curve of the pixel array is linear. While a linear response is satisfactory for capturing images containing similar brightness levels, it is not always satisfactory for capturing images with a large variation of brightness levels.

For a fixed integration time, pixels capturing bright areas of a scene will saturate much faster than pixels

capturing darker regions. When there is a large variation in the light intensities between the dark and light regions it is not possible to simultaneously capture the detail in the both regions.

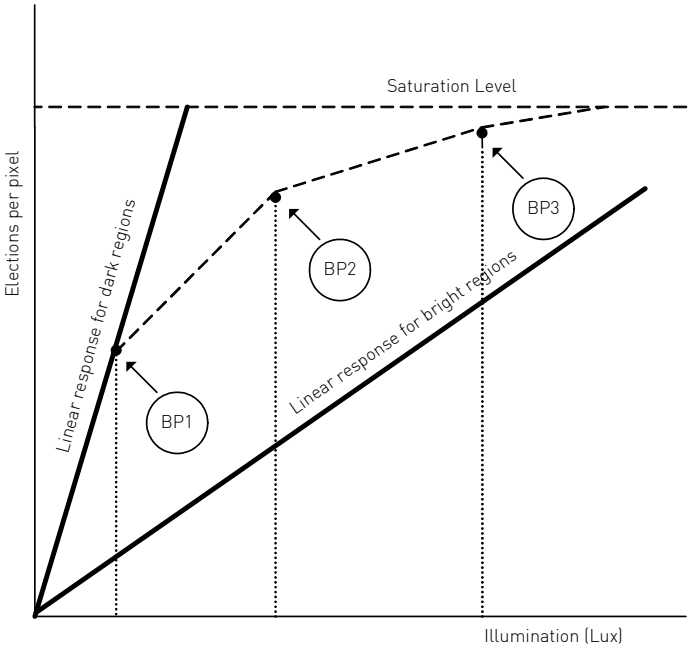


Figure 20: Linear and HDR Transfer Responses

Since the response of the human eye to light is non-linear, a non-linear response such as that shown with the dashed curve in Figure 20 would allow the detail in both the light and dark regions of the image to be captured and seen.

The timing and control circuit built into the KAC-00401 allows the linear response of the electro-optic response to be modified into a piece-wise linear response (approximate gamma).

The KAC-00401 integrated timing and control circuit allows up to three breakpoints to be programmed such that a piecewise linear response can be achieved as shown in Figure 21.

Three registers are provided to define each breakpoint. The Level register and Slope register.

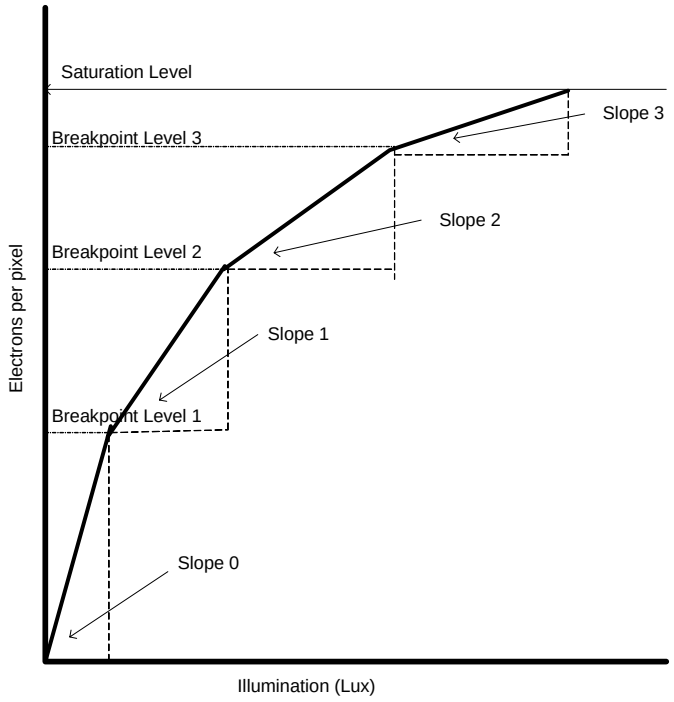


Figure 21: Breakpoint Programming

The sensitivity of the first branch, (slope 0 in Figure 21), is determined by the time settings and the image sensor characteristics. The sensitivity (slope), of the other branches is determined by the value programmed in the Slope registers. The levels at which the piecewise linear curve switches from one slope to another are determined by the values programmed in the Level registers.

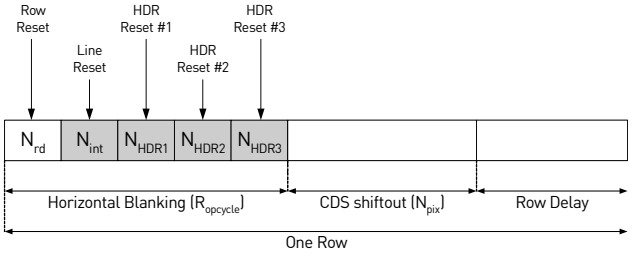
Use the BP3LEV, BP2LEV, and BP1LEV registers to program the level of each breakpoint and BP3SLOPEH, BP3SLOPEL, BP2SLOPEH, BP2SLOPEL, BP1SLOPEH, BP1SLOPEL to program the slope of each breakpoint, (refer to the HDR mode applications note).

The slope of every breakpoint can be less than one line of integration.

In some cases it may be desirable to reduce the time during which pixels in the array are allowed to integrate below the minimum of one row allowed by the partial frame integration.

This feature is called partial line integration, and is achieved by reducing the time between the reset of a row and the readout of that row:

Normal Operation



Partial Line Integration

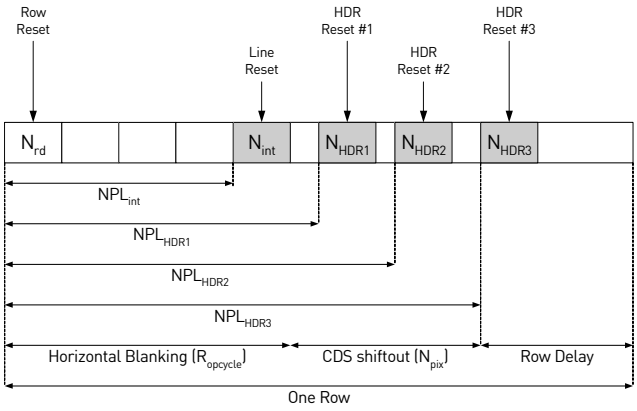


Figure 22: Partial Line Integration and HDR Reset

For more information please refer to the KAC-00401 piecewise linear application note.

SNAPSHOT MODE

Introduction

Two dedicated pins are provided on the KAC-00401, **snapshot** and **extsync** allowing the sensor to be externally controlled to capture a single image. The **snapshot** input pin is used to trigger a snapshot, while the **extsync** output pin is used to synchronize a light source, strobe or mechanical shutter. Note that partial frame integration is not possible in snapshot mode.

Taking a Snapshot

By default the sensor will operate in the **VIDEO** state (see Figure 23). To take a snapshot, the snapshot mode must be enabled by setting the *SnapEnable* bit in the SNAPSHOTMODE register to logic 1. This will cause the sensor to enter the **FREEZE** state at the end of the current frame. In the **FREEZE** state the sensor is idle. The sensor will leave the **FREEZE** state and return to **VIDEO** state when the snapshot mode is disabled (*SnapEnable* bit in the SNAPSHOTMODE register set to logic 0).

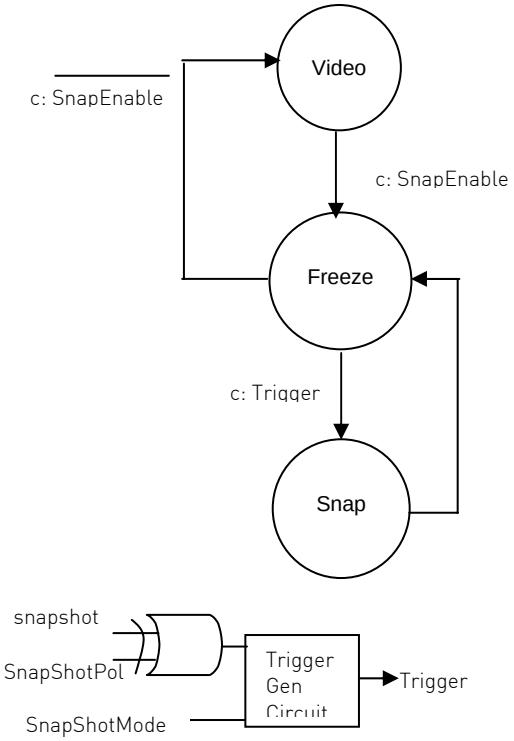


Figure 23: Snapshot Mode

Alternatively when an active snapshot signal is applied to the snapshot input pin an internal trigger signal, *TRIGGER*, is generated as shown in Figure 23. The trigger generation circuit will create two types of TRIGGER as follows:

- **Pulse Trigger** (*SnapshotMode* bit of the SNAPSHOTMODE register is cleared). In this

mode (the default) a single TRIGGER pulse will be generated.

- **Level Trigger** (*SnapshotMode* bit of the SNAPSHOTMODE register is set). In this mode the TRIGGER will remain high as long as the active level is held on the **snapshot** pin.

When a TRIGGER is generated the sensor will enter the SNAP state as shown in Figure 23.

The SNAP State in External Shutter Mode

To take a snapshot in external shutter mode, the ShutterMode bit of the SNAPSHOTMODE register must be set.

In this mode three consecutive operations will be carried out in the SNAP state as follows (see Figure 24):

- **Array Reset**, during which the **extsync** pin is kept inactive and the array is reset one row at a time. The number of times the array is reset is programmable from 1-8 frames (see the SsFrames bits in the SNAPSHOTMODE register).
- **Image Capture**, the **extsync** pin will activate. The width of the extsync signal can be programmed with the snapshot integration time registers, SNAPITH AND SNAPITL. The registers can be programmed with values from 0 to 32767 lines.
- **Array Read Out**, the third and final operation reads the image data out one row at a time after extsync goes inactive.

The Snapshot State in Normal Mode (default)

To take a snapshot in normal mode, the *ShutterMode* bit of the SNAPSHOTMODE register must be cleared. In this case the following consecutive operations will be carried out in the **SNAP** state (see Figure 24):

- **Array Reset**, during which the **extsync** pin is kept inactive and the array is reset one row at a time. The number of times the array is reset is programmable from 1-8 frames (see the SsFrames bits in the SNAPSHOTMODE register).
- **Image Capture**, the **extsync** pin will activate for the duration of the capture time. The length of the capture time can be programmed using the Frame delay and Row delay registers.
- **Array Read Out**, the third and final operation reads the image data out one row at a time. During this operation the extsync pin remains active.

Return to FREEZE State

When read out is complete the sensor will return to the **FREEZE** state.

Return to VIDEO State

If the snapshot mode is disabled before readout is complete (*SnapEnable* bit in the SNAPSHOTMODE register is set to a logic 0), then the sensor will return to the **VIDEO** state at the end of readout.

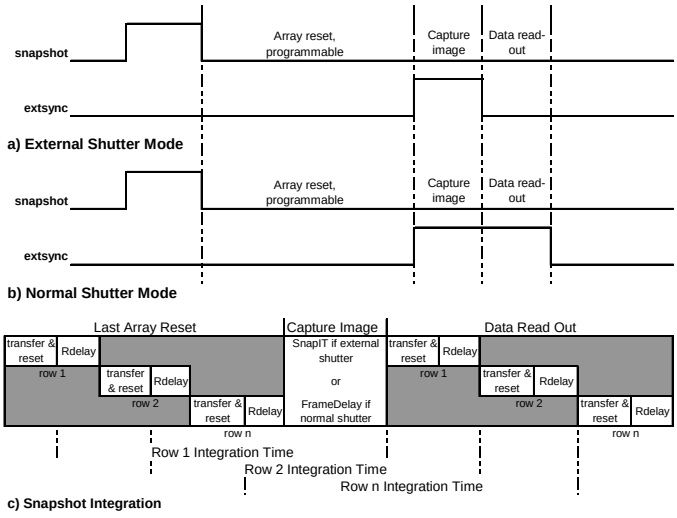


Figure 24: Snapshot Sequences

BLACK LEVEL AND OFFSET ADJUSTMENT

The KAC-00401 allows for both automatic and manual black level adjustment.

Manual Black Level and Offset Adjustment

To manually adjust the black level and offset one should use the BLACKCONFIG1 register. Set both bit[2] (ManFine) and bit[1] (ManCoarse) to a one. The manual black level and offset adjustment consists of a coarse adjustment in the analog domain and the fine adjustment in the digital domain. One can then use the Manual Level Black DAC 0-3 (registers 0x34h - 0x37h) for coarse control and Manual Level Digital Offset high and low (registers 0x39h - 0x3Fh).

Figure 25 shows the written value, the value on read back and the DAC code. The format for the coarse DAC value is two's complement with the sign inverted.

The format for the fine DAC is standard two's complement.

WRITE REG	READ REG	DAC CODE	WRITE REG	READ REG	DAC CODE
00	00	0	20	E1	31
01	01	-1	21	E1	31
02	02	-2	22	E2	30
03	03	-3	23	E3	29
04	04	-4	24	E4	28
05	05	-5	25	E5	27
06	06	-6	26	E6	26
07	07	-7	27	E7	25
08	08	-8	28	E8	24
09	09	-9	29	E9	23
0A	0A	-10	2A	EA	22
0B	0B	-11	2B	EB	21
0C	0C	-12	2C	EC	20
0D	0D	-13	2D	ED	19
0E	0E	-14	2E	EE	18
0F	0F	-15	2F	EF	17
10	10	-16	30	F0	16
11	11	-17	31	F1	15
12	12	-18	32	F2	14
13	13	-19	33	F3	13
14	14	-20	34	F4	12
15	15	-21	35	F5	11
16	16	-22	36	F6	10
17	17	-23	37	F7	9
18	18	-24	38	F8	8
19	19	-25	39	F9	7
1A	1A	-26	3A	FA	6
1B	1B	-27	3B	FB	5
1C	1C	-28	3C	FC	4
1D	1D	-29	3D	FD	3
1E	1E	-30	3E	FE	2
1F	1F	-31	3F	FF	1

Figure 25: Manual DAC Values

Automatic Black Level and Offset Adjustment

Clearing the ManFine and ManCoarse bits in the BLKLEVCONFIG1 register enables automatic black level and offset adjustment mode. The automatic black level adjustment is a two-step process. There is a coarse control, which is done via a feedback loop from the output of the ADC back to the summing node before the Amp as shown in Figure 26. The fine calibration is done purely in the digital domain.

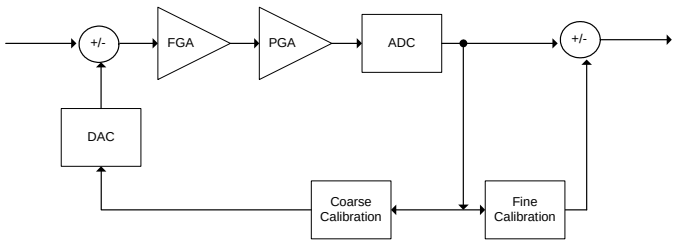


Figure 26: Digital Black Level and Offset Adjustment Loop

Figure 26 illustrates the automatic black level and offset compensation circuits contained within the sensor. For every frame, the digitized values of the black pixels are acquired and fed to the compensation level calculator circuit. The circuit is a digital first order exponential averaging filter. It calculates the compensation level that is required to ensure that for pixels that are optically black, the black level at the output of the ADC is equal to the desired black level. The desired black level target can be programmed by using the BLKTARGETL and BLKTARGETH registers.

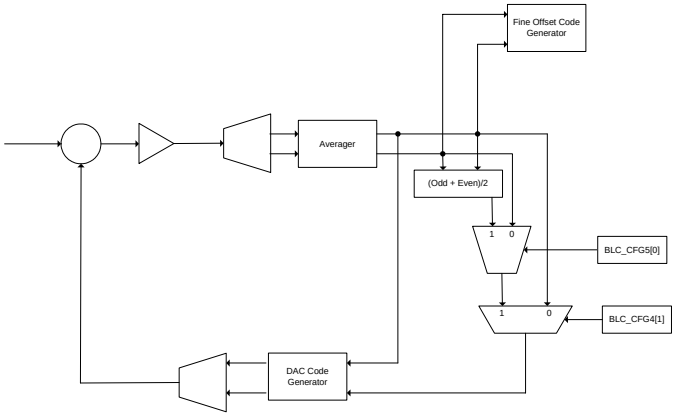


Figure 27: Digital Black Level and Offset Adjustment Loop – Monochrome Sensor

In monochrome mode two separate black level values are calculated for the odd and even columns. Black level compensation can be done in three ways: separate odd and even black level values can be applied, the odd value can be applied to both the odd and even column, and

finally the odd value can be applied to the odd column and an average of the odd and even column can be applied to the even column. Figure 27 illustrates these options.

By applying separate black level values for odd and even columns one can compensate for odd even column fixed pattern noise. Odd/Even correction is done by setting bit 0 of BLC_CFG5 to a 0 and setting bit 1 of BLC_CFG4 to a 1.

To have the odd column black level value used for both odd and even columns set BLC_CFG4 bit 1 to a 0.

Finally to apply the average of the odd and even columns to the even column black level value set BLC_CFG5 bit 0 to a 1 and set BLC_CFG4 bit 1 to a 1.

In color mode there is only one way to apply the black level correction (Set BLC_CFG5 register to 0x06h). Figure 28 illustrates how to read out the various black level values.

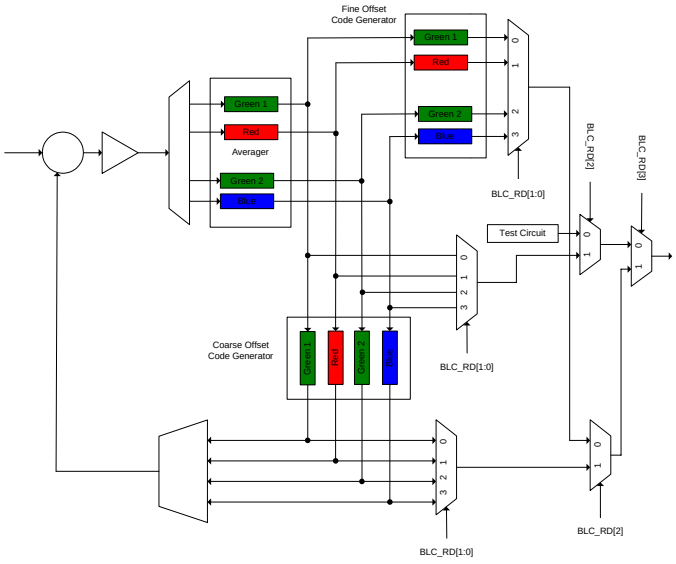


Figure 28: Black Level Compensation Read Back

The black level control loop not only controls the black level of the pixels in the sensor array, but also controls the offset of the PGAs and ADC in the system.

The speed at which the coarse black level adjustment converges is controlled with the alpha[3:0] bits in the BLKLEVCONFIG2 register. Small values ensure faster convergence but with more overshoot. Higher values reduce the noise in the calculated compensation value.

The speed at which the fine black level adjustment converges is controlled with the beta[3:0] bits in the BLKLEVCONFIG3 register. Small values ensure a fast convergence. High values reduce the noise in the calculated compensation level.

The optimal setting of both the alpha and beta parameters is the result of a compromise between convergence speed after power up and image quality.

Average Black Level Registers

The non-gained/compensated average of the middle 8 black pixels is stored in the Average Black Level Registers (AVRBLKH and AVRBLKL). These registers are updated every 64 frames. Various values in the black level compensation circuit can be read back based on values set in bits[3:0] of the BLC_READ register (see Figure 28).

Bits 3:0	Data Width	Data Type	Data available in AVRBLKH and AVRBLKL
00xx	14	Signed	Reserved
0100	14	Signed	Green on red row statistics from Fine offset calibration
0101	14	Signed	Red statistics from Fine Offset calibration
0110	14	Signed	Green on blue row statistics from Fine offset calibration
0111	14	Signed	Blue statistics from Fine Offset calibration
1000	6	Signed	Grean on red row Course DAC
1001	6	Signed	Red Course DAC
1010	6	Signed	Grean on blue row Course DAC
1011	6	Signed	Blue Course DAC
1100	14	Signed	Green on red row fine calibration value (use bottom 10 bits)
1101	14	Signed	Red fine calibration value (use bottom 10 bits)
1110	14	Signed	Green on blue row fine calibration value (use bottom 10 bits)
1111	14	Signed	Red fine calibration value (use bottom 10 bits)

SYSTEM MANAGEMENT

System Reset

Upon power up an on-chip power on reset block will ensure that the sensor is initialized to its reset state, after power up the sensor can be reset by asserting logic 0 on the Resetb pin. NOTE: The Resetb pin should only be held low for 3-5 Mclk cycles.

Power Up and Power Down

The power up sequence for the KAC-00401 is as follows:

1. Power up V_{IO} Supply.
2. Power up $V_{digital}$ Supply
3. Power up V_{analog} Supply
4. Apply Mclk

If this procedure is not possible within the system set up then follow the procedure in Application Note 3: Power Up/Down Sequence.

For power down of the KAC-00401 use the following sequence.

1. Power down sensor using register writes.
2. Remove Mclk
3. Power down V_{analog} Supply
4. Power down $V_{digital}$ Supply
5. Power down V_{IO} Supply.

Or follow the power down procedure in Application Note 3: Power Up/Down Sequence.

The sensor can be put into power down mode by writing a 1 to the PwDn bit in the MODE&CTRL register.

To power up the sensor by writing a 0 to the PwDn bit in the MODE&CTRL register.

BAD PIXEL DETECTION AND CORRECTION

The KAC-00401 has a built-in bad pixel detection and correction circuit that operates on the fly. Bad pixel correction is enabled at reset. Disable Bad pixel correction by writing a 1 to bit 0 of the BPC_CFG (0x59h) register.

In monochrome mode the bad pixel correction circuit uses the following algorithm:

Looking at a group of 3x3 pixels the pixels are ranked from lowest to highest value (R0(lowest), R1, R2,..., R6, R7, R8(highest)). Replace the center pixel with R2 if the center pixel is ranked R0 or R1 and smaller than 2 x R2 – Gl x (R6-R2). Replace the center pixel with R6 if the center pixel is ranked R7 or R8 and is larger than 2 x R6 + Gh x (R6 – R2). Gl and Gh are programmable values between 0 and 3. Use the GAMMA_H register (0x60h) to program Gh and use the GAMMA_L register (0x61h) to program Gl.

In color mode the bad pixel correction circuit uses the following algorithm:

For the red and blue pixels the algorithm uses only the adjacent pixels in the current row. If the center pixel is greater than any of the adjacent pixels and if the center pixel minus the maximum value of the two adjacent pixels is bigger than the threshold (Register 0x62, DC_RB_TH) then the center pixel is replaced with the larger of the two adjacent pixels.

If the center pixel is smaller than any of the adjacent pixels and the adjacent pixel minus the center pixel is greater than the threshold (Register 0x62, DC_RB_TH) then the center pixel is replaced with the smaller of the two adjacent pixels.

For the green pixels the algorithm uses the green pixels in a 3-row by 5-column array to determine whether or not the pixel is bad. If the center pixel is greater than any of the surrounding pixels and the center pixel minus the maximum vale of the 6 surrounding pixels is greater than the threshold (Register 0x63, DC_G_TH) then the center pixel is replaced with the largest of the six surrounding pixel values.

If the center pixel is smaller than any of the surrounding pixels and the minimum value of the six surrounding pixels minus the center pixel is greater than the threshold (Register 0x63, DC_G_TH) then the center pixel is replaced with the smallest of the six surrounding pixel values.

SERIAL BUS

The serial bus interface consists of the Sda (serial data), Sclk (serial clock) and Sadr (device address select) pins. The KAC-00401 serial bus can only operate as a slave.

Start/Stop Condition

The serial bus will recognize logic 1 to a logic 0 transition on the Sda pin while Sclk pin is at a logic 1 as the start condition. A logic 0 to logic 1 transition on the Sda pin while the Sclk pin is at a logic 1 is interrupted as the stop condition as shown in Figure 29. Note that the register is still written too even if the stop bit is not executed correctly.

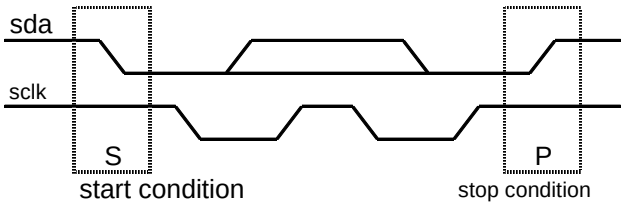


Figure 29: Start/Stop Condition

Device Address

The serial bus Device Address of the KAC-00401 is set by default to 1010101 (0x55h) when Sadr is tied low and by default to 0110011 (0x33h) when Sadr is tied high. The value for Sadr is set at power up. The device address can be changed by writing to the I2CdevAddr parameter in the I2CMODE Register.

Acknowledgement

The KAC-00401 will hold the value of the Sda pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on Sclk as shown in Figure 30.

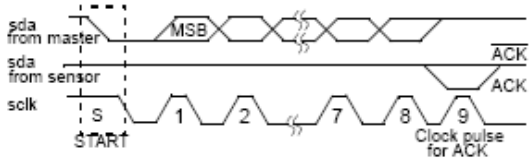


Figure 30: Acknowledge

Data Valid

The master must ensure that data is stable during the logic 1 state of the Sclk pin. All transitions on the Sda pin can only occur when the logic level on the Sclk pin is "0" as shown in Figure 31.

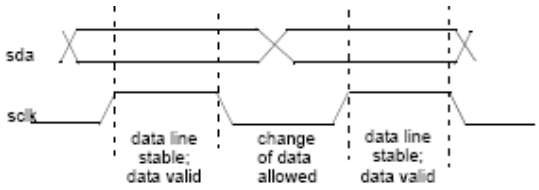


Figure 31: Data Validity

Byte Format

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an Acknowledge. The most significant bit of the byte is always transmitted first. See Figure 32.

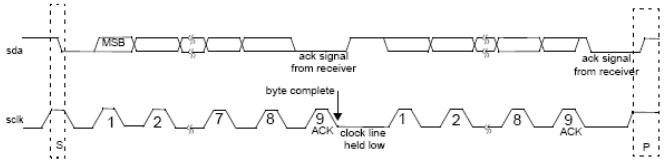


Figure 32: Serial Bus Byte Format

Write Operation

The master initializes a write operation with a Start Condition followed by the sensor's Device Address and Write bit. When the master receives an Acknowledge from the sensor it can transmit the 8-bit internal register address. The sensor will respond with a second Acknowledge. The master must then issue a new Start Condition followed by the sensor's Device Address and Read bit. The sensor will respond with a second Acknowledge signaling the master to transmit 8 data bits. A third Acknowledge is issued by the sensor when the data has been successfully received.

The write operation is completed when the master asserts a Stop Condition or a second Start Condition. See Figure 33.

Figure 33: Serial Write Operation

Read Operation

The master initiates a read operation with a Start Condition followed by the sensor's Device Address and Write bit. When the master receives an Acknowledge from the sensor it can transmit the internal Register

Address byte. The sensor will respond with a second Acknowledge. The master must then issue a new Start Condition followed by the sensor's Device Address and Read bit. The sensor will respond with an Acknowledge followed by the Read Data byte.

The read operation is completed when the master asserts a Not Acknowledge followed by a Stop Condition or a second Start Condition. See Figure 34.

Figure 34: Serial Bus Read Operation

DIGITAL VIDEO PORT

The captured image is placed onto a flexible 12-bit digital port as shown in Figure 9. The digital video port consists of programmable synchronization signals (Hsync, Vsync, Pclk).

By default the synchronization signals are configured to operate in slave mode. They can be programmed to operate in master mode.

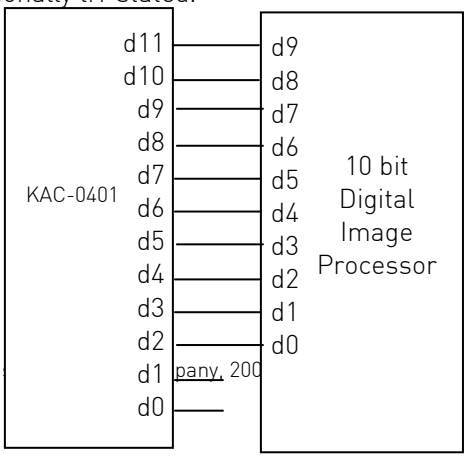
The following sections are a detailed description of the timing and programming modes of the digital video port.

Pixel data is output on a 12-bit digital video bus. This bus can be tri-stated by applying logic 1 to the OEb pin.

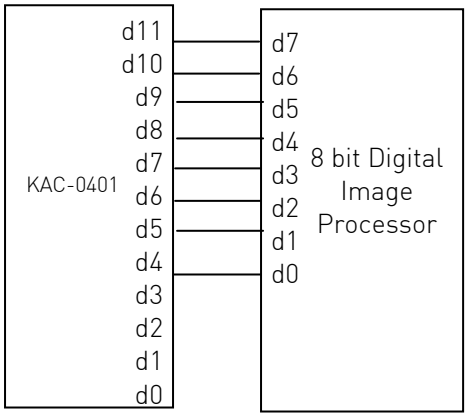
Digital Video Data Out Bus (d[11:0])

A programmable matrix switch (see VMODE0 register) is provided to map the output of the internal pixel framer to the pins of the digital video bus.

This feature allows a programmable digital gain to be implemented when connecting the sensor to 8 or 10 bit digital video processing systems as illustrated in Figure 35. The unused bits on the digital video bus can be optionally tri-stated.



a) KAC-0400 Connected to a 10-bit Digital Image Processor



b) KAC-0401 Connected to an 8-bit Digital Image Processor

Figure 35: Example of connection to 10/8 bit systems

Synchronization Signals in Master Mode

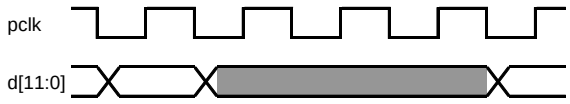
By default the sensor's digital video port's synchronization signals are configured to operate in master mode (MasterMode bit in the MODE&CTRL register set to logic 0). In master mode the integrated timing and control block controls the flow of data onto the 12-bit digital port, three synchronization outputs are provided:

- Pclk – is the pixel clock output pin
- Hsync – is the horizontal synchronization output signal
- Vsync – is the vertical synchronization output signal

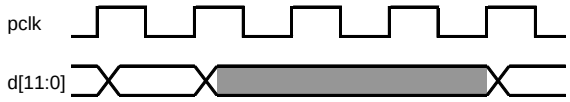
Pixel Clock Output Pin

The pixel clock output pin, **Pclk**, is provided to act as a synchronization reference for the pixel data appearing at the digital video output bus pins **d[11:0]**. This pin can be programmed to operate in two modes.

- In free running mode, (set *PixClkMode* bit in the VMODE1 register to logic 0) the pixel clock output pin, **Pclk**, is always running with a fixed period. Pixel data appearing on the digital video bus **d[11:0]** are synchronized to a specified active edge of the clock as shown in Figure 36.



a) Pclk active edge negative

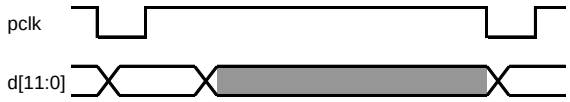


b) Pclk active edge positive (default)

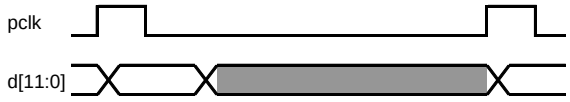
Invalid pixel data

Figure 36: Pclk in Free Running Mode

- In data ready mode, (set *PixClkMode* bit in the VMODE1 register to a logic 1), the pixel clock output pin **Pclk** will produce a pulse with a specified level every time valid pixel data appears on the digital video bus **d[11:0]** as shown in Figure 37.



a). Pclk active edge negative



b). Pclk active edge

Invalid pixel data

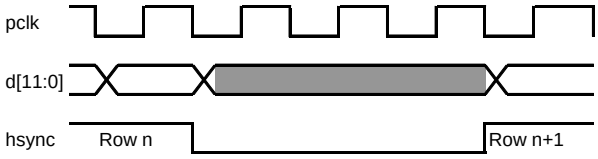
Figure 37: Pclk in Data Ready Mode

By default the pixel clock is in free running mode active low (pixel data changes on the positive edge of the clock) with a period equal to the internal *Hclk*. The active edge of the clock can be programmed such that pixel data changes on the positive or negative edge of the clock (see the *PixClkPol* bit in the VMODE1 register).

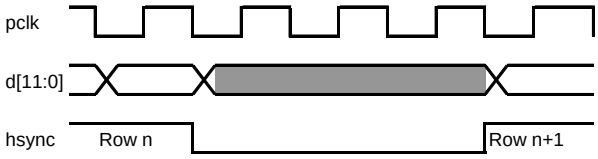
Horizontal Synchronization Output Pin (Hsync)

The horizontal synchronization output pin, Hsync, is used as an indicator for row data. The Hsync output pin can be programmed to operate in two modes as follows:

- Level Mode, (set the *HsyncMode* bit of the VMODE1 register to a logic 0), should be used when the pixel clock, **Pclk**, is programmed to operate in free running mode. In level mode the **Hsync** output pin will go to the specified level (high or low depending on the logic level of the VsyncPol bit in the VMODE1 register) at the start of each row and remain at that level until the last pixel of that row is read out on **d[11:0]** as shown in Figure 38. The **Hsync** level is always synchronized to the active edge of **Pclk**.



a). Hsync programmed to be active high (default)

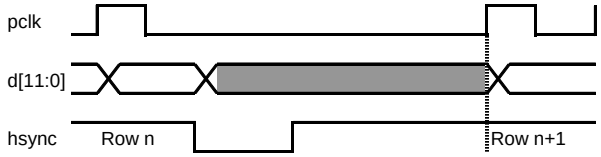


b). Hsync – programmed to be active low

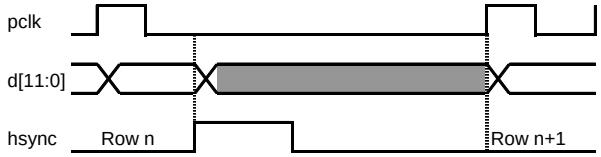
Figure 38: Hsync in Level Mode

- Pulse mode, (set the *HsyncMode* bit of the VMODE1 register to a logic 1), should be used when the pixel clock, **Pclk**, is programmed to operate in data ready mode. In pulse mode the **Hsync** output pin will produce a pulse at the end of each row. The width of the pulse will be a minimum of four **Pclk** cycles and its polarity can be programmed (see the VsyncPol bit in the VMODE1 register) as shown in Figure 39. The

Hsync level is always synchronized to the active edge of Pclk.



a). Hsync programmed to be active high



b). Hsync programmed to be active low

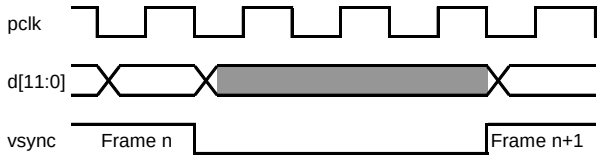
Figure 39: Hsync in Pulse Mode

By default the first pixel data at the beginning of each row is placed on the digital video bus as soon as Hsync is activated. It is possible to program up to 15 dummy pixels to be readout at the beginning of each row before the real pixel data is readout. This feature is supported for both level and pulse mode. Use the *HsyncAdjust* parameter in the VMODE0 register to specify the required number of dummy pixels.

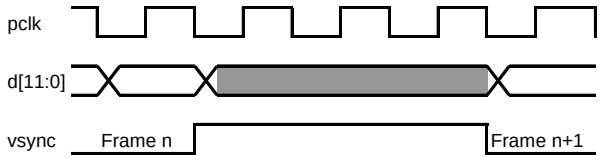
Vertical Synchronization Output Pin (Vsync)

The vertical synchronization output pin, Vsync, is used as an indicator for pixel data within a frame. The Vsync output pin can be programmed to operate in two modes as follows:

- Level mode, (set HsyncMode bit in the VMODE1 register to a logic 0), should be used when pixel clock, pclk, is programmed to operate in free running mode. In level mode the Vsync output pin will go to a specified level (high or low depending on the logic level of the VsyncPol bit in the VMODE1 register) at the start of each frame and remain at that level until the last pixel of that row in the frame is placed on d[11:0] as shown in Figure 40. The Hsync level is always synchronized to the active edge of Pclk.



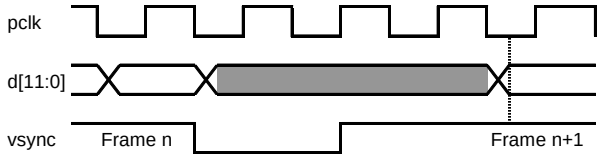
a). Vsync programmed to be active high



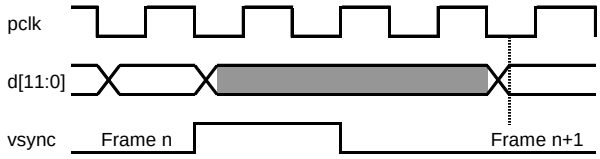
b). Vsync programmed to be active low

Figure 40: Vsync in Level Mode

- Pulse mode, (set VsyncMode bit in the VMODE1 register to a logic 1), should be used when the pixel clock, Pclk, is programmed to operate in data ready mode. In pulse mode the Vsync output pin will produce a pulse at the end of each frame. The width of the pulse will be a minimum of four Hclk cycles and its polarity can be programmed (see VsyncPol bit in the VMODE1 register) as shown in Figure 41. The Vsync pulse is always synchronized to the active edge of Pclk.

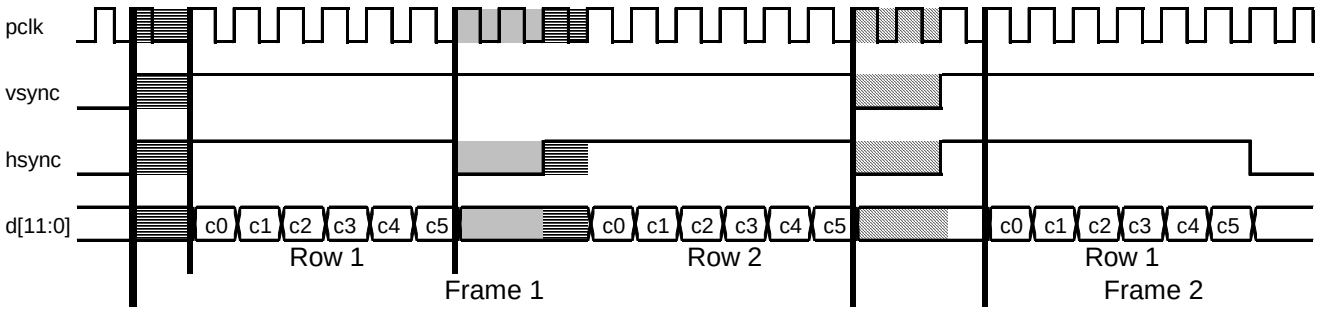


a). Vsync programmed to be active high



b). Vsync programmed to be active low

Figure 41: Vsync in Pulse Mode

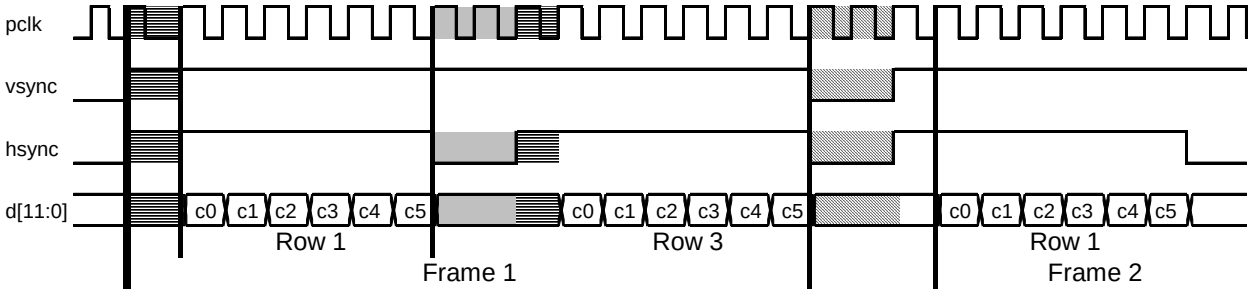


Programmable row delay

Programmable inter-frame delay

Programmable Hsync to 1st valid pixel delay

Figure 42: Example of Digital Video Port Timing in Progressive Scan Mode

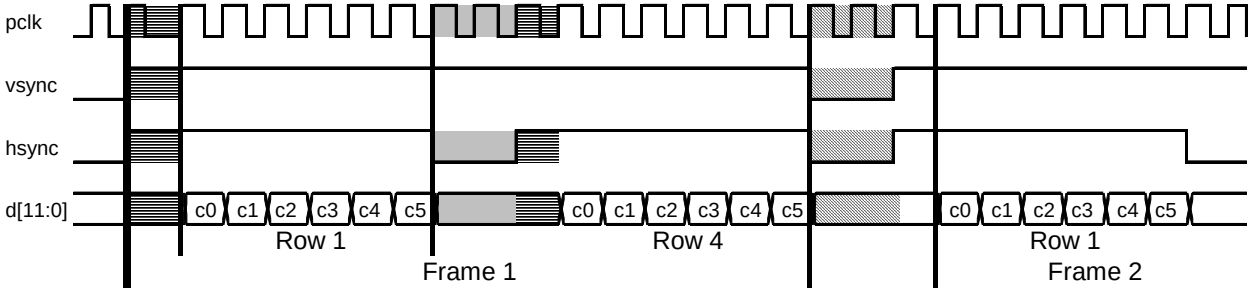


Programmable row delay

Programmable inter-frame delay

Programmable Hsync to 1st valid pixel delay

Figure 43: Example of Digital Video Port Timing in 2:1 Sub-sampling Mode



Programmable row delay

Programmable inter-frame delay

Programmable Hsync to 1st valid pixel delay

Figure 44: Example of Digital Video Port Timing in 4:2 Sub-sampling Mode

Synchronization Signals in Slave Mode

Slave mode can be used to synchronize two or more sensors. The sensor's digital video port's synchronization signals can be programmed to operate in slave mode. In slave mode the integrated timing and control block will only start frame and row processing upon the receipt of triggers from an external source.

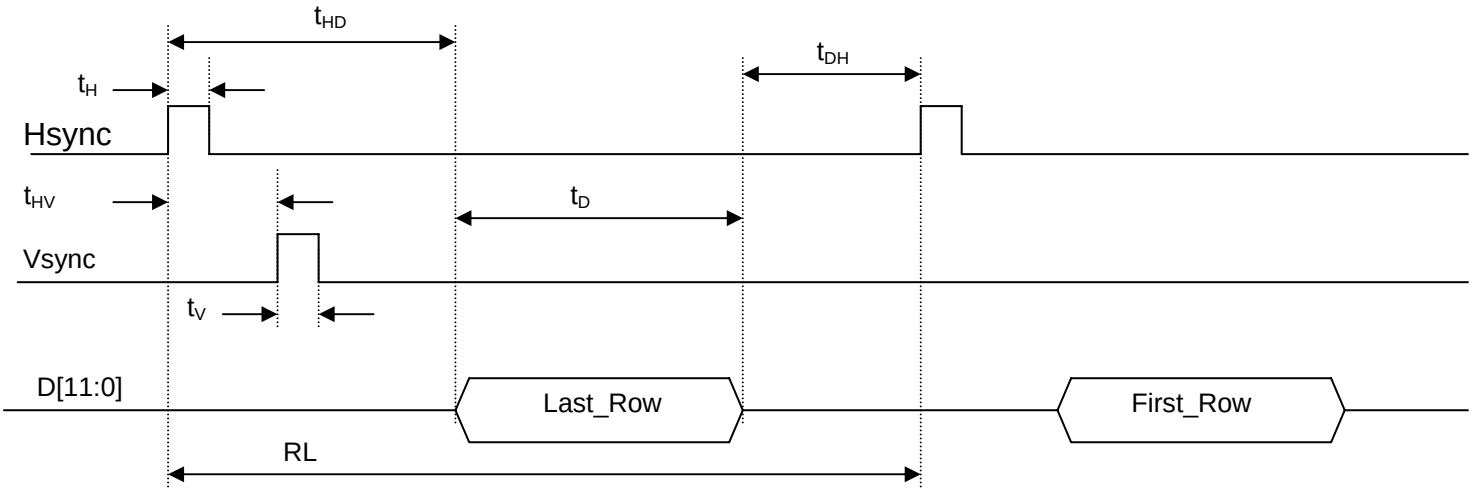
To enable slave mode on the KAC-00401, set register MODECTRL (address 0x03) bit 5 (this bit is cleared by default). This value is not double buffered or frame buffered. Once this bit is set, the device will operate in slave mode, and is triggered by HSYNC and VSYNC. To run the device in slave mode, the following signals are needed:

Hsync: horizontal trigger pin

Vsync: vertical trigger pin

Mclk: master clock, divided by the value of the HCLKGEN register (0x02).

To trigger a start of frame, the signals should be asserted as shown below:



where:

t_H : width of horizontal pulse
t_{HV}: delay between assertion of Hsync and assertion of Vsync
t_V: width of vertical trigger pulse
t_{HD}: delay before data appears on the video outputs
t_D: length of the output data
t_{DH}: time from end of last pixel of the row until the start of the next trigger

t_H: should be asserted high for at least 2 Pclk periods. Triggering of the horizontal circuitry is achieved by a low to high edge on the DMclk signal with Hsync high. Hsync has to be de-asserted low at least two Pclk periods before the end of a row.

RL (row length): RL = 420 + (x2 – x1 + 1) Pclk periods

Where
x2 = scan window column end value
x1 = scan window column start value

NOTE: The "assertion value" of Hsync and Vsync is high, and is not programmable.

t_{HV}: Vsync must be triggered within 2 Pclk cycles of asserting Hsync for the last row if one wants the first row of the next frame to start at the proper time. In this case, the first row of the new frame will follow after the present row is clocked out, as is shown in the diagram.
NOTE: If t_{HV} is violated, array addressing will restart two rows later.

t_V : minimum pulse with of 1 Pclk cycle and a maximum of (RL – 4) * Pclk

Triggering of the next frame is achieved by a low to high edge on the Pclk signal with Vsync high

t_{HD}: This value is given by t_{HD} = 228 + x1 [Pclk periods]

Where
x1 = display window column start value

t_D = [x2 – x1 + 1]* [Pclk periods]
Where
x1 = display window column start value
x2 = display window column end value

Label	Descriptions	Min	Typ	Max
t_H	Pulse width of row trigger	2 * Pclk		[228+x0]*Pclk + [x2-x1 + 1]* Pclk – 2*Pclk
t_{HD}	First pixel out after rising edge of row trigger[1]	[228 + x0]*Pclk		[228 + x0]*Pclk
RL	Minimum time between row triggers[2]	[420 + (x2 – x1 + 1] *Pclk		
t_{HV}	Time to assert next frame trigger after last row trigger in current frame	0		2*Pclk
t_V	Pulse width of Frame trigger	2 *mclk		(RL – 4) * Pclk

Where
x1 = display window column start value
x2 = display window column end value

MEMORY MAP

Address	Register	Reset Value	Description	Double Buffered
00h	DEVID	18h	Device ID Register	No
01h	REV	C0h	Revision Register	No
02h	VCLKGEN	01h	Clock Generation Register	No
03h	MODE&CTRL	0Dh	Mode and Control Register	No
04h - 07h		00h	Reserved	No
08h	SCANCONFIG	00h	Scan Configuration Register	Yes
09h	I2CMODE	55h	I2C Serial Interface Configuration Register	No
0Ah	VMODE0	00h	Digital Video Bus Configuration Register 0	No
0Bh	VMODE1	00h	Digital Video Bus Configuration Register 1	No
0Ch	WROWS	00h	Scan Window Row Start Register	Yes
0Dh	WROWE	E7h	Scan Window Row End Register	Yes
0Eh	WROWMSB	10h	Scan Window Row MSB Register	Yes
0Fh	WCOLS	09h	Scan Window Column Start Register	Yes
10h	WCOLE	F6h	Scan Window Column End Register	Yes
11h	WCOLMSB	20h	Scan Window Column MSB Register	Yes
12h	FDELAYL	00h	Frame Delay Low Register	Yes
13h	FDELAYH	00h	Frame Delay High Register	Yes
14h	RDELAYL	00h	Row Delay Low Register	Yes
15h	RDELAYH	00h	Row Delay High Register	Yes
16h	ITIMEL	00h	Integration Time High Register	Yes
17h	ITIMEH	00h	Integration Time Low Register	Yes
18h	BP3LEV	00h	HDR Mode Break Point 3 Level Register	Yes
19h	BP3SLOPEL	00h	HDR Mode Break Point 3 Slope Low Register	Yes
1Ah	BP3SLOPEH	00h	HDR Mode Break Point 3 Slope High Register	Yes
1Bh	BP2LEV	00h	HDR Mode Break Point 2 Level Register	Yes
1Ch	BP2SLOPEL	00h	HDR Mode Break Point 2 Slope Low Register	Yes
1Dh	BP2SLOPEH	00h	HDR Mode Break Point 2 Slope High Register	Yes
1Eh	BP1LEV	00h	HDR Mode Break Point 1 Level Register	Yes
1Fh	BP1SLOPEL	00h	HDR Mode Break Point 1 Slope Low Register	Yes
20h	BP1SLOPEH	00h	HDR Mode Break Point 1 Slope High Register	Yes
21h - 22h			Reserved	
23h	SNAPITL	00h	Snapshot Low Integration Time Register	No
24h	SNAPITH	00h	Snapshot High Integration Time Register	No
25h	SNAPMODE	00h	Snapshot Mode Configuration Register	No
26h	BLKCONFIG1	00h	Black Level Configuration Register 1	No
27h	READ_SEL	00h	Debug Readout Control	No
28h	DAC_THRESHOLD	26h	Charge DAC Threshold	No
29h	BLKCONFIG5	00h	Black Level Configuration Register 5	No
2Ah	DAC_STEP	22h	Charge DAC Step Size	No
2Bh	BLKCONFIG2	08h	Black Level Configuration Register 2	No
2Ch	BLKTARGETL	20h	Black Level Target Low	No
2Dh	BLKTARGETH	00h	Black Level Target High	No
2Eh	BLKCONFIG3	48h	Black Level Configuration Register 3	No
2Fh	BLKCONFIG4	6Ah	Black Level Configuration Register 4	No
30h	BLFOFFSTH0	05h	Black Level Fine Offset Threshold 0	Yes
31h	BLFOFFSTH1	0Ah	Black Level Fine Offset Threshold 1	Yes
32h	BLFOFFDLT0	05h	Black Level Fine Offset Delta 0	Yes
33h	BLFOFFDLT1	0Ah	Black Level Fine Offset Delta 1	Yes
34h	BLC_DAC_0	00h	Manual Black Level DAC Channel 0	Yes
35h	BLC_DAC_1	00h	Manual Black Level DAC Channel 1	Yes
36h	BLC_DAC_2	00h	Manual Black Level DAC Channel 2	Yes
37h	BLC_DAC_3	00h	Manual Black Level DAC Channel 3	Yes
38h	BLC_DOFFS_0L	00h	Manual Black Level Digital Offset 0 Low	Yes
39h	BLC_DOFFS_0H	00h	Manual Black Level Digital Offset 0 High	Yes
3Ah	BLC_DOFFS_1L	00h	Manual Black Level Digital Offset 1 Low	Yes

Address	Register	Reset Value	Description	Double Buffered
3Bh	BLC_DOFFS_1H	00h	Manual Black Level Digital Offset 1 High	Yes
3Ch	BLC_DOFFS_2L	00h	Manual Black Level Digital Offset 2 Low	Yes
3Dh	BLC_DOFFS_2H	00h	Manual Black Level Digital Offset 2 High	Yes
3Eh	BLC_DOFFS_3L	00h	Manual Black Level Digital Offset 3 Low	Yes
3Fh	BLC_DOFFS_3H	00h	Manual Black Level Digital Offset 3 High	Yes
40h	PGA0	00h	Programmable Gain Amplifier 0	Yes
41h	PGA1	00h	Programmable Gain Amplifier 1	Yes
42h	PGA2	00h	Programmable Gain Amplifier 2	Yes
43h	PGA3	00h	Programmable Gain Amplifier 3	Yes
44h	FGA	00h	Fine Gain Amplifier	Yes
45h	Reserved	80h	Reserved	No
46h-4Fh			Reserved	
50h	CPCLKGEN	01h	Charge Pump Clock Generation	No
51h	CLOCKMODES	08h	Controls clocking modes	No
52h-58h			Reserved	
59h	BPCCFG	0Dh	Bad Pixel Correction Configuration	No
5Ah-5Fh			Reserved	
60h	GAMMAH	00h	Gamma High	No
61h	GAMMAL	00h	Gamma Low	No
62h	DC_RB_TH	96h	Bad Pixel Threshold Red and Blue Channel	No
63h	DC_G_TH	64h	Bad Pixel Threshold Green Channel	No
64h	ILINETIME1H	00h	Partial Line Integration Time 1 High	Yes
65h	ILINETIME1L	00h	Partial Line Integration Time 1 Low	Yes
66h	PARBP3SLOPEL	00h	HDR Mode BP3 Partial Line Slope Low	Yes
67h	PARBP3SLOPEH	00h	HDR Mode BP3 Partial Line Slope High	Yes
68h	PARBP2SLOPEL	00h	HDR Mode BP2 Partial Line Slope Low	Yes
69h	PARBP2SLOPEH	00h	HDR Mode BP2 Partial Line Slope High	Yes
6Ah	PARBP1SLOPEL	00h	HDR Mode BP1 Partial Line Slope Low	Yes
6Bh	PARBP1SLOPEH	00h	HDR Mode BP1 Partial Line Slope High	Yes
6Ch		00h	Reserved	No
6Dh	OVERSAT	00h	Over saturation	No
6Eh	AVRBLKL	n/a	Average Black Level Low	No
6Fh	AVRBLKH	n/a	Average Black Level High	No
70h	DWROWS	04h	Display Window Row Start	Yes
71h	DWROWE	E3h	Display Window Row End	Yes
72h	DWROWMSB	10h	Display Window Row MSB	Yes
73h			Reserved	
74h		00h	Reserved	No
75h	TIMING_MODES	00h	Analog Timing Modes (analog debug)	No
76h	TIMING_MODES2	B8h	Analog Timing Modes (analog debug)	No
77h-8Bh			Reserved	No
8Ch	HSYNCDELAY	00h	Hsync Delay	No
8Dh	VSYNCDELAY	00h	Vsync Delay	No
8Eh	EXTSYNCDELAY	00h	External Sync Delay	No
8Fh - CFh			Reserved	
D0h	UPDATE	00h	Update Register	No
D1h		00h	Reserved	No
D2h	WRITE_PROTECT_S	00h	Scan Configuration Write Protect	No
D3h	WRITE_PROTECT_A		Global Write Protect	No
D4h-FFh			Reserved	

REGISTER SET

The following section describes all available registers in the KAC-00401 register bank and their function.

Device ID

Address 00 Hex
Mnemonic DEVID
Type Read Only
Reset Value 18 Hex

Bit	Bit Symbol	Description
7:0	DevId	Sensor's Device ID

Silicon Revision

Address 01 Hex
Mnemonic REV
Type Read Only
Reset Value C0 Hex

Bit	Bit Symbol	Description
7:0	SiRev	Sensor Silicon Revision

Clock Generation

Address 02 Hex
Mnemonic VCLKGEN
Type Read/Write
Reset Value 01 Hex

Bit	Bit Symbol	Description
7:5		Reserved
4:0	HclkGen	Use to divide the frequency of the sensors master clock input, **Mclk**, and generate the sensor's internal clock, *hclk*.

HclkGen	Divisor
0x00	1
0x01	2 (default)
0x02	4
0x03	6
0x04	8
0x05-0x07	Reserved

Mode and Control

Address 03 Hex
Mnemonic MODE&CTRL
Type Read/Write
Reset Value 0D Hex

Bit	Bit Symbol	Description
7	Update	Set this bit in order to update the double buffered register values. This bit is self clearing.
6		Reserved
5	Slave Mode	Set to a logic 1 to operate the sensor in slave mode. Set to logic 0 to operate the sensor in master mode.
4		Reserved
3		Reserved
2		Reserved
1		Reserved
0	PwDn	Set to a logic 1 to power down the chip. All internal clocks will be turned off in this mode. Set to a logic 0 to set the sensor in power up mode.

NOTE: Bit 7 of this register and bit 0 of Register 0xD0 (Update Register) perform the same function. Either can be used to update the double buffered registers.

Scan Configuration

Address 08 Hex
Mnemonic SCANCONFIG
Type Read/Write (Double Buffered bits 2 and 3)

Reset Value 00 Hex

Bit	Bit Symbol	Description
7	Color	Set to a logic 1 when using a color sensor. Set to a logic 0 to operate using a monochrome sensor.
6	VScanDir	Set to a logic 0, (the default), to set the sensor's vertical scan direction to operate from bottom to top. Set to a logic 1, to set the sensor's vertical scan direction to operate from top to bottom.
5	VSub	Set to a logic 0, (the default), to disable vertical sub-sampling. Set to a logic 1 to enable vertical sub-sampling.
4	HScanDir	Set to a logic 0, (the default), to set the sensor's horizontal scan direction to operate from left to right. Set to a logic 1, to set the sensor's horizontal scan direction to operate from right to left.
3	HSub	Set to a logic 0, (the default), to disable horizontal sub-sampling. Set to a logic 1 to enable horizontal sub-sampling.
2	Hbin	Set to a logic 1 to enable horizontal binning. Set to a logic 0 to disable horizontal binning.
1		Reserved
0	DisableUpdate	Set to a logic 1 disable update bit. When this bit is set all registers values take effect as soon as they are written.

I²C Mode

Address 09 Hex
Mnemonic I2CMODE
Type Read/Write

Reset Value 55 Hex

Bit	Bit Symbol	Description
7	DevAddrEn	Set to a 1 in order to enable the programmed address
6:0	I2CDevAddr	Use to program the device address of I²C compatible interface. By default, the value is 55 hex.

Digital Video Mode 0

Address 0A Hex
Mnemonic VMODE0
Type Read/Write
Reset Value 00Hex

Bit	Bit Symbol	Description
7:6	PixDataSel	Use to program the number of active bits on the digital video bus d[11:0], starting from the MSB (d[11]). Inactive bits are tri-stated.
		00 — 12 bit mode, bits d[11:0], of the digital video bus are active. This is the default mode.
		01 — 10 bit mode, bits d[11:2] of the digital video bus are active.
		10 — 8 bit mode, bits d[11:4] of the digital video bus are active.
		11 — Reserved
5:4	PixDataMSB	Use to program the routing of the MSB output of the internal video ADC to a bit on the digital video bus.
		00 — A/D[11:0]->d[11:0]
		01 — A/D[10:0]->d[11:1]
		10 — A/D[9:0]->d[11:2]
		11 — A/D[8:0]->d[11:3]
3	Saturation	This bit should be set if bits 5:4 are programmed to anything other than 00. This bit guarantees that when routing the lower bits to upper bits of the sensor the sensor is saturated even after the ADC value is above the maximum bit routed to bit 11 of the sensor. For example if bits 5:4 are set to 11 and the the code value out of the ADC was 001000000000 then setting this bit would assure that the value out of the sensor would be 111111111111 where as if this bit was not set the output would be
2	PixDataMSB7	This bit enables the routing of A/D[7:0]->d[11:4].
1:0	DataRouting	Use to program the routing of the MSB output of the internal video A/D to a bit on the digital video bus.
		00 — No effect
		01 — bits d[1:0] will be clamped to 0
		10 — A/D[11:4]->d[7:0]
		11 — A/D[11:3]->d[9:0]

Digital Video Mode 1

Address 0B Hex
Mnemonic VMODE1
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7	PixClkMode	Set to a logic 0, (the default) to operate the pclk in "free running" mode. Set to a logic 1 to operate pclk in "data ready mode"
6	VsyncMode	Set to a logic 0, (the default) to operate vsync in "level mode". Set to a logic 1 to operate vsync in "pulse mode".
5	HsyncMode	Set to a logic 0, (the default), to operate hsync in "level mode", Set to a logic 1 to operate hsync in "pulse mode".
4	PixClkPol	Set to a logic 0, (the default), to force the active edge of the pixel clock to be positive. Set to a logic 1 to force the active edge of the pixel clock to be negative
3	VsyncPol	Set to a logic 0 (the default) to force vsync to generate a logic 1 during frame readout (Level Mode), or a positive pulse at the end of a frame readout (Pulse Mode). Set to a logic 1 to force vsync to generate a logic 0 during a frame readout (Level Mode), or a negative pulse at the end of a frame readout (Pulse Mode).
2	HsyncPol	Set to a logic 0 (the default) to force hsync to generate a logic 1 during row readout (Level Mode), or a positive pulse at the end of a row readout (Pulse Mode). Set to a logic 1 to force hsync to generate a logic 0 during a row readout (Level Mode), or a negative pulse at the end of a row readout (Pulse Mode).
1	PixData	Changes edge that pixel data is clocked out on.
0	TriExtsync	Set to tri-state extsync pin

Scan Window Start Row

Address 0C Hex
Mnemonic WROWS
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	WStartRow[7:0]	Use to program the scan window's start row address' LSBs. The MSBs can be programmed using the WROWMSB register

Scan Window End Row

Address 0D Hex
Mnemonic WROWE
Type Read/Write (Double Buffered)
Reset Value E7 Hex

Bit	Bit Symbol	Description
7:0	WEndRow[7:0]	Use to program the scan window's end row address' LSBs. The MSBs can be programmed using the WROWMSB register.

Scan Window Row MSB

Address 0E Hex
Mnemonic WROWMSB
Type Read/Write (Double Buffered)
Reset Value 10 Hex

Bit	Bit Symbol	Description
7:4	WEndRow[11:8]	Use to program the scan window's end row address's MSBs.
3:0	WStartRow[11:8]	Use to program the scan window's start row address's MSBs.

Scan Window Start Column

Address 0F Hex
Mnemonic WCOLS
Type Read/Write (Double Buffered)
Reset Value 09 Hex

Bit	Bit Symbol	Description
7:0	WStartCol[7:0]	Use to program the scan window's start column address' LSBs. The MSBs can be programmed using the WCOLMSB register.

Scan Window End Column

Address 10 Hex
Mnemonic WCOLE
Type Read/Write (Double Buffered)
Reset Value F6 Hex

Bit	Bit Symbol	Description
7:0	WEndCol[7:0]	Use to program the scan window's end column address' LSBs. The MSBs can be programmed using the WCOLMSB register.

Scan Window Column MSB

Address 11 Hex
Mnemonic WROWMSB
Type Read/Write (Double Buffered)
Reset Value 20 Hex

Bit	Bit Symbol	Description
7:4	WEndCol[11:8]	Use to program the scan window's end column address's MSBs.
3:0	WStartCol[11:8]	Use to program the scan window's start column address's MSBs.

Frame Delay Low

Address 12 Hex
Mnemonic FDELAYL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Fdelay[7:0]	Use to program the LSB's of the frame delay.

Frame Delay High

Address 13 Hex
Mnemonic FDELAYH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Fdelay[13:8]	Use to program the MSB's of the frame delay. Maximum programmable value 0x3Fh.

Row Delay Low

Address 14 Hex
Mnemonic RDELAYL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Rdelay[7:0]	Use to program the LSB's of the row delay.

Row Delay High

Address 15 Hex
Mnemonic RDELAYH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:5		Reserved
4:0	Rdelay[12:8]	Use to program the MSB's of the row delay. Maximum programmable value 0x1Fh.

Integration Time Low

Address 16 Hex
Mnemonic ITIMEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Itime[7:0]	**Program to set the LSBs of the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset. If Itime is increased the new value takes effect in 2 frames and if Itime is decreased the value takes effect the next frame.**

Integration Time High

Address 17 Hex
Mnemonic ITIMEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	Itime[14:8]	Use to program the MSB's of the integration time of the array. Maximum programmable value 0x7Fh.

Break Point 3 Level

Address 18 Hex
Mnemonic BP3LEV
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Bp3Level	This register defines the level at which the third breakpoint is applied when the sensor is operated in non-linear mode.

Breakpoint 3 Slope Low

Address 19 Hex
Mnemonic BP3SLOPEL (Double Buffered)
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Bp3Slope[7:0]	This register defines the slope of the curver above the third breakpoint when the sensor is operated in non-linear mode.

Breakpoint 3 Slope High

Address 1A Hex
Mnemonic BP3SLOPEH (Double Buffered)
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	Bp3Slope[14:8]	This register is used to program the MSBs of the slope of the curve after the third breakpoint.

Break Point 2 Level

Address 1B Hex
Mnemonic BP2LEV
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Bp2Level	This register defines the level at which the second breakpoint is applied when the sensor is operated in non-linear mode.

Breakpoint 2 Slope Low

Address 1C Hex
Mnemonic BP2SLOPEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp2Slope[7:0]	This register is used to program the LSBs of the slope of the curve after the second breakpoint, when the sensor is operated in HDR mode. When BP2SLOPE register is cleared no breakpoint will result.

Breakpoint 2 Slope High

Address 1D Hex
Mnemonic BP2SLOPEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	Bp2Slope[14:8]	This register is used to program the MSBs of the slope of the curve after the second breakpoint.

Break Point 1 Level

Address 1E Hex
Mnemonic BP1LEV
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Bp1Level	This register defines the level at which the first breakpoint is applied when the sensor is operated in non-linear mode.

Breakpoint 1 Slope Low

Address 1F Hex
Mnemonic BP1SLOPEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp1Slope[7:0]	This register is used to program the LSBs of the slope of the curve after the first breakpoint, when the sensor is operated in HDR mode. When BP1SLOPE register is cleared no breakpoint will result.

Breakpoint 1 Slope High

Address 20 Hex
Mnemonic BP1SLOPEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	Bp1Slope[14:8]	This register is used to program the MSBs of the slope of the curve after the first breakpoint.

Snapshot Integration Time Low

Address 23 Hex
Mnemonic SNAPITL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	SnapITL[7:0]	Use to program the LSBs of the image capture time in external shutter snapshot mode. (see figure 22)

Snapshot Integration Time High

Address 24 Hex
Mnemonic SNAPITH
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	SnapIT[14:8]	Use to program the MSBs of the image capture time in external snaphsot mode. (see figure 22)

Snapshot Mode Configuration

Address 25 Hex
Mnemonic SNAPMODE
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6	SnapPol	Set to a logic 1 to configure the SNAPSHOT input as active low. Set to a logic 0 to configure the SNAPSHOT input as active high
5	SnapEnable	Set to a logic 1 to configure the sensor to operate in snapshot mode. Set to a logic 0 (the default) to operate the sensor in video mode.
4	SnapShotMode	Set to a logic 1 to operate the **snapshot** pin to level mode. In level mode the sensor will continually run snapshot sequences as long as the **snapshot** pin is held active. Set to a logic 0 to operate the snapshot pin to pulse mode, in pulse mode the sensor will only out one snapshot per pulse.
3	ShutterMode	Set to a logic 1 to indicate that an external shutter will be used during snapshot mode. Set to a logic 0, (the default) to indicate that snapshot mode will be carried out without an external shutter.
2:0	SsFrames	Program to set the number of frames required before readout druing a snapshot (see Figure xx). The number of frames before readout equals SsFrames + 1. By default these bits are set to 111 resulting in eight frames before readout.

Black Level Configuration 1

Address 26 Hex
Mnemonic BLKLEVCONFIG1
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6	DoubleTh	Set to a logic 1 in order to double the threshold for the coarse balck level compensation
5		Reserved
4		Reserved
3		Reserved
2	ManFine	Set to a logic 1 in order to adjust the fine black level compensation manually.
1	ManCoarse	Set to a logic 1 in order to adjust the coarse black level compensation manually
0		Reserved

Data Read Back

Address 27 Hex
Mnemonic READ_SEL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	Channel_Select	00XX - Reserved 0100 - Green on Red row from fine offset calibration - Signed datatype 14 bits 0101 - Red statistics from fine offset calibration - Signed datatype 14 bits 0110 - Green on Blue row statistics from fine offset calibration - Signed data type 14 bits 0111 - Blue Statistics from fine offset calibration - signed data type 14 bits 1000 - Green on Red Row Course DAC value - Signed data type 6 bits 1001 - Red Course DAC - Signed data type 6 bits 1010 - Green on Blue Row Course DAC value - Signed data type 6 bits 1011 - Blue Course DAC value - Signed data type 6 bits 1100 - Green on Red Row data fine calibration value - data type signed - 10 bits (use bottom 10) 1101 - Red data fine calibration value - data type signed - 10 bits (use bottom 10) 1110 - Green on Blue Row data fine calibration value - data type signed - 10 bits (use bottom 10) 1111 - Blue data fine calibration value - data type signed - 10 bits (use bottom 10)

DAC Threshold

Address 28 Hex
Mnemonic DACThreshold
Type Read/Write
Reset Value 26 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	DACThres	DAC Threshold at unity gain in LSB's. Must be greater than DAC stepsize.

Black Level Configuration 5

Address 29 Hex
Mnemonic BLKLEVCONFIG5
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:3		
2:1	Gain_mode	Assigns which pga registers are used for color gain. 00: only one gain value for all colors 01: pga0 = 0x40h; pga1 = 0x41h; pga2 = 0x42h; pga3 = 0x40h; (for color with 3 gains - for R,B and one for GB and GR) 10: pga0 = 0x40h; pga1 = 0x41h; pga2 = 0x40h; pga3 = 0x41h (for two gain per line - odd/even in monochrome) 11: pga0 = 0x40h; pga1 = 0x41h; pga2 - 0x42h; pga3 = 0x43h (full color with individual gain for each channel)
0	Odd_Even_BLC	In monochrome mode when set this bit will calculate the offset correction as the average of the odd and even channels and apply the average to all pixels ((odd_offset + even_offset)/2). When cleared, two independent values for the offset will be calculated (one for odd and one for even channel). The odd offset will be applied to the odd channels and the even offset will be applied to the even channels. For color sensors always keep this bit set to 0.

NOTE: For color sensor recommended setting for register 0x29h = 0x06h and for monochrome sensor register 0x29h = 00h. Register 0x2F bits[1:0] must be set to 10 for bit 0 of this register to have any affect.

DAC Step Size

Address 2A Hex
Mnemonic DACStep
Type Read/Write
Reset Value 22 Hex

Bit	Bit Symbol	Description
7		Reserved
6:0	DACStep	DAC step size at unity gain. This should reflect the DAC's step size.

Black Level Configuration 2

Address 2B Hex
Mnemonic BLKLEVCONFIG2
Type Read/Write
Reset Value 08 Hex

Bit	Bit Symbol	Description
7		Reserved
6:4	ADCClip[2:0]	Use to program the number of ADC MSBs to be removed from the black level calculation
3:0	alpha[3:0]	Use to adjust the speed at which the black level calculation converges

Black Level Target Low

Address 2C Hex
Mnemonic BLKTARGETL
Type Read/Write
Reset Value 20 Hex

Bit	Bit Symbol	Description
7:0	BlkRef[7:0]	Use to program the low byte of the sensor's target black level.

Black Level Target High

Address 2D Hex
Mnemonic BLKTARGETH
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	BlkRef[11:8]	Use to program the high byte of the sensor's target black level.

Black Level Configuration 3

Address 2E Hex
Mnemonic BLKLEVCONFIG3
Type Read/Write
Reset Value 48 Hex

Bit	Bit Symbol	Description
7	BypassADC	Set to 1 to bypass black level compensation and bad pixel correction for debug purposes.
6	GainStpComp	Set to 1 for gain step compenastion
5	AntiFlicker1	Set to a logic 1 to adjust fine level speed dependence on black level average.
4	AntiFlicker0	Set to a logic 1 to adjust fine level speed dependence on coarse adjustment
3:0	beta[3:0]	Use to adjust the speed at which the fine black level offset compensation converges

Black Level Configuration 4

Address 2F Hex
Mnemonic BLKLEVCONFIG4
Type Read/Write
Reset Value 6A Hex

Bit	Bit Symbol	Description
7	BLCReset	When Set, resets the black level statistics for course and fine calibration to zero
6	Step Compensation Method	In step compensation convergence is achieved by stepping the fine calibration down in steps of no bigger than 2 codes. The initial offset is determined by a user-programmable initial step size. The initial step will only be applied when DAC values change
5	ExpMethod	Expontential IIR convergence Method (set by default). When set will use an expotential IIR filter to determine the fine offset correction. This was found to be the best convergence method for speed and stability. The weight of the IIR filter can be set using BLC_CFG4[3:2]. NOTE: ONLY 1 of the 3 methods can be used at one time (Expontential, Step, or Gain (BLC_CONFIG3[6]))
4	ExpMthdaHys	When cleared, will not round the divider of the expotential IIR. When set, will round. This in effect gives hysteresis o nthe convergence of the IIR, equal in code to the IIR strength - 1. For example, if the IIR strength is set to 4 then there will be a hysteresis of 3 codes before the IIR will start to converge again.
3:2	Exp_Method_Divisor	Divisor for expontential method when bit 6 is set.

Bit	Bit Symbol	Description
Continued		
1	FPN_BLC_Color	When set, provides the following: With both this bit and BLC_CFG5[0] set, in monochrome mode, this offset correction will operate on the average of odd and even channel statistics. In addition to this, there are two other modes: Independent statistics for odd and even channels [BLC_CFG[5] = 0) and one channel only [BLC_CFG4[1]=0].
0	Color_mode	This bit determines the amount of channels used for offset calibration. When set, statistics will be kept for 4 different chanels (in accordance with Bayer pattern). When cleared, monochrome mode is assumed, and either one or two channels will be used for statistics (see description for bit 1). Two channels are useful to remove odd-even fixed pattern noise.

Black Level Fine Offset Threshold0

Address 30 Hex
Mnemonic BLFOFFSTH0
Type Read/Write (Double Buffered)
Reset Value 05 Hex

Bit	Bit Symbol	Description
7:0	BlfOffsTh0	Use to program the smaller of the two fine calibration threshold levels. If the black level is corrected to less than this threshold value from BlkRef, the automatic calibration algorithm will stop compensation procedures.

Black Level Fine Offset Threshold1

Address 31 Hex
Mnemonic BLFOFFSTH1
Type Read/Write (Double Buffered)
Reset Value 0A Hex

Bit	Bit Symbol	Description
7:0	BlfOffTh1	Use to program the larger of the two fine calibration threshold levels. If the black level is corrected to greater than this threshold value from BlkRef, the automatic calibration algorithm will begin compensation procedures.

Black Level Fine Offset Delta0

Address 32 Hex
Mnemonic BLFOFFDLT0
Type Read/Write (Double Buffered)
Reset Value 05 Hex

Bit	Bit Symbol	Description
7:0	BlFOffDlt0	Use to program the smaller of the two correction values. If the actual black level is above BlfOffTh0 and below BlfOffTh1, the automatic calibration algorithm will add/subtract BlFOffDlt0 to the BlkLvlOfs. IF ((|Black Level| >= BlFOffsTh0) && (|Black Level| < BlFOffsTh1)) then BlkLvlOfs = BlkLvlOfs +/- BlFOffDlt0

Black Level Fine Offset Delta1

Address 33 Hex
Mnemonic BLFOFFDLT1
Type Read/Write (Double Buffered)
Reset Value 0A Hex

Bit	Bit Symbol	Description
7:0	BlFOffDlt1	Use to porgram the larger of the two correction values. If the black level is beyond BlkRng2 from BlkRef, the automatic calibration algorithm will add/subtract BlkDlt2 to the BlkLvlOfs If the actual black level is above BlfOffTh1, the automatic calibration algorithm will add/subtract BlFOffDlt2 to the BlkLvlOfs. IF (|Black Level| >= BlFOffsTh1) then BlkLvlOfs = BlkLvlOfs +/- BlFOffDlt1

Manual Black Level DAC Channel 0

Address 34 Hex
Mnemonic BLC_DAC_0
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	COFFS0	In manual mode, use to program the coarse compensation of channel 0. This is a 2's compliment value.

Manual Black Level DAC Channel 1

Address 35 Hex
Mnemonic BLC_DAC_1
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	COFFS1	In manual mode, use to program the coarse compensation of channel 1. This is a 2's compliment value.

Manual Black Level DAC Channel 2

Address 36 Hex
Mnemonic BLC_DAC_2
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	COFFS2	In manual mode, use to program the coarse compensation of channel 2. This is a 2's compliment value.

Manual Black Level DAC Channel 3

Address 37 Hex
Mnemonic BLC_DAC_3
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	COFFS3	In manual mode, use to program the coarse compensation of channel 2. This is a 2's compliment value.

Manual Black Level Channel 0 Fine Offset Low

Address 38 Hex
Mnemonic BLC_DOFFS_0L
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	FOFFS0L[7:0]	In manual mode, use to program the low byte of the fine compensation value.

Manual Black Level Channel 0 Fine Offset High

Address 39 Hex
Mnemonic BLC_DOFFS_0H
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	FOFFS0H[9:8]	In manual mode, use to program the high byte of the fine compensation of channel 0. This is a 2's compliment value.

Manual Black Level Channel 1 Fine Offset Low

Address 3AHex
Mnemonic BLC_DOFFS_1L
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	FOFFS1L[7:0]	In manual mode, use to program the low byte of the fine compensation value.

Manual Black Level Channel 1 Fine Offset High

Address 3B Hex
Mnemonic BLC_DOFFS_1H
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	FOFFS1H[9:8]	In manual mode, use to program the fine compensation of channel 1. This is a 2's compliment value.

Manual Black Level Channel 2 Fine Offset Low

Address 3CHex
Mnemonic BLC_DOFFS_2L
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	FOFFS2L[7:0]	In manual mode, use to program the low byte of the fine compensation value.

Manual Black Level Channel 2 Fine Offset High

Address 3D Hex
Mnemonic BLC_DOFFS_2H
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	FOFFS2H[9:8]	In manual mode, use to program the fine compensation of channel 2. This is a 2's compliment value.

Manual Black Level Channel 3 Fine Offset Low

Address 3E Hex
Mnemonic BLC_DOFFS_3L
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	FOFFS3L[7:0]	In manual mode, use to program the low byte of the fine compensation value.

Manual Black Level Channel 3 Fine Offset High

Address 3F Hex
Mnemonic BLC_DOFFS_3H
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	FOFFS3H[11:8]	In manual mode, use to program the fine compensation of channel 3. This is a 2's compliment value.

PGA0

Address 40 Hex
Mnemonic PGA
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:3		Reserved
2:0	PGA0	Use to program the analog gain from 1 to 2.35x in steps of 0.192x. Equation is Gain = 1 + 0.192 x Register setting.

PGA1

Address 41 Hex
Mnemonic PGA1
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:3		Reserved
2:0	PGA1	Use to program the analog gain from 1 to 2.35x in steps of 0.192x. Equation is Gain = 1 + 0.192 x Register setting.

PGA2

Address 42 Hex
Mnemonic PGA2
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:3		Reserved
2:0	PGA2	Use to program the analog gain from 1 to 2.35x in steps of 0.192x. Equation is Gain = 1 + 0.192 x Register setting.

PGA3

Address 43 Hex
Mnemonic PGA3
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:3		Reserved
2:0	PGA3	Use to program the analog gain from 1 to 2.35x in steps of 0.192x. Equation is Gain = 1 + 0.192 x Register setting.

FGA

Address 44 Hex
Mnemonic FGA
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	FGA	Use to program the global gain from 1 to 5.7x in 64 steps of 0.075x. Equation is Gain = 1 + 0.075 x register setting

FGA_HDR

Address 45 Hex
Mnemonic FGA_HDR
Type Read/Write
Reset Value 80 Hex

Bit	Bit Symbol	Description
7	DisableTracking	When set, will disable gain tracking. Default value is 1.
6:5	BP3_Gain	Programmable gain for Breakpoint 3
4:3	BP2_Gain	Programmable gain for Breakpoint 2
2:1	BP1_Gain	Programmable gain for Breakpoint 1
0	Tracking	When set, will assign programmable gain values in bits 6:1. When cleared, will track FGA[5:4]. Default is set to 0.

Charge Pump Clock Generation

Address 50 Hex
Mnemonic CPCLKGEN
Type Read/Write
Reset Value 01 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	CPClkGen	Use to divide the frequency fo the sensors master clock input, mclk, and genereate the charge pump clock. Minimum charge pump clock is 12Mhz

CPClkGen	Divisor
00	1
01	2 (default)
10	4
11	Reserved

Clocking Modes

Address 51 Hex
Mnemonic CLK_MODES
Type Read/Write
Reset Value 08 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3	InAnaClk	Set to 1 to invert analog clock. This bit should be set in order for first column to be output properly
2	InChargeClk	Set to 1 to invert charge pump clock
1	PwrDwnAnclk	Set to 1 to power down analog clock
0	PwrDwnChClk	Set to 1 to power down charge pump clock

NOTE: This register MUST be set to 0x08h for the sensor to output the first column correctly.

Bad Pixel Correction Configuration

Address 59 Hex
Mnemonic BPCCFG
Type Read/Write
Reset Value 0D Hex

Bit	Bit Symbol	Description
7:4		Reserved
3	HotPixCor	Set to 1 to enable hot pixel correction
2	ColdPixCor	Set to 1 to enable cold pixel correction
1		Reserved
0	EnBPC	Set to 1 to enable bad pixel correction

Gamma High

Address 60 Hex
Mnemonic GAMMAH
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	UpperSigma	Factor for upper sigma threshold for monochrome mode. Set to 0x01h for best performance.

Gamma Low

Address 61 Hex
Mnemonic GAMMAL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	LowerSigma	Factor for lower sigma threshold for monochrome mode. Set to 0x01h for best performance.

Bad Pixel Threshold Red and Blue Channel

Address 62 Hex
Mnemonic DC_RB_TH
Type Read/Write
Reset Value 96 Hex

Bit	Bit Symbol	Description
7:0	Threshold	Bad pixel threshold for red and blue pixels.

Bad Pixel Threshold Green Channel

Address 63 Hex
Mnemonic DC_G_TH
Type Read/Write
Reset Value 64 Hex

Bit	Bit Symbol	Description
7:0	Threshold	Bad pixel threshold for green pixels.

Partial Line Integration Low

Address 64 Hex
Mnemonic ILINETIME1L
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	ILINEL[7:0]	Program to set the LSBs of the partial line integration time of the array. The value programmed in the register is the number of clock cycles the pixel reset is delayed.

Partial Line Integration High

Address 65 Hex
Mnemonic ILINETIME1H
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	ILINEH[9:8]	Program to set the MSBs of the partial line integration time of the array. The value programmed in the register is the number of clock cycles the pixel reset is delayed.

HDR Mode BP3 Partial Line Slope Low

Address 66 Hex
Mnemonic PARBP3SLOPEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	PARABP3SLOPEL[7:0]	Program to set the LSBs of the number of clock cycles by which the reset o fthe slope after the 3rd breakpoint is delayed in partial line integration mode.

HDR Mode BP3 Partial Line Slope High

Address 67 Hex
Mnemonic PARBP3SLOPEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	PARABP3SLOPEH[9:8]	Program to set the MSBs of the number of clock cycles by which the reset o fthe slope after the 3rd breakpoint is delayed in partial line integration mode.

HDR Mode BP2 Partial Line Slope Low

Address 68Hex
Mnemonic PARBP2SLOPEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	PARABP2SLOPEL[7:0]	Program to set the LSBs of the number of clock cycles by which the reset o fthe slope after the 2nd breakpoint is delayed in partial line integration mode.

HDR Mode BP2 Partial Line Slope High

Address 69 Hex
Mnemonic PARBP2SLOPEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	PARABP2SLOPEH[9:8]	Program to set the MSBs of the number of clock cycles by which the reset o fthe slope after the 2nd breakpoint is delayed in partial line integration mode.

HDR Mode BP1 Partial Line Slope Low

Address 6AHex
Mnemonic PARBP1SLOPEL
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	PARABP1SLOPEL[7:0]	Program to set the LSBs of the number of clock cycles by which the reset o fthe slope after the 1st breakpoint is delayed in partial line integration mode.

HDR Mode BP1 Partial Line Slope High

Address 6BHex
Mnemonic PARBP1SLOPEH
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:2		Reserved
1:0	PARABP1SLOPEH[9:8	Program to set the MSBs of the number of clock cycles by which the reset o fthe slope after the 1st breakpoint is delayed in partial line integration mode.

Over Saturation

Address 6D Hex
Mnemonic OVERSAT
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3	DisEclThres	Set to 1 to disable eclipse threshold generation.
2	EnEclPwrSave	Set to 1 to enable eclipse power saving mode.
1:0	LEVEL	Two bit register used to control the level at which over saturation circuit takes effect. Use higher value as lighting becomes more intense. Default value is 00 00 : Least Aggresseive 01 : 10 : 11 : Most Aggressive

Average Black Level Low

Address 6E Hex
Mnemonic AVRBLKL
Type Read
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	AvrBlk[7:0]	This register reads the LSBs of the average black level of the black pixels. This is a read only register

Average Black Level High

Address 6F Hex
Mnemonic AVRBLKH
Type Read
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	AvrBlk[11:8]	This register reads the MSBs of the average black level of the black pixels. This is a read only register

Display Window Start Row

Address 70 Hex
Mnemonic DWROWS
Type Read/Write (Double Buffered)
Reset Value 26 Hex

Bit	Bit Symbol	Description
7:0	DWStartRow[7:0]	Use to program the display window's start address' LSBs. The MSBs can be programmed using the WROWMSB register.

Display Window End Row

Address 71 Hex
Mnemonic DROWE
Type Read/Write (Double Buffered)
Reset Value E3 Hex

Bit	Bit Symbol	Description
7:0	DWEndRow[7:0]	Use to program the display window's end row address' LSBs. The MSBs can be programmed using the WROWMSB register.

Display Window Row MSB

Address 72 Hex
Mnemonic DWROWMSB
Type Read/Write (Double Buffered)
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4	DWEndRow[11:8]	Use to program the display window's end row address' MSBs.
3:0	DWStartRow[11:8]	Use to program the display window's start row address MSBs.

HSYNC Delay Register

Address 8C Hex
Mnemonic HSYNCDELAY
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:4	Hsync_End	Sets the amount of Pclk periods that Hsync will transition after the last bit of video data appears on the Dout pins. Cleared by default
3		Reserved
2:0	Hsync_Start	Sets the amount of Pclk periods that Hsync will transition before the first bit of video data appears on the Dout pins. Cleared by default

VSYNC Delay Register

Address	8D Hex
Mnemonic	VSYNCDELAY
Type	Read/Write
Reset Value	00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:4	Vsync_End	Sets the amount of Pclk periods that Vsync will transition after the last bit of video data appears on the Dout pins. Cleared by default
3		Reserved
2:0	Vsync_Start	Sets the amount of Pclk periods that Vsync will transition before the first bit of video data appears on the Dout pins. Cleared by default

EXTSYNC Delay Register

Address	8E Hex
Mnemonic	EXTSYNCDELAY
Type	Read/Write
Reset Value	00 Hex

Bit	Bit Symbol	Description
7		Reserved
6:4	Extsync_End	Sets the amount of Pclk periods that Extsync will transition after the last bit of video data appears on the Dout pins. Cleared by default
3		Reserved
2:0	Extsync_Start	Sets the amount of Pclk periods that Extsync will transition before the first bit of video data appears on the Dout pins. Cleared by default

UPDATE

Address	D0 Hex
Mnemonic	UPDATE
Type	Read/Write
Reset Value	00 Hex

Bit	Bit Symbol	Description
7:1		Reserved
0	Update	Setting the update bit will assert functionality of the double buffered registers. Writing to double buffered registers does not assert functionality of the registers until the update bit is set. The bit is self clearing. Once set and double buffered registers are written the bit will clear.

NOTE: Using this register or bit 7 of register 0x03h does the same function.

WRITE PROTECT S

Address	D2 Hex
Mnemonic	WRITE_PROTECT_S
Type	Read/Write
Reset Value	00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	Scan_Protect	Writing bits[3:0] to 0101 protects scan register bits [7:3] from being written. Writing bits[3:0] to 1010 unprotects the scan register bits. Note: the read back values are different: scan register bits protected reads back as 0101; scan register bits unprotected reads back as 0000.

NOTE: Writing 0x05h only protects the following bits in the scan register: [7] – color mode, [6] vertical scan direction, [5] – vertical scan direction, [4] – horizontal scan direction, [3] – horizontal sub-sampling.

WRITE PROTECT S

Address D3 Hex
Mnemonic WRITE_PROTECT_A
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	Reg_Protect	Writing bits[3:0] to 0101 protects all registers from being written. Writing bits[3:0] to 1010 unprotects all registers. Note: the read back values are different: scan register bits protected reads back as 0101; scan register bits unprotected reads back as 0000.

TIMING INFORMATION

DIGITAL VIDEO PORT MASTER MODE TIMING

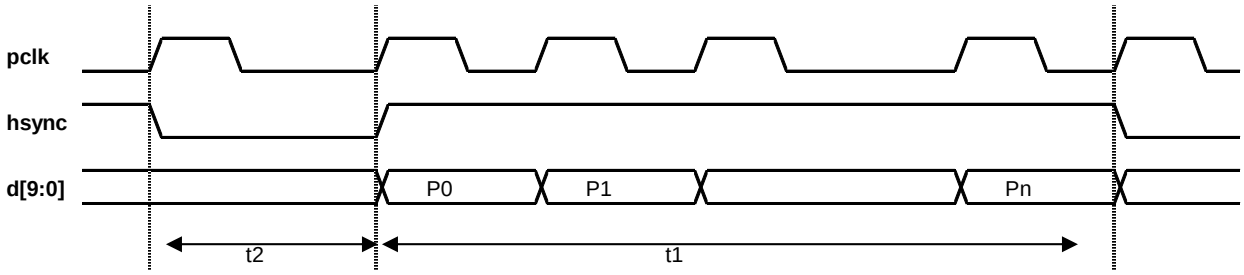


Figure 45: Row Timing Diagram

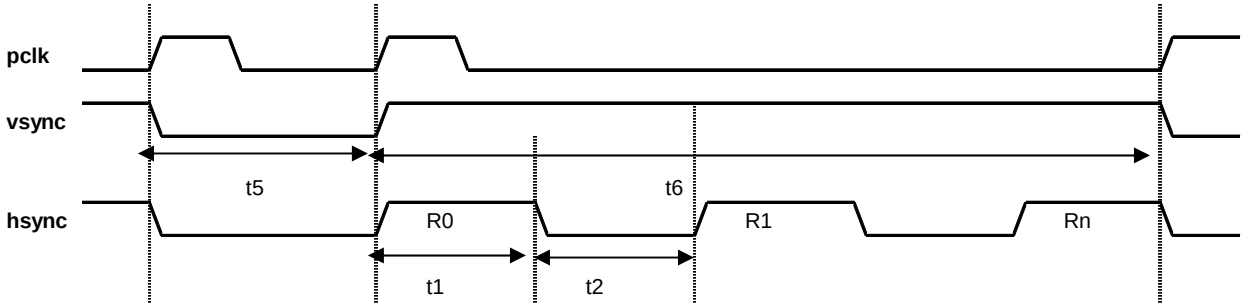


Figure 46: Frame Timing Diagram

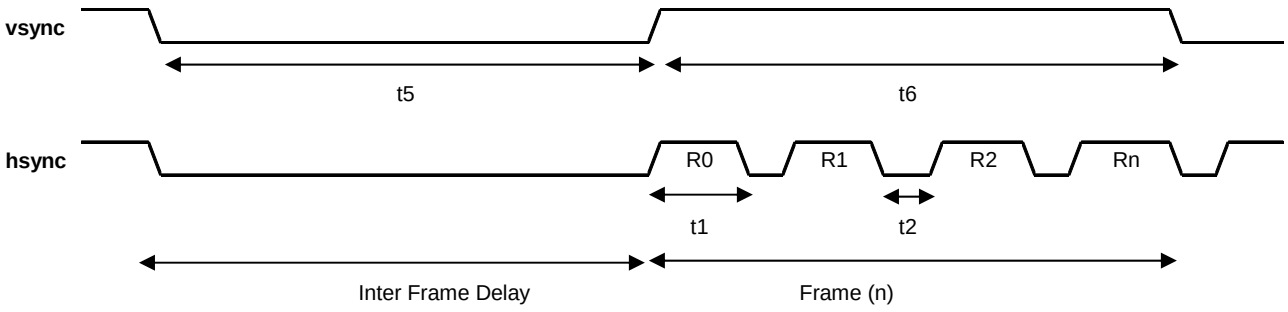


Figure 47: Frame Delay Timing Diagram (with Inter frame delay)

Label	Description		Min	Typ	Max
t0	pclk period		83..33ns	45.45ns	37.04ns
t1	hsync active[1,2]	level mode pulse mode	(HsyncEnd - HsyncStart + N_{pix} *MH_{factor}) * Hclk (HsyncEnd - HsyncStart + 4) * Hclk		
t2	hsync inactive[1,2]	level mode pulse mode	(RN_{Hclk} - N_{pix} * MH_{factor} + HsyncStart - HsyncEnd) * Hclk (RN_{Hclk} + HsyncStart - HsyncEnd - 4) * Hclk		
t3	first valid pixel after hsync active		t_{hstart} *Hclk		
t5	vsync inactive[1,3]	level mode pulse mode	((F_{delay} + 8) * RN_{Hclk} + $R_{opcycle}$ + R_{itime} + VsyncStart + VsyncEnd) * Hclk (FN_{Hclk} + VsyncStart - Vsync End - 4) * Hclk		
t6	vsync active[1,3]	level mode pulse mode	((VsyncEnd - VsyncStart) + RN_{Hclk} * Nrows * Mvfactor)) * Hclk (VsyncEnd - VsyncStart + 4) * Hclk		

Note1: See Frame Rate and Exposure Control on page 16 for definitions of RN_{Hclk} and FN_{Hclk}

Note 2: The values of HsyncStart and HsyncEnd are stored in the HSYNCDELAY register.

Note 3: The values of VsyncStart and VsyncEnd are stored in the VSYNCDELAY register.

DIGITAL VIDEO PORT SLAVE MODE TIMING

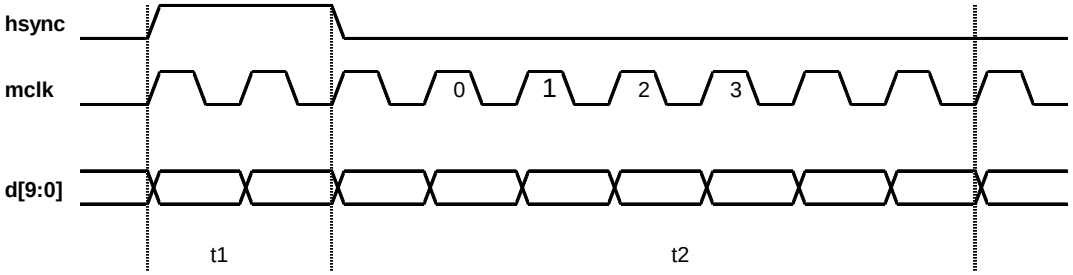


Figure 48: Slave Mode Row Trigger and Readout Timing Diagram

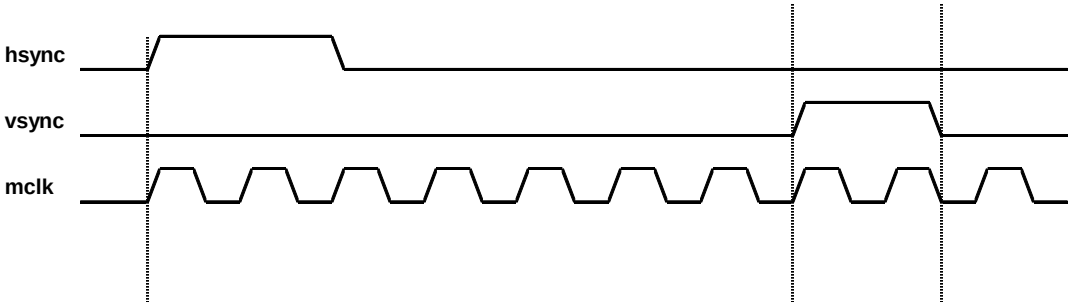


Figure 49: Slave Mode d[9:0], hsync and vsync to mclk Timing

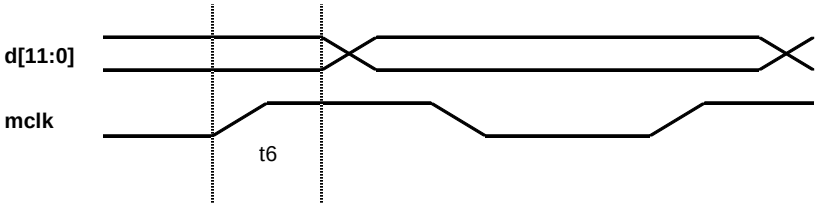


Figure 50: Rising Edge of mclk to valid Pixel Data

The following specifications apply for all supply pins = 3.3v and CL = 10µF unless otherwise noted.

1. See Frame Rate and Exposure Control on page 16 for definition of RN_{Hclk}.

DIGITAL VIDEO PORT SINGLE FRAME CAPTURE (SNAPSHOT MODE) TIMING

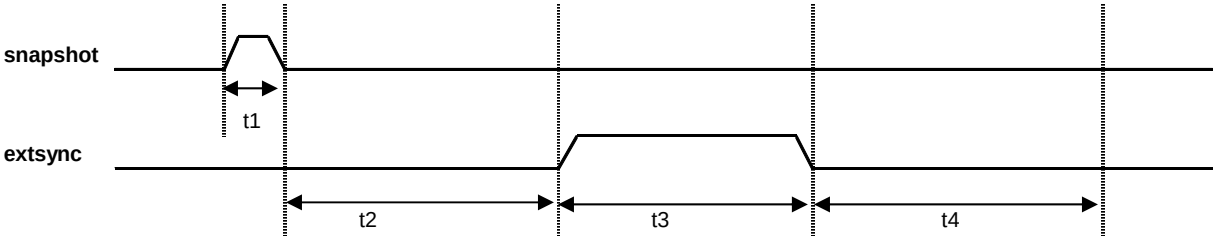


Figure 51: Snapshot Mode Timing with External Shutter

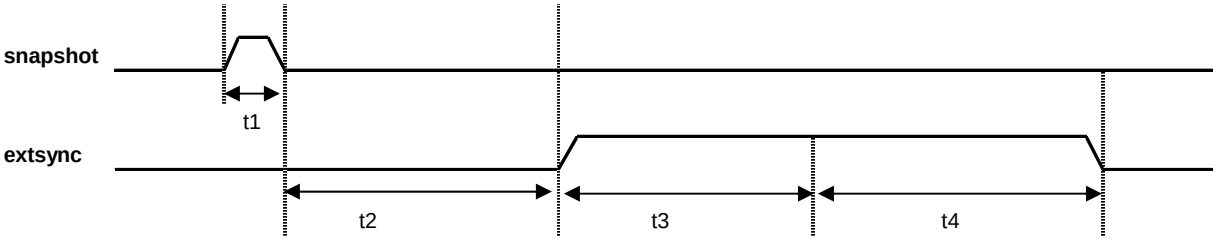


Figure 52: Snapshot Mode Timing without External Shutter

Label	Descriptions	Equation	
t1	Minimum Snapshot Trigger Pulse Width	2 * mclk	(see notes a &b)
t2	Minimum time from Snapshot Pulse to extsync	FN_{Hclk}	(see notes a &b)
t3	Array Integration Time	FN_{Hclk}	(see notes a &b)
t4	Pixel Read Out	FN_{Hclk}	(see notes a &b)

Note a: See Frame Rate and Exposure Control section for more details

Note b: See Snapshot Mode for more details.

I²C SERIAL BUS TIMING

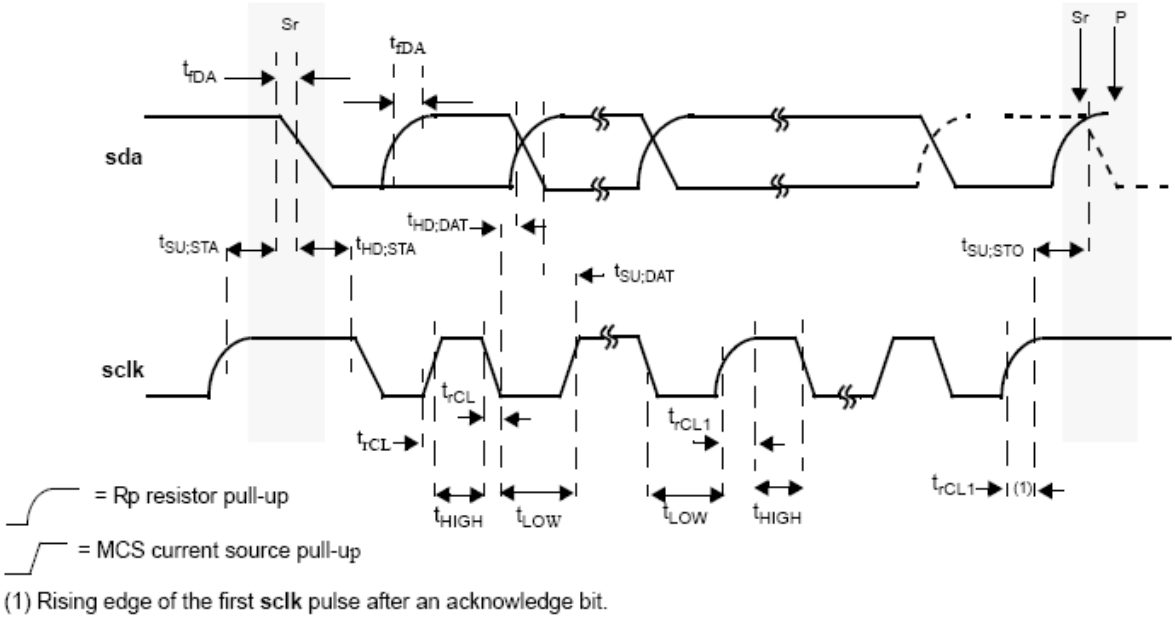


Figure 53: I²C Compatible Serial Bus Timing

Parameter	Symbol	Min	Max	Unit
sclk clock frequency	f_{SCLH}	0	400	KHz
Set up time (repeated) START condition	$f_{SU;STA}$	0.6	-	us
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	us
LOW period of sclk clock	t_{LOW}	1.3	-	us
HIGH period of the sclk clock	t_{HIGH}	0.6	-	us
Data set up time	$t_{SU;DAT}$	180	-	us
Data hold time	$t_{HD;DAT}$	0	0.9	us
Set up time for STOP condition	$t_{SU;STO}$	0.6		us

MECHANICAL INFORMATION

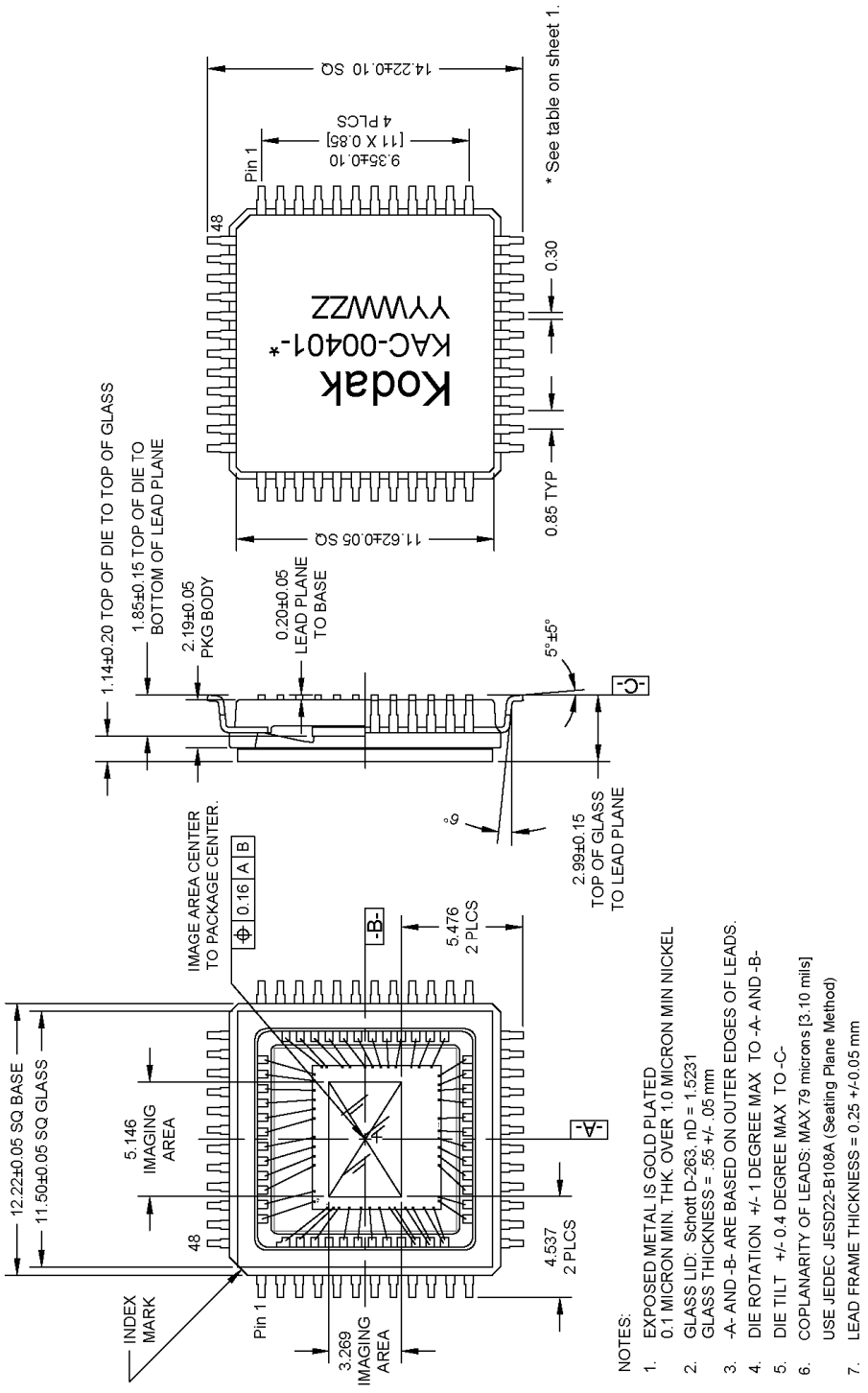


Figure 54: Completed Assembly

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release

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