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Memristors SPICE Modeling

Prof. Manoj. S. Kakade[1], Jeetendra Lekhraj Singh[2]

[1]*Department of Electronics & Telecommunication Engineering, Sinhgad college of Engineering Pune, India.*
[2]*Department of Electronics & Telecommunication Engineering, Dhole Patil college of Engineering Pune, India*

***Abstract*—Memristor is the fourth two terminal fundamental passive element and memristive effect was first published by Leon Chua in early 1970, Since then students and researchers are interested in exploring more practical possibilities and design application circuits But to design Memristors based circuits, an Accurate simulating models are very important. Testing circuits on practical Memristors will take few more years since its still in researchers stage. In this paper we provide near accurate computer models of memristor which will act as a tool to speed up its behavioral analysis and this will further help student and enthusiastic community to design innovative circuits and interesting applications with Memristors. This SPICE model is derived from HP based Mathematical model and its functionality can be shown on computer by simulation.**

***Keywords*—Memristors, SPICE, Mathematical model, ADALINE, HDL, Hysteresis , Eflux and Echarge.**

I. Introduction

The concept of a resistor with memory existed even before Leon Chua's publication on the memristor in 1970. In 1960, Prof. Bernard Widrow of Stanford University developed a new circuit element named the "memristor". This memristor proposed was three terminal device for which the conductance between two of the terminals was controlled by current flow (time-integral) in third terminal. Thus, the resistance of the memristor was controlled by charge. Memristors formed the basic components of the neural-network architecture called ADALINE (ADAptive Linear Neuron).

Between 1994 and 2008 there were many other devices developed with behavior similar to that of the memristor, but only the HP scientists were successful in finding link between their work and the memristor explained by Chua.

The purpose of this paper is to provide an accurate SPICE model of Memristor. The paper structure is as follows: Section II, After Introduction part provides information about physical and mathematical models for memristor, already published in [1] and [4]. Section IV describes Memristive based SPICE Model, After explanation of mathematical model in Section II. Section IV shows process flow and ends with results from SPICE simulations for the proposed model and last section VI describes application of Memristor.

II. Literature Survey

Memristors is also known to be the fourth passive element after Resistor (R), Capacitor (C) and Inductor (L). Its logical to develop a SPICE model, Since with reduction in die size (below 20nm) the effect of memristor will be eminent and cannot be ignored and hence conventional circuits will have to consider memristive effect into consideration and will provide opportunity to design circuits more effectively and which will also bring new design challenges. Hence accurate simulation tools will help foresee and overcome these design challenges.

In May 2008 HP-Lab based research group led Dr. Williams, published a report [1] on memristor, Its the fourth two terminal fundamental passive element and it was predicted in year 1970 by professor Chua in his paper [2] and reference from original work [1] has been taken for our analysis, the information like physical model of memristor.

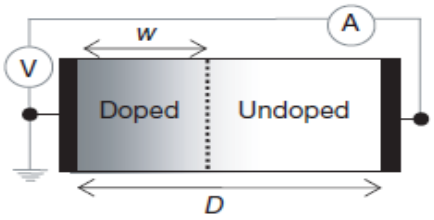

Figure 1. Memristor model according to [1].

The Memristors physical model [1], shown in Figure 1, is a thin film of D = 10 nm of consist of two TiO2 layers sandwiched between platinum contacts. one layers is undoped and other layer is doped so that it behaves like an semiconductor. The undoped layer has insulator property. And due to this complex material process consequence the doped region width (w) is proportional to electric charge passed through the device, The direction of electric current passing moves the boundary between them in same direction.

Thus cumulative resistance of the memristor Rmem is sum of two regions (doped and undoped regions), w is width of doped region with reference to total length D of both layer of TiO2 layer, And limiting values are Roff and Ron for memristor resistance when w = 0 and w = D.

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Usually the ratio is 10^2 -10^3 for these two resistances. The resistance of doped layer depends on the current and other factors stated [3] in Eq. 1.

$$R_{mem}(w/D) = R_{on}(w/D) + R_{off}(1-w/D), \quad (1)$$

$$\text{where } w / D \in (0,1) \quad (2)$$

The Value of Ron (~1Kohms) is resistance of the memristor if it is completely doped and Roff is its resistance if it is undoped.

As per Ohmic relation voltage and current: for memristor.

$$v(t) = R_{mem}(w) i(t) \quad (3)$$

Rmem (w/D) which is proportional to movement of speed of the boundary between the undoped and doped regions (dx/dt). Where x = w/D.

$$dx/dt = k\ i(t) f(x) \quad k=\text{constant} = (\mu d * Ron)/D^2 \quad (4)$$

Where μd = 10 – 14 m^2 s^ - 1 V^-1 is dopant mobility. As mentioned in [1], Small voltages in nanotechnology can produce enormous electric fields enough for a significant nonlinear in ionic transport. At thin film edges these nonlinear manifest themselves, where boundary's movement decreases gradually to zero. This nonlinear dopant drift can be modeled by the window function f(x) from the right side of Eq. 4. The window function [7] is:

$$f(x) = 1 - (2x - 1)^{2p} \quad (5)$$

Where p is a positive integer.

III. Experimentation

There are various ways to model the electrical characteristics of the Memristors (Rmem) listed below are few models which can be help provide memristive simulation models.

A. Spice Micro Model

The first approach, SPICE macro-models, is most appropriate as it is more readable for most of the readers and compatible to all SPICE versions. Apart this model can be readily used to simulate Analog circuits in combination with memristive element which can help primarily to redesign conventional circuits.

B. Hdl – Hardware Description Language

The second approach, HDL models, is more appropriate for detailed analysis since its low level language but language is comparatively most difficult.

C. C Programming

The third approach, C PROGRAMING based modeling is simpler but least accurate since this model doesn't include parametric details.

A. Spice Micro Model

The memristor memory effect is modeled using SPICE tool. The influence of boundary conditions and nonlinear drift are simulated by feedback function, f ( ) via nonlinear window.

As per Eq 1 the V-I relation of memristor is modeled as [3] :

$$R_{mem}(x) = R_{off} - x\Delta R, \text{ where } \Delta R = R_{off} - R_{on} \quad (6)$$

The SPICE model passes parameters like Ron, Roff resistance and initial resistance Rinit, width D of thin film, the windows function exponent p and μd the dopant mobility for direct computation of the various integral quantities like the time integrations of charge and flux. These parameters are key for results of SPICE analysis. These are available as internally controlled sources of Echarge and Eflux.

IV. Proposed Approch

The process flowchart to generate SPICE model of Memristor and simulating its results is shown in Figure 2.

We have used the Memristor mathematical model[3] in first place to design a working SPICE model and later the SPICE simulation tool has been used to do SPICE simulation and Analysis of the generated SPICE model.

PSPICE AD9.1 tool is used to simulate the SPICE Circuit / Spice Model (.cdr file loaded) of Pspice AD9.1.

Rmem Parameters are adjusted in order to achieve the perfect SPICE model.

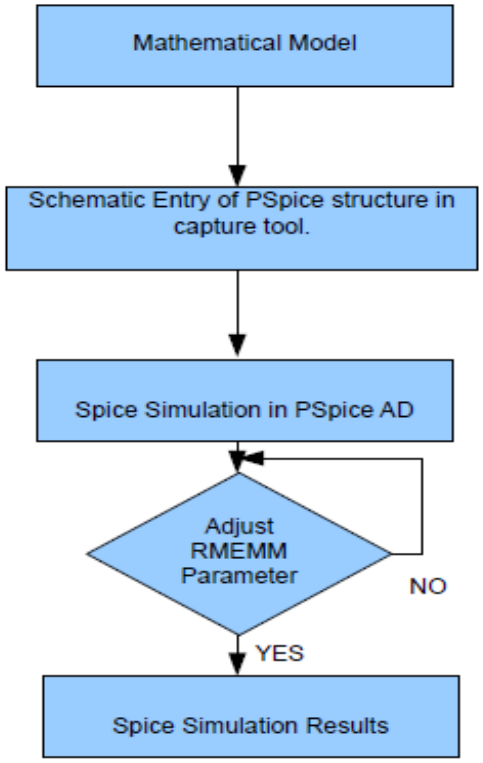

Figure 2. Process flowchart for SPICE model simulation.

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V. RESULTS

The Simulations of SPICE Memristor model Driven by Voltage using PSPICE, the width D of the TiO2 film is considered to be 10 nm and the dopant mobility μd = 10^-14 cm^2 s^-1 V^-1. The values assumed are Ron=1KΩ, Roff=100KΩ and initial resistance Rinit required to model the initial conditions of the capacitor is assumed to be 80KΩ. Figure. 3, 4, 5, 6 ,7and 8 shows simulation results.

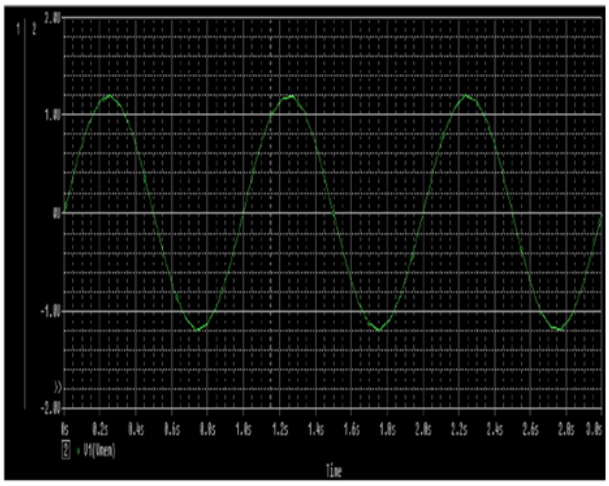

Figure 3.An input voltage applied to the memristor.

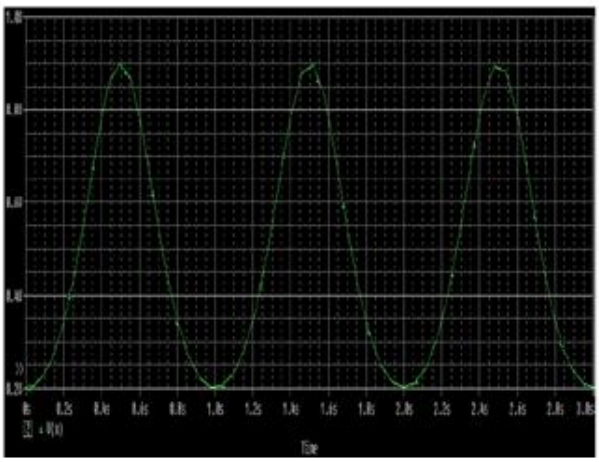

Figure 4.Waveform of the current through the memristor.

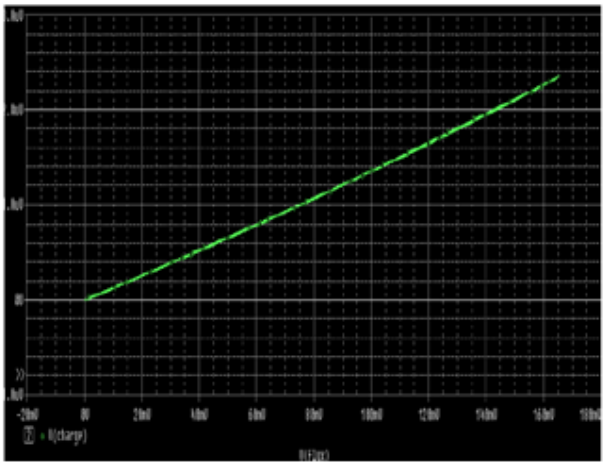

Figure 5. Charge-versus-flux curve for memristor.

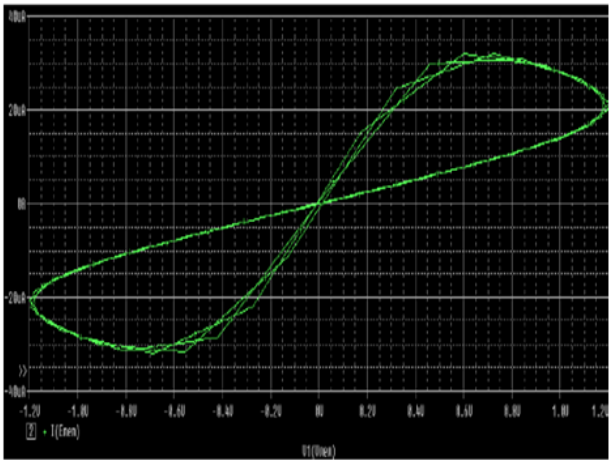

Figure 6. V I curve for input frequency of 1 Hz.

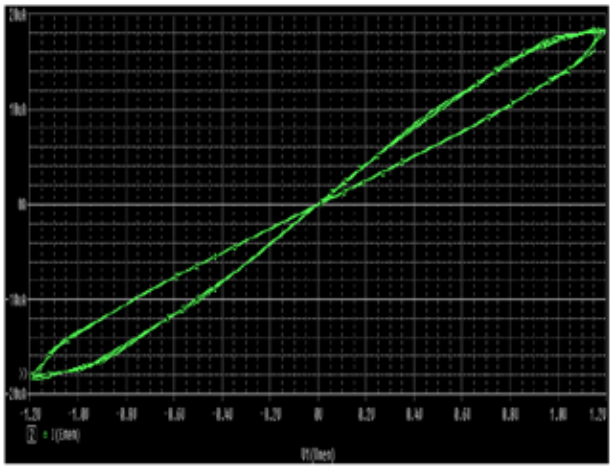

Figure 7. V I curve for input frequency of 1.5 Hz.

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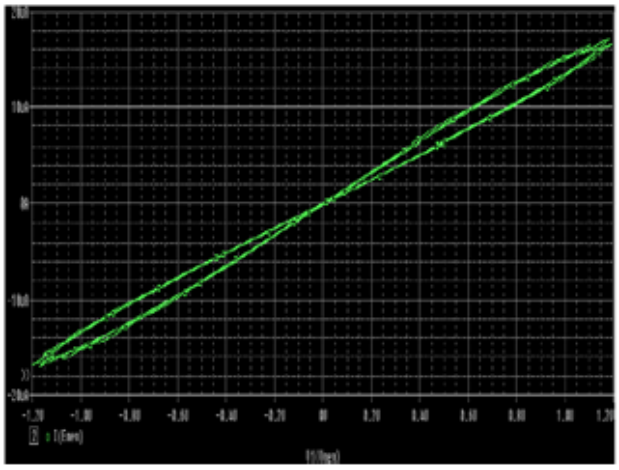

Figure 8. V I curve for input frequency of 2 Hz.

From Figure. 5, we can see that the flux—charge curve is a monotonically increasing curve. We can also observe the current—voltage "pinched hysteresis loop" and the hysteresis loop in Figure.11, There is shrinking in hysteresis loop with the increase in the input frequency. Thus, all the properties that are said to be a signature of a memristor are satisfied.

VI. Application Of Memristors

Its implications are extraordinary. And few applications of Memristors are NVRAM , FPGA's, MIMICING THE BRAIN (neural network) and ANALOG PARALLEL COMPS.

VII. Conclusion

The properties of the memristor and its model is simulated by subjecting it to various input voltages and noting the results obtained.

By redesigning certain elements of circuits by including Memristors, it's possible to obtain the same circuit function with fewer components, making the circuit itself cost effective and significant reduction in its power consumption. In fact, it can be hoped to combine traditional circuits elements with Memristors to produce a device to perform similar computation. Simulation tools and various models will help built efficient analog circuits. The SPICE models will empower to develop innovative circuits. With Possibility of fabricating Memristor and circuits on single CMOS wafer will make electronic system much cheaper and efficient.

Nanoscale devices will automatically bring in memristive effect which cannot be ignored to design a functioning circuits. Thus, 21st century might be revolutionize by Memristors as transistor did in 20th century.

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