A Compact SPICE Model of Unipolar Memristive Devices

Xudong Fang, Xuejun Yang, *Member, IEEE*, Junjie Wu, and Xun Yi

***Abstract*—This paper introduces a compact SPICE model of unipolar memristive devices. The model is based on the unipolar memristive system equations with the assistance of two resistance switching velocity functions for controlling the SET and RESET processes, respectively. Our model is highly parameterized by providing various adjustable model parameters. We verify the functionality of our model by the HSPICE simulation with parameters abstracted from a real device and a previous model. As an example of model application, we successfully use the model to simulate the stateful logic operations of the memristive implication gate circuit. Compared with previous models, the proposed model is of good efficiency, accuracy, and usability.**

***Index Terms*—Compliance current, memristive, model, simulation program for integrated circuits emphasis (SPICE), stateful logic, unipolar.**

I. Introduction

In recent years, the search for novel memory technologies and devices is right under the way due to the fact that conventional CMOS memory technologies are approaching their scaling limit [1]. Among the various novel candidate memory technologies, memristive devices (or in a narrow sense, resistive RAMs) have been considered as one of the most promising next-generation memory technologies in view of their low-power consumption, excellent scalability, simple cell structure, CMOS process compatibility, and especially, nonvolatile state-holding capability [2]–[7]. Besides the application to nonvolatile memories, memristive devices are also being studied for building stateful logic gates [8]–[10], modeling synapse in neuromorphic systems [7], [11], [12], and processing analog signals [13]–[15].

A memristive device usually stores one bit of information by its high-resistance state (HRS, OFF) and low-resistance state (LRS, ON), and the device resistance can be switched by external applied voltage or current [16], [17]. According to their resistive switching behaviors, memristive devices can be divided into two categories: unipolar and bipolar. For unipolar devices, the switching procedure does not depend on the polarity of the voltage and current signal, while for bipolar devices, SET to the ON state occurs at one voltage/current polarity and RESET to the OFF state occurs at the other voltage/current polarity [2], [3]. Note that the word *unipolar* is equivalent to the word *nonpolar* in describing a device, and the latter is used by some authors such as Liu *et al*. in [18].

Currently, both unipolar and bipolar devices have been used to build nonvolatile memories [4]–[7], [19], [20]. Generally speaking, compared with bipolar memristive devices, unipolar memristive devices usually feature larger switching ratio and better linear *I–V* correlation in LRS, which makes them good memory element candidates [18]–[20]. As for building crossbar memory, some researchers claimed that unipolar memristive devices are better than their bipolar counterparts in the sense that memory architectures built on the latter are more complex than those on the former [21]. This is not necessarily true in the real situation. Nevertheless, unipolar memristive devices do have an advantage in the one-diode one-memristor (1D1M) crossbar structure, since using unipolar memristive devices to construct 1D1M crossbars can both avoid the sneak path (or crosstalk) problem in the READ operation and solve the unwritable problem in the WRITE operation [22], [23].

Recently, there have already been a plethora of circuit models proposed for bipolar memristive devices [24]–[29]. However, an efficient and working circuit model for unipolar memristive devices can hardly be found. Therefore, it is quite necessary to develop a practical and compact circuit-level behavioral model of unipolar memristive devices for design and experiment with those devices.

In this paper, we propose an efficient and compact circuit model of unipolar memristive devices which can be integrated in any simulation program for integrated circuits emphasis (SPICE)-compatible circuit simulators. In order to build the SPICE model, we first derive the unipolar memristive system equations from the general memristive system equations [16], [30], [31], with the assistance of two resistance switching velocity functions (RSVFs) for controlling the SET and RESET processes, respectively. Our model is highly parameterized. The SET and RESET voltage thresholds, compliance current, and RSVFs that control the model behavior are set as model parameters, thus facilitating the use of the model.

Through the simulation in HSPICE with parameters abstracted from a real device and a previous model, we verify the functionality of our model and demonstrate that the proposed model satisfies all of the unipolar memristive device properties such as the ON/OFF resistive switching corresponding to voltage pulses and the unique *I–V* characteristics with current compliance. Using the proposed model, we successfully simulate the stateful logic operations of the memristive implication

Manuscript received December 11, 2012; revised June 5, 2013; accepted July 16, 2013. Date of publication July 30, 2013; date of current version September 4, 2013. This work was supported by the National University of Defense Technology. The review of this paper was arranged by Associate Editor A. Ghosh.

The authors are with the State Key Laboratory of High Performance Computing, National University of Defense Technology, Changsha 410073, China (e-mail: fangxudong@nudt.edu.cn; xjyang@nudt.edu.cn; junjie.ben@gmail.com; yixun@nudt.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2013.2275178

gate circuit, which demonstrates that our model can be applied to simulating stateful logic operations based on the unipolar memristive devices. The efficiency, accuracy, and usability of the model are shown in comparison with other models, and we also discuss the compliance current dependence issue and conclude that our model is able to reflect the compliance current (or temperature) effects on the real devices by precalculating required parameters of the model.

The rest of this paper is organized as follows. Section II details the modeling methodology. Section III shows the circuit structure of the model as well as its SPICE implementation. The experimental verification is done in HSPICE and presented in Section IV. In Section V, we use the proposed model to simulate the stateful logic operations of the memristive implication gate circuit as an example of model application. Comparison with previous models and the compliance current dependence issue of the model are discussed in Section VI. Finally, we summarize the paper in Section VII.

II. Unipolar Memristive System Equations

A memristive device can be described by the memristive system equations [30], which consist of a port equation and a state equation. The equations can take either a voltage-controlled form or a current-controlled form, and the two forms are equivalent mathematically. Since the most experimental data are attained and presented in the voltage sweep mode, we choose the voltage-controlled form. The nth-order voltage-controlled memristive system [30] is represented by

$$I_m = R_m^{-1}(\boldsymbol{x}, V_m, t)V_m \tag{1}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, V_m, t) \tag{2}$$

where V_m and I_m denote the voltage and current through the device, respectively, $\boldsymbol{x}$ is an n-dimensional vector denoting the internal states of the system, and the function R_m defines the memristance[1] of the system. (1) is called the port equation and (2) the state equation.

According to Chua, all the two-terminal nonvolatile memory devices based on the resistance switching are memristors, regardless of the device materials or the physical operating mechanisms [31]. Therefore, unipolar memristive devices also abide by the memristive system equations. For unipolar memristive devices, switching with threshold voltages is an intrinsic feature [2], [3]. The SET and RESET events happen by applying the voltage of one polarity and can occur both at the positive and negative voltage branches. The device in LRS/HRS is switched to HRS/LRS (RESET/SET process) by applying a voltage pulse with an absolute value larger than the RESET/SET threshold voltage. Note that for unipolar devices, the absolute value of SET threshold voltage is always larger than that of the RESET threshold voltage, and the RESET process will complete before the applied voltage reaches the SET threshold voltage.

In the real case, when the SET process is initiated, the current through the device will soar to a rather large value when the device approaches the ON state. In practice, the device current is usually limited by a compliance current to protect the device from the hard dielectric breakdown in the SET process [2], [3]. Furthermore, the internal states of unipolar memristive systems are narrowed down to just one state, i.e., memristance, which is the main concern of our model. With all the aforementioned factors taken into consideration, the general memristive system equations (1) and (2) are modified to the unipolar memristive system equations, which take the form of

$$I_m = \begin{cases} x^{-1}V_m, & |V_m| < V_{\rm set} \\ I_{cc}, & |V_m| \geq V_{\rm set} \end{cases} \tag{3}$$

$$\frac{dx}{dt} = \begin{cases} v_{\rm rst}(V_m)H(R_{\rm off} - x), & V_{\rm rst} \leq |V_m| < V_{\rm set} \\ v_{\rm set}(V_m)H(x - R_{\rm on}), & |V_m| \geq V_{\rm set} \\ 0, & \text{otherwise} \end{cases} \tag{4}$$

where in (3), $V_{\rm set}$ is the threshold voltage for the SET process, V_m and I_m are the voltage and current across the device, x is a scalar here and is equivalent to memristance ($x \equiv R_m$, since memristance is the only internal state chosen), and I_{cc} is the compliance current. Note that the compliance current is imposed only on the SET process to protect the device from hard dielectric breakdown, while in the RESET process I_m may be well beyond I_{cc}.

In (4), $V_{\rm rst}$ is the threshold voltage for the RESET process, $v_{\rm set}$ and $v_{\rm rst}$ are RSVFs for the SET and RESET processes, respectively (generation of $v_{\rm set}$ and $v_{\rm rst}$ is detailed later in this section). $R_{\rm off}$ and $R_{\rm on}$ are the memristance of HRS (OFF) and LRS (ON). $H(\ldots)$ is the *Heaviside* step function (unit step function) which takes the form of

$$H(y) = \frac{1}{2}(\text{sgn}(y) + 1) \tag{5}$$

where sgn$(\ldots)$ is a sign function.[2] The two $H(\ldots)$ functions guarantee that the memristance varies only between $R_{\rm on}$ and $R_{\rm off}$. Specifically, $H(x - R_{\rm on})$ makes sure that x never falls below $R_{\rm on}$ in the SET process and $H(R_{\rm off} - x)$ makes sure that x never rises above $R_{\rm off}$ in the RESET process.

With the memristive system equations in place, we can start to build the unipolar model. However, to make sure that the corresponding switching processes occur and only occur when V_m falls in the corresponding voltage ranges, as shown in (3) and (4), we propose two voltage threshold functions (VTFs) S and T in advance to realize the switching with thresholds.

A. Voltage Threshold Functions

We propose two VTFs, S and T, which serve as the tool functions to effect the switching with thresholds for the SET and RESET processes, respectively. The two VTFs are realized by the sign function and absolute value function,[3] which can be readily found in SPICE dialects such as HSPICE [32] and

[1] Memristance is of the same unit (Ω) with resistance, so we will not differentiate between the two in the rest of the paper.

[2] A sign function is defined in the form of sgn(x), which returns -1, if x is less than 0; 0, if x is equal to 0; and 1, if x is greater than 0.

[3] An absolute function is defined in the form of $abs(x)$, which returns the absolute value of x : $|x|$.

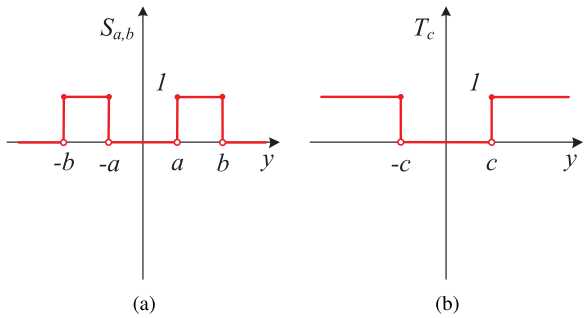


Fig. 1. Curves for the VTFs. (a) $S_{a,b}$ for RESET and (b) T_c for SET.

PSPICE [33]. S and T take the form of

$$S_{a,b}(y) = \text{sgn}[\text{sgn}(|y| - a) - \text{sgn}(|y| - b)] \tag{6}$$

$$T_c(y) = \text{sgn}[\text{sgn}(|y| - c) + 1] \tag{7}$$

where a and b are the threshold parameters, as shown by the breaking points of the curve in Fig. 1(a), and so is c in Fig. 1(b). In our model, a and c are substituted by V_{rst} and V_{set}, respectively, while b should be set to a value no greater than V_{set}, since the RESET process should well complete when V_m reaches V_{set}. As shown in Fig. 1, the magnitudes of (6) and (7) are either 0 or 1. With the help of VTFs, we can guarantee that the memristance of the model only changes in the voltage ranges where the values of the VTFs are equal to 1, thus realizing the switching with thresholds. By setting b to V_{set}, the VTFs take the forms of $S_{V_{\text{rst}},V_{\text{set}}}$ for the RESET process and $T_{V_{\text{set}}}$ for the SET process.

B. Resistance Switching Speed Functions

When the voltage threshold switching conditions are met, we have to know the resistance switching speed at any given applied voltage. The resistance switching speed functions (RSSFs), f and g, are proposed to designate the resistance switching speed for the SET and RESET processes, respectively, at any applied voltage. An RSSF may take a linear form or a nonlinear form, or even in a transcendental form, depending on the device characteristics and experimental environments such as temperature. Meanwhile, the RSSFs for SET and RESET are usually not the same since the physical mechanisms for SET and RESET are distinct. This is different from bipolar memristor models whose resistance switching speed is controlled by average ion mobility and window functions, and whose forward and backward resistance switching speeds are the same. Since there are few researches about the switching speed of unipolar memristive devices, we set RSSFs for SET and RESET as parameter functions in the model, and assume RSSFs in a linear form for simplicity in this paper. However, if further experimental data on the switching time are given, we can change the RSSFs into other forms to better model the device behavior. The RSSFs used in this paper take the form of

$$f(V_m) = \alpha|V_m| \tag{8}$$

$$g(V_m) = \beta|V_m| \tag{9}$$

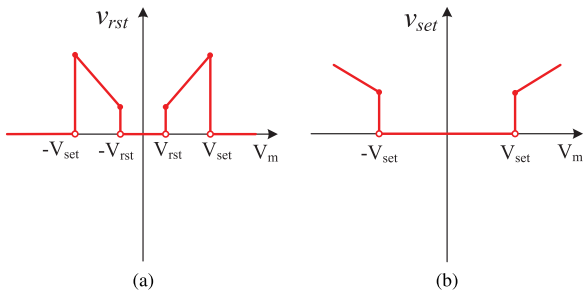


Fig. 2. Curves for the RSVFs. (a) v_{rst} for RESET and (b) v_{set} for SET.

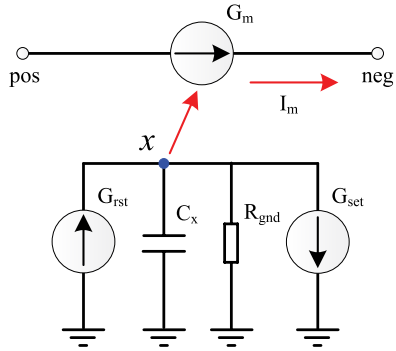


Fig. 3. Structure of the unipolar SPICE model.

where α and β are the coefficients for the SET and RESET resistance switching speeds, respectively. Note that setting RSSFs in a linear form does not mean that the resistance switches at a linear speed. To obtain a linear resistance switching speed, RSSFs should be set to constants.

C. Resistance Switching Velocity Functions

An RSVF specifies the resistance switching speed at a given applied voltage with voltage threshold constraints and is obtained by multiplying an RSSF with a VTF. Using the VTFs [see (6) and (7)] and RSSFs [see (8) and (9)] proposed previously, the RSVFs for SET and RESET can be expressed as

$$v_{\text{rst}}(V_m) = f(V_m)S_{V_{\text{rst}},V_{\text{set}}}(V_m) \tag{10}$$

$$v_{\text{set}}(V_m) = g(V_m)T_{V_{\text{set}}}(V_m). \tag{11}$$

The curves for the two RSVFs are shown in Fig. 2. The voltage range $[V_{\text{rst}}, V_{\text{set}})$ is where the RESET process happens and the voltage range $[V_{\text{set}}, +\infty)$ is where the SET process happens. With the RSVFs, the resistance switching velocity can be obtained at any applied voltage.

III. SPICE MODEL IMPLEMENTATION

In this section, we propose the HSPICE implementation of the unipolar memristive system equations in Section II. It is worth noting that although the model is implemented in HSPICE, it can also be realized in other SPICE dialects such as PSPICE.

The circuit structure of the proposed SPICE model is shown in Fig. 3. The unipolar memristive device is represented by a two terminal (pos, neg) subcircuit block. The port equation (3)

```
.SUBCKT unipolar_mem pos neg
.PARAM  Icc=30m                                   $ compliance current
.PARAM  Ron=16                                    $ ON resistance
.PARAM  Roff=160k                                 $ OFF resistance
.PARAM  Rinit=16                                  $ initial resistance
.PARAM  a=5E10                                    $ coefficient for RESET
.PARAM  b=1E10                                    $ coefficient for SET
.PARAM  Vrst=0.8                                  $ RESET threshold voltage
.PARAM  Vset=1.8                                  $ SET threshold voltage
.PARAM  delta=0.1                                 $ voltage offset
.PARAM  S(y)='sgn(sgn(abs(y)-Vreset)-sgn(abs(y)-Vset))'   $ Eq(6)
.PARAM  T(y)='sgn(sgn(abs(y)-Vset)+1)'                    $ Eq(7)
.PARAM  f(y)= 'a*abs(y)'                                  $ Eq(8)
.PARAM  g(y)='b*abs(y)'                                   $ Eq(9)
.PARAM  wrst(y)= 'S(y)*f(y)'                              $ Eq(10)
.PARAM  wset(y)='T(y)*g(y)'                               $ Eq(11)
1 Gm pos neg value='(abs(V(pos,neg))/V(x)-Icc)>0&&
  + (abs(V(pos,neg))>=(Vset-delta) ? Icc*sgn(V(pos,neg))  $ Eq(3)
  + : V(pos,neg)/V(x)'
2 Grst 0 x value='V(x)<Roff ? wrst(V(pos,neg)) : 0'
3 Gset x 0 value='V(x)>Ron ? wset(V(pos,neg)) : 0'        $ Eq(4)
4 Cx x 0 0.1
5 .IC V(x) 'Rinit'
6 Rgnd x 0 1T
.ENDS
```

Fig. 4. HSPICE implementation of the proposed model. The corresponding equations realized by the HSPICE codes are listed in the comments.

is modeled by the circuit in the upper part of Fig. 3. The voltage-controlled current source G_m generates the output current I_m according to the voltage $V(x)$ on the capacitor C_x. The state equation (4) is modeled by the circuit in the lower part of Fig. 3. The two voltage-controlled current source $G_{\rm set}$ and $G_{\rm rst}$ are both connected in parallel with C_x. The memristance of the modeled device is represented by the voltage $V(x)$ on C_x. The RESET process is modeled by letting $G_{\rm rst}$ feed charge into C_x, while the SET process is modeled by letting the reversely connected $G_{\rm set}$ drain charge away from C_x. The resistor $R_{\rm gnd}$ provides a dc path from the node x to ground, which is used by the simulator to determine the initial dc operating point in the simulation. $R_{\rm gnd}$ will not affect simulation results since it is endowed with a huge resistance. Note that the initial forming process is omitted from the model for simplicity (this will not affect the modeling since a real device is always used after initial forming).

The SPICE implementation of the circuit model in Fig. 3 is shown in Fig. 4. Our implementation is highly parameterized as depicted by the various $.PARAM$ cards. To be specific, the adjustable model parameters include ON/OFF resistances $R_{\rm on}/R_{\rm off}$, initial resistance $R_{\rm init}$, compliance current I_{cc}, SET and RESET voltage thresholds $V_{\rm set}$ and $V_{\rm rst}$, switching coefficients for SET and RESET α and β, voltage offset $delta$, and the adjustable parameter functions include RSVFs S and T and RSSFs f and g.

The HSPICE code of our model is very compact. Only six lines of functional SPICE code are needed to realize the model functions, as shown in the dashed block in Fig. 4. In contrast, the model proposed in [34] is implemented by at least 20 lines of functional SPICE code. In our model, SPICE code line 1 implements the circuit in the upper part of Fig. 3, namely, the port equation (3). The ternary function[4] in the expression of G_m is used to impose the compliance current limitation. The IF clause of the ternary function has two conditions: the former checks whether the port current is larger than the compliance current and the latter guarantees the compliance current limitation is only imposed on the SET process ($V_{\rm set}$ is subtracted by a little voltage offset $delta$ to reinforce the compliance current when the applied voltage sweeps back across $V_{\rm set}$.). The applied voltage in the expression of G_m is wrapped by the absolute function $abs()$ to make sure that the switching behavior is exactly symmetrical in the negative voltage branch when the opposite voltage is applied to the model.

SPICE code lines 2–6 implement the circuit in the lower part of Fig. 3, namely, the state equation (4). The resistance switching velocity function $v_{\rm set}$ and $v_{\rm rst}$ are integrated in the expressions of $G_{\rm set}$ (line 2) and $G_{\rm rst}$ (line 3), respectively, thus providing resistance switching speeds with threshold constraints. The two ternary functions in the expressions of $G_{\rm rst}$ and $G_{\rm set}$ correspond to the two $H(\ldots)$ functions in (4), respectively, which guarantees that the resistance of the model device will never raise above $R_{\rm off}$ and fall below $R_{\rm on}$. The initial memristance of the model, namely, the voltage on the capacitor C_x specified by line 4, is set by the $.IC$ statement in line 5. The resistor $R_{\rm gnd}$ with huge resistance in line 6 provides a dc path from node x to ground for the simulator to calculate the initial dc operating point in the simulation.

In our model, the use of jumping current sources, $G_{\rm rst}$ and $G_{\rm set}$, however, may cause memristance boundary violation since they cannot be shut OFF immediately when the memristance reaches either boundary. Therefore, one should carefully choose a sufficient small simulation time step to counteract the memristance boundary violation effect on the model, for obtaining reliable simulation results in a specific parameter configuration. In other words, the simplicity of the proposed model leads to convergence problems that require careful adjustment of the simulation parameters, especially the simulation time step. Generally speaking, the smaller the simulation step, the smaller the memristance violation. For example, in the simulation of Fig. 5(a), when the simulation time step in the $.TRAN$ option is set to 1 ns, $Ron' = 15.1\,\Omega\,(=0.944\,Ron)$; while the time step is set to 0.5 ns, $Ron' = 15.7\,\Omega\,(=0.981\,Ron)$. We choose 1 ns in Fig. 5(a) for reliable and fast simulation.

IV. Model Simulation

In this section, we perform model simulation in HSPICE, and compare the simulation results with the real device data in [19] and with the previous model in [34], respectively. Using our model, the parameters, such as $R_{\rm on}$ and $R_{\rm off}$, $V_{\rm rst}$ and $V_{\rm set}$, and I_{cc}, can directly be obtained from the experimental data (e.g., the *I–V* curve) of the prepared device being modeled. The switching coefficients α and β have to be separately set by oneself to best fit the model behavior.

[4]A ternary function is defined in the form of $a?b:c$, which means *IF a, THEN b, ELSE c* [32].

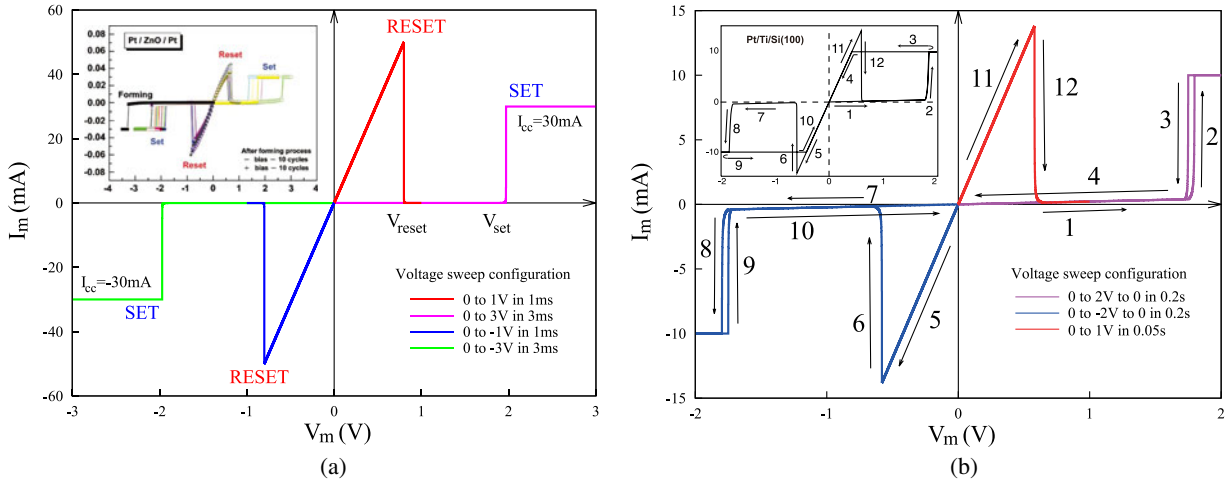


Fig. 5. Simulation results. (a) Simulated *I–V* characteristics versus the real device data in [19]. The inset shows the *I–V* curve of the real device and the legend shows the linear voltage sweep configuration. It can be seen that our model shows good agreement with the real device data. (b) Simulated *I–V* characteristics of our model versus those of the previous model in [34]. The inset shows the *I–V* curve of the model of the previous model and the legend shows the linear voltage sweep configuration. The behavior of the two models is largely the same except minor discrepancies which are explained in the text.

To model the real device, we first abstract the model parameters of the target device prepared in [19]. $R_{\rm on}$ and $R_{\rm off}$ are $16\,\Omega$ and $160\,\mathrm{k}\Omega$. $V_{\rm rst}$ and $V_{\rm set}$ are 0.8 and 1.8 V. I_{cc} is set at ± 30 mA. The switching coefficients α and β are chosen as 2×10^8 and 5×10^7, respectively. The initial state is set to $R_{\rm on}$. The simulation time step is chosen as 1 ns.

In order to reproduce the *I–V* characteristics of the target device shown in the inset of Fig. 5(a) (from [19, Fig. 2] which is the symbol curve for a unipolar memristive device), we perform voltage sweeps to the model. As shown in Fig. 5(a), in the positive branch, when a linear voltage sweep from 0 to 1 V in 1 ms is performed on the model, the expected RESET process happens when V_m passes $V_{\rm rst}$ and the model resistance is switched to $R_{\rm off}$. When another linear voltage sweep from 0 to 3 V in 3 ms is performed, the expected SET process happens when V_m passes $V_{\rm set}$ with $I_{cc} = 30$ mA and the model resistance is switched back to $R_{\rm on}$. The symmetrical resistance switching processes happen in the negative branch with $I_{cc} = -30$ mA. The simulated *I–V* curve shows rather good agreement with the *I–V* curve of the real device in the inset.

To compare the function of our model with that of the previous model in [34], we adopt the same model parameters used in [34] in the simulation. Through some computation, the parameters are obtained as follows: $R_{\rm on}$ and $R_{\rm off}$ are $42\,\Omega$ and $4.4\,\mathrm{k}\Omega$. $V_{\rm rst}$ and $V_{\rm set}$ are 0.58 and 1.75 V. I_{cc} is set at ± 10 mA. The switching coefficients α and β are chosen as 2×10^5 and 1×10^5, respectively. The initial state is set to $R_{\rm off}$. The simulation time step is chosen as $0.1\,\mu$s.

Fig. 5(b) shows the simulated *I–V* characteristics of our model and the inset shows the *I–V* characteristics of the model in [34]. Note that to produce the simulated *I–V* curve, a SET pulse is needed to switch the model resistance to $R_{\rm on}$ when the applied voltage changes polarity. It can be seen from the figure that the resistive switching behavior of the two models is the same when the applied voltage increases; however, when the applied voltage decreases, there are discrepancies between the two curves, which are denoted by arrow 3 and arrow 4 in the main figure and inset. In our model, when the applied voltage decreases and reenters the range $[V_{\rm rst}, V_{\rm set})$, the model resistance will be reset toward $R_{\rm off}$, since the voltage range $[V_{\rm rst}, V_{\rm set})$ is where the RESET process always happens in our model. In contrast, the model resistance keeps unchanged in [34] in this situation.

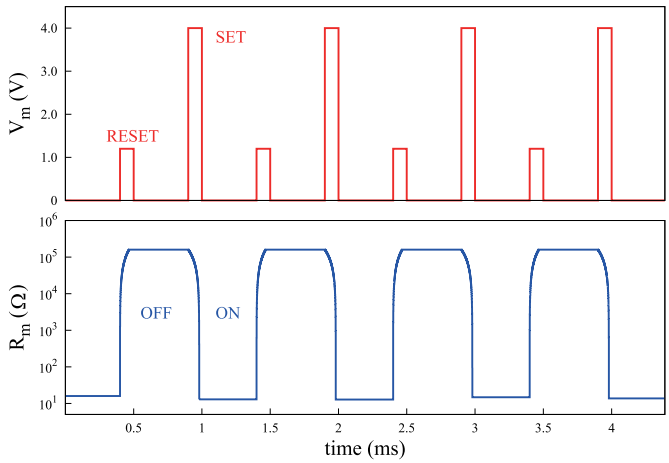


Fig. 6. Pulse responses of the proposed model with the model parameters from [19].

Although the resistance switching behavior of a real device has not been clearly defined in the literature when the applied voltage sweeps back and reenters the range $[V_{\rm rst}, V_{\rm set})$ (since it is not of main concern), it is more reasonable to assume that the RESET process will always happen in the range $[V_{\rm rst}, V_{\rm set})$, because a real device cannot discern whether the applied voltage positively enters or negatively enters the voltage range.

In addition, to check the model's usability for modeling memory cells, we present the voltage pulse responses of the model for the target device in [19]. The pulses are configured as follows: frequency 200 kHz, pulsewidth $1\,\mu$s, amplitudes 1.2 V for RESET and 3.0 V for SET. As shown in Fig. 6, the resistance state of the model is switched periodically to ON or OFF

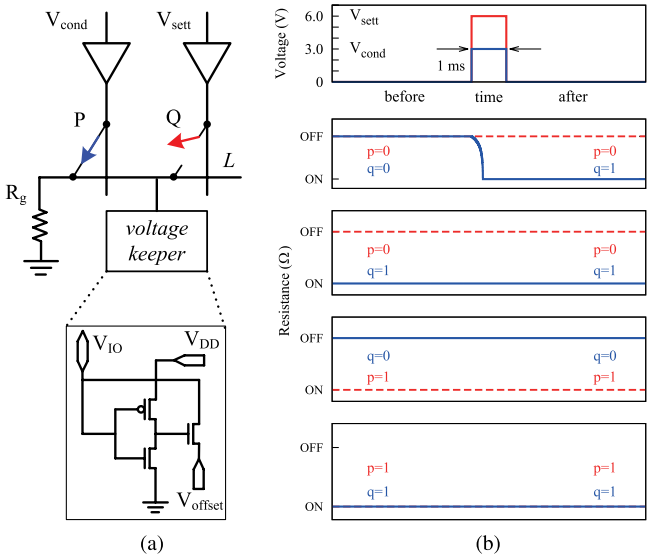


Fig. 7. Circuit structure and simulation results for the stateful implication operations. (a) Implication gate circuit with the voltage keeper. (b) Simulation results for the four resistance combinations of P and Q, where the red-dashed line denotes the resistance state of P, and the blue solid line denotes the resistance state of Q.

according to the voltage pulses applied. This result demonstrates that the model can simulate unipolar memristive memory cells quite well.

V. Model Application

In this section, we apply the proposed model to simulate the stateful logic operations of memristive implication (IMP) gates as an example of model application. The stateful IMP operations originally proposed by Borghetti *et al*. were based on bipolar switching materials [9], and later Sun *et al*. implemented the stateful IMP operations using unipolar switching devices [10]. The IMP gate circuit used in both researches is shown in Fig. 7(a), where two memristive devices P and Q are connected by a common horizontal nanowire L to the load resistor R_g. The IMP operations are implemented by simultaneously applying a $V_{\rm cond}$ pulse to P and a $V_{\rm sett}$ pulse to Q, and the result is then represented by the resistance state of Q. $V_{\rm cond}$ will not change the state of its driven device P, and $V_{\rm sett}$ is large enough to set its driven device Q. Note that the states of P and Q are represented by p and q, respectively, and logic $1(0)$ corresponds to the ON(OFF) state of the device.

When it comes to practical realization, the simple circuit of Fig. 7(a) meets a problem. In the case of both P and Q being in the OFF state (logic 0), the result of the IMP operation should be 1 since $0 \rightarrow 0 = 1$. But the simulation result shows that the resistance switching of Q will stop at an intermediate state between ON and OFF rather than reaching ON. This is because in our model the switching processes happen continuously rather than discretely and abruptly. The voltage drop on Q decreases with the reduction of the resistance of Q. When the voltage drop on Q is less than $V_{\rm set}$, the SET process will stop.

In order to obtain a full resistance switching of Q in this case, a voltage keeper circuit [35], shown in the lower part of Fig. 7(a), is added in parallel to R_g. The voltage keeper consists of a CMOS inverter and an NMOS gate, and is activated by setting V_{DD} and $V_{\rm offset}$. It keeps the voltage on the horizontal wire L low if it is initially low, otherwise it does not affect the IMP circuit. The voltage keeper can be reused by multiple logic blocks in a time multiplexing way. Note that the voltage keeper is in the peripheral circuit rather than being integrated with the nanoscale memristive crossbar, so the former will not increase the area and complexity of the latter. In fact, memristive crossbar memories [7] or memristive circuits [14], [15] always need a CMOS peripheral circuit to function as decoders or amplifiers. Nevertheless, the implication circuit can function even without the voltage keeper providing some resistance tolerance and refreshing metrics, which is beyond the scope of this paper.

The parameters for the simulation are extracted from [10]. $R_{\rm on}$ and $R_{\rm off}$ are 35 Ω and 10 kΩ. $V_{\rm rst}$ and $V_{\rm set}$ are 1.7 and 4 V. I_{cc} is ±10 mA. The switching coefficients α and β are 5×10^6 and 5×10^5, respectively. In addition, $V_{\rm cond}$ and $V_{\rm sett}$ are chosen as 3 and 6 V, and R_g is set at 500 Ω. The pulsewidth for $V_{\rm cond}$ and $V_{\rm sett}$ is 1 ms. The simulation time step is chosen as 0.1 μs. The results of the IMP operations are shown in Fig. 7(b). In all of the four cases, the correct implication results are yielded. Thus, we successfully simulate the IMP operations using the proposed model, which demonstrates that our model can also be applied to simulate stateful logic operations based on unipolar memristive devices.

VI. Discussion

In this section, we first compare our model with previous models in the literature and then discuss the compliance current (or temperature) dependence issue.

There are two circuit-level SPICE models of unipolar resistive devices which can be found in the literature. The model of Lee *et al*. [36] took no consideration for the compliance current issue and is not applicable to very-large-scale circuit-level simulation since it incorporated many nonlinear circuit elements, such as the operational amplifier and RS flip flops. The model of Akou *et al*. [34] is rather complex. For example, it used the double-well potential function, and manually set the compliance current according to the applied voltage pulse, the implementation of which is of low efficiency. Besides its complexity, one has to know the dependence of the ON state resistance and RESET current on the compliance before using the model. A detailed comparison among the three models is listed in Table I. It can be seen that our model is generally the best of the three in terms of efficiency, accuracy, and usability. Although the simplicity of our model does compromise the model convergence to some extent, it can be remedied by careful adjustment of the model parameters.

In our model, the compliance current is independent of other parameters; however, some researchers suggest that the effects of compliance current on the SET-state (ON) resistance and RESET current during the resistance switching are hardly negligible [34], [37], [38]. Although the detailed resistance switching mechanisms of unipolar memristive devices have not been revealed yet, it is generally believed that the switching is caused

TABLE I
COMPARISON OF DIFFERENT UNIPOLAR MODELS

Model	Lee *et al.* [36]	Akou *et al.* [34]	Fang *et al.* Our model
Functional code lines	N/A	>20	6
Modeling complexity	Simple	Complex	Compact
Generic and flexibility (parameter control)	Poor	Moderate	Good
Matching memristive system definition	No	No	Yes
Memristance switching	Discrete	Continuous	Continuous
Separate controls for SET and RESET	Yes	No	Yes
Model convergence	Bad	Moderate	Conditionally good
Accuracy comparing practical devices	Limited	Conditional	Good
Compliance current configuration	N/A	Manually	Automatically
Large-scale circuit simulation feasibility	No	Yes	Yes
Model portability	Limited	Good	Good

by the formation and rupture of conductive filaments under electric fields or thermal effects [2], [3], [39]. Namely, larger SET-state compliance current forms stronger filaments, thus yielding lower ON state resistance. As a result, stronger filaments need a larger RESET current to rupture.

However, as long as the analytical expression for the relation between the compliance current (or temperature) and the ON resistance (or the RESET current) is given, our model can reflect such relationship. Just as Fig. 5(b) shows, using our model, all the parameters needed are calculated in advance according to the compliance dependence relationship and then substituted into the model. Even more aggressively, the analytical equations for calculating the dependent parameters can be set as parameter functions in the model. In this way, the capacity of the model can be expanded.

VII. CONCLUSION

In summary, a compact behavioral model of unipolar memristive devices for SPICE simulation is proposed. The model is built on the unipolar memristive equations, which makes it easy to comprehend. By providing various adjustable parameters, the model is highly parameterized, which makes it easy to adopt. Using the model, we successfully simulate the stateful logic operations of the implication gate circuit, as an example of model application. Comparison with previous models shows that our model is of good efficiency, accuracy, and usability. Our model is also able to reflect the compliance current (or temperature) effects on the real devices by precalculating required parameters of the model.

REFERENCES

[1] (2011) The international technology roadmap for semiconductors: 2011. [Online]. Available: http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf

[2] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Mater.*, vol. 6, no. 11, pp. 833–840, 2007.

[3] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, no. 25–26, pp. 2632–2663, Jul. 2009.

[4] S. H. Jo and W. Lu, "CMOS compatible nanoscale nonvolatile resistance switching memory," *Nano Lett.*, vol. 8, no. 2, pp. 392–397, 2008.

[5] S. H. Jo, K.-H. Kim, and W. Lu, "High-density crossbar arrays based on a Si memristive system," *Nano Lett.*, vol. 9, no. 2, pp. 870–874, 2009.

[6] Y. C. Yang, F. Pan, Q. Liu, M. Liu, and F. Zeng, "Fully room-temperature-fabricated nonvolatile resistive memory for ultrafast and high-density memory application," *Nano Lett.*, vol. 9, no. 4, pp. 1636–1643, 2009.

[7] K.-H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, and N. Srinivasa, W. Lu, "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications," *Nano Lett.*, vol. 12, no. 1, pp. 389–395, 2012.

[8] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor-CMOS hybrid integrated circuits for reconfigurable logic," *Nano Lett.*, vol. 9, no. 10, pp. 3640–3645, 2009.

[9] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.

[10] X. Sun, G. Li, L. Ding, N. Yang, and W. Zhang, "Unipolar memristors enable "stateful" logic operations via material implication," *Appl. Phys. Lett.*, vol. 99, no. 7, pp. 072 101–072 103, 2011.

[11] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, 2010.

[12] G. Snider, R. Amerson, D. Carter, H. Abdalla, M. Qureshi, J. Léveillé, M. Versace, H. Ames, S. Patrick, B. Chandler, A. Gorchetchnikov, and E. Mingolla, "From synapses to circuitry: Using memristive memory to explore the electronic brain," *Computer*, vol. 44, no. 2, pp. 21–28, Feb. 2011.

[13] M. Itoh and L. O. Chua, "Memristor oscillators," *Int. J. Bifurcat. Chaos*, vol. 18, no. 11, pp. 3183–3206, 2008.

[14] Y. Pershin and M. Di Ventra, "Practical approach to programmable analog circuits with memristors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1857–1864, Aug. 2010.

[15] S. Shin, K. Kim, and S.-M. Kang, "Memristor applications for programmable analog ICs," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 266–274, Mar. 2011.

[16] L. O. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.

[17] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[18] M. Liu, Q. Liu, S. Long, and W. Guan, "Formation and annihilation of Cu conductive filament in the nonpolar resistive switching Cu/ZrO_2:Cu/Pt ReRAM," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2000, pp. 1–4.

[19] W.-Y. Chang, Y.-C. Lai, T.-B. Wu, S.-F. Wang, F. Chen, and M.-J. Tsai, "Unipolar resistive switching characteristics of ZnO thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 92, no. 2, pp. 022 110–022 112, 2008.

[20] Z. B. Yan, S. Z. Li, K. F. Wang, and J.-M. Liu, "Unipolar resistive switching effect in $YMn_{1-\delta}O_3$ thin films," *Appl. Phys. Lett.*, vol. 96, no. 1, pp. 012 103–012 105, 2010.

[21] Y. Zhang, Z. Duan, R. Li, C.-J. Ku, P. I. Reyes, A. Ashrafi, J. Zhong, and Y. Lu, "Vertically integrated ZnO-based 1D1R structure for resistive switching," *J. Phys. D: Appl. Phys.*, vol. 46, no. 14, pp. 145 101–145 105, 2013.

[22] H. Manem, J. Rajendran, and G. S. Rose, "Design considerations for multilevel CMOS/nano memristive memory," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 8, no. 1, pp. 6:1–6:22, Feb. 2012.

[23] Z.-J. Liu, J.-Y. Gan, and T.-R. Yew, "ZnO-based one diode-one resistor device structure for crossbar memory applications," *Appl. Phys. Lett.*, vol. 100, no. 15, pp. 153 503–153 506, 2012.

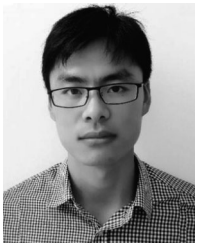
[24] Z. Biolek, D. Biolek, and V. Biolková, "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009.

[25] A. Rak and G. Cserey, "Macromodeling of the memristor in SPICE," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 4, pp. 632–636, Apr. 2010.

[26] S. Shin, K. Kim, and S.-M. Kang, "Compact models for memristors based on charge-flux constitutive relationships," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 4, pp. 590–598, Apr. 2010.

[27] D. Batas and H. Fiedler, "A memristor SPICE implementation and a new approach for magnetic flux-controlled memristor modeling," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 250–255, Mar. 2011.

[28] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: ThrEshold adaptive memristor model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 211–221, Jan. 2013.
[29] Y. V. Pershin and M. D. Ventra. (2013). SPICE model of memristive devices with threshold. [Online]. Available: http://arxiv.org/pdf/1204.2600v5.pdf
[30] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.
[31] L. O. Chua, "Resistance switching memories are memristors," *Appl. Phys. A: Mater. Sci. Process.*, vol. 102, no. 4, pp. 765–783, Jan. 2011.
[32] (1998, Jul.) Star-Hspice manual. [Online]. Available: http://web.engr.oregonstate.edu/∼moon/ece323/hspice98/files/Star-Hspice.pdf
[33] (2004, Jun.) Pspice user's guide. [Online]. Available: http://www.coe.montana.edu/ee/andyo/EE503/pspug.pdf
[34] N. Akou, T. Asai, T. Yanagida, T. Kawai, and Y. Amemiya, "A behavioral model of unipolar resistive RAMs and its application to HSPICE integration," *IEICE Electron. Exp.*, vol. 7, no. 19, pp. 1467–1473, 2010.
[35] M. Laiho and E. Lehtonen, "Cellular nanoscale network cell with memristors for local implication logic and synapses," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2010, pp. 2051–2054.
[36] J.-G. Lee, D. H. Kim, J. G. Lee, D. M. Kim, and K.-S. Min, "A compact HSPICE macromodel of resistive RAM," *IEICE Electron. Exp.*, vol. 4, no. 19, pp. 600–605, 2007.
[37] C. Rohde, B. J. Choi, D. S. Jeong, S. Choi, J.-S. Zhao, and C. S. Hwang, "Identification of a determining parameter for resistive switching of TiO_2 thin films," *Appl. Phys. Lett.*, vol. 86, no. 26, pp. 262 907–262 909, 2005.
[38] D. Ielmini, F. Nardi, and C. Cagli, "Universal reset characteristics of unipolar and bipolar metal-oxide RRAM," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3246–3253, Oct. 2011.
[39] A. Chen and M.-R. Lin, "Thermal effects and instability in unipolar resistive switching devices," in *Proc. 69th Annu. Device Res. Conf.*, 2011, pp. 167–168.



Xudong Fang was born in Zhuji, Zhejiang, China, in 1985. He received the B.S. and M.S. degrees in computer science and technology from the National University of Defense Technology, Changsha, China, in 2007 and 2009, respectively, where he is currently working toward the Ph.D. degree in the State Key Laboratory of High Performance Computing.

His research interests include supercomputer architecture, nanocomputing device architecture, and database architecture.

Xuejun Yang (M'12) received the B.S. degree from the Nanjing Communication Engineering Institute, Nanjing, China, the M.S. and Ph.D. degrees from the National University of Defense Technology, Changsha, China, in 1983, 1986, and 1991, respectively.

He is an Academician of the Chinese Academy of Science, Beijing, China, and the President of the National University of Defense Technology. He is currently a Professor in the State Key Laboratory of High Performance Computing, National University of Defense Technology. His research interests include supercomputer architecture, parallel and distributed operating system, parallel language, and compiler.

Junjie Wu received the B.S. and Ph.D. degrees in computer science and technology from the National University of Defense Technology, Changsha, China, in 2003 and 2009, respectively.

He is currently an Assistant Professor in the School of Computer Science, National University of Defense Technology. He is the Secretary General of the Technical Committee of Computer Architecture, China Computer Federation. His current research interests include computer architecture and quantum computing.

Xun Yi received the B.S. degree in computer science and technology from the National University of Defense Technology, Changsha, China, in 2006, and the Ph.D. degree in electronic device engineering from Kyushu University, Fukuoka, Japan, in 2011.

He is currently a Research Assistant Member in the State Key Laboratory of High Performance Computing, National University of Defense Technology. His research interests include design and characterization of novel semiconductor devices and novel materials for memory and logic applications, involving device fabrication and electrical characterization.