MEMRISTOR MODELING USING FINITE ELEMENT AND SPICE BASED SIMULATION

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Abstract- Memristor is a novel device which act as forth fundamental circuit element envisioned by Prof. Chua in 1971. Memristor devices has great interest in research ranging from memory and logic to neuromorphic systems due to its several advantages: non- volatality, good scalability, compatibility with CMOS technology. We study the ongoing models of memristor and compare them with known device specifications In the process of Memristor modelling using finite element, there is initial innovative approach is to implement basic model of it with the help of device modeling and simulation tool Comsol multiphysics 4.4. The successful modeling and simulation of Memristor will further lead to use for SPICE based circuit design.

Keywords- Comsol multiphysics 4.4, SPICE, Memristor

I. INTRODUCTION

In 2008, Williams et al., at Hewlett Packard, announced the first fabricated memristor device. However, a resistor with memory is not a new thing. If taking the example of nonvolatile memory, it dates back to 1960 when Bernard Widrow introduced a new circuit element named the memistor. The reason for choosing the name of memistor is exactly the same as the memristor, a resistor with memory. The memistor has three terminals and its resistance is controlled by the time integral of a control current signal. This means that the resistance of the memistor is controlled by charge. Widrow devised the memistor as an electrolytic memory element to form a basic structure for a neural circuit architecture called ADALINE (Adaptive Linear Neuron), which was introduced by him and his postgraduate student, Marcian Edward "Ted" Hoff. However, the memistor is not exactly what researchers were seeking at the nano scale. It is just a charge-controlled three-terminal (transistor) device. In addition, a two-terminal nano-device can be fabricated without nano scale alignment, which is an advantage over three-terminal nano-devices. Furthermore; the electrochemical memistors could not meet the requirement for the emerging trend of solid-state integrated circuitry.

Memristors are passive two-port elements with variable resistance (also known as a memristance). Changes in the memristance depend upon the history of the device (e.g., the memristance may depend on the total charge passed through the device, or alternatively, on the integral over time of the applied voltage between the ports of the device). To use EDA tools for simulations of memristor-based circuits, a specific memristor model is needed. Several memristor models have been proposed.A complementary GUI MATLAB program is also available in , useful for initial work with these memristor models. after long span The memristor was realized as a physical device in 2008 by HP labs research team lead by R.S.Williums. The HP memristor consists of a bipolar TiO2 thin film This discovery spurred a great interest in memristors. Memristors are considered as one of the possible future alternatives to current CMOS technology. Memristor- based technology provides much better scalability, higher utilization when used as memory, and overall lower power consumption.Formally,a current-controlled time-invariant memristive system is represented by

$$\frac{dw}{dt} = f(w, i) \tag{1}$$

$$v(t) = R(w, i)i(t) \tag{2}$$

Memory techonoly area of research captured great intrest in use of memristors because of its high density and low power consumption.To meet current increasing demand for speed of processer and its integrity current cmos based technology facing many challanges.Based on the International Technology Roadmap for Semiconductors (ITRS) report , it is predicted that by 2019, 16 nm half- pitch Dynamic Random Access Memory (DRAM) cells will provide a capacity around 46 GB/cm2, assuming 100% area efficiency. Interestingly, memristors promise extremely high capacity more than 110 GB/cm2 and 460 GB/cm2 for 10 nm and 5 nm half-pitch devices, respec- tively which is great achievement over DRAM cell. Even Static Random access memory also saturating with its physical limitations of utilisation of small area for large demand of memory capacity In addition, progress in utilizing other emerging memory technologies (such as eDRAM, mRAM, and PCRAM) is kiked back by their practical issues such

as compatibility with CMOS, their slow access time, and their limited scalability Over- all, a comprehensive study of memristor-based memory (modeling, design space, read/periphery logic) is lacking. There are many technical challenges that have to be overcome before fully utilizing memristors. One of the major challenges is designing a read circuit for the mem- ristor state. This issue arises because the read process interferes with the state of the memristor. In addition, the mathematical modeling of a memristor does not address the stability of its resistive state during the read process. Also, memristor modeling is hindered by the absence of experimental data for real memristor structures. Memristive devices can be used for applications such as memory , neuromorphic systems , analog circuits and logic design ,Different characteristics are important for the effective use of memristive devices in each of these applications, and an appropriate designer friendly physical model of a memristive device is therefore required. This paperis organised as follows section II introduces memristor as Forth fundamental circuit element postulated by chua.section III describes the SPICE model inroduced by HP lab in 2008.section IV gives comparative approach of different mathamatical models section V describes Methodology of finite element modelling (FEM) and spice simulation and result obtained.section VI conclude the paper.

II. FORTH FUNDAMENTAL CIRCUIT ELEMENT

In 1971 Luan Chua postulated hypothetical model which can sit with resister ,capacitor and inductor as Forth fundamental circuit element that connects mag- netic flux and electric charge in the same way as other three elements as shown in fig.(1) Chua showed the memristor characteristics by pinches in hysteresis loop. it was also shown that memristor cant be derived by one equation.Characterising a memristor system requires at least two equations shown in equation (1),(2). After the discovery of memristor by chua,HP lab invented memristor as physical device model in 2008 in the

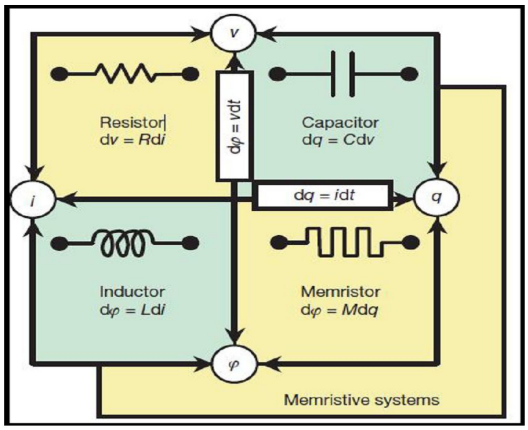

Fig. 1. Memristor:forth fundamental circuit element

form of TiO2 [6]. Their basic model had two platinum electrodes on the either end of the device. The surface of the bottom platinum wire was oxidized to make an extremely thin layer of platinum dioxide, which is highly conducting. Over this layer they deposited 2- 3 nm layer of Ti metal and the final layer was the top platinum electrode. After years of experiments, they finally realized that what theyhave was a memristor, as their i-v characteristic are similar to the one proposed by Chua.

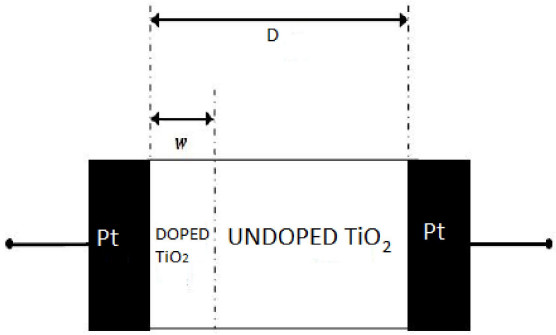

Fig. 2. memristor model

They observed that under the molecular layer, in- stead of platinum dioxide,there was only pure platinum. Above the molecular layer instead of titanium, they found an unexpected and unusual layer of titanium dioxide which was oxigen deficient which is termed as doped layer.formation of two oxide titanium results in the modulation of junctio layer on the application of external potential figure (3) shows the IV characteristics of memristor observed by HP lab.

III. SPICE MODEL OF MEMRISTOR

After characterising memristors BIOLEK formed a SPICE model using mathamatical modelling .As a

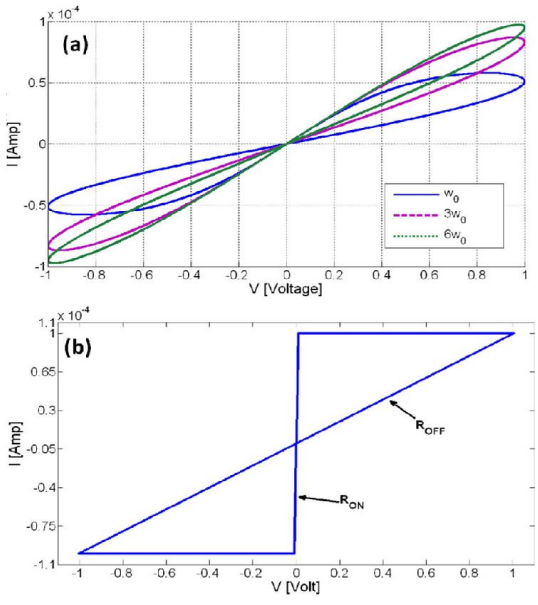

Fig. 3. I–V characteristics of Memristor

consequence of complex material processes, the width w of the doped region is modulated depending on the amount of electric charge passing through the memristor. With electric current passing in a given direction, the boundary between the two regions is moving in the same direction. The total resistance of the memristor, RMEM, is a sum of the resistances of the doped and undoped regions

$$R_{MEM}(x) = R_{ON}x + R_{OFF}(1-x) \quad (3)$$

where $x = \frac{w}{D}$ is the width of the doped region,referenced to the total legnth D of the TiO_2 layer,and R_{OFF} and R_{ON} are the limit values of the memristor resistances for $w = 0$ and $w = D$ The ratio of Two resistances is usually $10^2 - 10^3$ The Ohm's law relation is applicable between the memristor voltage and current:

$$v(t) = R_{MEM}(w)i(t) \quad (4)$$

The speed of the movement of the boundary between the doped and undoped regions depends on the resistance of doped area, on the passing current, and on other factors according to the state equation

$$\frac{dx}{dt} = Ki(t)f(x), \quad k = \frac{u_v R_{ON}}{D^2} \quad (5)$$

where u is dopant mobility. In nanoscale devices, small voltages can yield enormous electric fields, which can secondarily produce significant nonlinearities in ionic transport. These nonlinearities manifest themselves particularly at the thin film edges, where the speed of the boundary between the doped and undoped regions gradually decreases to zero. This phenomenon, called nonlinear dopant drift, can be modeled by the so-called window function f(x) on the right side of equation(3) The paper proposes the window function in the following form:

$$f(x) = 1 - (2x-1)^{2p} \quad (6)$$

where p is a positive integer. The form of function (4) guarantees zero speed of the x-coordinate when approaching either boundary. Moreover, the differences between the models with linear and nonlinear drift disappear when p increases. The SPICE model of the memristor, made up on the basis of state equations and equations modeling the boundary effects.The SPICE model of the memristor is designed such that it enables easy modification of the nonlinear relations describing the boundary effects. Such a modification can be done when the relevant data are specified by the manufacturer.Today, a lot of institutions are involved in research into the basic features of the memristor. This model triggered the invention of several linear and nonlinear models which focused the memrister applications in wide areas of research.

IV. MATHEMATICAL MODELS OF MEMRISTOR

The state of memristor is defined by its total resistance which in turn depends on width w thus 'w' is called as state variable of the memristor.increasing(decreasing) the size of doped region reduces(increases) the total resistance of the thin film by applying positive voltage to doped region. thus the memristor can be switched ON(low R) or OFF (high R) based on the direction of the current that goes through it.Memristive system can be described by

$$v = v(x, i, t) \quad (7)$$
$$\dot{x} = \dot{x}(x, i, t) \quad (8)$$

Equation (7) defines the I–V characteristic of the device. Equation (8) describes the state equation (drift equation) which models the drift speed of the charges assuming a uniform electric field applied to the device. There are many memristor models that satisfy the above two equations,which includes linear model ,nonlinear ion drift model,Team threshold adaptive memristor model,simmons tunnel barrier model[3] All the mathamatical model comparisn is summerised in the table I–V characteristics of memristor proposed by the above models is analysed using matlab 7.0. with equations of mathematical modelling proposed by strukov,williams.

TABLE I
COMPARISN OF MEMRISTOR MODELS

model	Linear	nonlinear ion drift	simmons tunnelling barrier	TEAM
state variable	$w\epsilon(0, D)$	$w\epsilon(0, 1)$	undoped region width	undoped region width
control mechanism	current controlled	voltage controlled	current controlled	current controlled
current voltage relationship	explicit	explicit	ambiguous	ambiguous
Matching memristive system defination	yes	yes	no	yes
Accuracy	lowest accuracy	low accuracy	Highest Accuracy	Sufficient Accuracy

V. METHODOLOGY

Its methodology works on the basic principles of HP Memristor Design. As the HP memristor this memristor model is also based on the fabrication of the memristor device design. The memristance of the device is depends on the following mathematical model:

$$M(p) = R_{OFF}(1 - \frac{R_{ON}}{\beta})q(t) \quad (9)$$

Where $\beta = \frac{D^2}{\mu D}$ Sievert (sV) or Weber (Wb), is defined as Dimensions of the magnetic flux $\phi(t)$. μD is Average Drift mobility in cm^2 /sV and D is TiO_2 Film Thickness. The R_{OFF} and R_{ON} are simply the 'on' and 'off' state resistances. Also q (t) defines the total charge passing through the memristor device in a time window, $(t - t_0)$. Notice that the memristor has an internal state. $q(t) = R(t-t0)i(t)dt$, as the state variable in a charge-controlled memristor gives the charge passing through the device and does not behave as storage charge as in a capacitor as incorrectly reported in some works. This concept is very important from two points of view. First of all, a memristor is not an energy-storage element. Second, this shows that the memristor is not merely a nonlinear resistor, but is a nonlinear resistor with charge as a state variable. The Design of memristive system depends on the fabrication process. It exploits a very thin-film TiO_2sandwiched between two platinum (Pt) contacts and one side of the TiO_2 is doped with oxygen vacancies, which are positively charged ions. Therefore, there is a TiO_2 junction where one side is doped and the other is un-doped. Such a doping process results in two different resistances: one is a high resistance (un-doped) and the other is a low resistance (doped). Hence, HP intentionally established a device that is illustrated in Fig. 2. The internal state variable, w, is also the variable length of the doped region. Roughly speaking, when w tends to 0 we have nonconductive channel and when w tends to D we have conductive channel.

A. FEM simulation

The FEM simulation of the device has been done using the semiconductor module of COMSOL Muliphysics. The Current design of the 2D memristor. Initial results of the memristor design shows the nonlinear behavior of the device design using i.e. with the increment of the voltage at one of the terminal of the device the device resistance is not continuously increases. In the whole simulation its resistance some times on and off.As discussed there are two types of region -doped and undoped. The doping has been done using oxigen vacancies.

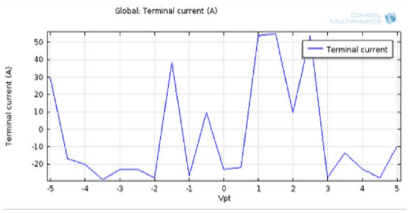

Fig. 4. Terminal current variation i.e. non-linear behaviour with applied voltage variation

The dopant concentration is given as, where dark red part shows the maximum dopant concentration.

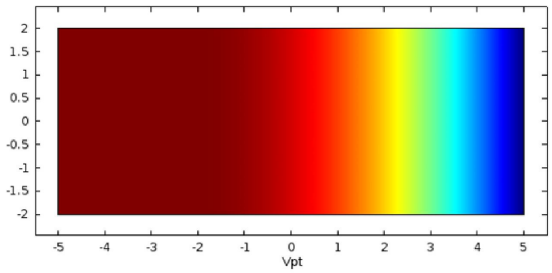

Fig. 5. Dopping concentration in memristor Device

B. Model Instantiation

memristor is first modelled using orcad simulation tool using subcircuit model presented in. modelling of memristor is then started with comsol multiphysics4:4. The modeling part of the Memristor is to simulate on available Comsol Multiphysics. In this direction the work has started from the basics of the Memristor Device modeling. The step wise work progress given as follows:

1) For Better simulation of doping region, insulation and charge carriers in a semiconductor device we have used the Semiconductor module of the Comsol Multyphysics 4.4

2) There has been used the basic device model with two Pt electrode and in middle there is given the two region Doped and Undoped TiO2.

3) In the Doped Area of the TiO2is doped with oxygen vacancies which are positively charged ions.

4) Geometry Selection of the device for 3D device Modeling. In which the D = 10nm;w = 3nm. where as for undoped bulk is designed with dimensions width = 7nm, depth= 3nm and Height= 4nm .For Doped Block Dimensions are (3,3,4)nm and for Pt electrode it is (1,3,4)nm.

C. SPICE simulation

The initial process of the Device design was to simulate and understand the device behavior on the basis of finite element modeling and simulation. After Finite element modeling the device can also be simulated using the spice code on the same stimuli condition which was applied in Finite Element Modeling. It uses some of the basic mathematical proven models to simulate its behavior in SPICE code. The memristance of the device is defined using the mathematical model stated in equation (3) Where Ron = 100 ohm, Roff = 16 kohm and X = w/D, Furthermore the memristor voltage is defined using the following defined models as given in equation (4) From HP model On the basis spice HP model we can simulate its Transient behavior for different function of the device.

Transient simulation of the device

Xmemrist aa 0 memristor Ron=100 Roff=16K Rinit=11K

D=10N uv=10F p=10

Vtest aa 0 SIN (0 1.2V 1 0 0 0)

.tran 1m 1s UIC

```
.plot tran V (aa) I (Vtest)
.option list node post=2 ingold=2 runlvl=0
.end
```

figure(6) shows the current flow in the memristor device which is not continuously increase or decrease with time it shows the on and off behavior of the memristor device along its width. figure(8) shows voltage change in the memristor device which is not continuously

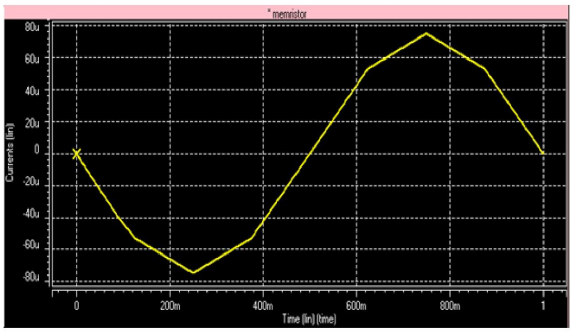

Fig. 6. current behaviour of memristor model

increase or decrease with time it shows the on and off behavior of the memristor device along its width. One of the most important properties attached with

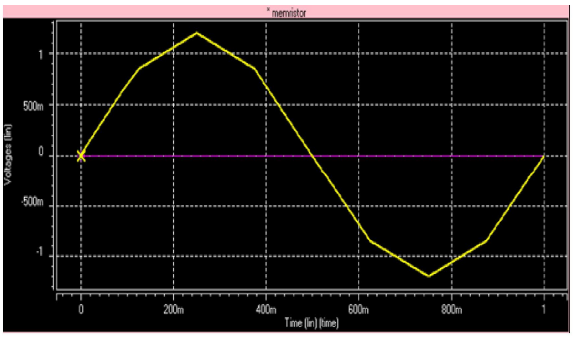

Fig. 7. voltage behaviour of memristor model

the memristive device design, the memristive device should show the hysteresis plot for its current – voltage relation. Hysteresis can be defined for its memory behavior in which it's "ON" resistance slightly change to the "OFF" resistance and when the device switch on it starts from its last conserved charge state. On the basis of its hysteresis behavior this device can be use for most of the analog operations. Next figure(9) shows its hysteresis plot.

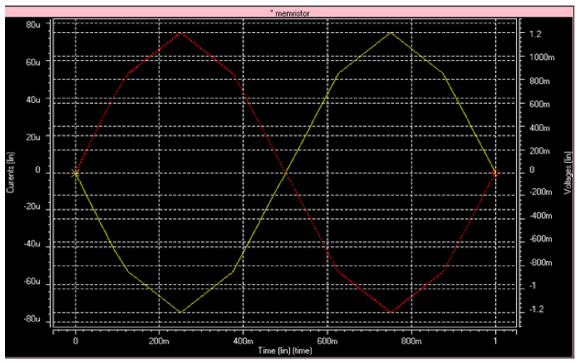

Fig. 8. Memristor Device hysterisis using transient simulation

CONCLUSION

The SPICE model of the memristor, made up on the basis of state equations and equations from the device modelling.The impact that the memristor can have on the existing technology is colossal. This paper presents the detail study of memristors on the basis of finite element modelling. Modelling of memristor using comsol multiphysics as simulation and modelling tool is become a novel approach. Memristors has certainly showed a lot of promise and also has the potential to be another milestone in the path of evolution of technology for better.

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