

Figure 1: Pulses created by rotary encoder

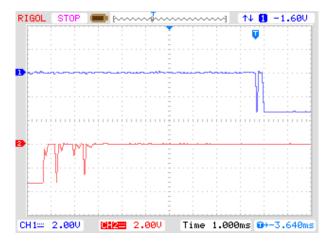


Figure 2: Multiple bounces visible when zoomed in

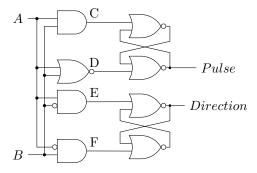


Figure 3: Logic gate circuit

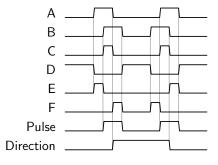


Figure 4: Clean waveforms

```
c <= a and b;
d <= a nor b;
e <= a and not b;
f <= b and not a;
dir <= dir_n nor e;
dir_n <= dir nor f;
pul <= pul_n nor d;
pul_n <= pul nor c;
pulse <= pul;
direction <= dir;</pre>
```

Figure 5: VHDL code of asynchronous design

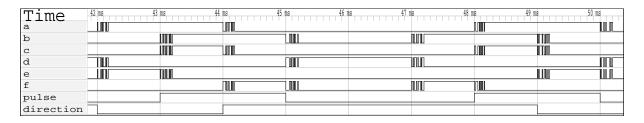


Figure 6: Waveforms of asynchronous design

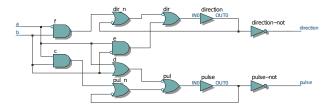


Figure 7: RTL view of asynchronous design

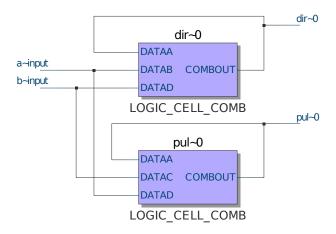


Figure 8: Reduced to two combinational loops

```
Warning: Found combinational loop of 2 nodes
Warning (332126): Node "decoder_inst|pul~0|dataa"
Warning (332126): Node "decoder_inst|pul~0|combout"
Warning: Found combinational loop of 2 nodes
Warning (332126): Node "decoder_inst|dir~0|dataa"
Warning (332126): Node "decoder_inst|dir~0|combout"
```

Figure 9: Combinational loop warning

```
c <= a xor b;
dir <= b when rising_edge(clock) and c = '1' else dir;
pul <= a when rising_edge(clock) and c = '0' else pul;
pulse <= pul;
direction <= dir;</pre>
```

Figure 10: VHDL code of synchronous design

Time	17 ms	18 ns	19 ms	20 ns	21 ns	22 ns	23 ms	24 ms	25 ns
clock									
a			Ш						
b				Ш				Ш	
С				Ш					
pulse									
direction									

Figure 11: Waveforms of synchronous design

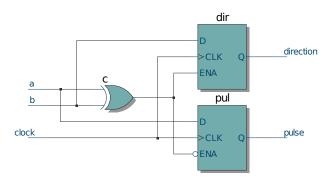


Figure 12: RTL view of synchronous design

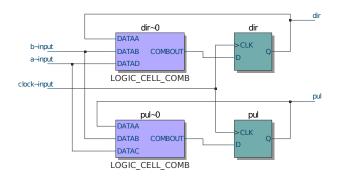


Figure 13: Technology map view of synchronous design