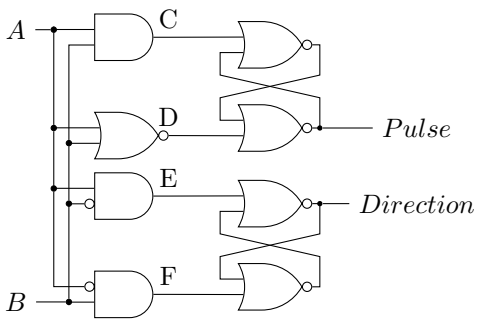

Figure 1: Logic gate circuit

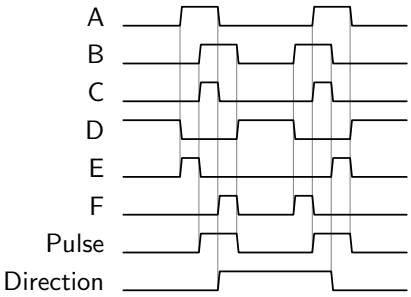

Figure 2: Clean waveforms

```
c <= a and b;
d <= a nor b;
e <= a and not b;
f <= b and not a;
dir <= dir_n nor e;
dir_n <= dir nor f;
pul <= pul_n nor d;
pul_n <= pul nor c;
pulse <= pul;
direction <= dir;
```

Figure 3: VHDL code of asynchronous design

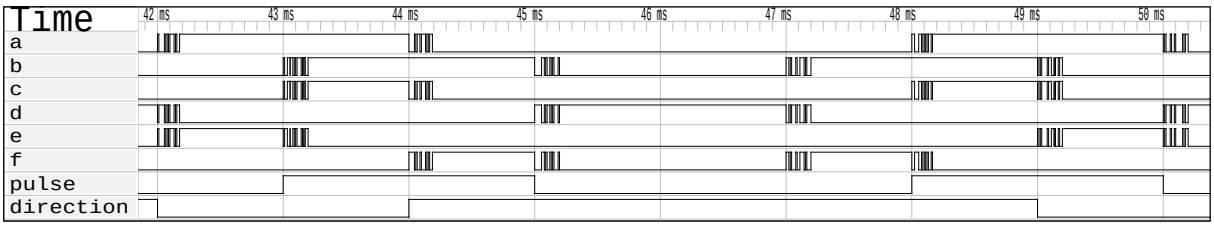

Figure 4: Waveforms of asynchronous design

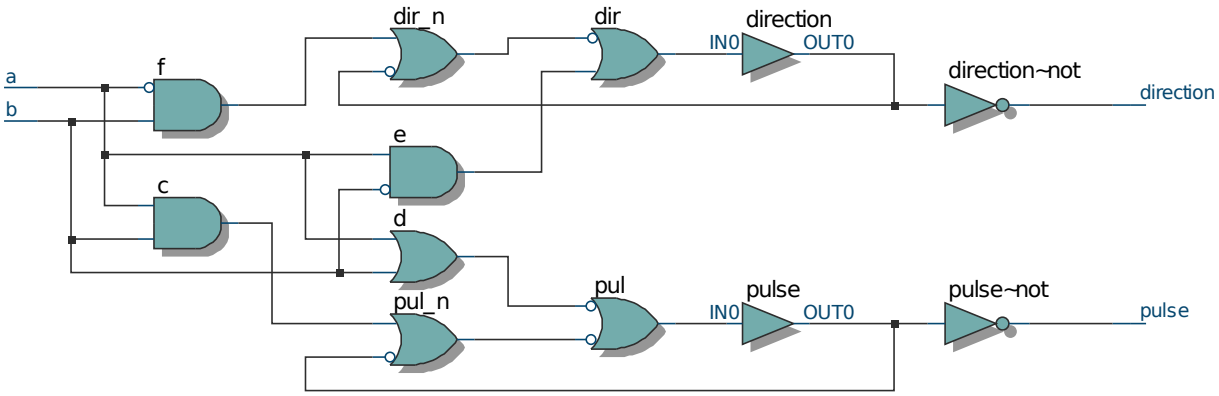

Figure 5: RTL view of asynchronous design

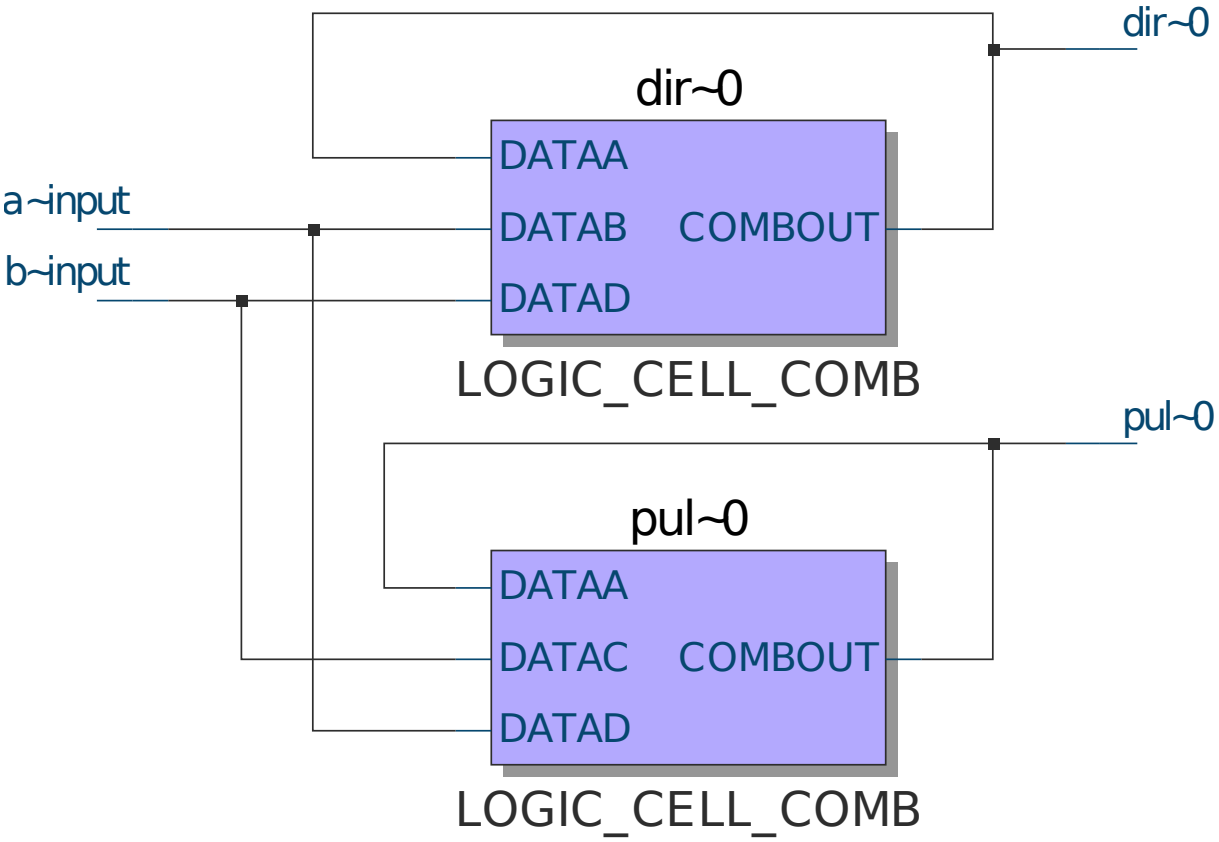

Figure 6: Reduced to two combinational loops

```
Warning: Found combinational loop of 2 nodes
Warning (332126): Node "decoder_inst|pul~0|dataa"
Warning (332126): Node "decoder_inst|pul~0|combout"
Warning: Found combinational loop of 2 nodes
Warning (332126): Node "decoder_inst|dir~0|dataa"
Warning (332126): Node "decoder_inst|dir~0|combout"
```

Figure 7: Combinational loop warning

```
c <= a xor b;
dir <= b when rising_edge(clock) and c = '1' else dir;
pul <= a when rising_edge(clock) and c = '0' else pul;
pulse <= pul;
direction <= dir;
```

Figure 8: VHDL code of synchronous design

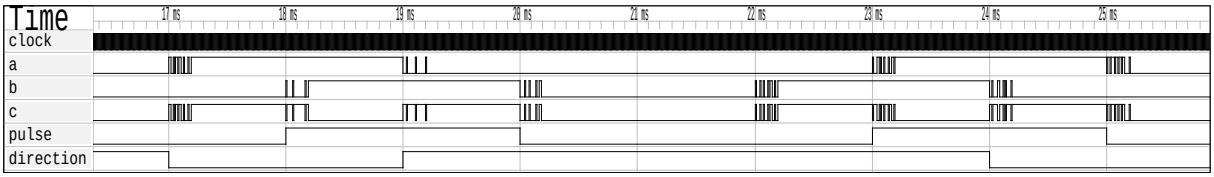

Figure 9: Waveforms of synchronous design

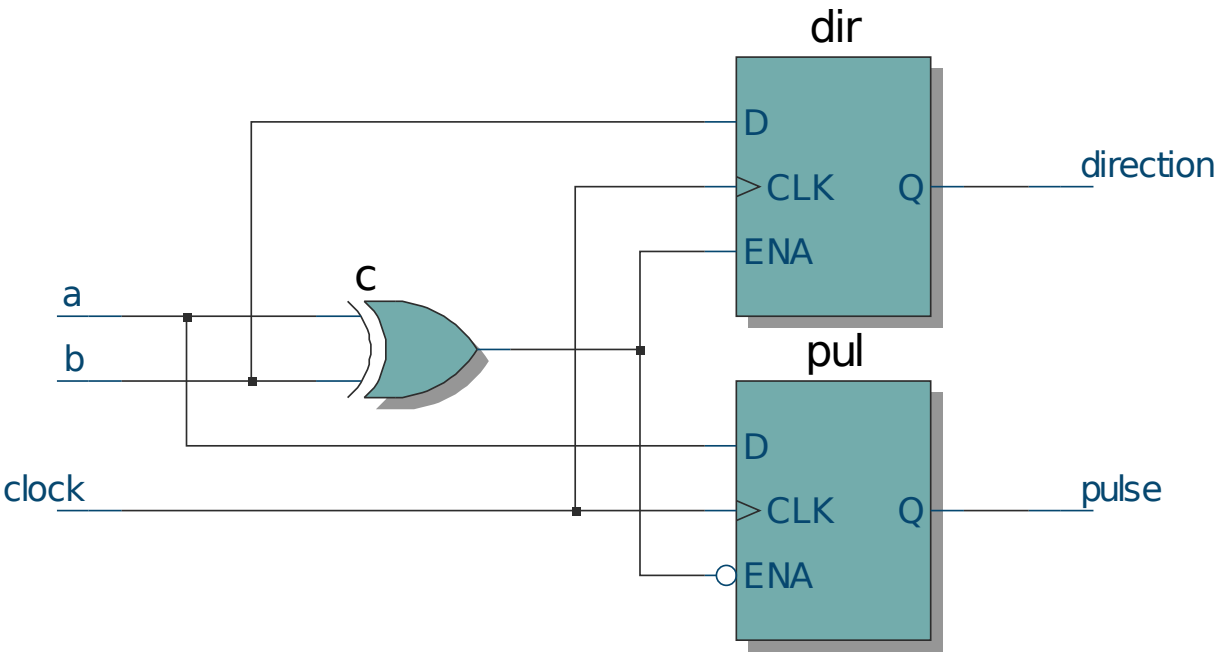

Figure 10: RTL view of synchronous design

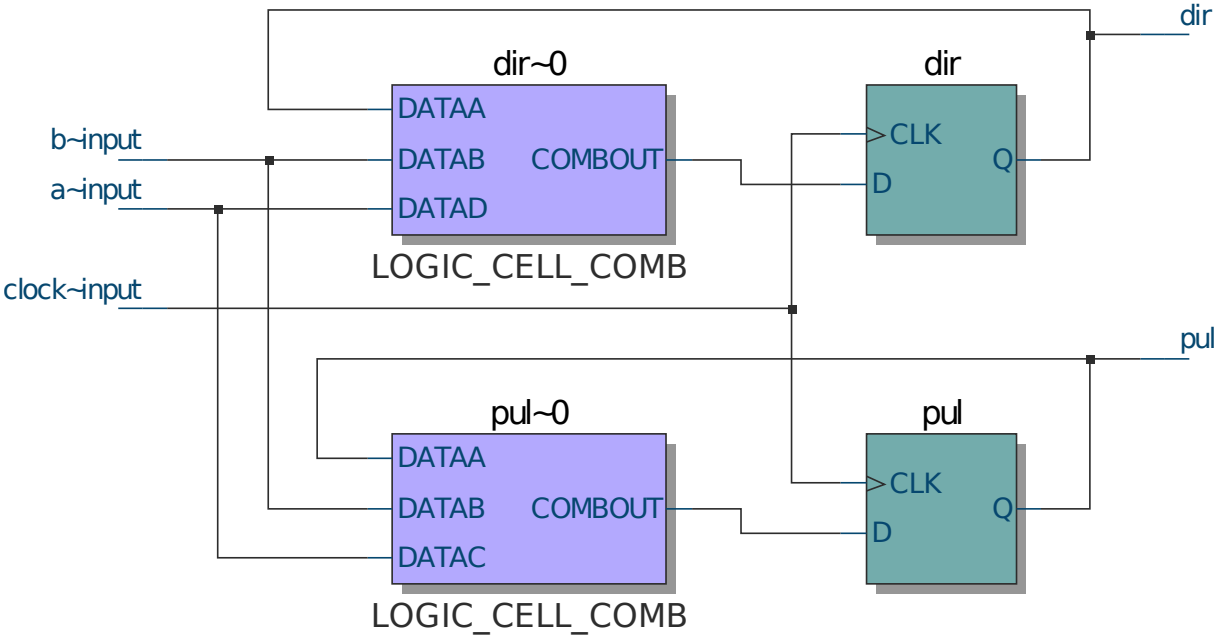

Figure 11: Technology map view of synchronous design