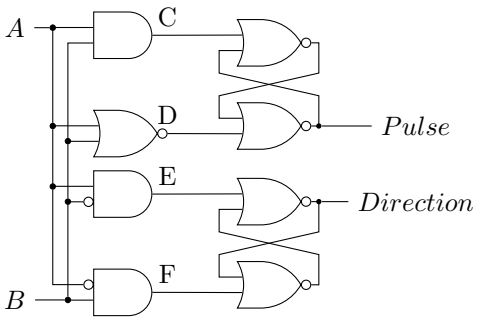


Figure 1: Logic gate circuit

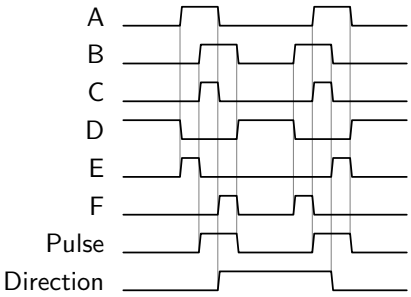


Figure 2: Clean waveforms

```
c <= a and b;
d <= a nor b;
e <= a and not b;
f <= b and not a;
dir <= dir_n nor e;
dir_n <= dir nor f;
pul <= pul_n nor d;
pul_n <= pul nor c;
pulse <= pul;
direction <= dir;
```

Figure 3: VHDL code


Figure 4: Waveforms from testbench, visualised by GTKWave

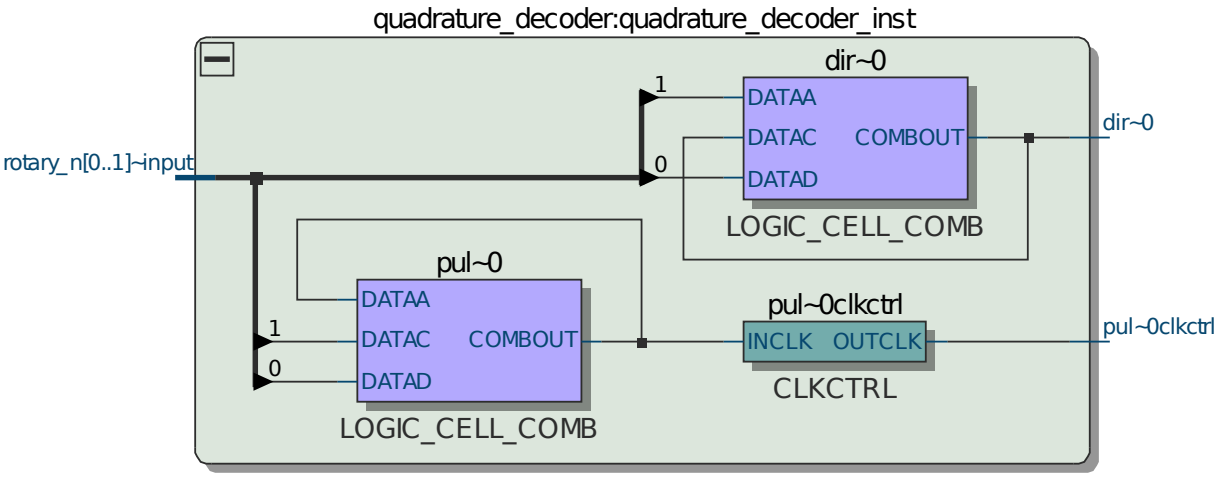


Figure 5: Reduced to two combinational loops by Altera Quartus