

Figure 1: Logic gate circuit

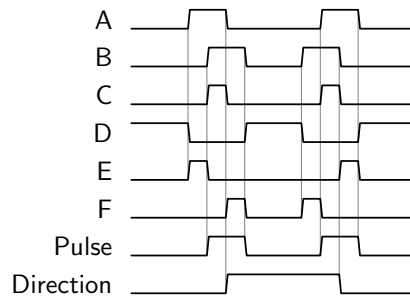


Figure 2: Clean waveforms

```

c <= a and b;
d <= a nor b;
e <= a and not b;
f <= b and not a;
dir <= dir_n nor e;
dir_n <= dir nor f;
pul <= pul_n nor d;
pul_n <= pul nor c;
pulse <= pul;
direction <= dir;

```

Figure 3: Asynchronous VHDL code

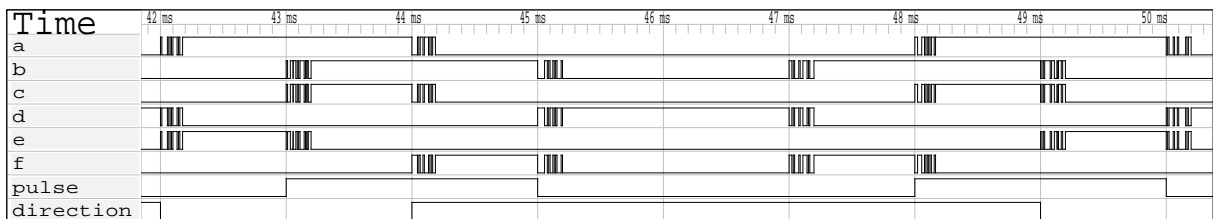


Figure 4: Waveforms of asynchronous quadrature decoder testbench, visualised by GTKWave

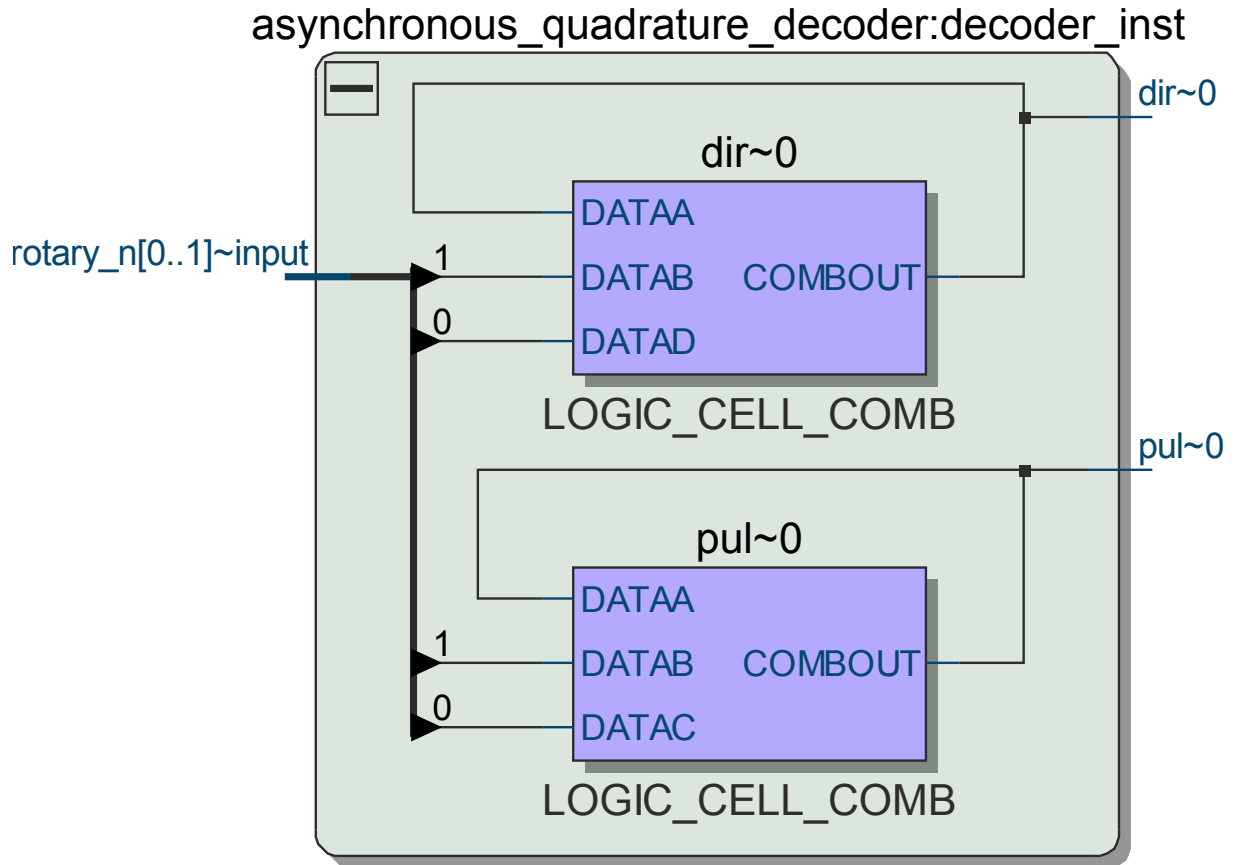


Figure 5: Reduced to two combinational loops by Altera Quartus

```
Warning (332125): Found combinational loop of 2 nodes
Warning (332126): Node "test1_inst|decoder_inst|pul~0|combout"
Warning (332126): Node "test1_inst|decoder_inst|pul~0|dataa"
Warning (332125): Found combinational loop of 2 nodes
Warning (332126): Node "test1_inst|decoder_inst|dir~0|combout"
Warning (332126): Node "test1_inst|decoder_inst|dir~0|dataa"
```

Figure 6: Combinational loop warning

```
c <= a xor b;
dir <= b when rising_edge(clock) and c = '1' else dir;
pul <= a when rising_edge(clock) and c = '0' else pul;
pulse <= pul;
direction <= dir;
```

Figure 7: Synchronous VHDL code

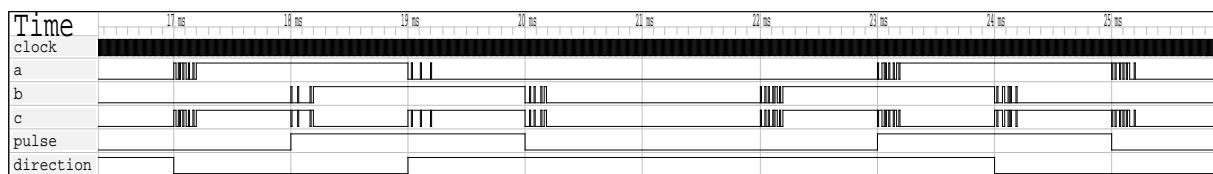


Figure 8: Waveforms of synchronous quadrature decoder testbench, visualised by GTKWave

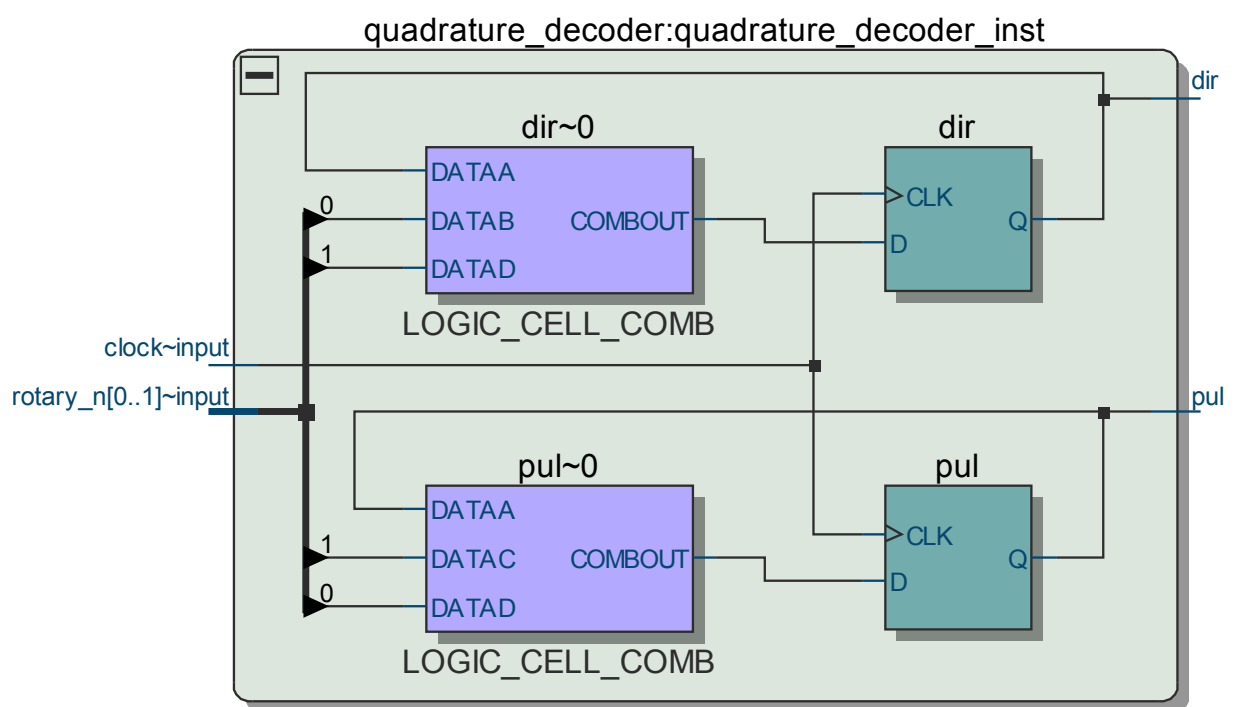


Figure 9: Reduced to two logic elements and two registers by Altera Quartus