Quadrature decoder with or without clock input
- or -
How to use a rotary encoder with an FPGA using VHDL

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Abstract

It has been a long time since I played with 74HCT devices to build an 16-Bit-ISA card bus interface. But times change and you wouldn't do that today having all these nice tools and devices. I'm talking of course about CPLD (sea of gates) and FPGA (lookup tables) devices and most important of all, their design synthesis tools. So I wanted to know, how rotary encoders work, how I could use them with FPGA's and also learn VHDL. It's gonna be fun, let's go!
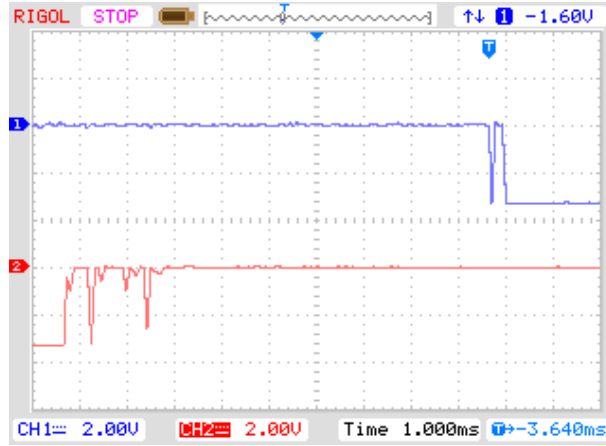
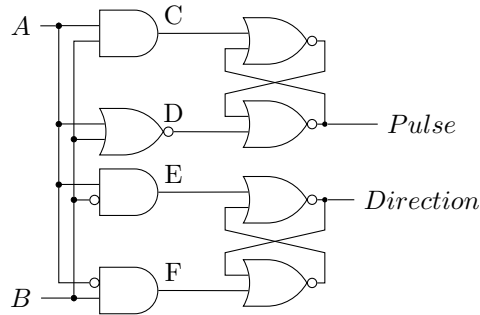Figure 1: Bounces caused by the mechanical switches of the rotary encoder
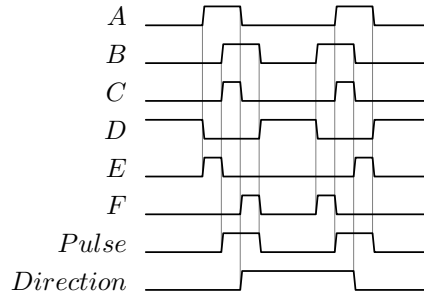

Figure 2: Logic gate circuit

Figure 3: Clean waveforms

```
c <= a and b;
d <= a nor b;
e <= a and not b;
f <= b and not a;
dir <= dir_n nor e;
dir_n <= dir nor f;
pul <= pul_n nor d;
pul_n <= pul nor c;
pulse <= pul;
direction <= dir;
```

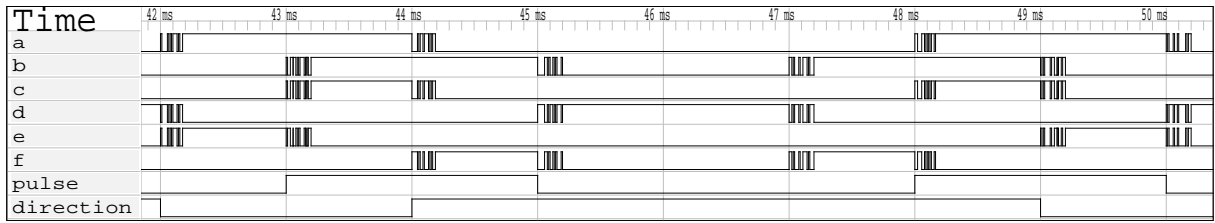Figure 4: VHDL code of asynchronous design

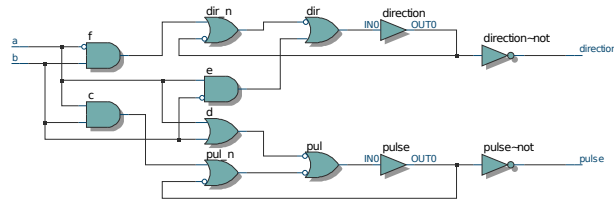Figure 5: Waveforms of asynchronous design

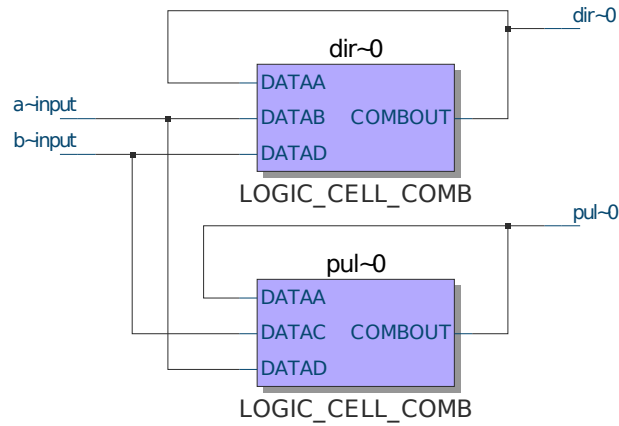Figure 6: RTL view of asynchronous design

Figure 7: Reduced to two combinational loops

```
Warning: Found combinational loop of 2 nodes
Warning (332126): Node "decoder_inst|pul~0|dataa"
Warning (332126): Node "decoder_inst|pul~0|combout"
Warning: Found combinational loop of 2 nodes
Warning (332126): Node "decoder_inst|dir~0|dataa"
Warning (332126): Node "decoder_inst|dir~0|combout"
```

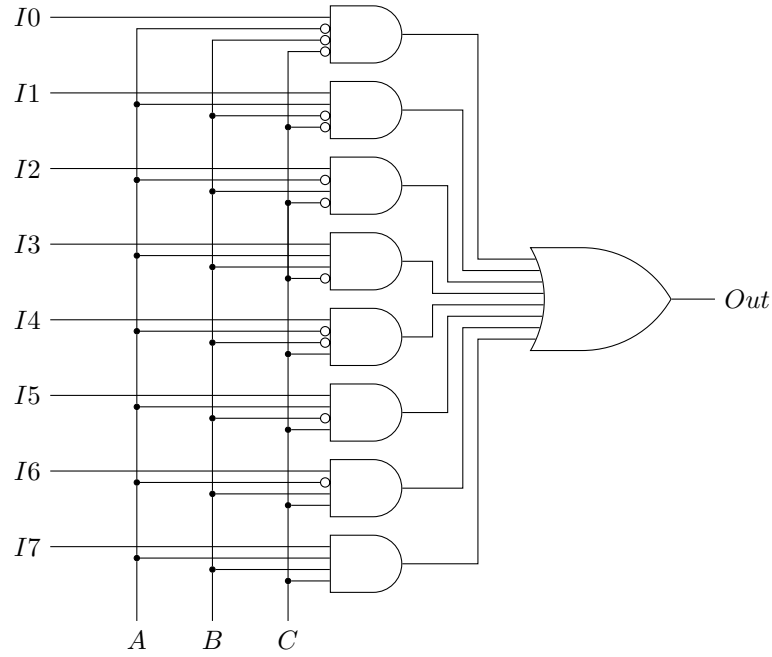Figure 8: Combinational loop warning
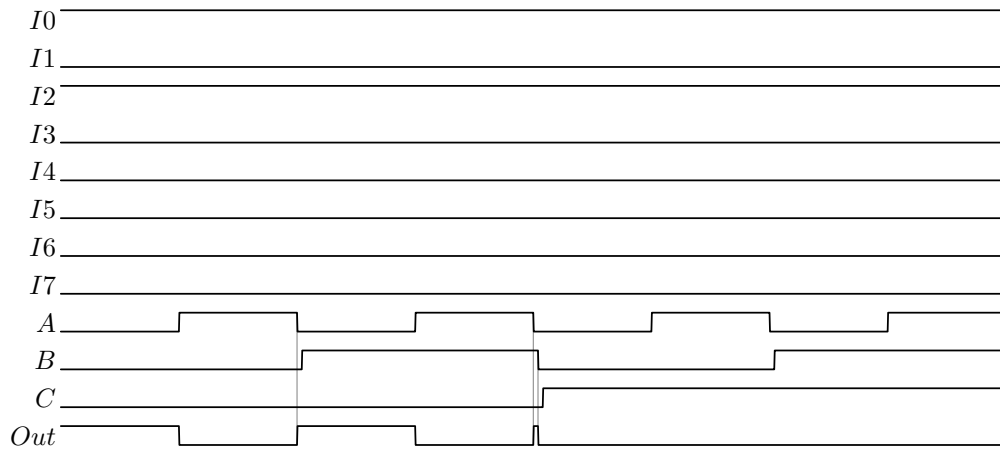
Figure 9: Lookup table logic circuit

Figure 10: Glitch on output when multiple inputs change at almost the same time

```
c <= a xor b;
dir <= b when rising_edge(clock) and c = '1' else dir;
pul <= a when rising_edge(clock) and c = '0' else pul;
pulse <= pul;
direction <= dir;
```

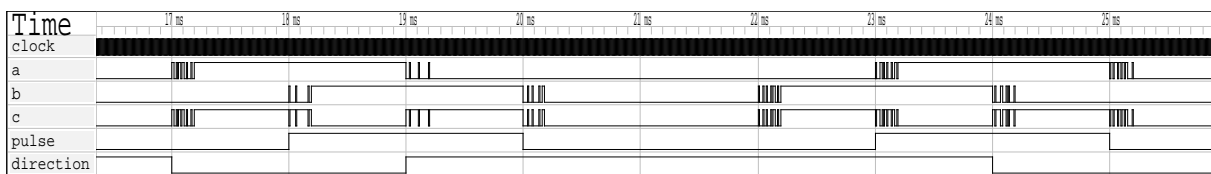Figure 11: VHDL code of synchronous design

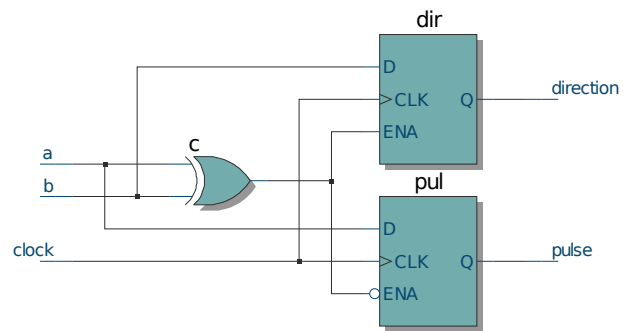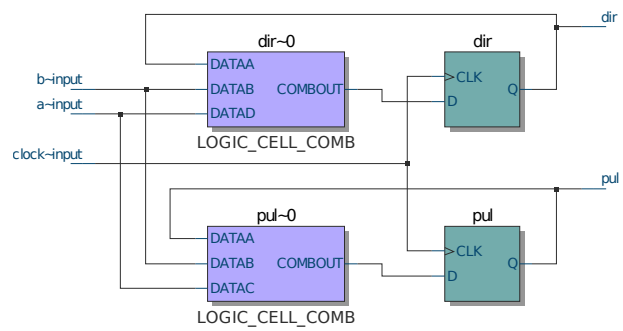Figure 12: Waveforms of synchronous design

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Figure 13: RTL view of synchronous design

Figure 14: Technology map view of synchronous design