Organizing the Dark Silicon Landscape: A Taxonomy-based Analysis on Current Solutions

Boris Vukajlovic and Marouan Bellari

Bachelor of Science, Informatica

December 15, 2024

1 Abstract

As we enter a time where the impressive performance gains promised by Dennard Scaling paired with Moore's Law waver. The thermal and power constraints modern day processors face continue to grow. Due to these constraints, a significant portion of on-chip transistors cannot be powered simultaneously – an actuality that is called Dark Silicon. As this growing challenge affects every layer of the processor design stack, it forces architects and developers to seek solutions that mitigate the impact of these dark transistor regions. This literature study presents a taxonomy that categorizes existing approaches to tackling Dark Silicon, offering a structured view to provide insight into the current state of Dark Silicon mitigation strategies and guiding future innovative efforts.

2 Introduction

Moore's 1965 and 1975 papers have been foundational in processor development. The 1965 paper emphasized the exponential growth in transistor count, later dubbed Moore's Law by Dr. Carver Mead, with an optimistic view that smaller feature sizes could address heat and power challenges[1]. In 1975, Moore revisited this prediction, adjusting the timeline, which remained accurate until early signs of slowdown in 2005 [2]. During the same time, Dennard Scaling, introduced in 1974 by R. H. Dennard and others, outlined how shrinking transistors maintained constant power density, enabling performance to scale with density without proportional power increases [3]. However, as physical limits emerged—such as quantum effects, leakage, and thermal dissipation—Dennard Scaling broke down [4]. This led to rising power consumption and thermal output, giving rise to Dark Silicon. Dark Silicon has been a significant challenge to modern day processor designers, as it limits the ability to fully power all on-chip transistors, limiting the future of computational performance gains. As a direct effect of this, modern computational performance gains now depend more on software optimization and alternative architectures than on hardware scaling alone [5].

As the dominant players within the multicore processor market have all implemented brilliant solutions to the pressing challenge of Dark Silicon, such as DVFS used in many consumer multicore processors to adjust the voltage and frequency at which it operates [6]. And ARM's *big.LITTLE* architecture which combines high-performance and energy-efficient cores to handle different types of workloads more effectively. To categorize all innovations across the processor design stack, we introduce a taxonomy that encompasses all innovations grounded in the principles of von Neumann computing [7]. The selection of references used in this study were motivated by: the need to introduce the concept and pressing issue of Dark Silicon and conceptualize the taxonomy by introducing an array of innovations, how these function and where they would live within the developed taxonomy. This literature study aims to utilize this developed taxonomy to uncover what insights could be taken from the categorization of each innovation by observing the layers of the processor design stack they would be associated with.

3 Analysis

To show a more comprehensive understanding of different types of Dark Sillicon innovations, this section talks about each taxonomy space in greater depth, elaborating on why specific examples qualify as instances of each category. As we introduce these categories it is important to note that many innovations naturally span multiple categories due to their multifaceted nature. For instance, a piece of software that relies on hardware instructions introduces a possible architectural dependency, which could lead it to occupy the intersection of Architectural- and Software-level solutions. To account for all computing paradigms that break from these classical computing norms, such as the quantum, photonic and neuromorphic computing paradigms. We address these separately within the taxonomy in the form of an added dimension, as they challenge the very basis of von Neumann computing.

To define the true boundaries of the subspaces created by the intersections of the spaces, we must look at whether innovations are actively exploiting characteristics of other spaces. If not, an innovation dependent on another space without being co-designed for this specific space is just an artifact of poor compatibility. In short, a *restriction* does not equate an *intersection*. The implications and findings we can derive from this overlap will be discussed in the Discussion 4.

3.1 Architectural-Level Solutions

Architectural-level innovations focus on innovations that operate at the micro-architectural or system design level. We define "architectural-level solutions" as those that primarily modify the processing units or memory hierarchies. As their main goal usually is to minimize power density, reduce thermal output and improve energy efficiency. These solutions clearly distinguish themselves from device- and material-level innovations, which target the fundamental materials and technologies such as those from the semiconductor or transistor. They are distinguishable from software-level as they do not realize themselves through code solutions, as these mostly focus on runtime scheduling, compiler optimization or other algorithms. While many solutions on the architectural-level may very well exist in the intersection with other spaces, to exist in this space, the innovation must exhibit some form of managing hardware structures to mitigate effects of Dark Silicon.

Such an architectural-level solution can be categorized by the use of conservation cores (C-Cores), such as those implemented in the GreenDroid project. GreenDroid integrates specialized energy efficient co-processors, also referred to as conservation cores, into the processor architecture. These cores are specifically designed to handle repetitive and computation-heavy tasks mainly found in mobile applications, like image processing or video decoding. By hardwiring these operations into dedicated hardware units, GreenDroid achieves significant reductions in energy usage up to $11\times$ lower energy consumption compared to executing the same tasks on general-purpose cores, which alone can massively mitigate Dark Silicon effects. This architectural innovation focuses on optimizing the processor's micro-architecture by including these specialized units alongside general-purpose cores [8]. The benefits are achieved entirely through hardware design, making GreenDroid a strictly architectural solution to Dark Silicon.

Power gating, another architectural-level solution to Dark Silicon, involves selectively turning off power to parts of a processor that are not in use, which reduces leakage currents that contribute to static power consumption. Narendra et al. provide a detailed analysis of power gating techniques, showing how sleep transistors are used to isolate inactive circuits from the power supply. Power gating operates entirely at the architectural level, as it involves the integration of additional circuitry into the processor's design to manage power delivery [9]. The technique is independent of material-level innovations, as it uses standard CMOS processes, and does not rely on software for its functionality, though software may assist in determining which components can safely enter a low-power state. This strictly hardware-based approach makes power gating an important architectural tool for mitigating Dark Silicon.

3.2 Software-level Solutions

Software-level innovations complement architectural innovations by providing dynamic management capabilities that adapt to power and thermal constraints in real time. This might be done by optimizing the way jobs are scheduled or compiled, rather than by physically altering the hardware or the underlying materials themselves. A solution can still be classified as a software-level solution if the approach depends on specific hardware or say transistor types. In such cases it is important to look at the *co-design* of the software. If the software does not actively exploit transistor-level features or architectural elements, it is not *co-designed* with those categorizations in mind. Its reliance on specific elements of the other spaces is in this case simply a product of limited portability. Often, the opposite case is true. Where power and performance optimizations often exploit hardware features such as the ones discusses below. This synergy means a very large subset of solutions in Dark Silicon naturally live in the intersection between the other spaces.

The use of Dynamic Voltage and Frequency Scaling (DVFS) can be categorized as a software-level solution to Dark Silicon, which adjusts a processor's voltage and frequency based on workload demands in real time. Weissel and Bellosa demonstrated the effectiveness of DVFS by implementing event-driven clock scaling in embedded systems. Their research showed that DVFS could achieve energy savings of up to 30% during idle periods by dynamically lowering voltage and clock frequency while maintaining computational performance during periods of high demand. Their implementation monitored workload characteristics and adjusted the processor's operating state accordingly, using software algorithms that interfaced directly with hardware voltage and clock control mechanisms [10]. DVFS relies entirely on software defined policies to achieve energy efficiency, operating within the constraints of existing hardware capabilities, which helps to mitigate the effects of Dark Silicon. The hardware itself does not dictate the power-saving behavior but only provides the knobs (e.g., voltage and frequency control points) that the software manipulates in response to workload conditions [10]. While the presence of co-design causing an intersection between software- and architectural-levels could be argued for some cases of specifically optimized DVFS, DVFS implementations often operate independently of the hardware's design process making it an exclusively

software solution.

Another software-level approach for Dark Silicon mitigation is thermal-aware task scheduling, as shown by Cochran and Reda. Their research developed algorithms that dynamically distribute workloads across processor cores to balance thermal loads and prevent localized overheating. Using predictive thermal modeling, their scheduler reduced peak chip temperatures by up to 15% without affecting overall system performance. This was achieved by continuously analyzing workload patterns and processor temperature profiles, ensuring that no single core experienced excessive thermal stress. The predictive model was implemented entirely in software and made real-time decisions about task placement and migration [11]. This innovation is strictly software-level because it does not require hardware modifications or changes to the underlying materials. Instead, it uses software algorithms to optimize how existing hardware is utilized, using temperature sensors already present on modern processors. The thermal-aware scheduler interacts with the operating system to allocate tasks intelligently, but it does not change the architecture of the processor or depend on any innovations at the device or material level.

3.3 Device- and Material-level Solutions

Device- and material-level innovations address the fundamental physical constraints of Dark Silicon by enhancing heat dissipation, reducing leakage or enabling more efficient transistor designs to mitigate Dark Silicon effects at the physical layer. These solutions go past simply reorganizing existing hardware, instead they encompass changes to the fundamental physical building blocks. Device- and material-level innovations typically happen below the architectural layer, if an approach consists of reorganizing processing units or memory this is more appropriate for the architectural category. They often create opportunities for different categories, leading to many intersections with those spaces. If a solution within a different space, when losing its material development, has their improvements negated. It illustrates its reliance on this space, such that it at least lives in an intersection with this space.

Innovation at the level of transistor materials and structures can be seen as an device and material-level solution to Dark Silicon. Mistry et al.'s work on high-k dielectric materials and metal gates is a big innovation in the field of transistor scaling. Their research replaced traditional silicon dioxide gate dielectrics with hafnium-based high-k materials, a development that reduced gate leakage by more than 10$\times$ compared to earlier designs. The high-k material's better dielectric properties allowed for greater capacitance control without the extreme thinness required by silicon dioxide, which mitigated quantum tunneling effects, which dominate at smaller scales. Additionally, by introducing metal gates to replace traditional polysilicon gates, the researchers minimized gate resistance and improved transistor performance, which can help mitigate Dark Silicon effects. These material-level innovations allowed the semiconductor industry to push beyond the limitations of silicon dioxide while continuing Moore's Law-like scaling [12]. This innovation is entirely a device- and material-level solution because it involves no changes to processor architecture or software. Instead, it focused on fundamental improvements in the physical structure and properties of transistors.

Another device- and material-level solution to Dark Silicon are FinFETs (Fin Field-Effect Transistors), introduced by Hisamoto et al., which is a structural innovation in transistor design that addressed the limitations of planar transistors at nanometer scales. FinFETs improved gate control over the channel by using a 3-dimensional, fin-like structure. This reduced short-channel effects and leakage currents. This design improved electrostatic control, which allows transistors to operate at lower voltages with higher efficiency. The vertical orientation of the fin structure also increased the effective surface area of the gate, enabling better switching characteristics without increasing the transistor's footprint. These features made FinFETs an important enabler of continued transistor scaling into the nanometer space [13]. This innovation is specifically a device- and material-level solution because it involves changes to the physical structure and design of transistors instead of their arrangement at the architectural level or how they are utilized by software. The innovation operates independently of any specific processor architecture or software implementation, focusing only on improving the physical attributes of individual transistors.

3.4 Beyond von Neumann Computing Solutions

BvNC innovations, short for Beyond von Neumann Computing, indicates a departure from the traditional von Neumann architecture [7]. This space includes architectures and computing approaches which transcend the sequential (multi)processor. Paradigms such as photonic and quantum computing represent transformative approaches to addressing Dark Silicon challenges by rethinking computation itself. These approaches leverage novel physical principles to overcome the limitations of traditional silicon-based architectures.

Photonic computing can be categorized as a Beyond von Neumann Computing solution to Dark Silicon, which uses light (photons) instead of electrons to perform computations. Photonic processors use the unique properties of light to perform matrix multiplications, which is an important operation in machine learning and other data-intensive tasks, at fast speeds and energy efficiency. By encoding data into light waves and performing computations via optical interference, photonic processors can achieve

operations at terahertz speeds, which exceeds the capabilities of traditional silicon-based processors. Shen et al.'s photonic chip demonstrated the ability to perform computations with a power efficiency 1000× greater than standard architectures for certain workloads [14]. This innovation lies beyond the von Neumann principles, as it abandons the sequential execution model and relies on the parallel and wave-like nature of light to perform computations.

Another instance of a Beyond von Neumann Computing solution to Dark Silicon is quantum computing, which redefines the way computers compute by using the principles of quantum mechanics. Different quantum processors such as IBM's quantum systems and Google's Sycamore chip use qubits that can exist in superposition states. This enables them to represent and process multiple possibilities simultaneously [15]. Quantum computing is great at solving certain types of problems, like simulating quantum systems or large number factorization, which are not attainable for classical von Neumann systems. Arute et al., experimenting with the Sycamore processor, managed to achieve quantum supremacy by demonstrating a computation that would take classical supercomputers thousands of years to complete in just 200 seconds [16]. Quantum computing addresses Dark Silicon challenges not by improving silicon efficiency, but by entirely bypassing traditional transistor based architectures, instead using quantum phenomena like entanglement and interference to achieve computational speed-ups.

4 Discussion

Having introduced the four spaces of our taxonomy, we can define each of these spaces as a set of innovations – Architectural (A), Device- and Material (M), Software (S) and Beyond von Neumann Computing (E) – together with an instance of an innovation I. Below is a visualization of the sets, note that the volume is arbitrary in the taxonomy 1, 2. As giving a meaning to these values would go against the nature of the theoretical sets.

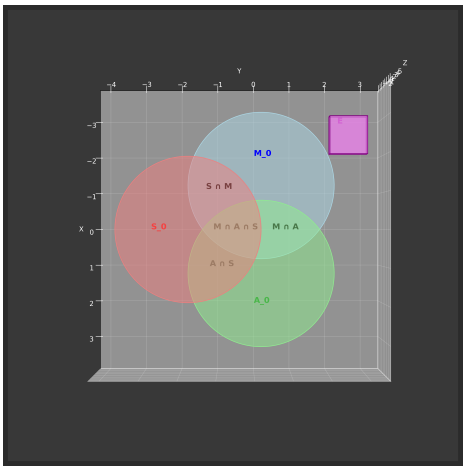

Figure 1: Topdown view of taxonomy

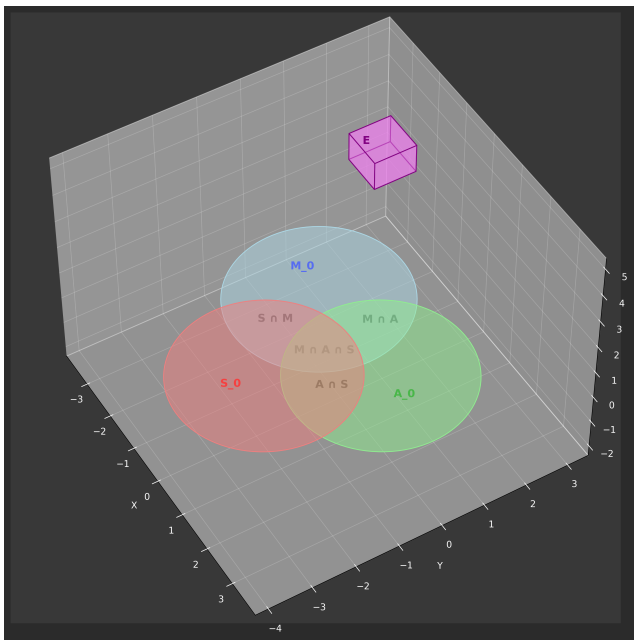

Figure 2: 3D overview of taxonomy

We now examine how innovations can span across these sets and the information we can extract from these behaviors. As outlined in the analysis 3, it is important to note that a restriction does not equate an intersection. Dependencies to a specific design layer without intentional co-design do not constitute intersections in the taxonomy. Since the set of innovations E does not contain any subsets created through intersection, we will not include it in the Discussion.

4.1 Single-space membership

1. $M_0 = M \setminus (A \cup S)$. This set describes solutions that *solely* rely on novel devices or materials 3.3.
2. $A_0 = A \setminus (M \cup S)$. This set describes innovations that *exclusively* exist in the Architectural space 3.1
3. $S_0 = S \setminus (A \cup M)$. This set describes solutions which are *only* grounded in software3.2.

Instances of the innovation $I \in M_0 \vee A_0 \vee S_0$ attempt to mitigate the effects of Dark Silicon through strategies isolated within their respective sets. Due to the lack of collaboration across sets, they may not fully exploit the available synergies that would be found in co-designed solutions. Looking towards the future, potentially optimizing these solutions through co-design could increase their yields. In the remainder of this section we will present instances of members that each subset accommodates.

$I \in M_0$ The aforementioned High-k dielectric materials and metal gates are a device- and material-level solution are an example of a device- and material-level solution, seeing as they reduce leakage currents and enable transistor scaling through innovations in transistor materials, without changing processor architecture or requiring software changes 3.3.

$I \in A_0$ The aforementioned conservation cores, such as those implemented in the GreenDroid project, are an example of an architectural solution, seeing as they optimize the processor's micro-architecture by integrating specialized hardware units for repetitive tasks, reducing energy consumption completely through hardware design without altering materials or requiring big software changes 3.1.

$I \in S_0$ The aforementioned DVFS are an example of a software-level solution, seeing as it dynamically adjusts processor voltage and frequency using software algorithms, optimizing energy efficiency without modifying the underlying hardware design or semiconductor materials. It relies only on software-defined policies to interface with existing hardware capabilities 3.2.

4.2 Double-space membership

1. $M \cap A$. Which describes solutions that live in the set representing the intersection between the Device- and Material-space 3.3 and the Architectural-space 3.1.

2. $A \cap S$. Which describes solutions that live in the set representing the intersection between the Architectural-space 3.1 and the Software-space 3.2.

3. $S \cap M$. Which describes solutions that live in the set representing the intersection between the Software-space 3.2 and the Device- and Material-space 3.3.

An innovation I living in one of the subsets–$I \in (M \cap A) \vee (A \cap S) \vee (S \cap M)$– represents co-design within the levels representing the intersecting sets. These innovations utilize the optimization capability of two domains which generally is more efficient than single-space solutions, while less complex than triple-space solutions. In the remainder of this section we will illustrate instances of innovations living in the double-space membership subsets.

$I \in (S \cap M)$ Approximate computing with voltage overscaling is an example of a solution to Dark Silicon that intersects software-level and device- and material-level innovations. Approximate computing is a paradigm where software allows small, tolerable errors in computations (e.g., in multimedia or machine learning tasks) to save energy. This approach is often paired with voltage overscaling at the hardware level, where the supply voltage is reduced below the normal level where specific materialistic properties are necessary. While this leads to occasional errors, the software manages these errors by ensuring they do not significantly impact overall application quality [17].

$I \in (M \cap A)$ 3D stacked memory with wide I/O interfaces is an example of a solution to Dark Silicon that intersects device- and material-level and architectural-level innovations. HBM (High Bandwidth Memory), which is a 3D stacked memory architecture, involves stacking DRAM layers vertically and connecting them with Through-Silicon Vias (TSVs). This approach greatly reduces memory access latency and power consumption while increasing bandwidth. Architecturally, processors are designed to interface with this memory using wide I/O interfaces that use the benefits of 3D stacking [18]. This solution operates at the architectural level through processor-memory interface designs specifically designed for 3D stacked memory. At the same time, it relies on device- and material-level innovations such as TSVs and advanced DRAM fabrication techniques.

$I \in (A \cap S)$ Heterogeneous multicore architectures with task-aware scheduling are an example of a solution to Dark Silicon that intersects architectural-level and software-level innovations. Heterogeneous multicore architectures, such as ARM's *big.LITTLE* design, combine high-performance cores with energy-efficient cores to handle different types of workloads. Task-aware scheduling software complements this architecture by assigning tasks to the appropriate core type based on workload characteristics. For example, lightweight background tasks are routed to energy-efficient cores, while performance-critical tasks are executed on high-performance cores [19]. This solution operates at the architectural level by designing processors with heterogeneous cores, and at the same time relies on software-level task scheduling to dynamically allocate workloads. The architectural dark silicion innovation provides the hardware changes necessary for power efficiency, while the scheduling software ensures that tasks uses the architecture effectively.

4.3 Triple-space membership

1. $M \cap A \cap S$. Which describes innovations that live in the intersection of all three spaces.

An innovation $I \in (M \cap A \cap S)$, is one which leverages capabilities of each space to tackle Dark Silicons core challenges of power density, thermal management or energy efficiency. Solutions within the subset – $M \cap A \cap S$ – are therefore a clear example of co-design. Due to this co-design, the innovation I is dependent on the success of each of its dependencies to a layer. This synergy often leads to improvements that are less likely to be observed within the sets of individual spaces. The innovation I tends to be higher in design complexity as well, as a direct consequence of its membership to its set. These characteristics of I can be considered general observations, rather than strict requirement. As the taxonomy does not distinguish between yields of each innovation as they are categorized. In the remainder of this section we will address instances of innovations living in the triple-space membership subset.

An example of a solution to Dark Silicon I that

lives in the set $M \cap A \cap S$ is dynamic thermal management (DTM) with thermal sensors. Dynamic Thermal Management systems use on-chip thermal sensors to monitor processor temperatures and dynamically adjust both hardware and software operations to prevent overheating. At the architectural level, processors are designed with fine-grained thermal zones and power gating capabilities. At the software level, runtime management systems decide when to throttle performance or migrate tasks based on sensor data. Device- and material-level innovations contribute by using reliable and efficient thermal sensors and materials with high thermal conductivity for heat dissipation [20]. This solution integrates architectural features such as power gating and thermal zones, runtime software for task management, and material-level innovations like advanced thermal sensors. Together, these components work together in synergy to address Dark Silicon challenges.

4.4 The Value of Co-Design

As our taxonomy allows us to identify the degree of co-design that exists within innovations based on the set it exists in. It is important to illustrate the definition of co-design and the practical benefits it brings. Co-design alludes to the development of hardware and software components to achieve some form of system-wide optimization, unlike approaches, that in our taxonomy 4 would fall within the single-space membership 4.1, where hardware and software is optimized in isolation. By considering the needs and capabilities of all domains that a processor consists of, co-design allows for the creation of more efficient approaches for mitigating the effects of Dark Silicon.

A clear cut example of the benefits of co-design can be illustrated through DSE–Design Space Exploration–, which integrates inter- and intra-application scenarios to optimize resource allocation in systems with dynamic workloads. Findings from DSE studies highlight its ability to improve efficiency by iteratively refining system configurations. This capability demonstrates co-design's value in maximizing hardware utilization and minimizing wasted energy [21].

4.5 Future Work

Our taxonomy provides a framework for classifying innovations that attempt to mitigate Dark Silicon. During this study we found several opportunities to enlarge or refine the scope of the taxonomy for future work. An important insight from our analysis is that generalizations about an innovation's complexity and efficiency often depend on the constraints and barriers defined within each set. It is of concern to note the fact that innovations that simply depend on other layers—without utilizing them in a co-design context—do not live in the intersections of sets. This highlights a limitation: the portability of an innovation cannot be assumed through the membership of an innovation to a subset. For example, a poorly portable innovation might still exist exclusively in the software-innovation set.
To address this, we propose incorporating dependency levels into the taxonomy, organizing innovations based on the degree to which they rely on other domains. Innovations with strong dependencies on other layers could be positioned closer to the edges of their respective sets, while highly portable solutions would find themselves closer to the center within their subsets. To illustrate, a software-level innovation with a high level of architectural dependencies might be placed near the boundary between the S_0 and A_0 subsets, still within the S_0 set. While portable software innovations would live at the heart of the S_0 subset.

It is important to note that, as this taxonomy is theoretical, categorizing the dependency levels through the *amount* of dependencies will lead to misleading conclusions. As the number of dependencies does not truly represent how portable a innovation is –certain dependencies can be more pressing than others–. However, estimations based on a developed portability-score in practice can still provide meaningful insights and enable accurate generalizations for all innovations.

5 Conclusion

This literature study suggest a taxonomy for categorizing innovations which attempt to mitigate the challenges of Dark Silicon. By looking at these innovations through the lens of their four developed categories: Device- and Material (M), Architectural (A), Software (S) and Beyond von Neumann Computing ($BvNC$), we provided a framework that was able to show how innovations interacted, overlapped and how their characteristics might differ according to their membership to a subset within the taxonomy.
Our taxonomy emphasizes the distinction between co-designed innovations and dependencies within innovations. As one can be an indication of greater efficiency and complexity, while the other is just an indication of poor portability. Since we were limited in assessing the levels of dependency, this gap presents an opportunity for future work.

In closing, the developed taxonomy we present is to be utilized to understand where developed innovations stand in their battle against Dark Silicon. As it organizes a collection of innovations in the taxonomy's space, we use this arrangement of innovations to extract insights into their characteristics. This allows us to suggest improvements upon these innovations and exposes the gaps for potential future work.

References

[1] Gordon E. Moore. “Cramming More Components onto Integrated Circuits”. In: *Electronics* 38.8 (1965), pp. 114–117.

[2] Prof. Dr.-Ing. Christian Märtin. “Post-Dennard Scaling: The New Era of Computing Performance”. In: (2014).

[3] R.H. Dennard et al. “Design of Ion-Implanted MOSFET’s with Very Small Physical Dimensions”. In: *IEEE Journal of Solid-State Circuits* 9.5 (1974), pp. 256–268.

[4] David J Frank et al. “Device Scaling Limits of Si MOSFETs and Their Application Dependencies”. In: *Proceedings of the IEEE* 89.3 (2001), pp. 259–288.

[5] Karl Rupp. *Microprocessor Trend Data*. GitHub Repository. 2018.

[6] Gernot Heiser. “Dynamic Voltage and Frequency Scaling: The Laws of Diminishing Returns”. In: *ResearchGate* (2010).

[7] John von Neumann. *First Draft of a Report on the EDVAC*. Tech. rep. University of Pennsylvania, 1945.

[8] Rehan Hameed et al. “Understanding Sources of Inefficiency in General-Purpose Chips”. In: *ACM SIGARCH Computer Architecture News*. Vol. 38. 3. 2010, pp. 37–47.

[9] Siva G. Narendra and Anantha P. Chandrakasan. *Leakage in Nanometer CMOS Technologies*. Springer, 2006.

[10] Andreas Weissel and Frank Bellosa. “Process Cruise Control: Event-Driven Clock Scaling for Dynamic Power Management”. In: *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*. 2002, pp. 238–246.

[11] Ryan Cochran and Sherief Reda. “Thermal Prediction and Adaptive Control Through Workload Phase Detection”. In: *Proceedings of the 46th Annual Design Automation Conference*. 2010, pp. 62–67.

[12] Kaizad Mistry et al. “A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging”. In: *IEEE International Electron Devices Meeting*. 2007, pp. 247–250.

[13] Digh Hisamoto et al. “FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm”. In: *IEEE Transactions on Electron Devices* 47.12 (2000), pp. 2320–2325.

[14] Yichen Shen, Nicholas C. Harris, Scott Skirlo, et al. “Deep Learning with Coherent Nanophotonic Circuits”. In: *Nature Photonics* 11 (2017), pp. 441–446.

[15] Frank Arute et al. “Quantum supremacy using a programmable superconducting processor”. In: *Nature* 574.7779 (2019), pp. 505–510.

[16] Frank Arute, Kunal Arya, Ryan Babbush, et al. “Quantum Supremacy Using a Programmable Superconducting Processor”. In: *Nature* 574 (2019), pp. 505–510.

[17] Hadi Esmaeilzadeh et al. “Architecture Support for Disciplined Approximate Programming”. In: *Proceedings of ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*. 2012, pp. 301–312.

[18] J.-H. Lee, J.-W. Kim, et al. “High Bandwidth Memory (HBM) with TSV”. In: *Proceedings of IEEE International Electron Devices Meeting (IEDM)*. 2016, pp. 1–4.

[19] Peter Greenhalgh. “big.LITTLE Processing with ARM Cortex-A15 & Cortex-A7”. In: (2011).

[20] David Brooks and Margaret Martonosi. “Dynamic Thermal Management for High-Performance Microprocessors”. In: *Proceedings of IEEE High-Performance Computer Architecture (HPCA)*. 2001, pp. 171–182.

[21] Andy Pimentel and Peter van Stralen. “Scenario-based Design Space Exploration”. In: *Handbook of Hardware/Software Codesign*. Ed. by Soonhoi Ha and Jürgen Teich. Springer, 2018. Chap. 9.