Experiment-7

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**Questions:**

1.To design 2 to 4 line decoder

Aim:To design a 2 to 4 line decoder

Truth Table:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **E** | **A** | **B** | **D0** | **D1** | **D2** | **D3** |
| 0 | X | X | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

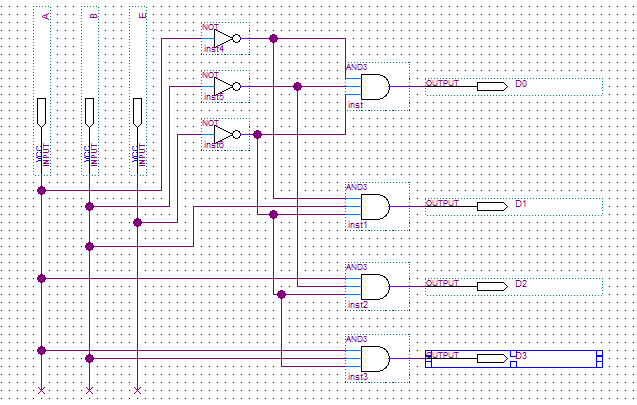
Boolean Expressions:

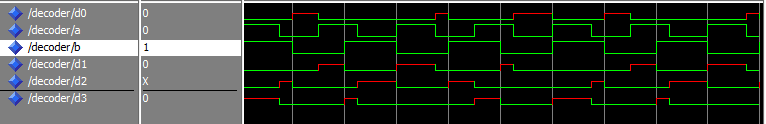
DO=A’B’E’

D1=A’BE’

D2=AB’E’

D3=ABE’





2. Design a logic circuit to control the traffic light as per the given details. Vehicle detection sensors are placed along C and D (main road) and lanes A and B (access road). These sensor outputs are LOW (0) when no vehicle is present and HIGH (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic:

a.The east-west (E-W) traffic light will be green whenever both lanes C and D are occupied.

b.The E-W light will be green whenever either C or D is occupied but lanes A or B are not occupied.

c.The north-south (N-S) light will be green whenever both lanes A and B are occupied but C or D are not occupied.

d. The N-S light will also be green when either A or B is occupied while C and D are both vacant.

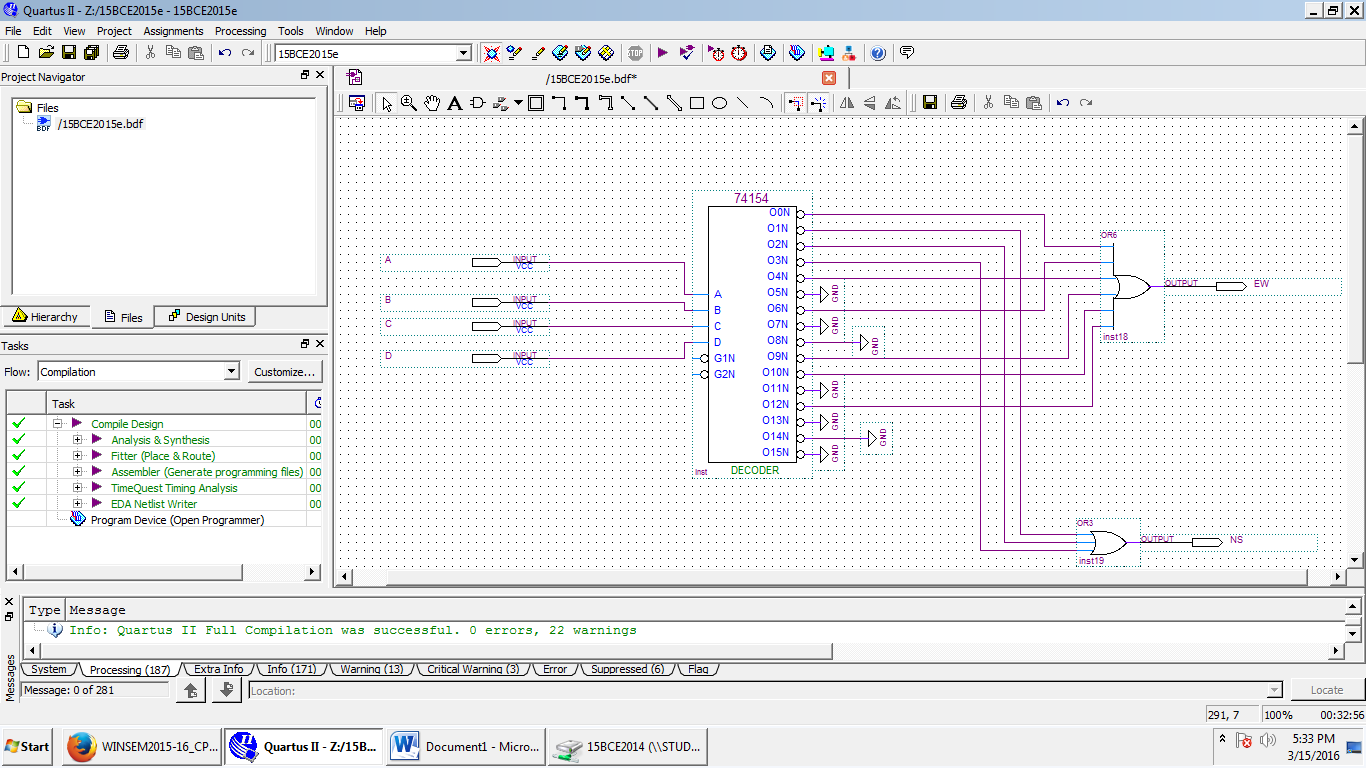
e. The E-W light will be green when no vehicles are present.

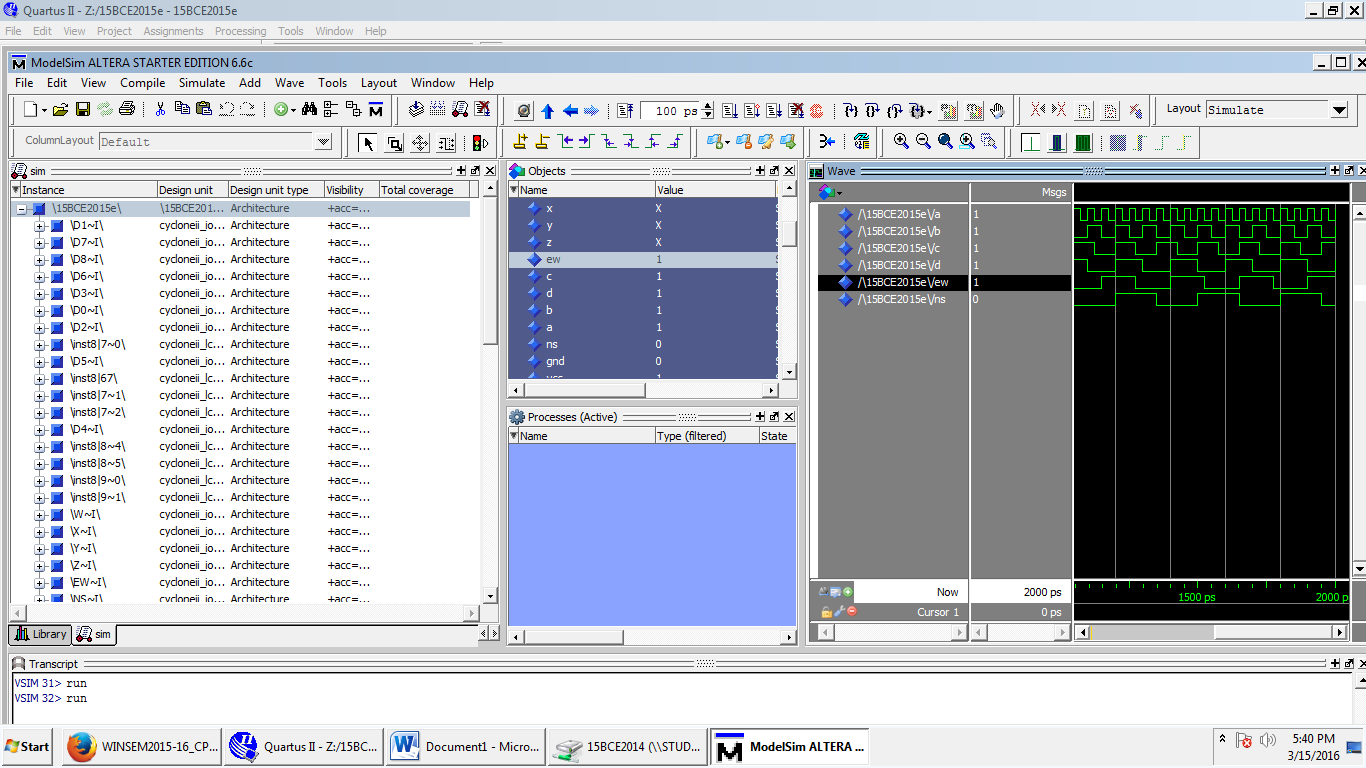
Using the sensor outputs A, B, C and D as inputs, N-S and E-W be two outputs that go high when the corresponding light to be green. Simulate the above scenario using decoders.

Aim: To design a logic circuit for the above conditions

Truth Table:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| D | C | B | A | EW | NS |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 |





3.To design decimal to BCD encoder

Aim: To design decimal to BCD encoder

Truth Table:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Y3** | **Y2** | **Y1** | **Y0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

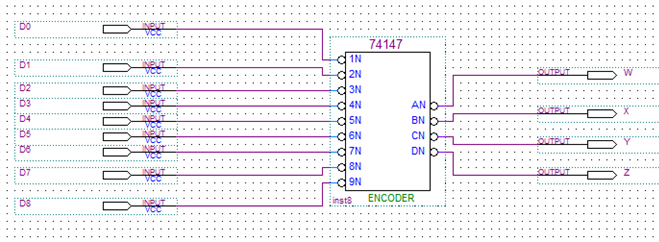
Boolean Expressions:

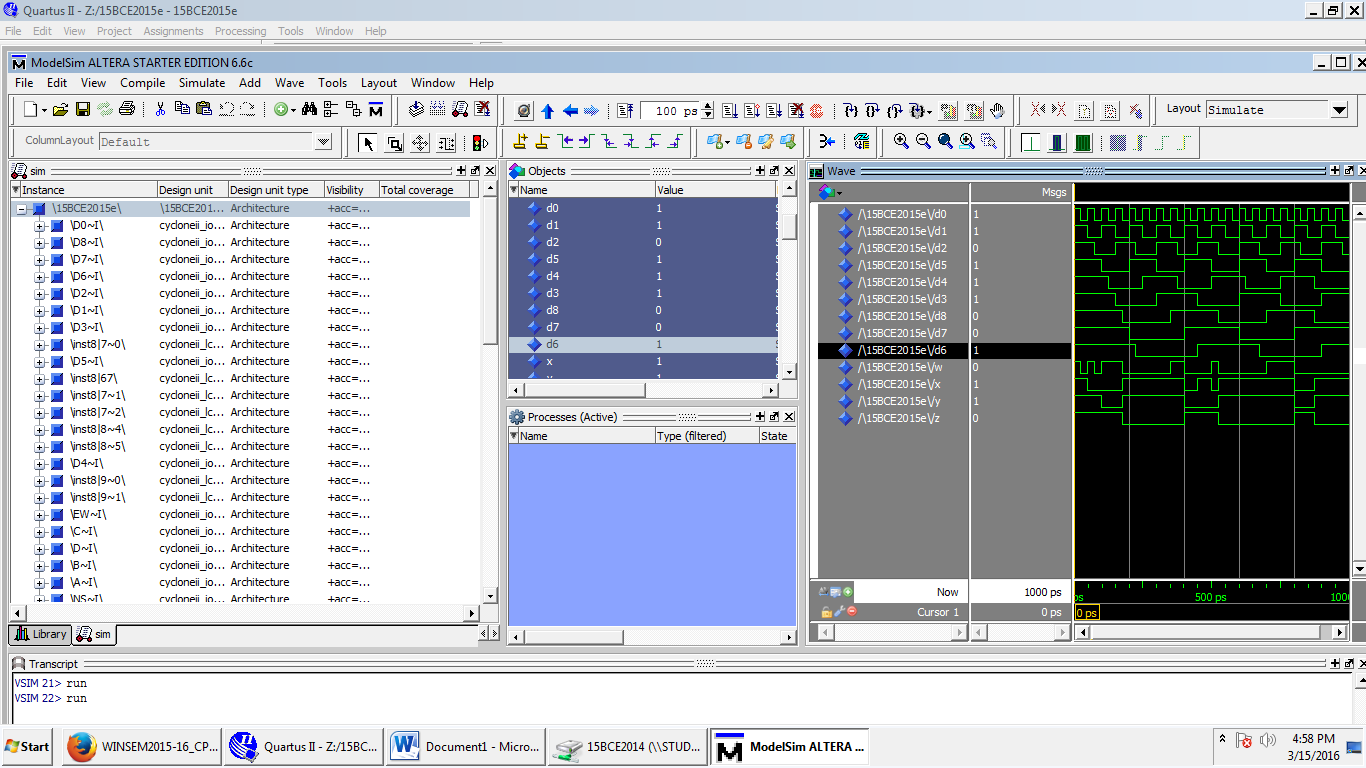
YO=D1+D3+D5+D7+D9

Y1=D2+D3+D6+D7

Y2=D4+D5+D6+D7

Y3=D8+D9





4. To design and implement 8 line to 3 line priority encoder. Include an output ‘E’ (enable) to

indicate that at least one input is ‘1’.

Aim: To design and implement 8 line to 3 line priority encoder

Truth Table:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Q2** | **Q1** | **Q0** | **E** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | X | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | X | X | X | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | X | X | X | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | X | X | X | X | X | 1 | 0 | 1 | 1 |
| 0 | 1 | X | X | X | X | X | X | 1 | 1 | 0 | 1 |
| 1 | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 |

Boolean Expressions:

Q0=D1+D3+D5+D7

Q1=D2+D3+D6+D7

Q2=D4+D5+D6+D7

