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**Digital Logic Lab Procedure**

1. Click Quartus II 32 bit

2. Click “ Create a New Project”

3. Press Next

4. Fill up the 5 pages

(1) Introduction- press next

(2) Page1- Directory, Name, Top-Level Entity(page 1 of 5)

What is the working directory for this project?

• Choose Z drive (Before choosing the z drive create a folder in the z drive for the

new project)

• From the Z drive , select the folder, you have created

• Press OK

(3) Page 2-Add files [page 2 of 5]—press next

(4) Page3-Family & Device Settings [page 3 of 5]

• Under Device Family—Select Cyclone II

• Under Available Devices – Choose the Name- EP2C20F484C7

• Click Next

(5) Page -4 EDA Tool Settings [page 4 of 5]

• Under Tool Type – Select Simulation

• Select Tool Name as ModelSim-Altera

• Format- VHDL

• Choose the option—Run gate-level simulation automatically after compilation

• Press next

(6) Page 5-Summary [page 5 of 5]—click Finish

5. Click File – Press New

6. Select – Design Files- Select Block Diagram/Schematic File

7. Click Symbol Tool- to draw the logic gates

8. Select : d:/altera/10.1/quartus/libraries

9. Select: primitive/logic

10. Under logic choose the corresponding logic gate, then click ok

11. Place the gate in the right place. Then press ESC to remove the symbol more than once.

12. Press pin tool to attach the input and output to the gate.

13. Double click on the input to change the pin name, press delete and erase the old name and give

new name for the Input and output.

14. Click Tools(menu) in the menu bar

a. Choose Options then General then EDA Tools options

b. Under EDA tool option – Select ModelSim-Altera

c. Select the icon near the ModelSim-Altera and set the path as

d. D:/altera/10.1/modelsim\_ase/win32aloem

e. Press OK

15. Save the File under the same folder you created the project

16. Go the Project Navigator Window

17. Select File—Right Click and click the set top level as entity

18. Then Press Compile button

19. After the ModelSim Altera STARTER EDITION Window has opened

20. open the folder work

21. Right click the file name and press Simulate

22. Right click on the inputs and outputs, select “add”, then “ to wave”, then “selected signals”.

23. To give input and to observe the output

a. Right the one of the input, select “force”, give the input value

b. Repeat the process for all the inputs.

c. Click on run button to view the output and also the wave.

24. Second method to verify the output

a. Right click the input and select Clock

b. Different clock period for different inputs.

c. Select the clock period as 100 and duty cycle as 50 ( For logic gates alone) – for input 1

d. Select the clock period as 150 and duty cycle as 50 ( For logic gates alone) – for input 2

25. To zoom the waves press control button in the keyboard +scroll, the mouse

To open an existing file, first you have to open the projects and then the files in the corresponding project

can be opened from the files folder in the project navigator window.