**CORDIC Background**

CORDIC (coordinate rotation digital computer) is a method that applies a wide range of elementary functions in a hardware efficient method, using rotations. This calculation method was discovered by Jack Volder in 1959 during his time in the aero-electronics department of Convair, Fort Worth [1]. Jack Volder and his team were tasked with replacing the analogue computer-driven navigation system of the B-58 bomber with a digital successor. At this time there was no known digital equivalent to the analogue resolver, with the digital solutions of the time resorting to approximations and/or table look-up for trigonometric functions [2]. After initially attempting to encode the sine and cosine functions or a an intermediatory solution similar, to no avail, the following equations (fig. 1) were derived from trigonometric equations found in the 1946 edition of the Handbook of Chemistry and Physics [2].



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Figure 1: Early beginnings of the CORDIC algorithm [2]

Based on the two equations seen in figure 1, the digital equivalent to an analogue resolver was developed. The equations can be used to implement the rotation of vector ‘R’ (as defined by orthogonal coordinates) through either positive or negative angles equal to the magnitude of tan(). Using this logic, it was then deemed possible to utilize a sequence of rotations with increasing powers of *n* to be used to rotate R through a desired angle.

The CORDIC algorithm, is designed efficiently solve these trigonometric functions while avoiding multiplication. To do this it resorts to two fundamentals: as aforementioned the desired angle is achieved by assuming that it is equal to rotating the vector by several smaller angles. Secondly that choosing small elementary angles in a way that upholds tan(ø) = . By adhering to both these fundamentals a rotation of a desired angle can be achieved by a bitwise shift rather than resorting to multiplication. This practice is extremely efficient when compared to the multiplication or other complex alternatives [3]. This achieves a high throughput rate along with a great reduction in hardware complexity as well as the latency of implementation. [4]

**How CORDIC works**

The Hardware structure of CORDIC can be derived from the following equations:

Chart

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Figure 2: Derived equations used to model CORDIC hardware structure [5]

Using these equations, it can be seen that the basic CORDIC implementation can be achieved using the following hardware architecture which can be seen in figure 3 below. However, this is not the only way to implement the CORDIC processor. These other architectures can differ depending on whether they are constrained on efficiency or area etc.

The principal modules of this design are counter, adder/subtractor, shifters, multiplexers, and a ROM. The basic CORDIC architecture is sequential. The design below contains three simple structures which execute the equations displayed above in figure 2. The register is used to store the result of the previous iteration and iterations are obtained through the simple up counter which keeps track of the current iteration, degree of shift and accessing ROM address. The decision for clockwise or anti-clockwise rotation is obtained from the sign bit of the error angle z. The multiplication of is achieved by a shift of *i* bits. The x or y values are updated using a right shift also. The initial values for the variables are loaded through the multiplexer. These angular values are presented to the adder block along with the previous value for angular computation [6].

Diagram

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Figure 3: Basic CORDIC Architecture [6]

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