

# HILL XIONG

Computer Engineering Undergrad

**Address:** Elk Grove, CA, 95758

**Language:** C++, HTML/CSS, Matlab, Verilog, MIPS

**Github:** [github.com/xempst](https://github.com/xempst)

**Webpage:** [xempst.github.io](http://xempst.github.io)

[junfengxiong@ucsb.edu](mailto:junfengxiong@ucsb.edu)

<https://www.linkedin.com/in/hill-xiong-162135161/>

(916) 541-5477

## Summary

Undergraduate Computer Engineer at University of California: Santa Barbara looking for Software Engineer Internship. Through course works, I have build up an understanding of data structures, algorithms, and computer architecture, and I wish to apply everything I learned in practical use.

## Education

**Computer Engineering B.S.** - University of California: Santa Barbara

2021

- GPA: 3.2
- Expected Graduation: June 2021

## Academic Courses

**Data Structure and Algorithms I in C++** - University of California: Santa Barbara

2019

- Implemented Max-Heap to output 3 student with the highest grade of a given gradebook data
- Implemented Prims/Kruskal Algorithm to generate a MST of a given weighted graph

**Data Structure and Algorithms II in C++** - University of California: Santa Barbara

2019

- Used DP to efficiently calculate the similarity of 2 DNA strings
- Implemented Randomized Algorithm to find the linear regression line of a given data set

**Image Processing in Matlab** - University of California: Santa Barbara

2019

- Implemented Seam-Carving and Randomized Patch Match method for content-aware image resizing
- Implemented Richardson-Lucy Algorithm to denoise an image using a known-blur filter

**Computer Network in C** - University of California: Santa Barbara

2019

- Designed and Implemented a TCP hangman server/client capable of multiple concurrent games by using threads
- Understand different routing protocols (e.g. Link-State, Distance-Vector, BGP)

**Computer Architecture in Verilog/MISP** - University of California: Santa Barbara

2019

- Simulated a MISP single/multi cycle processor in ModelSim
- Wrote a calculator and radix sorting algorithm using MISP assembly language

**Circuit Design in Verilog** - University of California: Santa Barbara

2019

- Programed a FPGA to be able to be used as a microcontroller for tail-light signal of a car
- Programed a FPGA to work as a timer when connected to a LED display

## Personal Project

**Personal Website** - [xempst.github.io](http://xempst.github.io)

2018

- Built a personal resume website using HTML and CSS

**Visual Novel Game** - Programmer/Story Writer

2017

- Choice driven game with multiple ending written in Python