General Purpose I/O Controller User Guide

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IPextreme®, Inc.

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PREFACE

This document describes the functionality of the General Purpose I/O Controller (GPIO). The GPIO is the General Purpose I/O Controller synthesizable IP core from National Semiconductor.

Intended Audience

This user guide is intended for intended for system designers who are developing software for the GPIO. Readers of this manual are expected to be familiar with chip design technology and electronic design automation (EDA) tools.

Document Organization

This user guide is organized as follows:

- Chapter 1: Functional Description describes GPIO features and functionality.
- Chapter 2: Registers describes GPIO registers.
- Appendix A: Register Summary provides a quick reference of the GPIO register list and layout, as well as the layout of the channels.

Related Documentation

For the complete list of GPIO documentation, refer to the *General Purpose I/O Controller Documentation Guide*.

Getting Help

To get help with the GPIO product, send e-mail to support@ip-extreme.com.

If you are an IPextreme customer with a current support contract, log on to the IPextreme IP Distribution and Support Portal at https://xpack.ip-extreme.com.

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CHAPTER 1
FUNCTIONAL DESCRIPTION

The General Purpose I/O Controller (GPIO) provides a bidirectional port (generically called Px in this document) with alternate function capability to an external off-chip interface. More than one GPIO may be used within a system. For example, if the system includes 3 GPIO units, their port names would be PA, PB, and PC.

As an external interface, the GPIO is designed for direct connection to I/O pins. The GPIO is used to share I/O pins for general-purpose and alternate functions such as input, output, or bidirectional pads from other peripherals such as UARTs or timers that require off-chip connections.

Top-Level Interface Signals

Each of the Px signals may be configured for input or output. Two internal weak pull-up/pull-down signals are provided to allow the pin to be held at a high/low level when used as an input, or in an open-drain scheme. The GPIO is configurable for 16 or 32 GPIO channels. Table 1 and Table 2 list the chip-level interface signals of the GPIO for the 16 and 32-channel configurations, respectively. For more details on the hardware configuration and IP-level signal names, refer to the *General Purpose I/O Controller Integration Guide*.

TABLE 1: TOP-LEVEL INTERFACE (32 GPIO CHANNELS)

Signal Name	Type	Description
Px[31:0]	I/O	GPIO ports Px0 through Px31

TABLE 2: TOP-LEVEL INTERFACE (16 GPIO CHANNELS)

Signal Name	Type	Description
Px[15:0]	I/O	GPIO ports Px0 through Px15

Features

The I/O pin characteristics are fully programmable. Each pin can be configured to operate as a tristate output, push/pull output, input with weak pull-up, input with weak pull-down, or high-impedance input. Different pins within the same port can be configured individually to operate in different modes.

Register bits, multiplexers, and buffers allow the port pin to be configured to operate in various modes. To reduce power consumption, input buffers configured for general-purpose I/O are enabled only when they are read. When configured for an alternate function, the input buffers are enabled continuously.

The GPIO port has the following features:

- Each pin can function as an input or output port
- The Port Direction Register controls the port direction
- Internal weak pull-up, pull-down
- Direct low-impedance analog input
- Read-back on all registers
- Each pin may be controlled by other modules by its software-selectable alternate function and alternate source
- Selectable high drive current option

The following section describes the architectural structure of 16/32-bit GPIO ports. The description is presented for a generic port referred to as Px.

General-Purpose I/O Ports

Figure 1 is a block diagram of the GPIO. The GPIO controls an I/O pad that supports the features listed below.

Output Buffer

The output buffer is a tristate buffer with a weak pull-up/pull-down capability. The output type can be either CMOS or TTL. The driving capabilities depend on the technology chosen and the I/O pad selected.

Weak Pull-up/ Pull-down

To enable the weak pull-up/pull-down capability, the respective bit of the Port Weak Pull-up/Pull-down Direction Register (PxPDR) must be set to ‘1’ or ‘0’ respectively, and then the corresponding bit of Port Weak Pull-up/Pull-down Enable Register (PxWKPU) must be set to ‘1’. The pull-up/pull-down can be used to prevent an input from being in an undefined state.

Input Buffer

The input buffer has an enable input. When enabled, the buffer inputs the pin's logic level. When disabled, the input is blocked to prevent leakage currents from flowing.

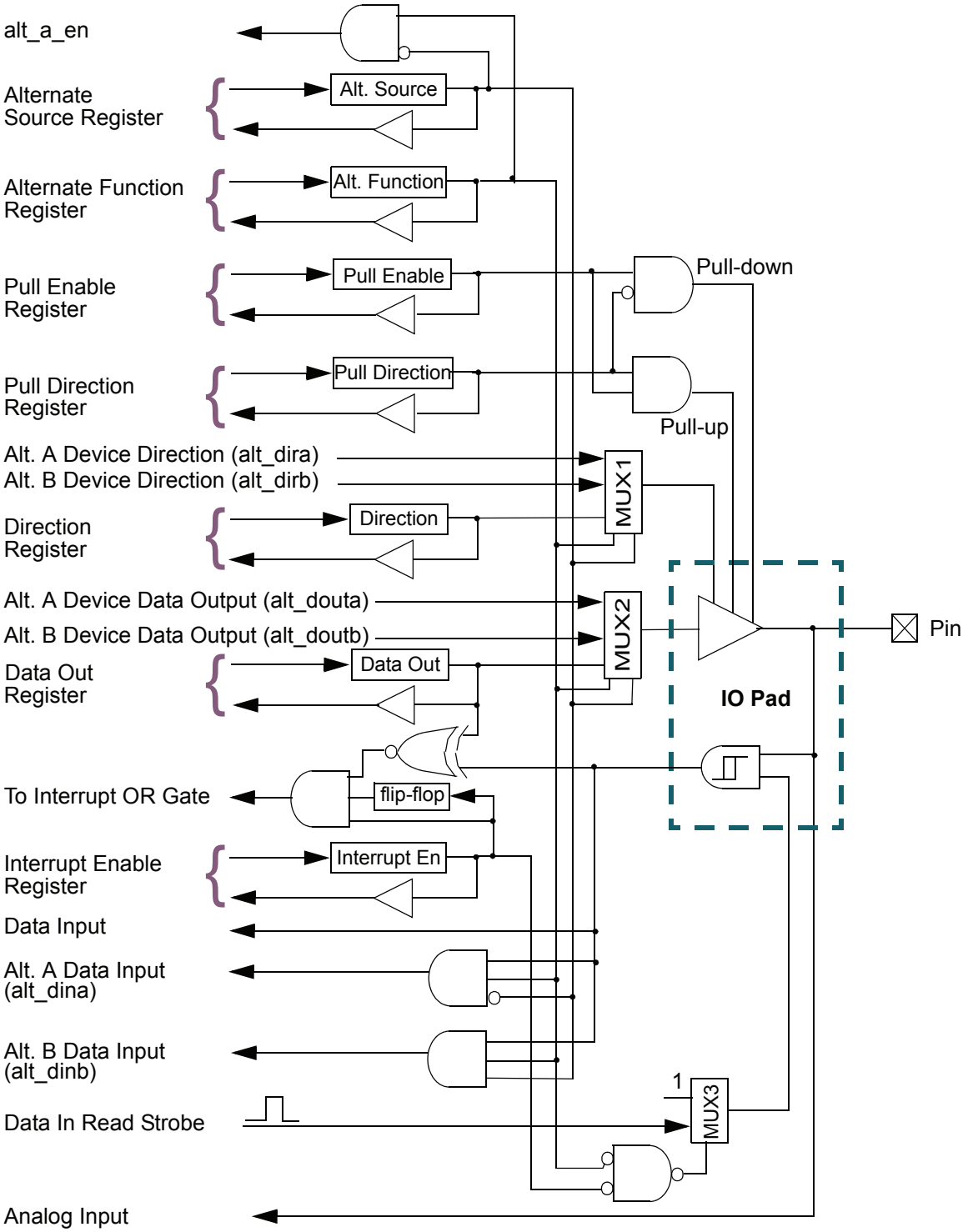


FIGURE 1: GPIO BLOCK DIAGRAM

Analog Input

A direct low-impedance path to the pin is provided to allow the inputs of an analog module (an analog-to-digital converter, for example) to be connected directly to the pin.

Interrupt Enable

The general-purpose I/O pin can be used as a level-sensitive interrupt input by following this sequence:

1. Set PxDIR to ‘0’.
2. Set PxALT to ‘0’.
3. Set the desired interrupt polarity into the PxDOUT register.
4. Enable the interrupt by setting PxIEN to ‘1’.

The interrupt signals from the 32 bits of the GPIO are OR’ed together to make one interrupt that is sent to an interrupt controller.

The Port Interrupt Enable Register (PxIEN) can be used to enable the read-back path from the pad through the I/O cell. This makes is possible to monitor the input value continuously.

Open-Drain Operation

In open-drain operation, the output buffer is toggled between driving logic low and tristate (high-impedance mode).

To use the general-purpose I/O pin as an inverting open-drain output buffer, software should clear the corresponding bit in PxDOUT and then use PxDIR to set the value to the port pin. When the signal’s direction is set as output (1), a value of ‘0’ is forced. When the direction is set for input (0), the output buffer is in tristate. The internal weak pull-up/pull-down can be used to pull the signal high or low when in tristate mode.

High Drive

The pin’s high-drive current output is selected by setting the appropriate bit of the High Drive Enable Register (PxHDRV).

Alternate Functions

If alternate function is programmed for a channel, that channel’s direction is controlled and its input/output data is read and written from a peripheral connected to one of two alternate sources (A or B). Each channel supports two alternate sources; software selects the currently active source (A or B) for each channel.

CHAPTER 2
REGISTERS

All of the port registers are 16 or 32-bit read/write registers, except for the Port Data In Register (PxDIN), which is read-only. Each register bit controls the function of the corresponding port pin. For example, PxDIR.2 (bit 2 of the PxDIR register) controls the direction of port pin Px[2].

All software accesses to any GPIO register must be greater than or equal to the size of the respective register. See “Register Summary” on page 17 for the complete list of registers.

Port Alternate Function Register (PxALT)

PxALT controls the use of the Px pins to function either as general-purpose I/O pins or as alternate function I/O pins. Each Px pin can be controlled independently.

When a PxALT bit is cleared (0), the corresponding pin is used as a general-purpose I/O pin. The output buffer is controlled by the Port Direction (PxDIR) and Port Data Output (PxDOUT) registers, and the input buffer is routed to the Port Data Input Register (PxDIN). In this case, the input buffer is blocked except when the buffer is actually being read.

When a bit in PxALT is set (1), the corresponding pin is used for an alternate function. The output buffer data and the state (tristate) are controlled by signals that originate from the alternate module. The input buffer is always enabled in this case.

Software should first select the alternate source by means of the Port Alternate Source Select Register (PxALTS), then the alternate function in PxALT, and then initialize the module that uses the alternate function on the pin. Altering this sequence may result in a glitch on the corresponding port pin.

A reset sets the Port Alternate Function Register (PxALT) to its reset value, which is a hardware configuration parameter (PxALT_RESET_VALUE).

15/31	0
Px Pins Alternate Function Enable	

- 0: General-purpose I/O selected
- 1: Alternate function selected

Port Alternate Source Select Register (PxALTS)

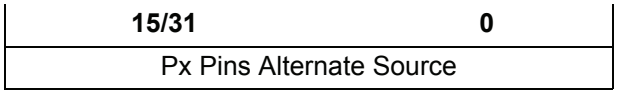
PxALTS controls the use of each of the port pins for alternate source A or for alternate source B.

When a PxALTS bit is cleared (0), the corresponding pin is used as an alternate function from alternate source A. The output buffer is controlled by the *alt_dira[i]* and *alt_douta[i]* signals and the input buffer is routed to the *alt_dina[i]* signal. The settings of the bits in this register have no effect if the corresponding bit in PxALT is cleared (0). The output signal *alt_a_en[i]* can be used to indicate to the device or to I/O cells that alternate source A is currently selected.

When a PxALTS bit is set (1), the corresponding pin is used as an alternate function from alternate source B. The output buffer is controlled by the *alt_dirb[i]* and *alt_doutb[i]* signals and the input buffer is routed to the *alt_dinb[i]* signal. The settings of the bits in this register have no effect if the corresponding bits in PxALT are cleared (0).

Software should first select the alternate source by means of PxALTS, then the alternate function in PxALT, and then initialize the module that uses the alternate function on the pin. Altering this sequence may result in a glitch on the corresponding port pin.

A reset sets the Port Alternate Source Select Register (PxALTS) to its reset value which is a hardware configuration parameter (PxALTS_RESET_VALUE).

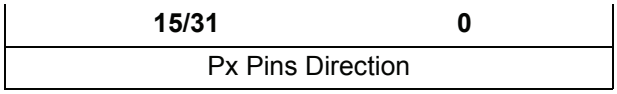


- 0: Alternate source A selected
- 1: Alternate source B selected

Port Direction Register (PxDIR)

PxDIR selects the direction of the Px pins except when using an alternate function. When an alternate function is used, the peripheral controls port direction. Each bit in the PxDIR register, when set (1), causes the corresponding port signal to serve as an output port, thus enabling the output buffer. When cleared, the port serves as an input port signal, thus putting the output buffer in the tristate state.

Upon reset, PxDIR is cleared (0). This configures all the pins in port Px as input pins.



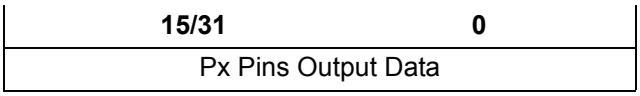
- 0: Input selected, output buffer in tristate
- 1: Output buffer selected

Port Data Output Register (PxDOUT)

PxDOUT holds the data to be driven on output port pins. When the pins are configured as outputs and no alternate function is enabled, writing to this register changes the output value. Reading the register returns the last value written to the register.

When an interrupt is enabled through the PxIEN register, the PxDOUT register specifies the signal level that asserts the interrupt.

A system reset leaves the register contents unchanged. At power-up, PxDOUT contains undefined data.



- 0: Drive output pin low
- 1: Drive output pin high

Port Data Input Register (PxDIN)

PxDIN is a read-only register. Reading from PxDIN returns the current value of the respective port pins. The software can read this register at any time, even when the pin is configured as an output.

15/31	0
Px Pins Input Data	

- 0: Pin is low
- 1: Pin is high

Port Weak Pull-up/Pull-down Direction Register (PxPDR)

PxPDR controls the pull-up/pull-down device direction of the associated pins. The pull-up device direction is set when the respective bit of PxPDR is set. The pull-down device direction is set when the respective bit of PxPDR is reset. In both general-purpose I/O or alternate function modes, the pin pull-up function is enabled by PxWKPU.

A reset sets the PxPDR register is set to its reset value which is a hardware configuration parameter (PxPDR_RESET_VALUE).

15/31	0
Px Pins Weak Pull-up/Pull-down Direction	

- 0: Pull-down selected
- 1: Pull-up selected

Port Weak Pull-up/Pull-down Enable Register (PxWKPU)

PxWKPU controls the pull-up/pull-down enable of the associated pins. Pull-up is enabled when the respective bit of PxPDR is set, the respective bit of PxWKPU is set, and the port buffer is disabled (tristate). The pull-down device is enabled when the respective bit of PxPDR is reset, the respective bit of PxWKPU is set, and the port buffer is tristated. For both general-purpose I/O and alternate function, the pin pull-up/pull-down function is enabled by PxWKPU.

A reset sets the PxWKPU register is set to its reset value which is a hardware configuration parameter (PxWKPU_RESET_VALUE).

15/31	0
Px Pins Weak Pull-up/Pull-down Enable	

- 0: Pull-up/pull-down disabled
- 1: Pull-up/pull-down enabled

Port Interrupt Enable Register (PxIEN)

PxIEN controls enabling level-sensitive interrupts from the associated pins. The interrupt is enabled when the respective bit of PxIEN is set. Prior to setting PxIEN, software should clear PxDIR and PxALT. Software should also set the desired polarity into PxDOUT.

Upon reset, PxIEN is cleared (0), disabling all interrupts.

PxIEN can be used to enable the read-back path from the pad through the I/O cell. This makes it possible to monitor the input value continuously.

15/31	0
Px Interrupt Enable	

- 0: Interrupt disabled
- 1: Interrupt enabled

High Drive Enable Register (PxHDRV)

PxHDRV controls the impedance of the I/O associated pins, if used for general-purpose I/O. To select high drive on a pin, the appropriate register bit should be set high (1).

After reset, PxHDRV is cleared to 0.

15/31	0
Px High Drive Enable	

- 0: High drive disabled
- 1: HIgh drive enabled

APPENDIX A
REGISTER SUMMARY

Table 3 and Table 4 list the GPIO registers. Table 5 and Table 6 show the layout of each register. For a more detailed description of each register, see “Registers” on page 11.

TABLE 3: REGISTER LIST (32 GPIO CHANNELS)

Register Name	Size [bits]	Register Address	Access Type	Value After Reset
PxALT	32	00_{16}	Read/Write	0000_0000_{16} – $FFFF\_FFFF_{16}$ Depends on parameter configuration
PxDIR	32	04_{16}	Read/Write	0000_0000_{16}
PxDIN	32	08_{16}	Read Only	$XXXX\_XXXX_{16}$
PxDOUT	32	$0C_{16}$	Read/Write	$XXXX\_XXXX_{16}$
PxWKPU	32	10_{16}	Read/Write	0000_0000_{16} – $FFFF\_FFFF_{16}$ Depends on parameter configuration
PxHDRV	32	14_{16}	Read/Write	0000_0000_{16}
PxALTS	32	18_{16}	Read/Write	0000_0000_{16} – $FFFF\_FFFF_{16}$ Depends on parameter configuration
PxIEN	32	$1C_{16}$	Read/Write	0000_0000_{16}
PxPDR	32	20_{16}	Read/Write	0000.0000_{16} – $FFFF\_FFFF_{16}$ Depends on parameter configuration

TABLE 4: REGISTER LIST (16 GPIO CHANNELS)

Register Name	Size [bits]	Register Address	Access Type	Value After Reset
PxALT	16	00_{16}	Read/Write	0000_{16} – $FFFF_{16}$ Depends on parameter configuration
PxDIR	16	04_{16}	Read/Write	0000_{16}
PxDIN	16	08_{16}	Read Only	$XXXX_{16}$
PxDOUT	16	$0C_{16}$	Read/Write	$XXXX_{16}$
PxWKPU	16	10_{16}	Read/Write	0000_{16} – $FFFF_{16}$ Depends on parameter configuration
PxHDRV	16	14_{16}	Read/Write	0000.0000_{16}
PxALTS	16	18_{16}	Read/Write	0000_{16} v $FFFF_{16}$ Depends on parameter configuration
PxIEN	16	$1C_{16}$	Read/Write	0000_{16}
PxPDR	16	20_{16}	Read/Write	0000_{16} – $FFFF_{16}$ Depends on parameter configuration

TABLE 5: REGISTER LAYOUT (32 GPIO CHANNELS)

GPIO Registers	31	0
PxALT	Px Pins Alternate Function Enable	
PxDIR,	Px Pins Direction	
PxDIN	Px Pins Output Data	
PxDOUT	Px Pins Input Data	
PxWKPU	Px Pins Weak Pull-up/Pull-down Enable	
PxHDRV	Px Pins High Drive Strength	
PxALTS	Px Pins Alternate Source	
PxIEN	Px Pins Interrupt Enable	
PxPDR	Px Pins Weak Pull-up/Pull-down Direction	

TABLE 6: REGISTER LAYOUT (16 GPIO CHANNELS)

GPIO Registers	15	0
PxALT	Px Pins Alternate Function Enable	
PxDIR,	Px Pins Direction	
PxDIN	Px Pins Output Data	
PxDOUT	Px Pins Input Data	
PxWKPU	Px Pins Weak Pullup/Pulldown Enable	
PxHDRV	Px Pins High Drive Strength	
PxALTS	Px Pins Alternate Source	
PxIEN	Px Pins Interrupt Enable	
PxPDR	Px Pins Weak Pullup/Pulldown Direction	