CX24116
Advanced Modulation DVB-S2 Demodulator and FEC Decoder

Data Sheet

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February 2006

CONEXANT

Ordering Information

Model Number	Description	Package
CX24116-12Z	Advanced Modulation DVB-S2 Demodulator and FEC Decoder	Pb (Lead)-free 100-pin eTQFP

Revision History

Revision	Date	Description
A	October 31, 2005	Initial release.
B	February 17, 2006	Second release.

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CX24116

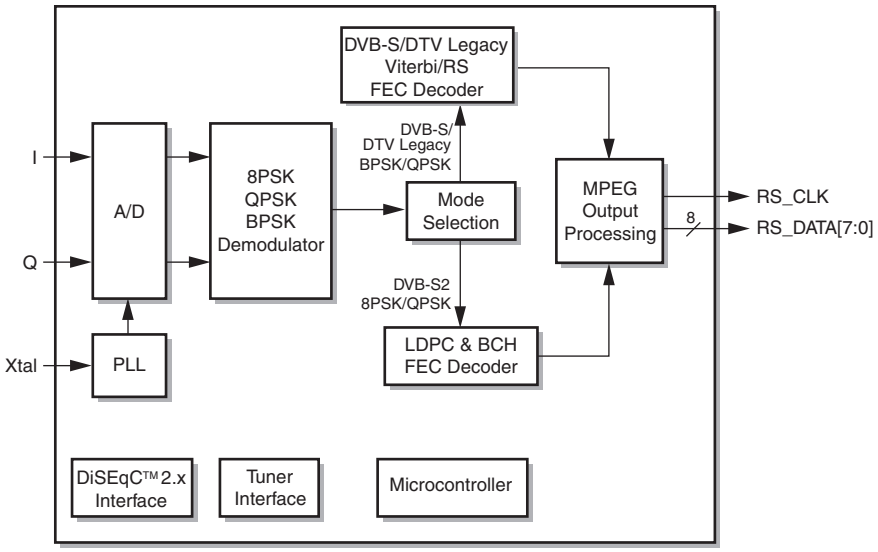
Advanced Modulation DVB-S2 Demodulator and FEC Decoder

The CX24116 complies with the open DVB-S2 standard for advanced modulation (8PSK modulation with LDPC/BCH Forward Error Correction), as well as DVB-S and DTV Legacy specifications. When combined with a satellite tuner, such as the CX24118A, the CX24116 provides a complete broadband satellite front-end solution for DVB-S2 satellite set-top boxes.

The CX24116 provides many advanced features that enhance overall system performance. An on-chip microcontroller enables fast signal acquisition, Es/No estimation and system monitoring, and saves software integration time by minimizing the external driver code requirement. The automatic acquisition state machine searches for and acquires the carrier within ±10 MHz range during initial acquisition and performs a smart search to reacquire during fade condition. The CX24116 has integrated Signal-to-Noise Ratio (SNR) and Bit Error Rate (BER) monitors for channel-performance measurements that simplify production testing.

The CX24116 is DiSEqC™ 2.x compliant, enabling two-way communication between the set-top box and peripheral satellite equipment.

Functional Block Diagram



Distinguishing Features

- Transmission format support:
  - LDPC/BCH (DVB-S2)
    - 8PSK: SR = 10–30 MSps
    - QPSK: SR = 10–30 MSps
  - DVB-S: SR = 2–45 MSps
  - DTV Legacy: SR = 20 MSps
- Automatic acquisition
  - ±10MHz acquisition range
- Serial/parallel output data interface
- Integrated SNR and BER monitors
- DiSEqC 2.x compliant
- Power down mode
- Internal microcontroller

Applications

- DVB-S2 set-top boxes
- PC receivers
- Residential gateways

Contents

Figures

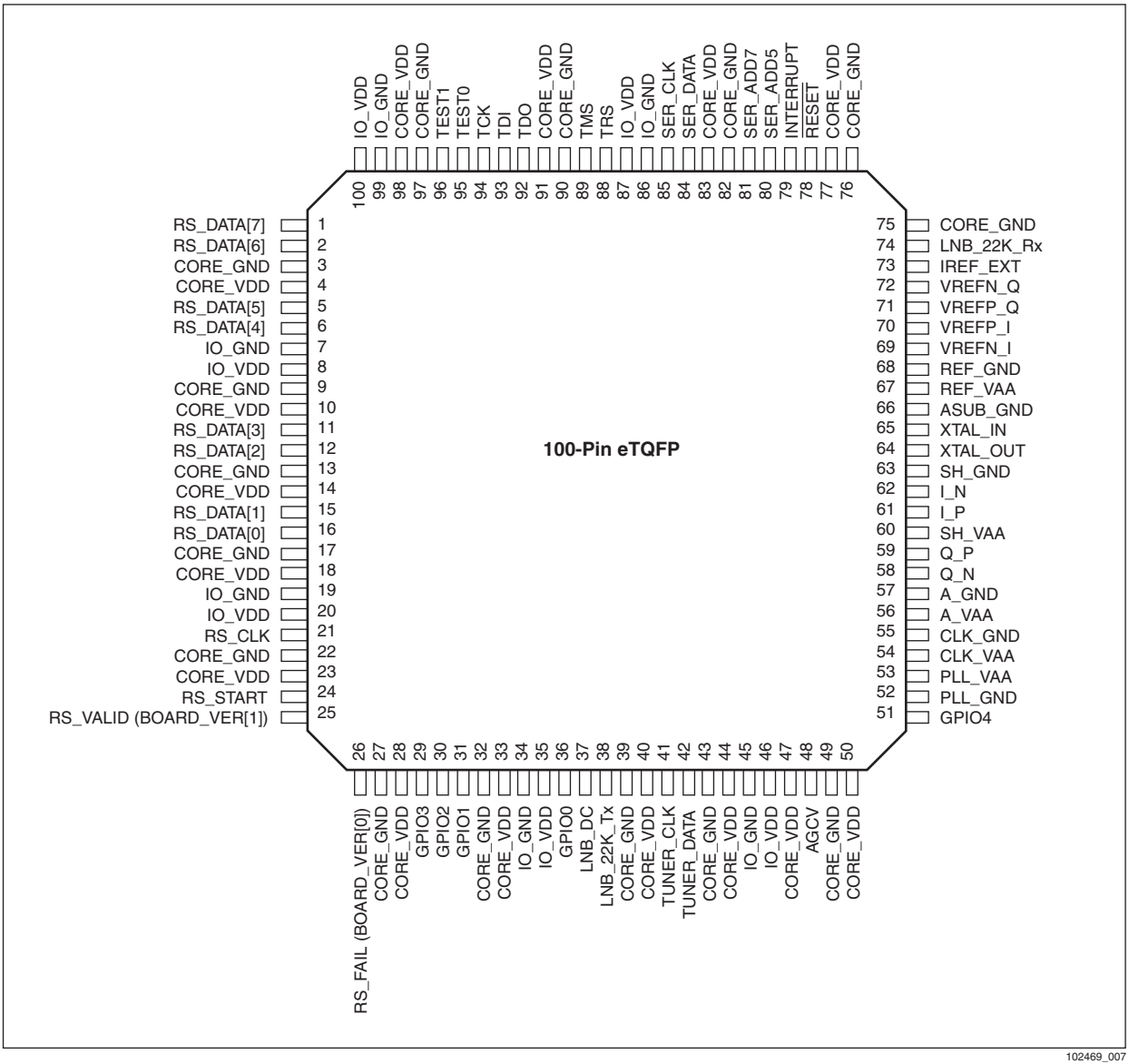
Tables

1 Pin Descriptions

1.1 Pin Diagram

Figure 1 provides a pinout of the CX24116.

Figure 1. Pinout Diagram



1.2 Pin Assignments

Table 1 lists the CX24116 pin names, numbers, types, and descriptions.

Table 1. Pin Assignments *(1 of 3)*

Pin Name	Pin Number	Type	Pin Description
MPEG Data Interface Pins			
RS_DATA[7:0]	1, 2, 5, 6, 11, 12, 15, 16	Output	MPEG data interface data pins. In serial mode, data can be produced on RS_DATA0 or RS_DATA7.
RS_CLK	21	Output	MPEG data interface clock pin.
RS_START	24	Output	MPEG data interface control signal - START.
RS_VALID (BOARD_VER[1])	25	Output	MPEG data interface control signal - VALID. This pin is also the BOARD_VER[1] pin.
RS_FAIL (BOARD_VER[0])	26	Output	MPEG data interface control signal - FAIL. This pin is also the BOARD_VER[0] pin.
Serial Programming Interface Pins			
SER_ADD5	80	Input	Bits 7 and 5 of the serial programming interface 8-bit address. Both pins are internally pulled up.(1)
SER_ADD7	81	Input	
SER_DATA	84	I/O	Serial programming interface data. Open drain. Internally pulled up.(1)
SER_CLK	85	Input	Serial programming interface clock. Internally pulled up.(1)
Tuner Interface Pins			
TUNER_CLK	41	Output	Clock signal to the tuner. Open drain.
TUNER_DATA	42	I/O	Data signal to the tuner. Open drain. Internally pulled up.(1)
AGCV	48	Output	AGC control output to the tuner.
Crystal Interface Pins			
XTAL_OUT	64	Output	Crystal oscillator pins. See Section 2.1 for recommended circuit configurations.
XTAL_IN	65	Input	
General Purpose Input/Output (GPIO) Pins			
GPIO3	29	I/O	GPIO. Optional open drain.(2)
GPIO2	30	I/O	GPIO. Optional open drain.(2)
GPIO1	31	I/O	GPIO. Optional open drain.(2)
GPIO0	36	I/O	GPIO. Optional open drain.(2)
GPIO4	51	I/O	GPIO. Optional open drain.(2)

Table 1. Pin Assignments *(2 of 3)*

Pin Name	Pin Number	Type	Pin Description
LNB Interface Pins			
LNB_DC	37	Output	LNB DC control signal. Optional open drain.(3)
LNB_22K_Tx	38	Output	LNB tone transmit signal.
LNB_22K_Rx	74	Input	LNB tone receive signal.
A/D Converter Pins			
Q_N	58	Input	-Q ADC analog input. Rin = 11 kΩ .
Q_P	59	Input	+Q ADC analog input. Rin = 11 kΩ .
I_P	61	Input	+I ADC analog input. Rin = 11 kΩ .
I_N	62	Input	-I ADC analog input. Rin = 11 kΩ .
VREFN_I	69	A	Negative reference output for external filtering.
VREFP_I	70	A	Positive reference output for external filtering.
VREFP_Q	71	A	Positive reference output for external filtering.
VREFN_Q	72	A	Negative reference output for external filtering.
IREF_EXT	73	A	External reference resistor connection.
JTAG Pins			
TRS	88	Input	JTAG pin. Internally pulled up.(1) Tie this pin to 0 V.
TMS	89	Input	JTAG pin. Internally pulled up.(1) Leave this pin unconnected.
TDO	92	Output	JTAG pin. Leave this pin unconnected.
TDI	93	Input	JTAG pin. Internally pulled up.(1) Leave this pin unconnected.
TCK	94	Input	JTAG pin. Tie this pin to 3.3 V.
Miscellaneous			
BOARD_VER[1:0]	25, 26	Input	Board version input. The state of BOARD_VER[1:0] at power-up can be read from register field SysBoardVer[1:0] to determine board settings. Can be tied to pull up or pull down.
RESET	78	Input	Chip reset. Active low. Internally pulled up.(1)
INTERRUPT	79	Output	Interrupt signal. Active low. Open drain.
TEST0	95	Input	Test pin. Tie this pin to ground for normal operation.
TEST1	96	Input	Test pin. Tie this pin to ground for normal operation.

Table 1. Pin Assignments *(3 of 3)*

Pin Name	Pin Number	Type	Pin Description
Power and Ground Pins			
CORE_GND	3, 9, 13, 17, 22, 27, 32, 39, 43, 49, 75, 76, 82, 90, 97,	Ground	Core ground.
CORE_VDD	4, 10, 14, 18, 23, 28, 33, 40, 44, 47, 50, 77, 83, 91, 98	Power	Digital core power: 1.25 V.
IO_GND	7, 19, 34, 45, 86, 99	Ground	I/O ground.
IO_VDD	8, 20, 35, 46, 87, 100	Power	Digital I/O power: 3.3 V.
ASUB_GND	66	Ground	Substrate ground.
REF_GND	68	Ground	Ground.
PLL_GND	52	Ground	PLL and crystal oscillator ground.
PLL_VAA	53	Power	Analog PLL and crystal oscillator power: 3.3 V.
CLK_VAA	54	Power	Analog clock generation circuitry power: 3.3 V.
CLK_GND	55	Ground	Clock generation circuitry ground
A_VAA	56	Power	Analog power supply: 3.3 V.
A_GND	57	Ground	Ground.
SH_VAA	60	Power	Analog I/Q channel power: 3.3 V.
SH_GND	63	Ground	Ground.
REF_VAA	67	Power	Analog bandgap and reference buffer circuitry power: 3.3 V.
Exposed Paddle	—	Thermal	Solder the exposed paddle to PCB ground. For more information, see Section 4.2.

FOOTNOTES:

(1) Internal pullup = 150 kΩ.

(2) This optional open drain pin is controlled by LLF 0x4E.

(3) This optional open drain pin is controlled by LLF 0x23.

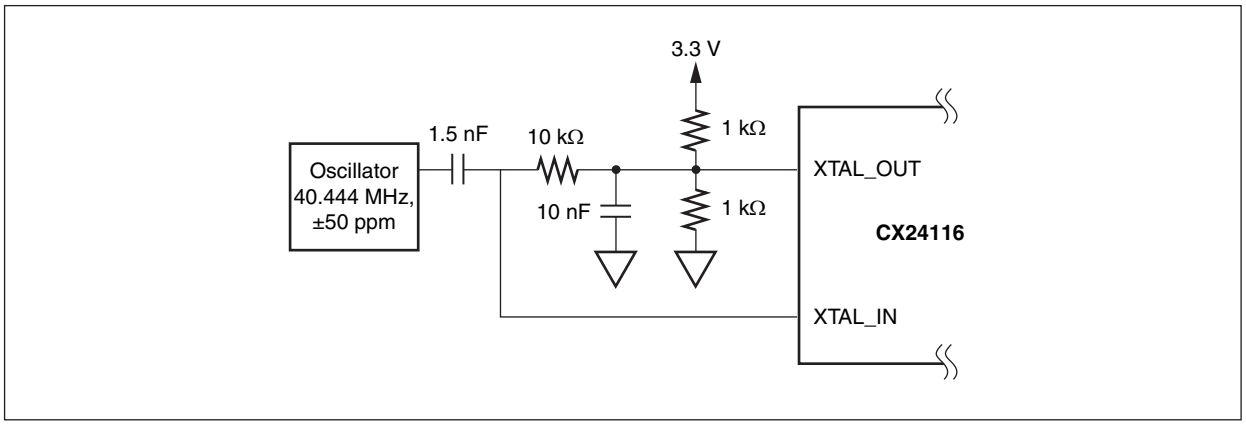
GENERAL NOTE: Digital I/O pads can drive 3.6 mA when low (0 V) and 7.8 mA when high (3.3 V).

2 Functional Descriptions

2.1 System Clock

The system clock is derived from the crystal oscillator pins XTAL_IN and XTAL_OUT. The oscillator can operate with a crystal or driven by a single-ended clock. When using an external clock, the circuit in Figure 2 is recommended.

Figure 2. Recommended External Clock Circuit



The clock from the oscillator is multiplied by the internal PLL to generate the system and sample clocks. Register bit PLLLock (0xFD[7]) gives the status of the PLL lock. When PLLLock = 1, the PLL is stable at the specified frequency. Calculations for critical clock frequencies are given below.

VCO frequency

$= \frac{f_{xtal}}{1} \times$ PLLMult[5:0]; when PLLPreDiv = 1

$= \frac{f_{xtal}}{2} \times$ PLLMult[5:0]; when PLLPreDiv = 0

Main clock frequency = 2 x f_{vco} / SYSMainClkDiv[2:0]

ADC sample frequency = f_{vco} / 4; when ADCClkDiv = 1

= f_{vco} / 6; when ADCClkDiv = 0

2.2 A/D Converters

CX24116 has two differential 8-bit A/D converters that run at the sample frequency. The sample frequency must be at least two times the highest symbol rate used.

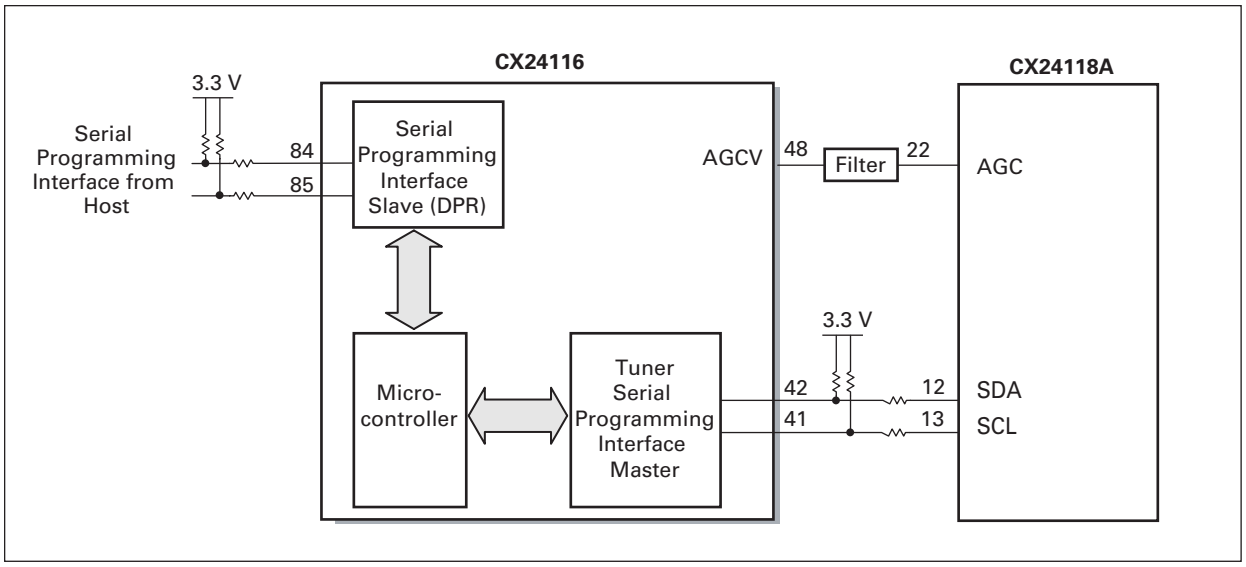
2.3 Tuner Control Interface

The CX24116 tuner control interface is compatible with CX24118A and CX24128 tuners. This interface consists of an isolated serial programming interface and an AGC signal. Legacy tuner controls LD and FILTERV, formerly passed between the demodulator and tuner as physical signals, are accessed through tuner registers. Both serial programming interface pins are open drain in order to support multiple masters.

2.3.1 Tuner Serial Programming Interface Control

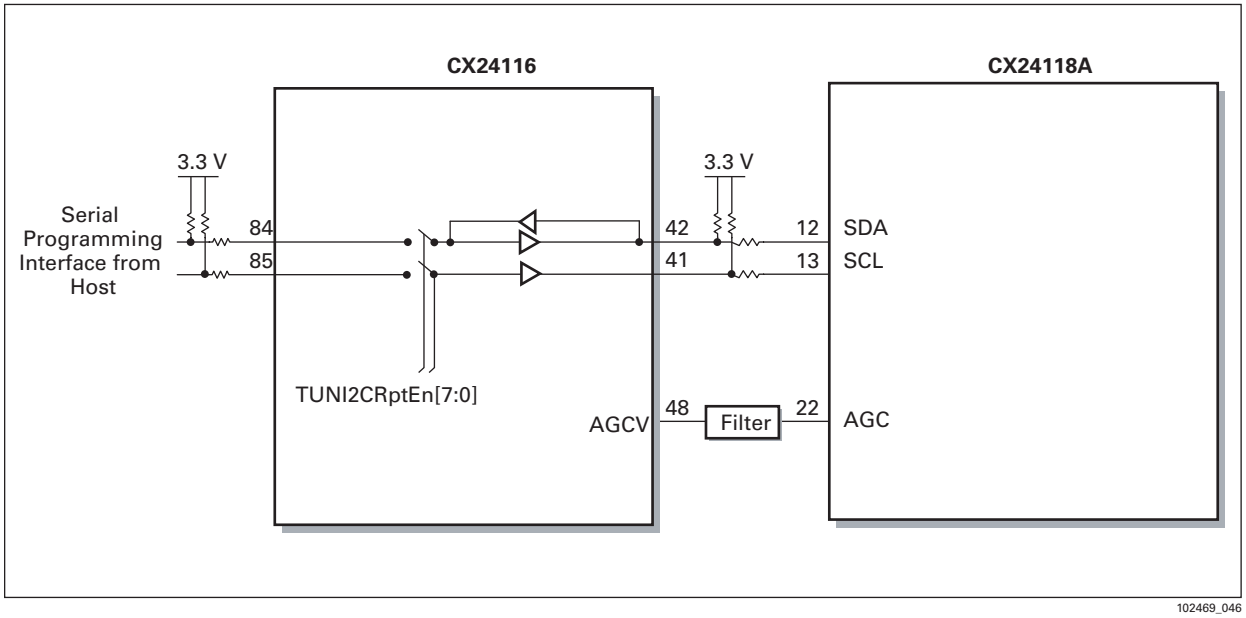
The primary means of controlling the tuner is through the firmware, with no access from the host processor. Figure 3 illustrates this method. Tuners CX24118A and CX24128 are both supported using this method.

Figure 3. Tuner Control Interface (with Firmware Support)



When firmware support is not available for a tuner (tuners other than CX24118A or CX24128), tuner pass-through can be used. Figure 4 illustrates the tuner control interface in pass-through mode.

Figure 4. Tuner Control Interface (Pass-through)



To enable pass-through mode, write 0x55 to register field TUNI2CRptEn[7:0] (0xE9[7:0]). This will connect the main serial programming interface to the tuner bus. When a stop condition is issued by the master, serial programming interface pass-through is automatically disabled. The following examples illustrate how to use tuner serial programming interface pass-through.

2.3.1.1 Tuner Pass-through Write Procedure

1. Send the start condition.
2. Send the CX24116's address with the read/$\overline{\text{write}}$ bit low (write), and receive an ACK.
3. Send address 0xE9, and receive an ACK.
4. Send 0x55 to TUNI2CRptEn[7:0] (0xE9[7:0]) and receive an ACK.
   – Pass-through is now enabled.
5. Send a repeat-start condition.
6. Send the tuner's address with the read/$\overline{\text{write}}$ bit low (write), and receive an ACK.
   – 0x28 or 0xA8 for the CX24118A and CX24128 tuners.
7. Send the tuner register address of interest, and receive an ACK.
8. Send one byte of data, and receive an ACK.
9. Step 7 can be repeated for multiple bytes in subsequent registers.
10. Send a stop condition.
    – When a stop condition is issued by the master, the CX24116 disables serial programming interface pass-through.

2.3.1.2 Tuner Pass-through Read Procedure

1. Send the start condition.
2. Send the CX24116's address with the read/$\overline{\text{write}}$ bit low (write), and receive an ACK.
3. Send address 0xE9, and receive an ACK.
4. Send 0x55 to TUNI2CRptEn[7:0] (0xE9[7:0]), and receive an ACK.
   – Pass-through is now enabled.

5. Send a repeat-start condition.
6. Send the tuner's address with the read/write bit low (write), and receive an ACK.
   – 0x28 or 0xA8 for the CX24118A and CX24128 tuners.
7. Send the tuner register address of interest, and receive an ACK.
8. Send a repeat-start condition.
   – It is critical that a repeat-start condition is sent at this point instead of separate stop and start conditions, because the CX24116 disables serial programming interface pass-through when a stop condition is detected.
9. Send the tuner's address with the read/write bit high (read), and receive an ACK
   – 0x29 or 0xA9 for the CX24118A and CX24128 tuners.
10. Receive a byte from the desired register and transmit an ACK.
11. Step 9 can be repeated for multiple bytes in subsequent registers.
12. Transmit a stop condition.
    – When a stop condition is issued by the master, the CX24116 disables serial programming interface pass-through.

2.3.2 AGC Signal

The AGC function is a closed-loop system. The CX24116 sends the control signal AGCV (pin 48) to the tuner via a Sigma-Delta DAC output that ranges from 0 V to 3.3 V after filtering. The AGC control in the tuner responds to this signal by raising or lowering the gain in the I and Q paths. The I and Q signals are then sampled by the demodulator and their average voltage levels are determined; these levels are compared to a threshold that is fixed by the firmware. If the I and Q levels are lower than expected, the voltage level on the AGCV pin is raised; if the I and Q levels are higher than expected, the voltage level on the AGCV pin is lowered.

The AGCV voltage correlates to the AGC accumulator, which can be monitored by reading register field AGCAcc[9:0] (0x9D[7:6], 0x9E[7:0]).

In addition to normal, closed-loop operation, LLF 0x3B enables two AGC test modes. Test mode 1 freezes the current AGC accumulator value, and test mode 2 allows the AGC accumulator to be manually set. For more detail, see LLF 0x3B descriptions.

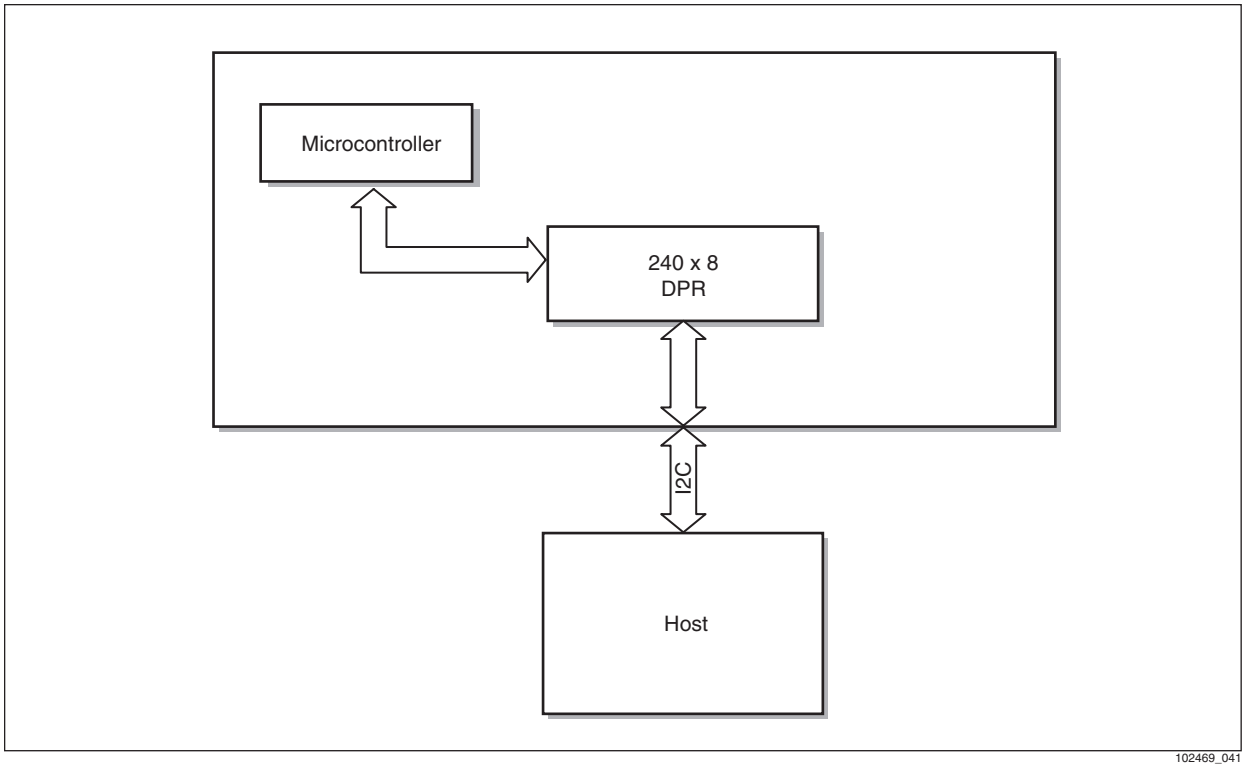
3 Communications and Control

The CX24116's control interface is a two-wire serial programming interface, as described in Section 3.2. There is no direct access to most of the device registers. Instead, Low Level Functions (LLFs) are written to the device's embedded microcontroller. For easy access, many parameters are written to the status registers by the microcontroller. A map and index of the CX24116 registers, including the LLFs, are provided in Section 3.3 and Section 3.4. A register detail for serial programming interface addresses 0x94 through 0xFF is provided in Section 3.5. A map and detailed descriptions of the LLFs are provided in Section 3.6 and Section 3.7.

3.1 Memory and Architecture

A simplified block diagram of the microcontroller's architecture is shown in Figure 5. It consists of a microcontroller and Dual Port RAM (DPR). LLFs are written to the DPR. Parameters can be read from the device's read-only status registers.

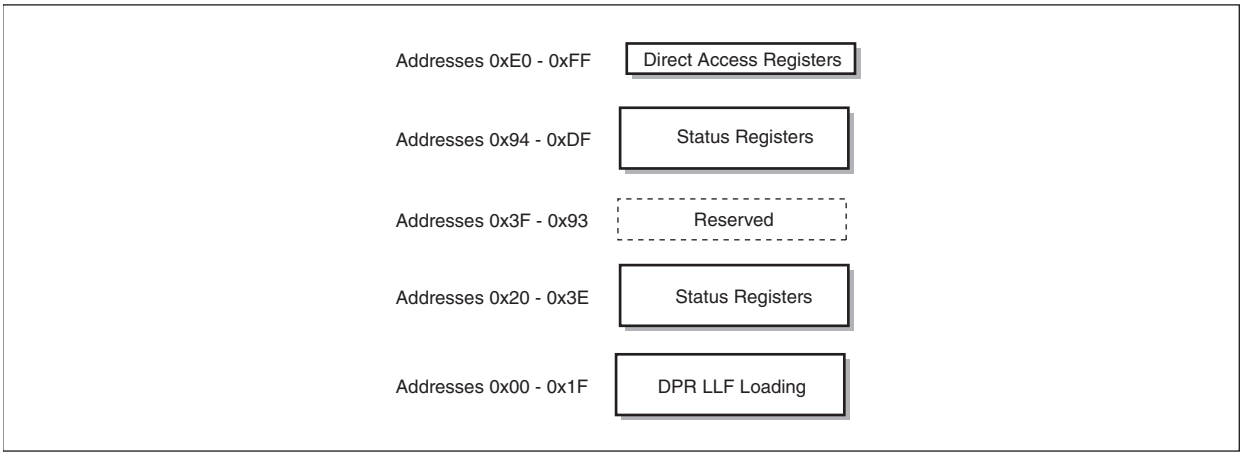
Figure 5. Simplified Microcontroller Architecture



3.1.1 Serial Programming Interface Address Definitions

Instead of directly accessing device registers, the serial programming interface addresses define memory function areas. These memory areas are shown in Figure 6.

Figure 6. Serial Programming Interface Address Mapping



3.1.2 Microcontroller Code and Data Loading

The embedded microcontroller within the CX24116 requires firmware code that must be downloaded to the device memory before operation. The microcontroller code and data loading area is located at serial programming interface addresses 0xF0–0xF7.

Table 2 gives the microcontroller code/data loading address map. Address 0xF7 contains the program code or data, and addresses 0xF5–0xF6 contain the 15-bit memory address that the data will be written to. The proper write sequence is address 0xF5, then 0xF6, and then 0xF7.

Table 2. Microcontroller Code/Data Loading Address Map

Address (Hex)	Data Bits							
	7	6	5	4	3	2	1	0
F0	Reserved				SYSPnXReset	SYSPnReset	MCPReset	MCReset
F4	I2CAutoIncDis	Reserved		MCLoadDis	Reserved		MCLoadSel	MCLoadEn
F5	MCLoadAdd[7:0]							
F6	Reserved	MCLoadAdd[14:8]						
F7	MCLoadData[7:0]							

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

The microcontroller address pointer is incremented automatically when address 0xF7 is written to. Therefore, once the starting memory address is specified (usually 0x0000), repeated writes to address 0xF7 will fill in memory in ascending order.

3.1.2.1 Example Microcontroller Code Loading Procedure

1. Reset the CX24116 by toggling the $\overline{\text{RESET}}$ pin.
2. Hold the microcontroller in reset by writing 0x03 to address 0xF0.
3. Enable loading and disable I2C auto-incrementing by writing 0x81 to address 0xF4.
4. Specify the starting address as 0x0000.
   a. Write 0x00 to address 0xF5.
   b. Write 0x00 to address 0xF6.
5. Write the data to address 0xF7.
6. Repeat step 5 until all of the program data has been written to memory.
7. Enable I2C auto-incrementing and disable loading by writing 0x10 to address 0xF4.
8. Release the microcontroller from reset by writing 0x00 to address 0xF0.

3.1.3 LLF Structure and Dual Port RAM (DPR)

The LLF structure, as shown in Table 3, consists of an op-code, a write token, and from 0 to 30 arguments. Each op-code defines a specific function with a predefined number of arguments. All op-codes are described later in this chapter. The write token is an arbitrary non-zero number that is assigned by the user for tracking purposes.

Table 3. DPR LLF Loading Address Map

Register Address	Register Field Name
00	LLFOpCode[7:0]
01	LLFArg1[7:0]
02	LLFArg2[7:0]
03	LLFArg3[7:0]
04	LLFArg4[7:0]
...	
1D	LLFArg29[7:0]
1E	LLFArg30[7:0]
1F	LLFWrtTok[7:0]

The DPR provides the means of communicating with the microcontroller. LLFs can be written to the DPR by writing to serial programming interface addresses 0x00–0x1F.

The op-code must be written to address 0x00 and its arguments must be written to addresses 0x01–0x1E. Arguments must be written to their appropriate addresses, as defined by the op-code definition. For example, if an op-code has only two arguments. argument 1 must be written to address 0x01, and argument 2 must be written to address 0x02. Registers for arguments that are not defined are ignored. The write token must be written to register 0x1F.

When writing an LLF, the op-code and arguments must be issued first, but can be in any order. The write token must be written last and tells the microcontroller that the LLF is complete and ready to be processed. After an LLF has been issued, the write token can be read to check the status of the LLF. If the write token is 0, then the LLF has been successfully received. An example LLF writing procedure is given below.

3.1.3.1 Example LLF Writing Procedure

Conditions

Write op-code 0x37 with 3 arguments in numerical order. The data values should be 0x22 for argument 1, 0x33 for argument 2 and 0x44 for argument 3. Use a write token value of 0x1F.

Procedure

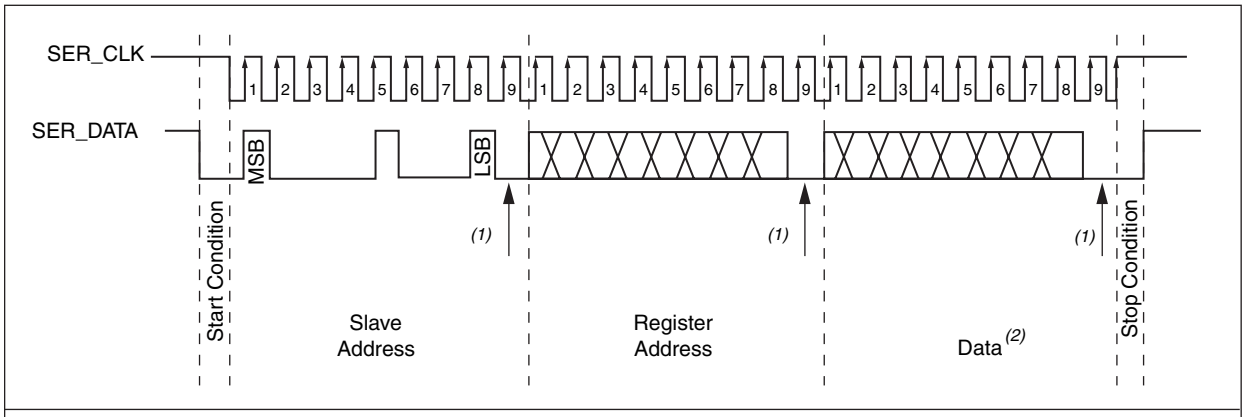
1. Write the op-code value of 0x37 to address 0x00.
2. Write the argument 1 value of 0x22 to address 0x01.
3. Write the argument 2 value of 0x33 to address 0x02.
4. Write the argument 3 value of 0x44 to address 0x03.
5. Write the write token value of 0x1F to address 0x1F.
   – The write token can be any arbitrary non-zero value.
6. Read the write token from address 0x1F.
   a. If the write token is 0, the LLF has been processed and the new LLFs can be issued.

3.2 Serial Programming Interface

3.2.1 General

The CX24116 uses a 400 kHz two-wire serial programming interface to program the device registers. The interface operates at 3.3 V input levels. Figure 7 illustrates the timing relationship between the SER_DATA and SER_CLK signals during a typical transaction. Both lines require external pullup resistors.

Figure 7. Serial Programming Interface Timing Diagram



FOOTNOTE:
(1) Acknowledge generated by CX24116.
(2) Subsequent bytes are assumed to be data for registers whose addresses follow in ascending order.

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Every data word must be 8 bits long (MSB first), followed by an acknowledge bit, generated by the receiving device. Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the slave address byte. If this is the CX24116 address, the CX24116 generates an acknowledge signal by pulling the SER_DATA line low during the ninth clock pulse. The eighth bit of the device address byte is the read/write bit (high = read from the device, low = write to the device). Data bytes are always acknowledged during the ninth clock pulse by the addressed device.

NOTE: During the acknowledge period, the master device must leave the SER_DATA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the CX24116 remains in the state defined by the last complete data byte transmitted, and any master acknowledge subsequent to reading the device address is ignored.

3.2.2 Device Address

The CX24116 device address is configured by the state of the SER_ADD7 and SER_ADD5 pins. SER_ADD7 and SER_ADD5 pins set the state of the seventh and fifth bits of the CX24116's 8-bit serial address, as listed in Table 4. Both pins are internally pulled up, so that when these two pins are left unconnected, the 7-bit device address is 0x55. Since bit 0 of the device address is a read/write bit, the device address is given as the 7 MSBs of the device address. Subsequent read and write addresses are given in Table 4.

Table 4. Serial Address Options

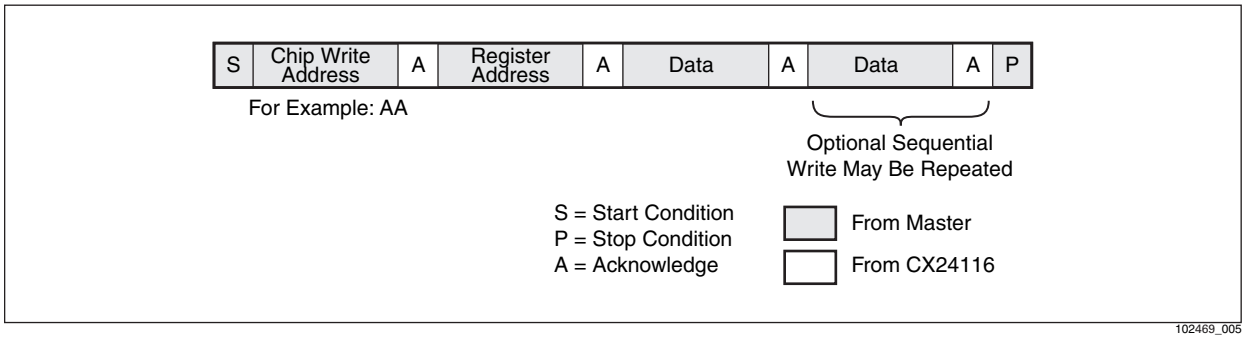
SER_ADD7	SER_ADD5	7-Bit Device Address		8-Bit Device Write Address (Hexadecimal)	8-Bit Device Read Address (Hexadecimal)
		Binary	Hexadecimal		
0	0	0000101	05	0A	0B
0	1	0010101	15	2A	2B
1	0	1000101	45	8A	8B
1 (Default)	1 (Default)	1010101	55	AA	AB

3.2.3 Write Function

A write transaction involves sending the device address byte with the read/$\overline{\text{write}}$ bit low, and following it with one or more bytes. The first byte following the device address byte is always a register address, which sets an internal register address pointer. If a second byte follows the device address byte, it is the data to be written to the register indexed in the first byte. Under normal conditions (auto-increment enabled), subsequent bytes are assumed to be data for registers whose addresses follow in ascending order, as the internal address pointer is incremented at the completion of each register write. The state of this internal address pointer upon exiting a write transaction is used for any read transactions that follow. Alternatively, the auto-incrementing function can be disabled by setting register bit I2CAutoIncDis (0xF4[7]) to 1. Figure 8 illustrates a typical register write sequence.

1. Master transmits the device address with the read/$\overline{\text{write}}$ bit low.
2. Master transmits the desired register address.
3. Master transmits the register data byte.
4. Subsequent registers are written until a stop condition is detected.

Figure 8. Serial Programming Interface Typical Write Sequence

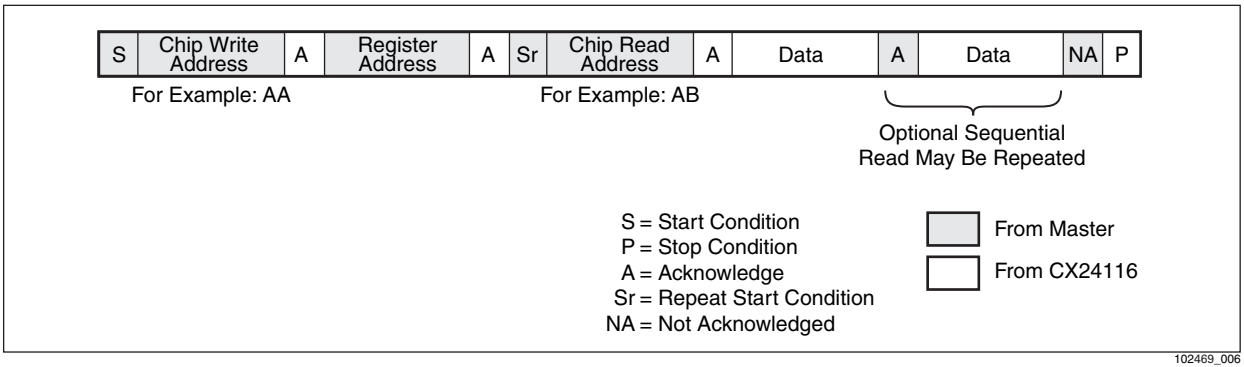


3.2.4 Read Function

A read transaction involves sending the device address byte with the read/$\overline{\text{write}}$ bit high, and receiving one or more bytes. The first byte returned after the device address byte makes up the contents of the last indexed register address. Any subsequent data bytes read come from registers whose address follows in ascending order as the internal address pointer is incremented at the completion of every read. The initial register address depends on the state of the pointer at the end of the last write transaction. Because writing even one data byte to a register will increment the address pointer, typically one would want to precede a read with a write transaction that sends only the register address byte. Figure 9 illustrates a typical register read sequence.

1. Master transmits the device address with the read/$\overline{\text{write}}$ bit low.
2. Master transmits the desired register address.
3. Master generates a repeat start.
4. Master transmits the device address with the read/$\overline{\text{write}}$ bit high.
5. Slave (CX24116) transmits the data byte to master.
6. Subsequent registers are read until a stop condition is detected.

Figure 9. Serial Programming Interface Typical Read Sequence



3.3 Register Bit Map

The register bit map is shown in Table 5. It contains information on the following types of registers, sorted by type:

- Low Level Function (LLF) loading registers
- Status registers (read-only)
- Fixed registers (direct access registers)

Device parameters can be read from the status registers, located at serial programming interface addresses 0x20–0x3E and 0x94–0xD7. The fixed registers, located at serial programming interface addresses 0xE0–0xFF, are active registers that affect part operation.

Table 5. Register Bit Map *(1 of 5)*

Register (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
LLF Loading Registers								
00	LLFOpCode[7:0]							
01	LLFArg1[7:0]							
02	LLFArg2[7:0]							
03	LLFArg3[7:0]							
04	LLFArg4[7:0]							
05	LLFArg5[7:0]							
06	LLFArg6[7:0]							
07	LLFArg7[7:0]							
08	LLFArg8[7:0]							
09	LLFArg9[7:0]							
0A	LLFArg10[7:0]							
0B	LLFArg11[7:0]							
0C	LLFArg12[7:0]							
0D	LLFArg13[7:0]							
0E	LLFArg14[7:0]							
0F	LLFArg15[7:0]							
10	LLFArg16[7:0]							
11	LLFArg17[7:0]							
12	LLFArg18[7:0]							
13	LLFArg19[7:0]							
14	LLFArg20[7:0]							
15	LLFArg21[7:0]							

***Table 5. Register Bit Map** (2 of 5)*

Register (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
16	LLFArg22[7:0]							
17	LLFArg23[7:0]							
18	LLFArg24[7:0]							
19	LLFArg25[7:0]							
1A	LLFArg26[7:0]							
1B	LLFArg27[7:0]							
1C	LLFArg28[7:0]							
1D	LLFArg29[7:0]							
1E	LLFArg30[7:0]							
1F	LLFWrtTok[7:0]							
Status Registers								
20	Reserved							MCResetS
94	SYSChipID[7:0]							
95	SYSChipVer[7:0]							
96	SYSFWVer[7:0]							
97	TUNFreqS[23:16]							
98	TUNFreqS[15:8]							
99	TUNFreqS[7:0]							
9A	ACQSRNomS[15:8]							
9B	ACQSRNomS[7:0]							
9C	ACQPilotEnS	ACQSICurr	ACQVitCRCurr[5:0]					
			ACQMCCurr[5:0]					
9D	AGCAcc[9:8]		TUNIOSync	Reserved	ACQRSBCH Sync	ACQCvdSync	ACQDMDSync	TUNPLLLock
9E	AGCAcc[7:0]							
9F	ACQFreqOff[15:8]							
A0	ACQFreqOff[7:0]							
A1	ACQSROff[15:8]							
A2	ACQSROff[7:0]							
A3	ESNOCount[15:8]							
A4	TUNReg00[7:0]							

Table 5. Register Bit Map *(3 of 5)*

Register (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
A5	TUNReg01[7:0]							
A6	TUNReg02[7:0]							
A7	TUNReg03[7:0]							
A8	TUNReg10[7:0]							
A9	TUNReg11[7:0]							
AA	TUNReg12[7:0]							
AB	TUNReg13[7:0]							
AC	TUNReg14[7:0]							
AD	TUNReg15[7:0]							
AE	TUNReg16[7:0]							
AF	TUNReg17[7:0]							
B0	TUNReg18[7:0]							
B1	TUNReg19[7:0]							
B2	TUNReg1A[7:0]							
B3	TUNReg1B[7:0]							
B4	TUNReg1C[7:0]							
B5	TUNReg1D[7:0]							
B6	TUNReg1E[7:0]							
B7	TUNReg1F[7:0]							
B8	TUNReg20[7:0]							
B9	TUNReg21[7:0]							
BA	Reserved				INTLNBRx RdyEnS	INTLNBTx RdyEnS	INTRSBCH UnLockEnS	INTRSBCH LockEnS
BB	Reserved				INTLNBRxRdy	INTLNBTxRdy	INTRSBCHUn Lock	INTRSBCHLock
BC	LNBToneS	LNBRxRdy	LNBTxRdy	LNBBstModSel	LNBDCS	LNBDi2RxLength[2:0]		
BD	LNBDi2RxError[7:0]							
BE	LNBDi2RxMsg1[7:0]							
BF	LNBDi2RxMsg2[7:0]							
C0	LNBDi2RxMsg3[7:0]							
C1	LNBDi2RxMsg4[7:0]							

***Table 5. Register Bit Map** (4 of 5)*

Register (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
C2	LNBDi2RxMsg5[7:0]							
C3	LNBDi2RxMsg6[7:0]							
C4	LNBDi2RxMsg7[7:0]							
C5	LNBDi2RxMsg8[7:0]							
C6	BERRSBchCBtEC[31:24]							
C7	BERRSBchCBtEC[23:16]							
C8	BERRSBchCBtEC[15:8]							
C9	BERRSBchCBtEC[7:0]							
CA	BERRSBchUcFmEC[15:8]							
CB	BERRSBchUcFmEC[7:0]							
CC	BERRSBchErrRdy[7:0]							
CD	BERCRCUcFmEC[15:8]							
CE	BERCRCUcFmEC[7:0]							
CF	BERCRCErrRdy[7:0]							
D0	TUNDrvErr[7:0]							
D4	MCCounter[7:0]							
D5	ESNOCount[7:0]							
D6	LNBDi2RxPar[7:0]							
D7	Reserved							FECOCDisS
DB	BERWinAdj[15:8]							
DC	BERWinAdj[7:0]							
DD	BERCRCWinAdj[15:8]							
DE	BERCRCWinAdj[7:0]							
Fixed Registers								
E0	Reserved						PLLClkDis	PLLDis
E1	Reserved						ADCDis	Reserved
E5	Reserved	PLLPreDiv	Reserved					
E8	Reserved			SYSBoardVer[1:0]		Reserved		
E9	TUNI2CRptEn[7:0]							
EA	SYSClkDis[7:0]							

Table 5. Register Bit Map *(5 of 5)*

Register (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
F0	Reserved				SYSXReset	SYSReset	MCPReset	MCReset
F1	Reserved		PLLCPCntl[5:0]					
F2	Reserved		PLLMult[5:0]					
F3	Reserved	MPGClkSmthDiv[2:0]			Reserved	SYSMainClkDiv[2:0]		
F4	I2CAutoIncDis	Reserved		MCLoadDis	Reserved		MCLoadSel	MCLoadEn
F5	MCLoadAdd[7:0]							
F6	Reserved	MCLoadAdd[14:8]						
F7	MCLoadData[7:0]							
F8	Reserved					SYSLDPCClkDiv[2:0]		
F9	Reserved							ADCClkDiv
FD	PLLLock	GPIORdVal[6:0]						
Chip Information								
FE	SysChipVer[7:0]							
FF	SysChipID[7:0]							

3.4 Register Index

The register index is shown in Table 6. It contains information on the following types of registers, sorted by field name:

- Low Level Function (LLF) loading registers
- Status registers (read-only)
- Fixed registers (direct access registers)
- Parameter or argument names within LLFs

Table 6. Register Index *(1 of 8)*

Field Name	Location	Register or Argument	Description
ACQAlpha[1:0]	LLF 0x11	Arg12[1:0]	Alpha or Roll-off Factor
ACQCREn[7:0]	LLF 0x11	Arg13[7:0]	Viterbi Code Rate Search Enable
ACQCvdSync	Status Register	9D[2]	Viterbi or LDPC Sync Indicator
ACQDMDSync	Status Register	9D[1]	Demodulator Sync Indicator
ACQFreqMax[15:0]	LLF 0x11	Arg8[7:0], Arg9[7:0]	Frequency Search Range
ACQFreqOff[15:0]	Status Register	9F[7:0] A0[7:0]	Frequency Offset
ACQMCCurr[5:0]	Status Register	9C[5:0]	Current Mode Code
ACQModCode[5:0]	LLF 0x11	Arg7[5:0]	Mode Code (Modulation Format and Transport Spec)
ACQMode[1:0]	LLF 0x11	Arg6[1:0]	Acquisition Mode
ACQPilotEn[1:0]	LLF 0x11	Arg7[7:6]	Pilot Enable
ACQPilotEnS	Status Register	9C[7]	Pilot Enable Status
ACQPRFreqNom[15:0]	LLF 0x11	Arg10[7:0], Arg11[7:0]	Nominal Phase Rotator Frequency
ACQRSBCHSync	Status Register	9D[3]	Reed-Solomon or BCH Sync Indicator
ACQSICurr	Status Register	9C[6]	Current Spectral Inversion State
ACQSISearch[1:0]	LLF 0x11	Arg6[3:2]	Spectral Inversion Search Select
ACQSRNom[15:0]	LLF 0x11	Arg4[7:0]. Arg5[7:0]	Nominal Symbol Rate
ACQSRNomS[15:0]	Status Register	9A[7:0] 9B[7:0]	Nominal Symbol Rate Status
ACQSROff[15:0]	Status Register	A1[7:0] A2[7:0]	Symbol Rate Offset
ACQVitCRCurr[5:0]	Status Register	9C[5:0]	Current Viterbi Code Rate

Table 6. Register Index *(2 of 8)*

Field Name	Location	Register or Argument	Description
ADCClkDiv	Fixed Register	F9[0]	ADC Clock Divider
ADCDis	Fixed Register	E1[1]	ADC Disable
AGCAcc[9:0]	Status Register	9D[7:6] 9E[7:0]	Front-End AGC Accumulator
AGCMode[1:0]	LLF 0x3B	Arg1[1:0]	Front-End AGC Mode
AGCVal[9:0]	LLF 0x3B	Arg2[1:0], Arg3[7:0]	Front-End AGC Accumulator Value in Manual Mode
BERCRCErrRdy[7:0]	Status Register	CF[7:0]	CRC Error Count Ready Indicator
BERCRCUcFmEC[15:0]	Status Register	CD[7:0], CE[7:0]	CRC Uncorrected Frame Error Count
BERCRCWinAdj[15:0]	Status Register	DD[7:0], DE[7:0]	CRC Window Adjustment
BERRSBchCBtEC[31:0]	Status Register	C6[7:0] C7[7:0] C8[7:0] C9[7:0]	Reed-Solomon or BCH Corrected Bit Error Count (NBC, DVB-S, or DTV Legacy)
BERRSBchErrRdy[7:0]	Status Register	CC[7:0]	Reed-Solomon or BCH Error Count Ready Indicator (NBC, DVB-S, or DTV Legacy)
BERRSBchUcFmEC[15:0]	Status Register	CA[7:0] CB[7:0]	Reed-Solomon or BCH Uncorrected Frame Error Count (NBC, DVB-S, or DTV Legacy)
BERWin	LLF 0x3C	Arg1[0]	BER Window Size
BERWinAdj[15:0]	Status Register	DB[7:0], DC[7:0]	BER Window Adjustment
ESNOCount[15:0]	Status Register	A3[7:0], D5[7:0]	EsN0 Count
FECOCDis	LLF 0x34	Arg1[0]	Outer FEC Code Error Correction Disable
FECOCDisS	Status Register	D7[0]	Outer FEC Code Error Correction Disable Status
GPIODir[4:0]	LLF 0x32	Arg1[4:0]	GPIO Direction
GPIODirMsk[4:0]	LLF 0x32	Arg2[4:0]	GPIO Direction Mask
GPIOMode[4:0]	LLF 0x4E	Arg1[4:0]	GPIO Mode
GPIORdVal[6:0]	Fixed Register	FD[6:0]	GPIO Read Value
GPIOVal[4:0]	LLF 0x33	Arg1[4:0]	GPIO Write Values
GPIOValMsk[4:0]	LLF 0x33	Arg2[4:0]	GPIO Write Mask

Table 6. Register Index *(3 of 8)*

Field Name	Location	Register or Argument	Description
I2CAutoIncDis	Fixed Register	F4[7]	I2C Auto Increment Disable
INTLNBRxRdy	Status Register	BB[3]	LNB Receive Message Ready Interrupt
INTLNBRxRdyEn	LLF 0x30	Arg1[3]	LNB Receive Message Ready Interrupt Enable/Clear
INTLNBRxRdyEnS	Status Register	BA[3]	LNB Receive Message Ready Interrupt Enable Status (read-only)
INTLNBRxRdyMsk	LLF 0x30	Arg2[3]	LNB Receive Message Ready Interrupt Mask
INTLNBTxRdy	Status Register	BB[2]	LNB Transmit Message Ready Interrupt (read-only)
INTLNBTxRdyEn	LLF 0x30	Arg1[2]	LNB Transmit Message Ready Interrupt Enable/Clear
INTLNBTxRdyEnS	Status Register	BA[2]	LNB Transmit Message Ready Interrupt Enable Status (read-only)
INTLNBTxRdyMsk	LLF 0x30	Arg2[2]	LNB Transmit Message Ready Interrupt Mask
INTRSBCHLock	Status Register	BB[0]	Reed-Solomon or BCH Lock Interrupt
INTRSBCHLockEn	LLF 0x30	Arg1[0]	Reed-Solomon or BCH Lock Interrupt Enable/Clear
INTRSBCHLockEnS	Status Register	BA[0]	Reed-Solomon or BCH Lock Interrupt Enable Status (read-only)
INTRSBCHLockMsk	LLF 0x30	Arg2[0]	Reed-Solomon or BCH Lock Interrupt Mask
INTRSBCHUnLock	Status Register	BB[1]	Reed-Solomon or BCH Unlock Interrupt
INTRSBCHUnLockEn	LLF 0x30	Arg1[1]	Reed-Solomon or BCH Unlock Interrupt Enable/Clear
INTRSBCHUnLockEnS	Status Register	BA[1]	Reed-Solomon or BCH Unlock Interrupt Enable Status (read-only)
INTRSBCHUnLockMsk	LLF 0x30	Arg2[1]	Reed-Solomon or BCH Unlock Interrupt Mask
LNBBstModSelS	Status Register	BC[4]	LNB Tone Burst Modulation Select Status
LNBBurstEn	LLF 0x20	Arg6[0]	DiSEqC Transmit Tone Burst Enable.
LNBBurstModSel	LLF 0x21	Arg1[0]	DiSEqC Transmit Tone Burst Modulation Select
LNBDC	LLF 0x22	Arg1[0]	LNB DC Level Control
LNBDCODEn	LLF 0x23	Arg2[0]	LNB_DC Pin Open Drain Enable
LNBDCPol	LLF 0x23	Arg1[0]	LNB_DC Pin Polarity
LNBDCS	Status Register	BC[3]	LNB DC Level Status
LNBDi2RxError[7:0]	Status Register	BD[7:0]	DiSEqC 2.x Received Message Error Indicator
LNBDi2RxExpWin[1:0]	LLF 0x20	Arg1[1:0]	DiSEqC 2.x Receive Message Expiration Window
LNBDi2RxLength[2:0]	Status Register	BC[2:0]	DiSEqC 2.x Received Message Length
LNBDi2RxMsg1[7:0]	Status Register	BE[7:0]	First Byte of Received DiSEqC 2.x Message

Table 6. Register Index *(4 of 8)*

Field Name	Location	Register or Argument	Description
LNBDi2RxMsg2[7:0]	Status Register	BF[7:0]	Second Byte of Received DiSEqC 2.x Message
LNBDi2RxMsg3[7:0]	Status Register	C0[7:0]	Third Byte of Received DiSEqC 2.x Message
LNBDi2RxMsg4[7:0]	Status Register	C1[7:0]	Fourth Byte of Received DiSEqC 2.x Message
LNBDi2RxMsg5[7:0]	Status Register	C2[7:0]	Fifth Byte of Received DiSEqC 2.x Message
LNBDi2RxMsg6[7:0]	Status Register	C3[7:0]	Sixth Byte of Received DiSEqC 2.x Message
LNBDi2RxMsg7[7:0]	Status Register	C4[7:0]	Seventh Byte of Received DiSEqC 2.x Message
LNBDi2RxMsg8[7:0]	Status Register	C5[7:0]	Eighth Byte of Received DiSEqC 2.x Message
LNBDi2RxPar[7:0]	Status Register	D6[7:0]	LNB DiSEqC 2.x Receive Data Parity
LNBDi2RxSel[1:0]	LLF 0x21	Arg2[1:0]	DiSEqC 2.x Receive Mode Select
LNBDi2RxTDThresh[7:0]	LLF 0x20	Arg5[7:0]	DiSEqC 2.x Receive Tone Detection Threshold
LNBDi2ToneAmp[5:0]	LLF 0x20	Arg2[5:0]	DiSEqC 2.x Transmit Message Tone Amplitude
LNBLongMsg	LLF 0x21	Arg4[0]	DiSEqC Long Message Flag
LNBMoreMsg	LLF 0x21	Arg3[0]	More DiSEqC Messages Flag
LNBMsg1[7:0]	LLF 0x21	Arg6[7:0]	First Byte of Transmit DiSEqC Message
LNBMsg2[7:0]	LLF 0x21	Arg7[7:0]	Second Byte of Transmit DiSEqC Message
LNBMsg3[7:0]	LLF 0x21	Arg8[7:0]	Third Byte of Transmit DiSEqC Message
LNBMsg4[7:0]	LLF 0x21	Arg9[7:0]	Fourth Byte of Transmit DiSEqC Message
LNBMsg5[7:0]	LLF 0x21	Arg10[7:0]	Fifth Byte of Transmit DiSEqC Message
LNBMsg6[7:0]	LLF 0x21	Arg11[7:0]	Sixth Byte of Transmit DiSEqC Message
LNBMsgLength[1:0]	LLF 0x21	Arg5[1:0]	DiSEqC Transmit Message Length
LNBRxRdy	Status Register	BC[6]	LNB Receive Ready (read and write capable)
LNBTone	LLF 0x23	Arg3[0]	LNB Continuous Tone Control
LNBToneFreq[11:0]	LLF 0x20	Arg3[3:0], Arg4[7:0]	LNB Tone Frequency
LNBToneMode[1:0]	LLF 0x20	Arg7[1:0]	LNB Tone Mode
LNBToneS	Status Register	BC[7]	LNB Continuous Tone Status
LNBTxRdy	Status Register	BC[5]	LNB Transmit Ready
MCCounter[7:0]	Status Register	D4[7:0]	Microcontroller Counter

Table 6. Register Index *(5 of 8)*

Field Name	Location	Register or Argument	Description
MCLoadAdd[14:0]	Fixed Register	F6[6:0] F5[7:0]	Microcontroller Data Load Address
MCLoadData[7:0]	Fixed Register	F7[7:0]	Microcontroller Load Data
MCLoadDis	Fixed Register	F4[4]	Microcontroller Data Load Disable
MCLoadEn	Fixed Register	F4[0]	Microcontroller Data Load Enable
MCLoadSel	Fixed Register	F4[1]	Microcontroller Data Load Select
MCPReset	Fixed Register	F0[1]	Microcontroller Peripheral Reset
MCReset	Fixed Register	F0[0]	Microcontroller Reset
MCResetS	Status Register	20[0]	Microcontroller Reset Status
MPEGSyncPunc	LLF 0x13	Arg3[2]	Sync Word Puncture Control
MPGClkGap	LLF 0x13	Arg1[1]	MPEG Clock Gap Control
MPGClkPol	LLF 0x13	Arg4[0]	MPEG Clock Polarity
MPGClkPos	LLF 0x13	Arg4[1]	MPEG Clock Position
MPGClkSmoothDiv2[7:0]	LLF 0x10	Arg6[7:0]	MPEG Clock Smoothing Divider
MPGClkSmthDiv[2:0]	Fixed Register	F3[6:4]	MPEG Smoothed Clock Divider
MPGDataWidth	LLF 0x13	Arg1[0]	MPEG Data Output Format
MPGFailMode	LLF 0x13	Arg2[2]	MPEG Fail Signal Mode Select
MPGFailNullEn	LLF 0x13	Arg3[1]	MPEG Fail Null Data Enable
MPGFailPol	LLF 0x13	Arg2[5]	MPEG Fail Signal Polarity
MPGHiZClk	LLF 0x13	Arg5[0]	MPEG RS_CLK Pin High-Impedance Control
MPGHiZData	LLF 0x13	Arg5[2]	MPEG RS_DATA[7:1] Pin High-Impedance Control
MPGHiZData0	LLF 0x13	Arg5[1]	MPEG RS_DATA[0] Pin High-Impedance Control
MPGHiZFail	LLF 0x13	Arg5[4]	MPEG RS_FAIL Pin High-Impedance Control
MPGHiZStart	LLF 0x13	Arg5[3]	MPEG RS_START Pin High-Impedance Control
MPGHiZValid	LLF 0x13	Arg5[5]	MPEG RS_VALID Pin High-Impedance Control
MPGNullDataVal	LLF 0x13	Arg3[0]	MPEG Null Data Value
MPGSerDataOut	LLF 0x13	Arg3[4]	MPEG Serial Data Output Pin Select
MPGStartMode	LLF 0x13	Arg2[0]	MPEG Start Signal Mode Select

Table 6. Register Index *(6 of 8)*

Field Name	Location	Register or Argument	Description
MPGStartPol	LLF 0x13	Arg2[3]	MPEG Start Signal Polarity
MPGTEIEn	LLF 0x13	Arg1[2]	MPEG Transport Error Indicator Bit Enable
MPGValidMode	LLF 0x13	Arg2[1]	MPEG Valid Signal Mode Select
MPGValidPol	LLF 0x13	Arg2[4]	MPEG Valid Signal Polarity
PLLClkDis	Fixed Register	E0[1]	PLL Clock Disable
PLLCPCntl[5:0]	Fixed Register	F1[5:0]	PLL Charge Pump Control
PLLDis	Fixed Register	E0[0]	PLL Disable
PLLLock	Fixed Register	FD[7]	PLL Lock Indicator
PLLMult[5:0]	Fixed Register	F2[5:0]	PLL Multiplier
PLLPreDiv	Fixed Register	E5[6]	PLL PreDivider
SYSBoardVer[1:0]	Fixed Register	E8[4:3]	Board Version Read Value
SysChipID[7:0]	Fixed Register	FF[7:0]	Chip ID
SYSChipID[7:0]	Status Register	94[7:0]	Chip ID
SysChipVer[7:0]	Fixed Register	FE[7:0]	Chip Revision
SYSChipVer[70]	Status Register	95[7:0]	Chip Revision
SYSClkConst[15:0]	LLF 0x10	Arg4[7:0], Arg5[7:0]	System Clock Constant
SYSClkDis[7:0]	Fixed Register	EA[7:0]	System Clock Disable
SYSFWVer[7:0]	Status Register	96[7:0]	Firmware Version
SYSFWVerRdCntl[1:0]	LLF 0x35	Arg1[1:0]	Firmware Version Read Control
SYSLDPCClkDiv[2:0]	Fixed Register	F8[2:0]	LDPC Clock Divider
SYSLDPCClkDiv2[2:0]	LLF 0x10	Arg9[7:0]	LDPC Clock Divider
SYSMainClkDiv[2:0]	Fixed Register	F3[2:0]	Main Clock Divider
SYSMainClkDiv2[2:0]	LLF 0x11	Arg14[2:0]	Main Clock Divider
SYSReset	Fixed Register	F0[2]	Non X-Clock Reset
SYSSampFreq[31:0]	LLF 0x11	Arg15[7:0], Arg16[7:0], Arg17[7:0], Arg18[7:0]	Sample Frequency

Table 6. Register Index *(7 of 8)*

Field Name	Location	Register or Argument	Description
SYSXReset	Fixed Register	F0[3]	X-Clock Block Reset
SYSXtalFreq[15:0]	LLF 0x10	Arg7[7:0], Arg8[7:0]	Crystal Frequency
TUNBW	LLF0x15	Arg1[0]	Tuner Bandwidth Adjust
TUNDrvErr[7:0]	Status Register	D0[7:0]	Tuner Driver Error
TUNFreq[23:0]	LLF 0x11	Arg1[7:0], Arg2[7:0. Arg3[7:0]	Tuner Frequency
TUNFreqS[23:0]	Status Register	97[7:0] 98[7:0] 99[7:0]	Tuner Frequency Status
TUNI2CRptEn[7:0]	Fixed Register	E9[7:0]	Tuner I2C Repeat Enable
TUNInitSel	LLF 0x14	Arg1[0]	Tuner Initialization Select
TUNIOSync	Status Register	9D[5]	Low-Priority Sync Indicator
TUNOutRefDiv	LLF 0x14	Arg2[0]	Tuner Clock Reference Output Divider Select
TUNPLLLock	Status Register	9D[0]	Tuner PLL Lock Indicator
TUNRdAdd[7:0]	LLF 0x38	Arg1[7:0]	Tuner Read Address
TUNReg00[7:0]	Status Register	A4[7:0]	Shadowed Tuner Register 00 (CX24118A only)
TUNReg01[7:0]	Status Register	A5[7:0]	Shadowed Tuner Register 01 (CX24118A only)
TUNReg017[7:0]	Status Register	AF[7:0]	Shadowed Tuner Register 17 (CX24118A only)
TUNReg02[7:0]	Status Register	A6[7:0]	Shadowed Tuner Register 02 (CX24118A only)
TUNReg03[7:0]	Status Register	A7[7:0]	Shadowed Tuner Register 03 (CX24118A only)
TUNReg10[7:0]	Status Register	A8[7:0]	Shadowed Tuner Register 10 (CX24118A only)
TUNReg11[7:0]	Status Register	A9[7:0]	Shadowed Tuner Register 11 (CX24118A only)
TUNReg12[7:0]	Status Register	AA[7:0]	Shadowed Tuner Register 12 (CX24118A only)
TUNReg13[7:0]	Status Register	AB[7:0]	Shadowed Tuner Register 13 (CX24118A only)
TUNReg14[7:0]	Status Register	AC[7:0]	Shadowed Tuner Register 14 (CX24118A only)
TUNReg15[7:0]	Status Register	AD[7:0]	Shadowed Tuner Register 15 (CX24118A only)
TUNReg16[7:0]	Status Register	AE[7:0]	Shadowed Tuner Register 16 (CX24118A only)
TUNReg18[7:0]	Status Register	B0[7:0]	Shadowed Tuner Register 18 (CX24118A only)

Table 6. Register Index *(8 of 8)*

Field Name	Location	Register or Argument	Description
TUNReg19[7:0]	Status Register	B1[7:0]	Shadowed Tuner Register 19 (CX24118A only)
TUNReg1A[7:0]	Status Register	B2[7:0]	Shadowed Tuner Register 1A (CX24118A only)
TUNReg1B[7:0]	Status Register	B3[7:0]	Shadowed Tuner Register 1B (CX24118A only)
TUNReg1C[7:0]	Status Register	B4[7:0]	Shadowed Tuner Register 1C (CX24118A only)
TUNReg1D[7:0]	Status Register	B5[7:0]	Shadowed Tuner Register 1D (CX24118A only)
TUNReg1E[7:0]	Status Register	B6[7:0]	Shadowed Tuner Register 1E (CX24118A only)
TUNReg1F[7:0]	Status Register	B7[7:0]	Shadowed Tuner Register 1F (CX24118A only)
TUNReg20[7:0]	Status Register	B8[7:0]	Shadowed Tuner Register 20 (CX24118A only)
TUNReg21[7:0]	Status Register	B9[7:0]	Shadowed Tuner Register 21 (CX24118A only)
TUNSleep	LLF 0x36	Arg1[0]	Tuner Sleep Control
TUNWrtAdd[7:0]	LLF 0x37	Arg1[7:0]	Tuner Write Address
TUNWrtData[7:0]	LLF 0x37	Arg2[7:0]	Tuner Write Data
VCOFreq[23:0]	LLF 0x10	Arg1[7:0], Arg2[7:0], Arg3[7:0]	VCO Frequency in kHz

3.5 Register Detail

This section provides the register detail for serial programming interface addresses 0x20–0x3E and 0x94–0xFF. For detail on LLF loading registers (serial programming interface addresses 0x00 through 0x1F), see Table 3 in Section 3.1.3.

NOTE: Fixed registers listed with an R suffix are read-only; with a W suffix are write-only; with no suffix are read- and write-capable.

NOTE: Status registers are read-only.

3.5.1 Status Registers

Register 20

Register	D7	D6	D5	D4	D3	D2	D1	D0
20	Reserved							MCResetS
MCResetS	Microcontroller Reset Status. 0 = Microcontroller has not been reset. 1 = Microcontroller has been reset by an abnormal event. For diagnostic purposes only.							
GENERAL NOTES: Reserved bits should be left at their existing values unless otherwise specified.								

Register 94

Register	D7	D6	D5	D4	D3	D2	D1	D0
94	SYSChipID[7:0]							
SYSChipID[7:0]	Chip ID. Once the firmware has been downloaded and is operational, it will update this register with the chip ID from register 0xFF. The ID number for the CX24116 is 5.							

Register 95

Register	D7	D6	D5	D4	D3	D2	D1	D0
95	SYSChipVer[7:0]							
SYSChipVer[7:0]	Chip Revision. Once the firmware has been downloaded and is operational, it will update this register with the chip revision number from register 0xFE. The current revision number of the CX24116 is 1.							

Register 96

Register	D7	D6	D5	D4	D3	D2	D1	D0
96	SYSFWVer[7:0]							

SYSFWVer[7:0] Firmware Version.

To retrieve the current firmware version, use the following procedure:

- Set SYSFWVerRdCntl (Opcode 0xA6, Arg1) to 0, then read register SYSFWVer[7:0] to get “A."
- Set SYSFWVerRdCntl to 1, then read register SYSFWVer[7:0] to get "B."
- Set SYSFWVerRdCntl to 2, then read register SYSFWVer[7:0] to get "C."
- Set SYSFWVerRdCntl to 3, then read register SYSFWVer[7:0] to get "D."
- Assemble the components of the firmware number such that the complete version number is A.B.C.D (For example: 1.4.47.0). Where:

A = Major version number.
B = Public release number.
C = Build number.
D = Minor or patch number.

Register 97–99

Register	D7	D6	D5	D4	D3	D2	D1	D0
97	TUNFreqS[23:16]							
98	TUNFreqS[15:8]							
99	TUNFreqS[7:0]							

TUNFreqS[23:0] Tuner Frequency Status.

Register 9A–9B

Register	D7	D6	D5	D4	D3	D2	D1	D0
9A	ACQSRNomS[15:8]							
9B	ACQSRNomS[7:0]							

ACQSRNomS[15:0] Nominal Symbol Rate Status.

Register 9C

Register	D7	D6	D5	D4	D3	D2	D1	D0
9C	ACQPilotEnS	ACQSICurr	ACQVitCRCurr[5:0]					
			ACQMCCurr[5:0]					

ACQPilotEnS Pilot Enable Status.
0 = Pilot is off.
1 = Pilot is on.

ACQSICurr Current Spectral Inversion State.
0 = Not inverted.
1 = Inverted.

ACQVitCRCurr[5:0] Current Viterbi Code Rate.
In DVB-S and DTV Legacy modes, this register field represents the current Viterbi code rate.

ACQMCCurr[5:0] Current Mode Code.
This register field gives the current Mode Code (see the following table).

Receiver Operation Modes	ACQMCCurr[5:0]
LDPC/BCH QPSK ½	4
LDPC/BCH QPSK 3/5	5
LDPC/BCH QPSK 2/3	6
LDPC/BCH QPSK ¾	7
LDPC/BCH QPSK 4/5	8
LDPC/BCH QPSK 5/6	9
LDPC/BCH QPSK 8/9	10
LDPC/BCH QPSK 9/10	11
LDPC/BCH 8PSK 3/5	12
LDPC/BCH 8PSK 2/3	13
LDPC/BCH 8PSK ¾	14
LDPC/BCH 8PSK 5/6	15
LDPC/BCH 8PSK 8/9	16
LDPC/BCH 8PSK 9/10	17
DTV Legacy ½	40
DTV Legacy 2/3	41
DTV Legacy 6/7	44
DVB-S ½	46
DVB-S 2/3	47
DVB-S 3/4	48
DVB-S 5/6	49
DVB-S 7/8	50

Register 9D–9E

Register	D7	D6	D5	D4	D3	D2	D1	D0
9D	AGCAcc[9:8]		TUNIOSync	Reserved	ACQRSBCHSync	ACQCvdSync	ACQDMDSync	TUNPLLLock
9E	AGCAcc[7:0]							

AGCAcc[9:0] Front-End AGC Accumulator.
This unsigned integer corresponds to the voltage on the AGCV pin, such that:

AGCV (in volts) ≅ Vdd x (AGCAcc[9:0] / 1023)

TUNIOSync Tuner I/O Synchronization Bit.
This bit is used to synchronize the driver with the firmware. Before an LLF that communicates with the tuner is issued, this bit is set to 0. When the firmware completes all tuner I/O transactions, it resets this bit to 1.

ACQRSBCHSync Reed-Solomon or BCH Sync Indicator.
0 = Not in Sync.
1 = In Sync.

ACQCvdSync Viterbi or LDPC Sync Indicator.
0 = Not in Sync.
1 = In Sync.

ACQDMDSync Demodulator Sync Indicator.
0 = Not in Sync.
1 = In Sync.

TUNPLLLock Tuner PLL Lock Indicator.
0 = Not in Sync.
1 = In Sync.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Register 9F–A0

Register	D7	D6	D5	D4	D3	D2	D1	D0
9F	ACQFreqOff[15:8]							
A0	ACQFreqOff[7:0]							

ACQFreqOff[15:0] Frequency Offset.
This two's complement number is the total frequency offset as seen by the demodulator in kHz.

Register A1–A2

Register	D7	D6	D5	D4	D3	D2	D1	D0
A1	ACQSROff[15:8]							
A2	ACQSROff[7:0]							
ACQSROff[15:0]	Symbol Rate Offset. This two's complement number is the symbol rate offset in kSps.							

Register A3

Register	D7	D6	D5	D4	D3	D2	D1	D0
A3	ESNOCount[15:8]							
ESNOCount15:8]	EsN0 Count. (Range = 0 to 300_d). This register is the MSB of ESNOCount[15:0]. The LSB is located in register 0xD5. EsN0 (in dB) = ESNOCount[15:0] / 10. The EsN0 range is from 0 dB to 30.0 dB.							

Register A4–B9

Register	D7	D6	D5	D4	D3	D2	D1	D0
A4	TUNReg00[7:0]							
A5	TUNReg01[7:0]							
A6	TUNReg02[7:0]							
A7	TUNReg03[7:0]							
A8	TUNReg10[7:0]							
A9	TUNReg11[7:0]							
AA	TUNReg12[7:0]							
AB	TUNReg13[7:0]							
AC	TUNReg14[7:0]							
AD	TUNReg15[7:0]							
AE	TUNReg16[7:0]							
AF	TUNReg17[7:0]							
B0	TUNReg18[7:0]							
B1	TUNReg19[7:0]							
B2	TUNReg1A[7:0]							
B3	TUNReg1B[7:0]							
B4	TUNReg1C[7:0]							
B5	TUNReg1D[7:0]							
B6	TUNReg1E[7:0]							
B7	TUNReg1F[7:0]							
B8	TUNReg20[7:0]							
B9	TUNReg21[7:0]							

TUNRegXX[7:0]	Shadowed Tuner Register Number XX (CX24118A only). The CX24118A tuner registers are shadowed here. Each time a tuner register is written to or read from by the firmware, its corresponding shadowed tuner register is updated.

Register BA

Register	D7	D6	D5	D4	D3	D2	D1	D0
BA	Reserved				INTLNBRx RdyEnS	INTLNBTx RdyEnS	INTRSBCH UnLockEnS	INTRSBCH LockEnS

INTLNBRxRdyEnS LNB Receive Message Ready Interrupt Enable Status (read-only).
0 = Register bit INTLNBRxRdy and the INTERRUPT pin will not respond when a DiSEqC 2.x message is received.
1 = Register bit INTLNBRxRdy and the INTERRUPT pin will both be triggered when a DiSEqC 2.x message is received.

INTLNBTxRdyEnS LNB Transmit Message Ready Interrupt Enable Status (read-only).
0 = Register bit INTLNBTxRdy and the INTERRUPT pin will not respond when a DiSEqC 2.x message has been transmitted.
1 = Register bit INTLNBTxRdy and the INTERRUPT pin will both be triggered when a DiSEqC 2.x message has been transmitted.

INTRSBCHUnLockEnS Reed-Solomon or BCH Unlock Interrupt Enable Status (read-only).
0 = Register bit INTRSBCHUnLock and the INTERRUPT pin will not respond when the Reed-Solomon or BCH block falls out of lock.
1 = Register bit INTRSBCHUnLock and the INTERRUPT pin will both be triggered when the Reed-Solomon or BCH block falls out of lock.

INTRSBCHLockEnS Reed-Solomon or BCH Sync Interrupt Enable Status (read-only).
0 = Register bit INTRSBCHLock and the INTERRUPT pin will not respond when the Reed-Solomon or BCH block locks to the signal.
1 = Register bit INTRSBCHLock and the INTERRUPT pin will both be triggered when the Reed-Solomon or BCH block locks to the signal.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register BB

Register	D7	D6	D5	D4	D3	D2	D1	D0
BB	Reserved				INTLNBRx Rdy	INTLNBTx Rdy	INTRSBCH UnLock	INTRSBCH Lock

INTLNBRxRdy DiSEqC Receive Message Ready Interrupt.
This register bit is enabled using LLF 0x30.
0 = The triggering event has not occurred.
1 = A DiSEqC 2.x message has been received.

INTLNBTxRdy DiSEqC Transmit Message Ready Interrupt (read-only).
This register bit is enabled using LLF 0x30.
0 = The triggering event has not occurred.
1 = A DiSEqC message has been transmitted.

INTRSBCHUnLock Reed-Solomon or BCH Unlock Interrupt (read-only).
This register bit is enabled using LLF 0x30.
0 = The triggering event has not occurred.
1 = The Reed-Solomon or BCH block has changed from a state of locked to not-locked.

INTRSBCHLock Reed-Solomon or BCH Lock Interrupt (read-only).
This register bit is enabled using LLF 0x30.
0 = The triggering event has not occurred.
1 = The Reed-Solomon or BCH block has changed from a state of not-locked to locked.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register BC

Register	D7	D6	D5	D4	D3	D2	D1	D0
BC	LNBToneS	LNBRxRdy	LNBTxRdy	LNBBstModSelS	LNBDCS	LNBDi2RxLength[2:0]		

LNBToneS

LNB Continuous Tone Status.
0 = Tone off.
1 = Tone on.

LNBRxRdy

LNB Receive Ready (read and write capable).
This register bit will be automatically updated when the triggering event occurs. Write a 0 to this register bit to clear it.

0 = No triggering event has occurred.
1 = A DiSEqC 2.x message has been received. To retrieve the message, use the following procedure:

- Clear LNBRxRdy by setting it to 0.
- Read register field LNBDi2RxLength[3:0] to determine the message length.
- Read the number of bytes specified by register field LNBDi2RxLength[3:0] from registers LNBMsg1[7:0]–LNBMsg8[7:0].

LNBTxRdy

LNB Transmit Ready.
0 = The DiSEqC transmitter is busy.
1 = The DiSEqC transmitter is ready to send a new message.

LNBBstModSelS

LNB Tone Burst Modulation Select Status.
0 = Unmodulated Tone Burst.
1 = Modulated Tone Burst.

LNBDCS

LNB DC Level Status.
This register bit reflects the setting of LNBDC (LLF 0x24, Arg1).
0 = 0 V on LNB_DC pin.
1 = 3.3V on LNB_DC pin.

LNBDi2RxLength[2:0]

DiSEqC 2.x Received Message Length.
When a DiSEqC message has been received, this register field gives its length. The maximum length of a received message is 8 bytes.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register BD

Register	D7	D6	D5	D4	D3	D2	D1	D0
BD	LNBDi2RxError[7:0]							

LNBDi2RxError[7:0]	DiSEqC 2.x Received Message Error Indicator. When configured for DiSEqC 2.x operation (LNBDi2RxSel[1:0] = 00, or 01), this register indicates the location of any byte errors in a received message. A value of 1 in any bit location of this register indicates that there is an error in that byte. For example, a value of 0100,0000b indicates that there is an error in byte 7 of the received message.

Register BE–C5

Register	D7	D6	D5	D4	D3	D2	D1	D0
BE	LNBDi2RxMsg1[7:0]							
BF	LNBDi2RxMsg2[7:0]							
C0	LNBDi2RxMsg3[7:0]							
C1	LNBDi2RxMsg4[7:0]							
C2	LNBDi2RxMsg5[7:0]							
C3	LNBDi2RxMsg6[7:0]							
C4	LNBDi2RxMsg7[7:0]							
C5	LNBDi2RxMsg8[7:0]							

LNBDi2RxMsg1[7:0]	First Byte of Received DiSEqC 2.x Message.
LNBDi2RxMsg2[7:0]	Second Byte of Received DiSEqC 2.x Message.
LNBDi2RxMsg3[7:0]	Third Byte of Received DiSEqC 2.x Message.
LNBDi2RxMsg4[7:0]	Fourth Byte of Received DiSEqC 2.x Message.
LNBDi2RxMsg5[7:0]	Fifth Byte of Received DiSEqC 2.x Message.
LNBDi2RxMsg6[7:0]	Sixth Byte of Received DiSEqC 2.x Message.
LNBDi2RxMsg7[7:0]	Seventh Byte of Received DiSEqC 2.x Message.

Register C6–C9

Register	D7	D6	D5	D4	D3	D2	D1	D0
C6	BERRSBchCBtEC[31:24]							
C7	BERRSBchCBtEC[23:16]							
C8	BERRSBchCBtEC[15:8]							
C9	BERRSBchCBtEC[7:0]							
BERRSBchCBtEC[31:0]	Reed-Solomon or BCH Corrected Bit Error Count (NBC, DVB-S, or DTV Legacy). Reed-Solomon or BCH corrected bit errors are counted over a window of 2^{16} or 2^8 blocks.							

Register CA–CB

Register	D7	D6	D5	D4	D3	D2	D1	D0
CA	BERRSBchUcFmEC[15:8]							
CB	BERRSBchUcFmEC[7:0]							
BERRSBchUcFmEC[15:0]	Reed-Solomon or BCH Uncorrected Frame Error Count (NBC, DVB-S, or DTV Legacy). Reed-Solomon or BCH uncorrected frame errors are counted over a window of 2^{16} or 2^8 blocks.							

Register CC

Register	D7	D6	D5	D4	D3	D2	D1	D0
CC	BERRSBchErrRdy[7:0]							
BERRSBchErrRdy[7:0]	Reed-Solomon or BCH Error Count Ready Indicator. (NBC, DVB-S, or DTV Legacy). After each Reed-Solomon 2^{16}- or 2^8-block measurement window has expired, this counter will increment.							

Register CD–CE

Register	D7	D6	D5	D4	D3	D2	D1	D0
CD	BERCRCUcFmEC[15:8]							
CE	BERCRCUcFmEC[7:0]							
BERCRCUcFmEC[15:0]	CRC Uncorrected Frame Error Count. CRC uncorrected frame errors are counted over a window of 2^{16} or 2^8 blocks.							

Register CF

Register	D7	D6	D5	D4	D3	D2	D1	D0
CF	BERCRCErrRdy[7:0]							
BERCRCErrRdy[7:0]	CRC Error Count Ready Indicator. After each 2^{16} or 2^{8} measurement window has expired, this counter will increment.							

Register D0

Register	D7	D6	D5	D4	D3	D2	D1	D0
D0	TUNDrvErr[7:0]							
TUNDrvErr[7:0]	Tuner Driver Error. This register is for diagnostic purposes only. 0 = No tuner errors. 1 = Invalid serial programming interface address. 2 = Invalid tuner detected.							

Register D4

Register	D7	D6	D5	D4	D3	D2	D1	D0
D4	MCCounter[7:0]							
MCCounter[7:0]	Microcontroller Counter. This counter can be used to monitor the activity of the microcontroller.							

Register D5

Register	D7	D6	D5	D4	D3	D2	D1	D0
D5	ESNOCount[7:0]							
ESNOCount[7:0]	ESN0 Count. (Range = 0 to 300d). This register is the LSB of ESNOCount[15:0]. The MSB is located in register 0xA3. EsN0 (in dB) = ESNOCount[15:0]/10 The EsN0 range is from 0 dB to 30.0 dB							

Register D6

Register	D7	D6	D5	D4	D3	D2	D1	D0
D6	LNBDi2RxPar[7:0]							
LNBDi2RxPar[7:0]	LNB DiSEqC 2.x Receive Data Parity. This register gives the parity of the received DiSEqC 2.x data, specified by LNBDi2RxMsg1[7:0] - LNBDi2RxMsg8[7:0] so that each bit in this register is the parity bit of the xth data byte. For example, bit D0 (the first bit) gives the parity of byte 1, bit D1 gives the parity of byte 2, etc.							

Register D7

Register	D7	D6	D5	D4	D3	D2	D1	D0
D7	Reserved							FECOCDisS
FECOCDisS	Outer FEC Code Error Correction Disable Status. This register bit reflects the setting of FECOCDis (LLF 0x34, Arg1). 0 = MPEG data output will be error corrected by the outer code (RS or BCH). 1 = MPEG data output will not be error corrected by the outer code (for testing purposes only).							
GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.								

Register DB–DC

Register	D7	D6	D5	D4	D3	D2	D1	D0
DB	BERWinAdj[15:8]							
DC	BERWinAdj[7:0]							
BERWinAdj[15:0]	BER Window Adjustment.							

Register DD–DE

Register	D7	D6	D5	D4	D3	D2	D1	D0
DD	BERCRCWinAdj[15:8]							
DE	BERCRCWinAdj[7:0]							
BERCRCWinAdj[15:0]	CRC Window Adjustment.							

3.5.2 Fixed Registers

Register E0

Register	D7	D6	D5	D4	D3	D2	D1	D0
E0	Reserved						PLLClkDis	PLLDis

PLLClkDis PLL Clock Disable.
0 = Normal PLL clock operation.
1 = Disable the clock at the output of the PLL (for test purposes only).

PLLDis PLL Disable
0 = Enable PLL.
1 = Disable PLL. Used in sleep mode and for test purposes.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register E1

Register	D7	D6	D5	D4	D3	D2	D1	D0
E1	Reserved						ADCDis	Reserved

ADCDis ADC Disable.
0 = Enable ADC.
1 = Disable ADC. Used in sleep mode and for test purposes.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register E5

Register	D7	D6	D5	D4	D3	D2	D1	D0
E5	Reserved	PLLPreDiv	Reserved					

PLLPreDiv PLL Predivider.
The crystal clock is divided by this divider before the PLL, such that:

$$F_{vco} = \frac{Fxtal}{(1 \text{ or } 2)} \times PLLMult[5:0]$$

where:
0 = ÷ 2
1 = ÷ 1

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register E8

Register	D7	D6	D5	D4	D3	D2	D1	D0
E8	Reserved			SYSBoardVer[1:0]		Reserved		

SYSBoardVer[1:0]	Board Version Read Value. At power-up, the board version is read from pins BOARD_VER[1:0] and stored in this register field.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified..

Register E9

Register	D7	D6	D5	D4	D3	D2	D1	D0
E9	TUNI2CRptEn[7:0]							

TUNI2CRptEn[7:0]	Tuner I2C Repeat Enable. To activate the tuner I2C repeater, set TUNI2CRptEn[7:0] to 0x55. When an I2C stop condition is issued, the repeater will stop.

Register EA

Register	D7	D6	D5	D4	D3	D2	D1	D0
EA	SYSClkDis[7:0]							

SYSClkDis[7:0]	System Clock Disable. Setting this register to 0xFF shuts down all system clocks. This control should be used to put the part into sleep mode and for diagnostic purposes. Setting this register to 0x00 returns the IC to normal operation.

Register F0

Register	D7	D6	D5	D4	D3	D2	D1	D0
F0	Reserved				SYSXReset	SYSReset	MCPReset	MCReset

SYSXReset	X-Clock Block Reset. 0 = Does nothing. 1 = Blocks that use the X-Clock are reset.
SYSReset	Non X-Clock Reset. 0 = Does nothing. 1 = Blocks that do not use the X-Clock are reset.
MCPReset	Microcontroller Peripheral Reset.
MCReset	Microcontroller Reset.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified..

Register F1

Register	D7	D6	D5	D4	D3	D2	D1	D0
F1	Reserved		PLLCPCntl[5:0]					

PLLCPCntl[5:0]	PLL Charge Pump Control.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Register F2

Register	D7	D6	D5	D4	D3	D2	D1	D0
F2	Reserved		PLLMult[5:0]					

PLLMult[5:0]	PLL Multiplier. f_{VCO} = (XTAL / 2)*PLLMult[5:0]
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Register F3

Register	D7	D6	D5	D4	D3	D2	D1	D0
F3	Reserved	MPGClkSmthDiv[2:0]			Reserved	SYSMainClkDiv[2:0]		

MPGClkSmthDiv[2:0]	MPEG Smoothed Clock Divider. Smoothed Clock Frequency = 2*VCO / MPGClkSmthDiv[2:0] Set this register field to 4.
SYSMainClkDiv[2:0]	Main Clock Divider. Main Clock Frequency = 2*VCO / SYSMainClkDiv[2:0] Set to 4 for symbol rates above 30 MSps, and set to 6 for symbol rates equal to or below 30 MSps.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified..

Register F4

Register	D7	D6	D5	D4	D3	D2	D1	D0
F4	I2CAutoIncDis	Reserved		MCLoadDis	Reserved		MCLoadSel	MCLoadEn

I2CAutoIncDis I2C Auto Increment Disable.
0 = Successive reads or writes to the CX24116 will read from or write to incremental addresses.
1 = The CX24116 will not auto increment after successive reads or writes.

MCLoadDis Microcontroller Data Load Disable.
0 = Loading is enabled.
1 = Loading is disabled.

MCLoadSel Microcontroller Data Load Select.
0 = Program code.
1 = Program data. Program data loading is currently not used.

MCLoadEn Microcontroller Data Load Enable.
0 = Loading is disabled.
1 = Loading is enabled.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Register F5–F6

Register	D7	D6	D5	D4	D3	D2	D1	D0
F5	MCLoadAdd[7:0]							
F6	Reserved	MCLoadAdd[14:8]						

MCLoadAdd[14:0] Microcontroller Data Load Address.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified..

Register F7

Register	D7	D6	D5	D4	D3	D2	D1	D0
F7	MCLoadData[7:0]							

MCLoadData[7:0] Microcontroller Load Data.

Register F8

Register	D7	D6	D5	D4	D3	D2	D1	D0
F8	Reserved					SYSLDPCClkDiv[2:0]		

SYSLDPCClkDiv[2:0] LDPC Clock Divider.
This clock is only active when a DVB-S2 (LDPC) mode is being used. For normal operation, set this value to 6.

Register F9

Register	D7	D6	D5	D4	D3	D2	D1	D0
F9	Reserved							ADCClkDiv

ADCClkDiv	ADC Clock Divider. Set to 0 for symbol rates above 30 MSps, and set to 0 for symbol rates equal to or below 30 MSps. Use this bit in combination with SYSMainClkDiv[2:0]. When this bit is set to 1, sample rate = fvco/4. When this bit is set to 0, sample rate = fvco/6.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified..

Register FD

Register	D7	D6	D5	D4	D3	D2	D1	D0
FD	PLLLock	GPIORdVal[6:0]						

PLLLock	PLL Lock Indicator. 0 = The CX24116 PLL is not locked. 1 = The CX24116 PLL is locked.
GPIORdVal[6:0]	GPIO Read Values. This register field gives the values of the GPIO pins under all drive conditions, including input, output, or secondary function (such as LNBDC).

Register FE

Register	D7	D6	D5	D4	D3	D2	D1	D0
FE	SysChipVer[7:0]							

SysChipVer[7:0]	Chip Revision. The current revision number for the CX24116 is 1.

Register FF

Register	D7	D6	D5	D4	D3	D2	D1	D0
FF	SysChipID[7:0]							

SysChipID[7:0]	Chip ID. The ID number for the CX24116 is 5.

3.6 Op-Code Map

The LLFs are specified by op-codes. Each op-code has a corresponding set of arguments (see Section 3.7). In the software driver, there is a corresponding driver function that creates and executes each LLF. Table 7 lists each customer LLF name, number, and corresponding driver function name.

Table 7. Op-Code Map

Op-Code		Driver Function
Name	**Number**	
Channel Change		
SetVCOFrequency	0x10	PHANTOM_LLF_SetVCOFrequency
ChangeChannel	0x11	PHANTOM_LLF_ChangeChannel
MPEGConfig	0x13	PHANTOM_LLF_MPEGConfig
TunerInit	0x14	PHANTOM_LLF_TunerInit
TunerBandwidthAdjust	0x15	PHANTOM_LLF_TunerBandwidthAdjust
LNB		
LNBConfig	0x20	PHANTOM_LLF_LNBConfig
LNBSend	0x21	PHANTOM_LLF_LNBSend
LNBDCLevel	0x22	PHANTOM_LLF_LNBDCLevel
LNBPCBConfig	0x23	PHANTOM_LLF_LNBPCBConfig
Utility and Debug		
InterruptControl	0x30	PHANTOM_LLF_InterruptControl
SetGPIODirection	0x32	PHANTOM_LLF_SetGPIODirection
SetGPIOOut	0x33	PHANTOM_LLF_SetGPIOOut
DisableCorrection	0x34	PHANTOM_LLF_DisableCorrection
UpdateFirmwareVersion	0x35	PHANTOM_LLF_UpdateFirmwareVersion
SetTunerSleepMode	0x36	PHANTOM_LLF_SleepModeSetting
TunerWrite (CX24118A)	0x37	PHANTOM_LLF_TunerWrite
TunerRead (CX24118A)	0x38	PHANTOM_LLF_TunerRead
AGCControl	0x3B	PHANTOM_AGCControl
BERControl	0x3C	PHANTOM_BERControl
SetGPIOMode	0x4E	PHANTOM_SetGPIOMode

3.7 Op-Code Detail

All LLF op-codes and LLF arguments (parameters) are 8 bits, unless otherwise stated. Arguments that are smaller than 8 bits are right-aligned (their lsb is bit 0). Values not specified are not defined and should not be used.

Op-Code 0x10: SetVCOFrequency

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	VCOFreq[23:16]							
2	VCOFreq[15:8]							
3	VCOFreq[7:0]							
4	SYSClkConst[15:8]							
5	SYSClkConst[7:0]							
6	MPGClkSmoothDiv2[7:0]							
7	SYSXtalFreq[15:8]							
8	SYSXtalFreq[7:0]							
9	SYSLDPCClkDiv2[2:0]							

VCOFreq[23:0]
VCO Frequency in kHz.
VCOFreq[23:0] = (Clock/2)*PLLMult[5:0]
Clock is the incoming clock frequency in kHz. When used with the CX24118A, Clock is usually 40,444 kHz. This parameter is included to synchronize the firmware with the driver.

SYSClkConst[15:0]
System Clock Constant.
SYSClkConst[15:0] = 2^{34}/ VCOFreq[23:0]
For purposes of speed and efficiency, this constant is used for various microcontroller calculations.

MPGClkSmoothDiv2[7:0]
MPEG Clock Smoothing Divider.
This parameter is included to synchronize the firmware with the driver. Set this parameter to 4.

SYSXtalFreq[15:0]
Crystal Frequency.
Enter the crystal frequency in kHz.

SYSLDPCClkDiv2[2:0]
LDPC Clock Divider.
This parameter is included to synchronize the firmware with the driver. For normal operation, set this value to 6.

Op-Code 0x11: ChangeChannel (page 1 of 3)

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	TUNFreq[23:16]							
2	TUNFreq[15:8]							
3	TUNFreq[7:0]							
4	ACQSRNom[15:8]							
5	ACQSRNom[7:0]							
6	Reserved				ACQSISearch[1:0]		ACQMode[1:0]	
7	ACQPilotEn[1:0]		ACQModCode[5:0]					
8	ACQFreqMax[15:8]							
9	ACQFreqMax[7:0]							
10	ACQPRFreqNom[15:8]							
11	ACQPRFreqNom[7:0]							
12	Reserved						ACQAlpha[1:0]	
13	ACQCREn[7:0]							
14	Reserved					SYSMainClkDiv2[2:0]		
15	SYSSampFreq[31:24]							
16	SYSSampFreq[23:16]							
17	SYSSampFreq[15:8]							
18	SYSSampFreq[7:0]							

TUNFreq[23:0] Tuner Frequency.
This 16-bit unsigned integer is in kHz, ranging from 925,000 kHz to 2,175,000. Numbers outside this range are invalid.

ACQSRNom[15:0] Nominal Symbol Rate.
This 16-bit unsigned integer is in kSps, ranging from 1,000 kSps to 45,000 kSps. Numbers outside this range are invalid.

ACQSISearch[1:0] Spectral Inversion Search Select.
This argument is not relevant in Advanced 8PSK and QPSK, since both spectral inversion states are always searched in Turbo mode.
00 = Search normal spectral state only.
01 = Search inverted spectral state only.
10 = Search both spectral states, normal first.
11 = Search both spectral states, inverted first.

(continued on next page)

Op-Code 0x11: ChangeChannel (page 2 of 3)

ACQMode[1:0]

Acquisition Mode.
0 = Nominal frequency is not used (Blind Acquisition).
1 = Nominal frequency is used (Quick Acquisition).
2 = Disable Acquisition (for test purposes only).
3 = Installation mode.
Disable Acquisition mode will disable the acquisition state machine and binning; however, the CTL will still be searching. If RF is removed (or signal is removed), the system will fall out of lock, and when the signal is restored it will not lock until acquisition is re-enabled using this LLF with QUICK or BLIND mode.

ACQPilotEn[1:0]

Pilot Enable.
This parameter is only valid in LDPC/BCH modes.
0 = Pilot is off.
1 = Pilot is on.

ACQModCode[5:0]

Mode Code (Modulation Format and Transport Spec).
The following table lists all valid Mode Codes and the transmission format that they correspond to. Values that are not listed are not valid.

Receiver Operation Modes	ACQModCode[5:0]
LDPC/BCH QPSK ½	4
LDPC/BCH QPSK 3/5	5
LDPC/BCH QPSK 2/3	6
LDPC/BCH QPSK ¾	7
LDPC/BCH QPSK 4/5	8
LDPC/BCH QPSK 5/6	9
LDPC/BCH QPSK 8/9	10
LDPC/BCH QPSK 9/10	11
LDPC/BCH 8PSK 3/5	12
LDPC/BCH 8PSK 2/3	13
LDPC/BCH 8PSK ¾	14
LDPC/BCH 8PSK 5/6	15
LDPC/BCH 8PSK 8/9	16
LDPC/BCH 8PSK 9/10	17
DTV Legacy ½	40
DTV Legacy 2/3	41
DTV Legacy 6/7	44
DVB-S ½	46
DVB-S 2/3	47
DVB-S 3/4	48
DVB-S 5/6	49
DVB-S 7/8	50

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Op-Code 0x11: ChangeChannel (page 3 of 3)

ACQFreqMax[15:0] Frequency Search Range.
This 16-bit unsigned integer is in kHz, ranging from 0 to 10,000 kHz. Numbers outside this range are not valid.

ACQPRFreqNom[15:0] Nominal Phase Rotator Frequency.
This signed integer (2's complement) is in kHz, ranging from -10,000 kHz to +10,000 kHz. The value is the acquisition state machine's starting place when in QUICK acquisition mode (ACQMode[7:0] = 1).

ACQAlpha[1:0] Alpha or Roll-off Factor.
0 = 0.2.
1 = 0.25.
2 = 0.35.
3 = Reserved.

ACQCREn[7:0] Viterbi Code Rate Search Enable.
When a bit in this argument has a value of 1, the code rate corresponding to that bit location will be searched in accordance with the following table. This argument is only relevant in DVB-S and DTV Legacy modes. Values that are not shown are not valid.

Format	Bit 7	D6	D5	D4	D3	D2	D1	D0
DVB-S	7/8	6/7	5/6	4/5	3/4	2/3	1/2	-
DTV Legacy	-	6/7	-	-	-	2/3	1/2	-

SYSMainClkDiv2[2:0] Main Clock Divider.
This register field sets the main clock frequency and should be written to prior to channel change. Set to 6 for symbol rates above 30 MSps and set to 4 for symbol rates below 30 MSps. This parameter is not dependent on transmission format. This parameter is included to synchronize the firmware with the driver.

F_{main} = 2*VCOFreq[15:0]/SYSMainClkDiv[7:0].

SYSSampFreq[31:0] Sample Frequency.
Enter the sample frequency in kHz. For purposes of speed and efficiency, this value is used for various microcontroller calculations.

$F_{sample} = F_{main}/2$.

Op-Code 0x13: MPEGConfig (page 1 of 2)

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved					MPGTEIEn	MPGClkGap	MPGDataWidth
2	Reserved		MPGFailPol	MPGValidPol	MPGStartPol	MPGFailMode	MPGValidMode	MPGStartMode
3	Reserved			MPGSerDataOut	Reserved	MPEGSyncPunc	MPGFailNullEn	MPGNullDataVal
4	Reserved						MPGClkPos	MPGClkPol
5	Reserved		MPGHiZValid	MPGHiZFail	MPGHiZStart	MPGHiZData	MPGHiZData0	MPGHiZClk

MPGTEIEn
MPEG Transport Error Indicator Bit Enable.
0 = TEI bit is not set when block errors occur.
1 = TEI bit is set when block errors occur.

MPGClkGap
MPEG Clock Gap Control.
0 = MPEG clock is present during parity.
1 = MPEG clock is gapped during parity.

MPGDataWidth
MPEG Data Output Format.
0 = Serial.
1 = Parallel.

MPGFailPol
MPEG Fail Signal Polarity.
0 = Active low.
1 = Active high.

MPGValidPol
MPEG Valid Signal Polarity.
0 = Active low.
1 = Active high.

MPGStartPol
MPEG Start Signal Polarity.
0 = Active low.
1 = Active high.

MPGFailMode
MPEG Fail Signal Mode Select.
0 = Active during non-parity data.
1 = Active during the first byte of each block only.

MPGValidMode
MPEG Valid Signal Mode Select.
0 = Active during non-parity data.
1 = Active during the first byte of each block only.

MPGStartMode
MPEG Start Signal Mode Select.
This bit sets the width of the MPEG Start signal in serial mode. The Start signal is always byte wide in parallel mode.
0 = Byte wide.
1 = Bit wide.

MPGSerDataOut
MPEG Serial Data Output Pin Select.
0 = Serial MPEG data is produced on pin RS_Data[0].
1 = Serial MPEG data is produced on pin RS_Data[7].

(continued on next page)

Op-Code 0x13: MPEGConfig (page 2 of 2)

MPEGSyncPunc	Sync Word Puncture Control. 0 = Sync word is not punctured. 1 = Sync word is punctured.
MPGFailNullEn	MPEG Fail Null Data Enable. 0 = Data is not modified during a failed packet. 1 = Data within a failed packed will be changed to Null Data as specified by MPGNullDataVal.
MPGNullDataVal	MPEG Null Data Value. 0 = Null data will be replaced with 0. 1 = Null data will be replaced with 1. Null data is defined as gaps and data during a failed packet. DTV Legacy.
MPGClkPos	MPEG Clock Position. This bit is only active in parallel mode. 0 = Clock changes with the data. 1 = Clock changes 1/8 of a clock period after the data transition.
MPGClkPol	MPEG Clock Polarity. 0 = Data changes on the rising edge of the clock. Sampling is expected on the falling edge of the clock. 1 = Data changes on the falling edge of the clock. Sampling is expected on the rising edge of the clock.
MPGHiZValid	MPEG RS_VALID Pin High-Impedance Control. 0 = Normal operation. 1 = High impedance.
MPGHiZFail	MPEG RS_FAIL Pin High-Impedance Control. 0 = Normal operation. 1 = High impedance.
MPGHiZStart	MPEG RS_START Pin High-Impedance Control. 0 = Normal operation. 1 = High impedance.
MPGHiZData	MPEG RS_DATA[7:1] Pin High-Impedance Control. 0 = Normal operation. 1 = High impedance.
MPGHiZData0	MPEG RS_DATA[0] Pin High-Impedance Control. 0 = Normal operation. 1 = High impedance.
MPGHiZClk	MPEG RS_CLK Pin High-Impedance Control. 0 = Normal operation. 1 = High impedance.

Op-Code 0x14: TunerInit

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							TUNInitSel
2	Reserved							TUNOutRefDiv

TUNInitSel Tuner Initialization Select.
This bit selects the tuner to initialize in a dual tuner system. Select tuner A in a single tuner system.
0 = Tuner A is selected for initialization.
1 = Tuner B is selected for initialization.

TUNOutRefDiv Tuner Clock Reference Output Divider Select.
0 = Use a tuner output reference divider of 1.
1 = Use a tuner output reference divider of 2.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x15: TunerBandwidthAdjust

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							TUNBW

TUNBW Tuner Bandwidth Adjust.
This LLF should be called the following two times: (1) before acquiring a channel, with TUNBW set to 1, and (2) after acquiring a channel, with TUNBW set to 0.

0 = Tuner BW is narrowed to reject adjacent channel interference.
1 = Tuner BW is opened to match the requested carrier search range.

Op-Code 0x20: LNBConfig

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved						LNBDi2RxExpWin[1:0]	
2	Reserved		LNBDi2ToneAmp[5:0]					
3	Reserved				LNBToneFreq[11:8]			
4	LNBToneFreq[7:0]							
5	LNBDi2RxTDThresh[7:0]							
6	Reserved							LNBBurstEn
7	Reserved						LNBToneMode[1:0]	

LNBDi2RxExpWin[1:0] DiSEqC 2.x Receive Message Expiration Window.
00 = 150 ms.
01 = 166 ms.
10 = 182 ms.
11 = 200 ms.

LNBDi2ToneAmp[5:0] DiSEqC 2.x Transmit Message Tone Amplitude.
This parameter sets the 22kHz output tone peak-to-peak amplitude (Range = 2 to 63). Values 0 and 1 are not valid.
Tone Amplitude (Vp_p) = 7.18V/ LNBDi2ToneAmp[5:0]

LNBToneFreq[11:0] LNB Tone Frequency.
Tone Frequency (kHz) = (LNBToneFreq[15:0]*Clock)/ 218
Clock is the incoming clock frequency in kHz (usually 40,444 kHz). For normal operation (22 kHz) with a 40.444 MHz crystal, set to 143d.

LNBDi2RxTDThresh[7:0] DiSEqC 2.x Receive Tone Detection Threshold.
This argument sets the criteria by which the existence of a 22kHz tone is detected. (Range = 0 to 255d). A lower argument value corresponds to a lower threshold value in mVpp (easier to detect). Set to 40d.

LNBBurstEn DiSEqC Transmit Tone Burst Enable.
0 = Tone burst will not be appended to a transmitted DiSEqC message sequence.
1 = Tone burst will be appended to a transmitted DiSEqC message sequence.

LNBToneMode[1:0] LNB Tone Mode (Transmit Only).
0 = Tone mode with PWM generated sine wave.
1 = Tone mode with TTL levels.
2 = Envelope mode.

Op-Code 0x21: LNBSend (page 1 of 2)

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							LNBBurst ModSel
2	Reserved						LNBDi2RxSel[1:0]	
3	Reserved							LNBMoreMsg
4	Reserved							LNBLongMsg
5	Reserved						LNBMsgLength[1:0]	
6	LNBMsg1[7:0]							
7	LNBMsg2[7:0]							
8	LNBMsg3[7:0]							
9	LNBMsg4[7:0]							
10	LNBMsg5[7:0]							
11	LNBMsg6[7:0]							

LNBBurstModSel DiSEqC Transmit Tone Burst Modulation Select.
0 = Unmodulated tone burst.
1 = Modulated tone burst.

LNBDi2RxSel[1:0] DiSEqC 2.x Receive Mode Select.
00b = Interrogation mode.
01b = Quick reply mode.
10b = Transmit-only mode.
11b = Reserved.

LNBMoreMsg More DiSEqC Messages Flag.
0 = The current message is the last message of the sequence.
1 = More messages will be appended to the sequence.

LNBLongMsg DiSEqC Long Message Flag.
0 = Message is 3–6 bytes in length.
1 = Long message. Additional bytes will be appended to the current message.

LNBMsgLength[1:0] DiSEqC Transmit Message Length.
Message length = 3 + LNBMsgLength[1:0].

LNBMsg1[7:0] First Byte of Transmit DiSEqC Message.
This argument is the first byte of a transmitted LNB Message.

LNBMsg2[7:0] Second Byte of Transmit DiSEqC Message.
This argument is the second byte of a transmitted LNB Message.

LNBMsg3[7:0] Third Byte of Transmit DiSEqC Message.
This argument is the third byte of a transmitted LNB Message.

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Op-Code 0x21: LNBSend (page 2 of 2)

LNBMsg4[7:0]	Fourth Byte of Transmit DiSEqC Message. This argument is the fourth byte of a transmitted LNB Message.
LNBMsg5[7:0]	Fifth Byte of Transmit DiSEqC Message. This argument is the fifth byte of a transmitted LNB Message.
LNBMsg6[7:0]	Sixth Byte of Transmit DiSEqC Message. This argument is the sixth byte of a transmitted LNB Message.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x22: LNBDCLevel

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							LNBDC

LNBDC	LNB DC Level Control. This bit sets the DC level of the LNB_DC pin. The relationship between the voltage on this pin and the voltage being transmitted to the LNB (13V or 18V) will depend on the external regulator circuitry. The voltage at the LNB_DC pin when LNBDCPol (LLF 0x23, Arg1) is set to 0 is given below. When LNBDCPol is 1, the settings are reversed. 0 = 0 V on LNB_DC pin. 1 = 3.3V on LNB_DC pin.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x23: LNBPCBConfig

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							LNBDCPol
2	Reserved							LNBDCODEn
3	Reserved							LNBTone

LNBDCPol	LNB_DC Pin Polarity. This bit sets the relationship of argument LNBDC (LLF 0x22, Arg1) and the LNB_DC pin as follows. Also see the LNBDC description. 0 = Normal LNB_DC pin polarity. 1 = Inverted LNB_DC pin polarity.
LNBDCODEn	LNB_DC Pin Open Drain Enable. The state of this bit controls the configuration of the LNB_DC pin. 0 = CMOS output. 1 = Open drain (requires external pull-up).
LNBTone	LNB Continuous Tone Control. 0 = Tone off. 1 = Tone on.
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x30: InterruptControl

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved				INTLNBRxRdyEn	INTLNBTxRdyEn	INTRSBCHUnLockEn	INTRSBCHLockEn
2	Reserved				INTLNBRxRdyMsk	INTLNBTxRdyMsk	INTRSBCHUnLockMsk	INTRSBCHLockMsk

INTLNBRxRdyEn LNB Receive Message Ready Interrupt Enable/Clear.
0 = Enable the INTLNBRxRdy interrupt if INTLNBRxRdyMsk is 1. The Status of this interrupt can be read from register bit INTLNBRxRdy (0xBB[3]).
1 = Clear the INTLNBRxRdy interrupt if it has triggered.

INTLNBTxRdyEn LNB Transmit Message Ready Interrupt Enable/Clear.
0 = Enable the INTLNBTxRdy interrupt if INTLNBTxRdyMsk is 1. The Status of this interrupt can be read from register bit INTLNBTxRdy (0xBB[2]).
1 = Clear the INTLNBTxRdy interrupt if it has triggered.

INTRSBCHUnLockEn Reed-Solomon or BCH Unlock Interrupt Enable/Clear.
0 = Enable the INTRSBCHUnLock interrupt if INTRSBCHUnLockMsk is 1. The Status of this interrupt can be read from register bit INTLNBTxRdy (0xBB[1]).
1 = Clear the INTRSBCHUnLock interrupt if it has triggered.

INTRSBCHLockEn Reed-Solomon or BCH Lock Interrupt Enable/Clear.
0 = Enable the INTRSBCHLock interrupt if INTRSBCHLockMsk is 1. The Status of this interrupt can be read from register bit INTLNBTxRdy (0xBB[0]).
1 = Clear the INTRSBCHLock interrupt if it has triggered.

INTLNBRxRdyMsk LNB Receive Message Ready Interrupt Mask.
0 = INTLNBRxRdy is masked, so that writing to it will do nothing.
1 = INTLNBRxRdy is not masked, so that writing to it will perform the specified operation (enable or clear).

INTLNBTxRdyMsk LNB Transmit Message Ready Interrupt Mask.
0 = INTLNBTxRdy is masked, so that writing to it will do nothing.
1 = INTLNBTxRdy is not masked, so that writing to it will perform the specified operation (Enable or clear).

INTRSBCHUnLockMsk Reed-Solomon or BCH Unlock Interrupt Mask.
0 = INTRSBCHUnLock is masked, so that writing to it will do nothing.
1 = INTRSBCHUnLock is not masked, so that writing to it will perform the specified operation (Enable or clear).

INTRSBCHLockMsk Reed-Solomon or BCH Lock Interrupt Mask.
0 = INTRSBCHLock is masked, so that writing to it will do nothing.
1 = INTRSBCHLock is not masked, so that writing to it will perform the specified operation (Enable or clear).

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x32: SetGPIODirection

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved			GPIODir[4:0]				
2	Reserved			GPIODirMsk[4:0]				

GPIODir[4:0]

GPIO Direction.
If bit [i] of GPIODir[4:0] is 1, then GPIO[i] is an INPUT.
If bit [i] of GPIODir[4:0] is 0, then GPIO[i] is an OUTPUT.

GPIODirMsk[4:0]

GPIO Direction Mask.
If bit [i] of GPIODirMsk[4:0] is 1, then GPIO[i] is set to the value specified by GPIODir[i].
If bit [i] of GPIODirMsk[4:0] is 0, then do not change the direction of GPIO when GPIODir[i] is changed.

For example: To set GPIO3 as an output, GPIO4 as an input and not change any other GPIO directions, use the following settings:

GPIODir[4:0] = xxx1 0xxxb
GPIODirMsk[4:0] = 0001 1000b

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x33: SetGPIOOut

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved			GPIOVal[4:0]				
2	Reserved			GPIOValMsk[4:0]				

GPIOVal[4:0]

GPIO Write Values.
When the GPIO[i] pin is configured as a GPIO output and GPIOValMsk[i] is 1, the value written to bit GPIOVal[i] will be sent to the GPIO[i] pin.

GPIOValMsk[4:0]

GPIO Write Mask.
If bit [i] of GPIOValMsk[4:0] is 1, pin GPIO[i] is set to the value specified by GPIOVal[i].
If bit [i] of GPIOValMsk[4:0] is 0, pin GPIO[i] does not change when GPIOVal[i] is modified.

For example: To set GPO3 to 1 without changing the value of any other GPIOs, use the following settings:

GPIOVal[4:0] = xxxx 1xxxb
GPIOValMsk[4:0] = 0000 1000b

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x34: DisableCorrection

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							FECOCDis

FECOCDis

Outer FEC Code Error Correction Disable.
0 = MPEG data output will be error corrected by the outer code (RS or BCH).
1 = MPEG data output will not be error corrected by the outer code (for testing purposes only).

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x35: UpdateFirmwareVersion

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved						SYSFWVerRdCntl[1:0]	

SYSFWVerRdCntl[1:0] Firmware Version Read Control.
This parameter specifies the portion of the firmware version that can be read from status register SYSFWVer[7:0] (0x96[7:0]), such that the complete version number is A.B.C.D (For example: 1.4.47.0).

Where:

0 = Read major version number (A).
1 = Read public release number (B).
2 = Read build number (C).
3 = Read minor or patch number (D).

Example – to read the firmware version:
Set SYSFWVerRdCntl[1:0] to 0, then read register SYSFWVer[7:0] (0x96[7:0]) to get A
Set SYSFWVerRdCntl[1:0] to 1, then read register SYSFWVer[7:0] to get B
Set SYSFWVerRdCntl[1:0] to 2, then read register SYSFWVer[7:0] to get C
Set SYSFWVerRdCntl[1:0] to 3, then read register SYSFWVer[7:0] to get D

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x36: SetTunerSleepMode

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							TUNSleep

TUNSleep Tuner Sleep Control.
0 = Normal tuner operation.
1 = Tuner is put into low power mode.

GENERAL NOTE: Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x37: TunerWrite

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	TUNWrtAdd[7:0]							
2	TUNWrtData[7:0]							

TUNWrtAdd[7:0] Tuner Write Address.

TUNWrtData[7:0] Tuner Write Data.
This LLF can be used to write a specific tuner address. For test purposes only.

Op-Code 0x38: TunerRead

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	TUNRdAdd[7:0]							

TUNRdAdd[7:0]	Tuner Read Address. This LLF can be used to read the specified tuner address. After writing this LLF, the tuner register value can be read from the mirrored tuner register in the status registers. For test purposes only.

Op-Code 0x3B: AGCControl

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved						AGCMode[1:0]	
2							AGCVal[9:8]	
3	AGCVal[7:0]							

AGCMode[1:0]	Front-End AGC Mode. 0 = Normal (closed loop). 1 = Freeze AGC at its current value. 2 = Freeze AGC and set its accumulator to the value specified by AGCVal[9:0].
AGCVal[9:0]	Front-End AGC Accumulator Value in Manual Mode. When AGCMode[1:0] is set to 2, this value is written to the AGC accumulator. (Range = 0 to 1023d).
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x3C: BERControl

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved							BERWin

BERWin	BER Window Size. 0 = 2^8 (blocks in DVB-S and DTV Legacy modes, and frames in DVB-S2 modes). 1 = 2^{16} (blocks in DVB-S and DTV Legacy modes, and frames in DVB-S2 modes).
GENERAL NOTE:	Reserved bits should be left at their existing values unless otherwise specified.

Op-Code 0x4E: SetGPIOMode

Argument	D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved			GPIOMode[4:0]				

GPIOMode[4:0]	GPIO Mode. If bit [i] of GPIOMode[4:0] is 0, then GPIO[i] is open drain. If bit [i] of GPIOMode[4:0] is 1, then GPIO[i] is TTL.

4 Application Information

4.1 Sleep Mode Procedures

4.1.1 Changing from Normal Operation to Sleep Mode

To change the demodulator from normal operation to sleep mode, use the following procedure:

1. Power down the tuner using Op-code 0x36 (if required).
2. Power down the demodulator by doing the following:
   a. Write 0xFF to register SYSClkDis[7:0] (0xEA[7:0]).
   b. Write 1 to register bit AGCDis (0xE1[1]).
   c. Write 1 to register bit PLLDis (0xE0[0]).

4.1.2 Changing from Sleep Mode to Normal Operation

To change the demodulator from sleep mode to normal operation, use the following procedure:

1. Put the demodulator into normal operation by doing the following:
   a. Write 0 to register bit PLLDis (0xE0[0]).
   b. Write 0 to register bit AGCDis (0xE1[1]).
   c. Write 0x00 to register SYSClkDis[7:0] (0xEA[7:0]).
2. Put the tuner into normal operation using Op-code 0x36.

4.2 Thermal Recommendations

The CX24116 uses a thermally enhanced Thin Quad Flat Pack (eTQFP) package with an exposed paddle underneath the device to dissipate heat. The exposed paddle is soldered directly to exposed PCB ground on the top layer of the board. Thermal vias then connect the top PCB layer to the other board layers. The more layers that are used, the better the thermal properties of the chip will be. The following table gives the CX24116 thermal layout recommendations.

Table 8. Thermal Recommendations

Parameter	Recommendations
Number of PCB layers(1)	4
Numbers of thermal vias	81 (9x9 square matrix)
Thermal via spacing	1 mm from center to center
Solder mask opening under exposed paddle(2)	10.3 x 10.3 mm
Metallization land pattern(3)	14 x 14 mm
Via diameter	0.33 mm drill-hole size with 1 oz copper plating

FOOTNOTES:

(1) As many of the layers should be grounded and connected to the thermal vias as possible.

(2) Same as the package exposed paddle.

(3) Same as package width, excluding the pins. This allows the metal pattern to be as wide as possible while still allowing the minimum 0.25 mm spacing between the metallization pattern and the pin pads. The area outside the solder mask opening to the pin pads are covered with solder mask.

4.3 Reset and Power Supply Sequencing

The 1.25 V and 3.3 V power supplies can be brought up in any order. However, the $\overline{\text{RESET}}$ pin should be held low until the voltages of both supplies reach their nominal values.

4.4 Serial Programming Interface Restrictions

For robust serial programming interface operation, care should be taken to avoid short glitches on the clock and data lines. A short glitch is a voltage transition from low to high to low (0 to 1 to 0) in less than 75 ns.

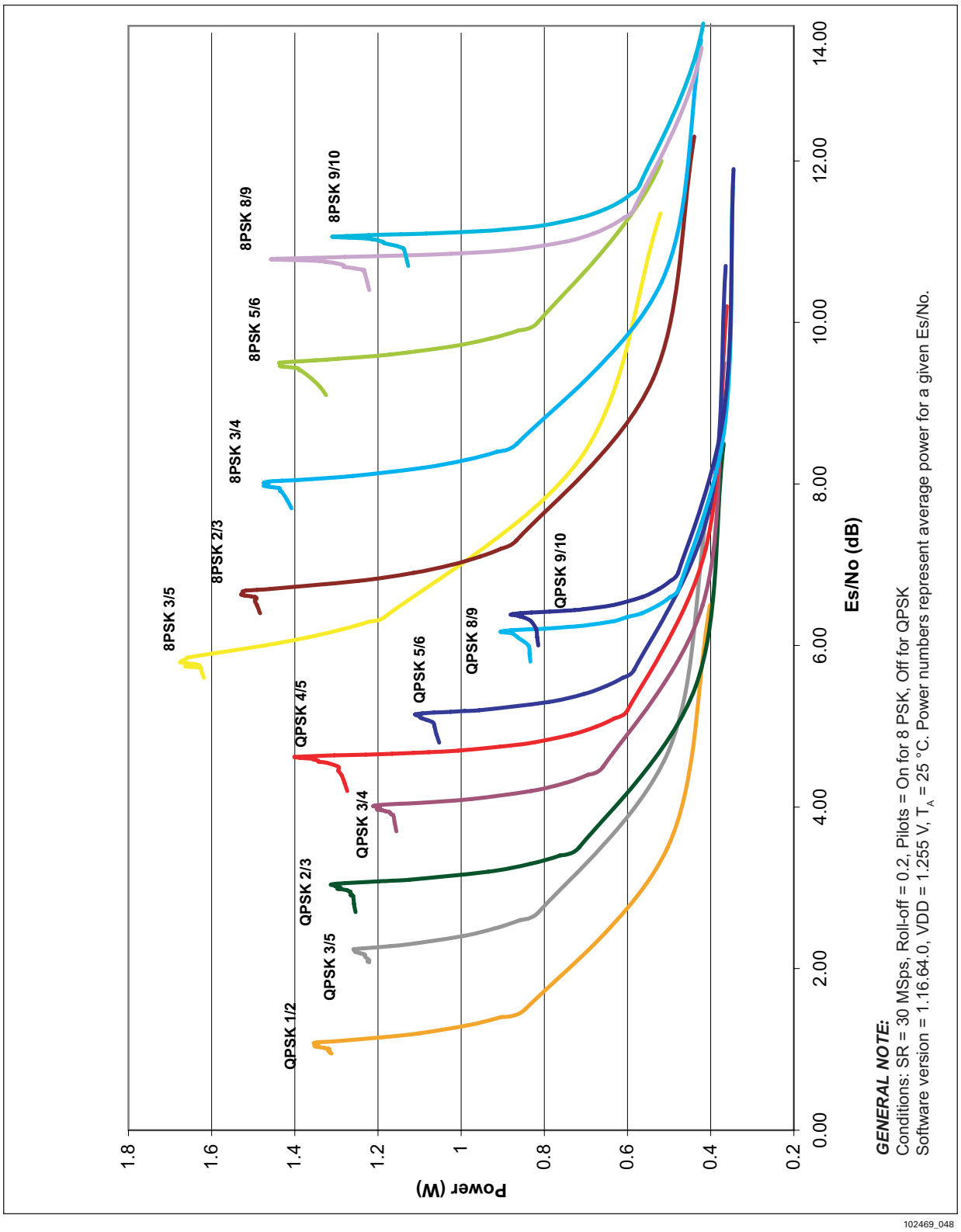
4.5 Dynamic Power Algorithm and Power Conditioning

The CX24116 uses a dynamic power algorithm to achieve optimum performance at the lowest power consumption level. Under higher Es/N0 conditions, power consumption is minimal, while at lower Es/N0 levels (where the extra performance is needed) power consumption is increased. This behavior is demonstrated in Figure 10.

Notice that the QEF threshold level for each of the code rates, which is several tenths of a dB above the DVB-S2 “ideal” (decoder only) QEF level, is to the right of the peak power value. Furthermore, the expected typical operating point is well to the right of the threshold point.

Care should be taken to ensure that current fluctuations do not cause the voltage to go outside of the voltage operating condition requirement of 1.25 V ±5 percent. To achieve this, it is recommended that a 1000uF capacitor be placed near the 1.25 V voltage regulator and that several 1 uF capacitors be placed near the IC power pins. Trace impedance between the regulator and the IC should also be kept to a minimum; ideally a power plane should be used. For the most up-to-date recommendations, see the most current CX24116-based Conexant reference design.

Figure 10. Typical Core Power vs. ES/No for LDPC/BCH Modes



5 Timing Specifications

5.1 MPEG Parallel Output Mode

Table 9 specifies the setup and hold values for the MPEG data relative to the MPEG clock in parallel mode. The following listing defines the acronyms used in Table 9.

Acronym	Definition
CPP	Clock period in parallel mode.
CRDS	Setup time, data to clock rise.
CRDH	Hold time, clock rise to data.
CIFDS	Setup time, data to inverted clock fall.
CIFDH	Hold time, inverted clock fall to data.
CAFDS	Setup time, data to advanced clock fall.
CAFDH	Hold time, advanced clock fall to data.
CARDS	Setup time, data to advanced clock rise.
CARDH	Hold time, advanced clock rise to data.
CAIRDS	Setup time, data to advanced inverted clock rise.
CAIRDH	Hold time, advanced inverted clock rise to data.
CAIFDS	Setup time, data to advanced inverted clock fall.
CAIFDH	Hold time, advanced inverted clock fall to data.

Table 9. MPEG Parallel Output Mode Timing *(1 of 2)*

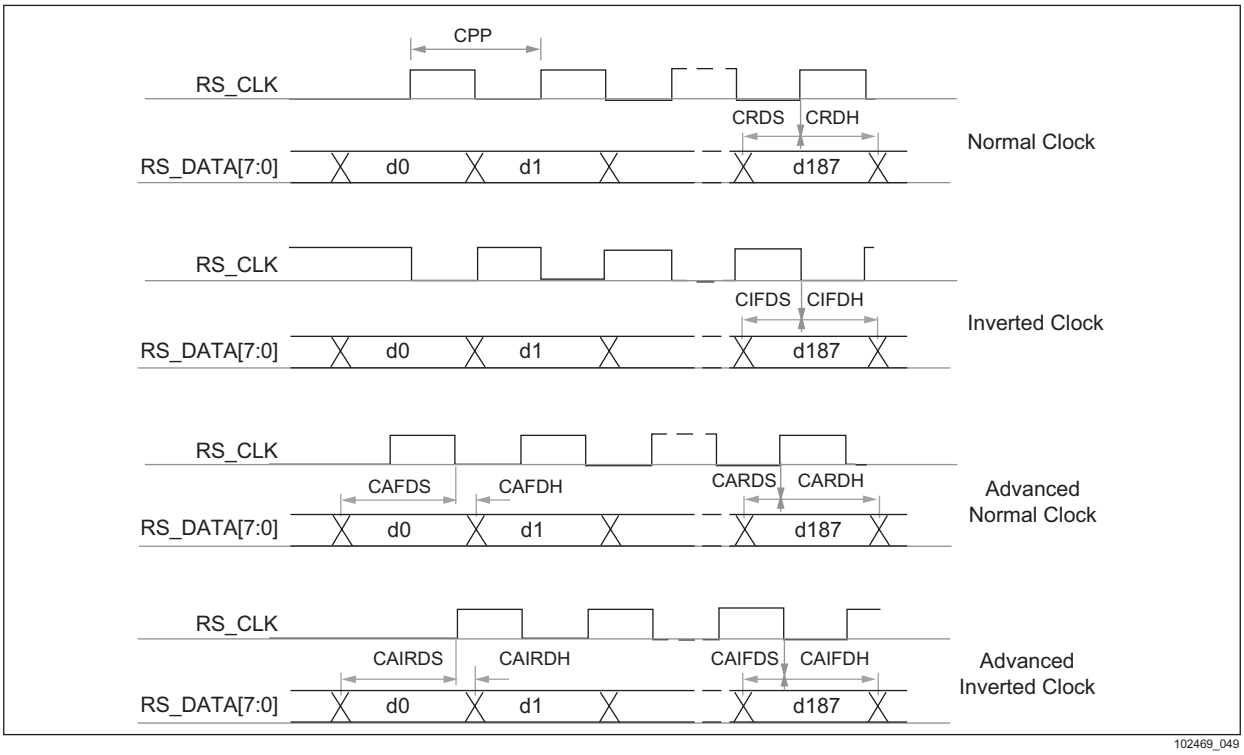
MPEG Data	Min	Units
CPP	100.00	ns
CRDS	45.74	ns
CRDH	49.66	ns
CIFDS	45.19	ns
CIFDH	50.10	ns

Table 9. MPEG Parallel Output Mode Timing (Continued) *(2 of 2)*

MPEG Data	Min	Units
CAFDS	82.69	ns
CAFDH	12.60	ns
CARDS	33.24	ns
CARDH	62.16	ns
CAIRDS	83.24	ns
CAIRDH	12.16	ns
CAIFDS	32.69	ns
CAIFDH	62.60	ns

Figure 11 shows the MPEG parallel output mode timing diagram.

Figure 11. MPEG Parallel Output Mode Timing Diagram



5.2 MPEG Serial Output Mode

Table 12 specifies the setup and hold values for the MPEG data relative to the MPEG clock in serial mode. The following listing defines the acronyms used in the table:

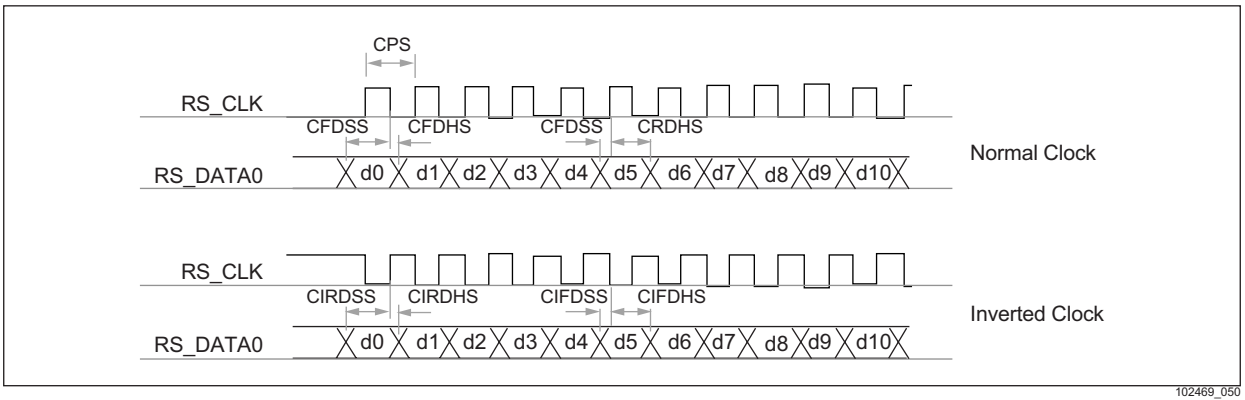
CPS	Clock Period
CFDSS	Setup time, data to clock fall.
CFDHS	Hold time, clock fall to data.
CRDSS	Setup time, data to clock rise.
CRDHS	Hold time, clock rise to data.
CIRDSS	Setup time, data to inverted clock rise.
CIRDHS	Hold time, inverted clock rise to data.
CIFDSS	Setup time, data to inverted clock fall.
CIFDHS	Hold time, inverted clock fall to data.

Table 10. MPEG Serial Output Mode Timing

MPEG Data	Min	Units
CPS	12.50	ns
CFDSS	9.60	ns
CFDHS	0.63	ns
CRDSS	3.80	ns
CRDHS	6.13	ns
CIRDSS	10.15	ns
CIRDHS	0.18	ns
CIFDSS	3.35	ns
CIFDHS	6.88	ns

Figure 12 shows the MPEG serial output mode timing diagram.

Figure 12. MPEG Serial Output Mode Timing Diagram



6 Electrical, Thermal, and Mechanical Specifications

6.1 Electrical and Thermal Specifications

Table 11 lists the absolute maximum ratings for the CX24116. Table 12 lists the recommended operating conditions, and Table 13 lists the electrical and thermal parameters.

Table 11. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
3.3 V Digital and Analog Power Supply Voltage: IO_VDD, REF_VAA, SH_VAA, A_VAA, CLK_VAA, PLL_VAA	–0.5	4.6	V
1.25 V Power Supply Voltage: CORE_VDD	—	1.8	V
Voltage at Any Digital Input Pin: V_{in}	–0.5	Vdd+0.3	V
DC Current Drain Per Vdd and Gnd Pairs: I_{in}	—	100	mA
Storage Temperature: T_s	–55	150	ºC
Lead Temperature (less than 10 seconds soldering): T_l	—	250	ºC
Junction Temperature: T_j	—	150	ºC

Table 12. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
3.3 V Digital and Analog Power Supply Voltage: IO_VDD, REF_VAA, SH_VAA, A_VAA, CLK_VAA, PLL_VAA	3.135	3.3	3.465	V
1.25 V Power Supply Voltage: CORE_VDD	1.19	1.25	1.31	V
Ambient Temperature: T_a	0	25	70	ºC
Junction Temperature: T_j	—	—	125	ºC

***Table 13. Electrical and Thermal Parameters** (1 of 2)*

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Low-Level Digital Input Voltage: V_{IL}	All digital inputs			0.8	V
High-Level Digital Input Voltage: V_{IH}	All digital inputs	2.0			V
High-Level Digital Output Voltage: V_{OH}	All digital outputs	2.4			V
Low-Level Digital Output Voltage: V_{OL}	All digital outputs			0.4	V
Symbol Rate	LDPC/BCH QPSK	10		30	MSps
	LDPC/BCH 8PSK	10		30	MSps
	DVB-S QPSK	2		45	MSps
	DTV Legacy		20		MSps
Carrier Acquisition	Range			10	± MHz
Gain Imbalance Compensation				3	± dB
Phase Imbalance Compensation				13	± Deg
A/D Converter	Input voltage range(1)		500		mVp-p
	Input impedance(2)		11		kΩ
Sample Frequency			91		MHz
AGCV	Output voltage range		3.3		V
Reset(3)	Minimum pulse duration	10			µs
Core Current (All 1.25 V Supplies)(4)	Normal operation, advanced transmission formats		See Plots	1842(5)	mA
	Normal operation, DVB-S and DTV Legacy		240(6)	488(7)	mA
	Sleep mode, all transmission formats		15		mA
3.3 V Current(4)	Normal operation, all transmission formats(8)		220	265(9)	mA
	Sleep mode, all transmission formats		60		mA
Thermal Resistance(10)	Junction to case: θjc		0.5		ºC/W
	Junction to ambient: θja		18		ºC/W

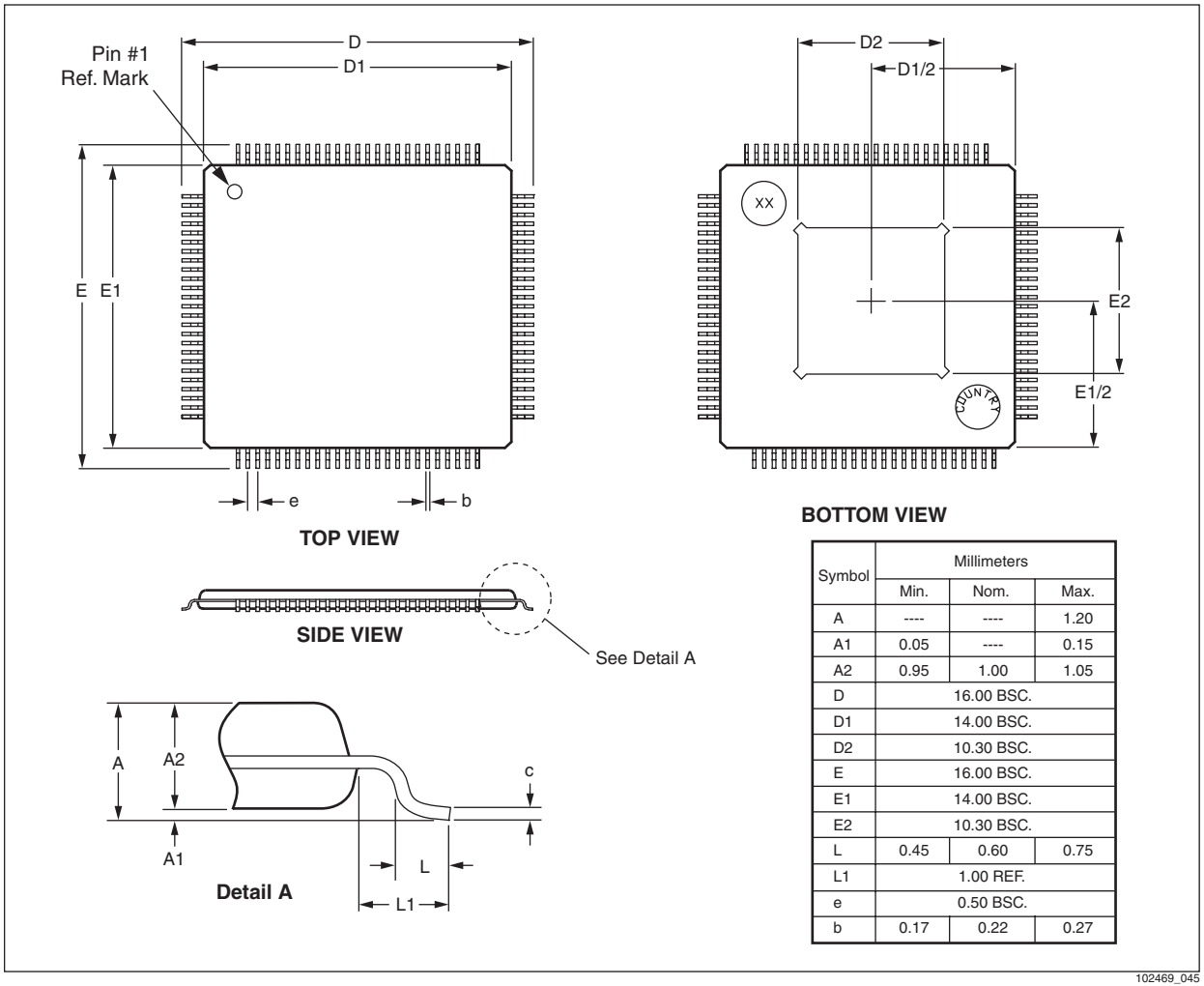
Table 13. Electrical and Thermal Parameters *(2 of 2)*

Parameter	Conditions	Minimum	Typical	Maximum	Unit
FOOTNOTES:					
(1) This is the total peak-to-peak voltage. When used single-ended, this voltage will be at each input. When used differentially, half of this voltage will appear at each input.					
(2) This is the input impedance of each input.					
(3) The $\overline{\text{RESET}}$ pin should be held low until after both power supplies (1.25 V and 3.3 V) have been brought up.					
(4) All current measurements taken with software version 1.16.64.0.					
(5) V = 1.313 V, Ta = 70 °C, worst-case ES/N0, peak current, LDPC/BCH 8PSK, SR = 30 MSps, CR = 3/5, Pilots = On, Roll-off = 0.2.					
(6) SR = 20 MSps, any code rate, T_A = 25 °C, V = 1.25 V.					
(7) DVB-S, SR = 45 MSps, CR = 7/8, V_{DD} = 1.313 V, T_A = 70 °C, software version 1.16.64.0.					
(8) When used with recommended external components.					
(9) V = 3.465 V, Ta = 0°C.					
(10) Using four-layer evaluation board.					

6.2 Mechanical Specifications

Figure 13 shows the CX24116 100-pin eTQFP.

Figure 13. 100-Pin eTQFP Diagram



Symbol	Millimeters		
	Min.	Nom.	Max.
A	----	----	1.20
A1	0.05	----	0.15
A2	0.95	1.00	1.05
D		16.00 BSC.	
D1		14.00 BSC.	
D2		10.30 BSC.	
E		16.00 BSC.	
E1		14.00 BSC.	
E2		10.30 BSC.	
L	0.45	0.60	0.75
L1		1.00 REF.	
e		0.50 BSC.	
b	0.17	0.22	0.27

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