Examensarbete
LITH-ITN-ED-EX--07/016--SE

Construction of a digital-TV receiver for the second-generation satellite broadcasting, DVB-S2

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2007-06-20

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Examensarbete utfört i Elektronikdesign
vid Linköpings Tekniska Högskola, Campus Norrköping

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Norrköping 2007-06-20

Avdelning, Institution
Division, Department

Institutionen för teknik och naturvetenskap

Department of Science and Technology

Datum
Date

2007-06-20

Språk
Language

☐ Svenska/Swedish
☒ Engelska/English

☐ _____

Rapporttyp
Report category

Examensarbete
☐ B-uppsats
☐ C-uppsats
☒ D-uppsats

☐ _____

ISBN

ISRN **LITH-ITN-ED-EX--07/016--SE**

Serietitel och serienummer
Title of series, numbering

ISSN

URL för elektronisk version

Titel
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Sammanfattning
Abstract

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The report consists of two objectives; a survey of the most commonly used standards for digital television today and the construction of a prototype receiver for the second generation satellite DVB-standard.

A thorough literature study and careful design resulted in a fully functioning system. Measurements performed on the DVB-S sections gave exemplary results. Comparing these results with corresponding measurements performed on the DVB-S2 section showed much better performance for DVB-S2 with the same code rates. This shows some of the advantages of the new standard and proving the coding theory right. New coding algorithms make it possible to transmit more information on noisier channels of inferior quality. In laymen´s words; DVB-S2 gives a better picture and more television channels on the same satellite compared to DVB-S.

Nyckelord
Keyword

modulationstekniker, digital-tv, dvb-s2, elektronikkonstruktion

Abstract

Digital television is one of the biggest broadcasting media available. All over the world television companies are rearranging their broadcasting from analogue to digital transmission. Former standard disagreements in the analogue era have lead to an agreement of one common European standard for digital television. Countries like USA and Japan have their own similar standards.

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Acknowledgements

A number of people have helped us making this thesis possible. First of all, we would like to thank everybody at Zenterio, especially our supervisor Sven Jansson, who was very helpful. We would also like to thank Kent Lundberg for giving us opportunity and recourses for this thesis.

We would also like to thank the following people who helped us in various ways: Erna Mehmedagic and Kam Hung To, our opponents for their constructive criticisms. Qin-Zhong Ye, our examiner at Institution of Science, University of Linköping, for his support and help.

Last but not least, we would like to thank our families and friends for their love and support.

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1 Introduction

1.1 Preface

This report describes a final year project conducted during spring 2007 at Zenterio AB. The project goal was to build and test a receiver for the new satellite standard for digital television broadcasting, DVB-S2.

1.2 About Zenterio AB

Zenterio AB was founded in March 2002 by 15 employees from Nokia Home Communications. Due to the dot-com crash, Nokia had to liquidate its R&D department in Linköping. Kent Lundberg, a born entrepreneur at Nokia, had a vision to keep 15 top experts and continue with Nokias mission. Major downsizing and cutting of salaries were the solutions to stay interactive. Today, with 28 employees, Zenterio is an established software company in digital TV and Set-Top-Boxes domain.

1.3 About the authors

The authors of the report are Anders Jonasson and Nedim Ramiz. Anders has completed his final year as a student in the Master of Science Program in Applied Physics and Electrical Engineering at University of Linköping. Nedim is currently completing his final year as a student in the Master of Science Program in Electronics Design Engineering at University of Linköping.

1.4 Background

Digital television is one of the biggest broadcasting media available. All over the world television companies are rearranging their broadcasting from analogue to digital transmission. Former standard disagreements in the analogue era have lead to an agreement of one common European standard for digital television. Five of the broadcasting standards are covered in this report. Those five standards are satellite S/S2, cable C, terrestrial T and handheld H. Countries like USA and Japan have their own similar standards.

1.5 Purpose

The main purpose of this thesis was to acquire a greater knowledge on digital television transmission systems and to construct a receiver for the second generation satellite standard, DVB-S2. The new standard is in many ways an improvement over the present DVB-S standard, and in the next couple of years more and more DVB-S2 channels will pop up. The receiver was built for testing and educational purposes.

1.6 Goal

Several different approaches will be covered in this thesis. The theoretical approach will discuss current broadcasting ability between different standards. Different broadcasting and modulations

techniques will be presented and analyzed. The practical approach consists of learning the design techniques and applying them later in the real product. The empirical approach will show the examined product after testing and measuring. The final goal will be to understand the biggest differences between broadcasting standards and keeping the knowledge in the case of future work in the area.

1.7 Method

For the theoretical knowledge of this thesis, a literature study of different broadcasting standards and modulation techniques has been performed. Comparison was made between the standards and modulation techniques to consider the advantages and disadvantages. The starting point was to understand the present DVB-S system and decide which components were compatible and available in order to construct a receiver for DVB-S2.

The most demanding task of this thesis was the Printed Circuit Board (PCB) layout due to its complexity in Electro Magnetic Compliance (EMC) and Radio Frequency (RF) design. The finishing point was to construct and install drivers and later on measure and test the finished product.

1.8 Target group

To fully understand the facts presented in this thesis a prior knowledge in electronics, physics, and hardware development is valuable. Even though the reader is presumed to have previous knowledge in the mentioned areas, most of the information should be relatively easy to consume.

1.9 Reading guide

This section contains a short description of each chapter and appendix in the report.

- Chapter 1 contains a short introduction to the thesis. The goal, purpose, background, method and target group are discussed.
- Chapter 2 shows the reader a quick overview of analogue modulation techniques, required to understand important terms in Chapter 3.
- Chapter 3 gives the reader an introduction to digital modulation techniques, describing important terms in digital transmission and digital television.
- Chapter 4 describes digital television systems all over the world. It also contains deeper and detailed information on second generation DVB satellite broadcasting.
- Chapter 5 contains speculations on the future of digital television.
- Chapter 6 briefly describes how satellite reception works.
- Chapter 7 describes the different subsystems needed to build a satellite receiver.

- Chapter 8 contains information about several different chipsets to build a receiver for second generation satellite Set-Top-Boxes.

- Chapter 9 explains the physical and electronic behavior of the components on the PCB, covering important issues of EMC compliance and showing the development of RF energy in circuits.

- Chapter 10 presents circuit design considerations such as calculations of voltages and currents between interactive components.

- Chapter 11 shows the actual final product and briefly explains its functions.

- Chapter 12 briefly describes the software drivers needed by the STB.

- Chapter 13 contains information about measurement and testing.

- Chapter 14 presents the report results.

- Chapter 15 contains a final conclusion, discussion and ideas about future work in the field of digital television.

- Chapter 16 lists the books, articles and doctorate works used in the thesis as literature framework.

2 Analog Modulations techniques

2.1 Amplitude Modulation (AM)

Amplitude modulation is characterized by that the message m(t), equation 2.1, decides the amplitude of a carrier frequency ω_c, see eq. 2.2

$$m(t) = M \cdot \cos(\omega_m t) \tag{2.1}$$

$$s(t) = m(t) \cdot \cos(w_c t) = M \cdot \cos(\omega_m t) \cdot \cos(\omega_c t) \tag{2.2}$$

The envelope of the resulting modulated signal is an approximation of the message. A problem appears when the message m(t) changes sign. When this happens the modulated signal s(t) will also change sign which results in that the carrier frequency changes phase 180 degrees. This problem is solved by the adding of a constant voltage to the message m(t). The constant voltage A in equation 2.3 will always, if A/M>1, result in a positive amplitude of the modulated signal s(t).

$$s(t) = \big(A + m(t)\big) \cdot \cos(\omega_c t) = C \cdot (1 + v \cdot \cos(\omega_m t)) \cdot \cos(\omega_c t) \tag{2.3}$$

The constant v in equation 2.3 is called the modulation index and is an indication of how much the modulated carrier varies around its original level. Equation 2.3 can also be described in a different way such as in equation 2.4.

$$s(t) = C \cdot \cos(\omega_c t) + \left(\frac{v \cdot C}{2}\right) \cdot \cos\big((\omega_c - \omega_m)t\big) + \left(\frac{v \cdot C}{2}\right) \cdot \cos\big((\omega_c + \omega_m)t\big) \tag{2.4}$$

Equation 2.4 contains three parts: The carrier frequency with amplitude C, one lower sideband in which the frequency varies between ω_c and $\omega_c - \omega_m$, and an upper sideband where the frequency varies between ω_c and $\omega_c + \omega_m$. This property characterizes Amplitude Modulation with Double SideBands (AM-DSB).

Amplitude modulation with double sidebands and carrier is inefficient in terms of power usage in relation of how much information is being sent. The quote between useful and the total signal effect is at most 33%. Most of the power is concentrated in the carrier signal which conveys no information and suppression of the carrier (double sideband suppressed carrier DSBSC) makes it more efficient. The sidebands are mirrors of each other, one of the sidebands can be suppressed without information loss (Single SideBand Suppressed Carrier, SSBSC). This will also make it more power efficient and lowers the required bandwidth by half. One more advantage of SSBSC is protection of selective fading. Fading occurs when the channel adds a non wanted phase difference between the upper and lower sideband. The result can be disastrous if the relative phase difference between the channels approach 180 degrees, which can cause the components to almost disappear. The foremost advantage of AM-DSB is the use of simple modulators and demodulators.

Vestigial Sideband Modulation (VSB) is a modulation scheme used by the ATSC DTV system. Traditional amplitude modulation generates a double sideband RF spectrum about the carrier frequency. The sidebands are mirrors of each other and one is redundant and can be discarded without information loss, see figure 2.1. Strategy is employed to some degree in VSB, in which the lower sideband has been partly suppressed. Using suppression of the lower sideband lowers the required bandwidth of the channel. The drawback is the demodulation becoming more troublesome. VSB is not as effective in terms of power usage as SSB but demodulation is more straightforward. Generally, when modulation is more directed towards the ideal SSB in terms of power and bandwidth efficiency, more advanced techniques are required for both modulation and demodulation [1].

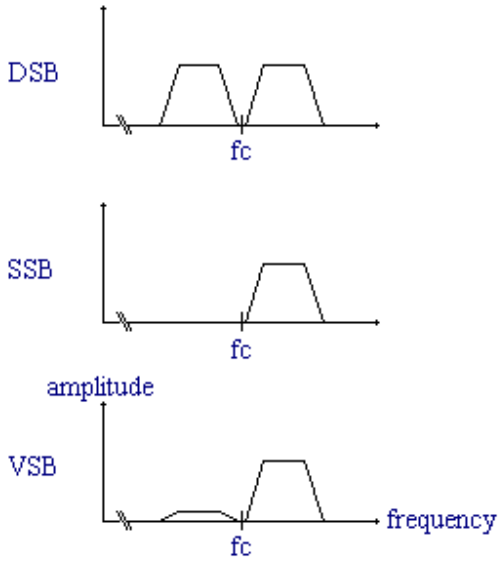

Figure 2.1 - AM-DSB, SSB and VSB described in the frequency plane

2.2 Frequency Modulation (FM)

Amplitude modulation was one of the first modulation techniques used. When radio transmissions became more and more used, the interest for new modulation techniques grew rapidly. To get more traffic in the air, the seek for a modulation form that could squeeze more information into a specified bandwidth begun. FM was proposed and was in the beginning thought to have a lower bandwidth than AM. This was not the case and the interest for FM shrunk rapidly. Nowadays FM is used frequently in a wide spectrum of radio transmission areas. Due to the constant amplitude, noise and interference sensitivity is much lower for FM than for AM. Another feature with FM is the lower sensitivity for nonlinearities. If FM is used on a nonlinear channel this will add components with multiples of the carrier frequency which easily could be filtered out.

When using frequency modulation the instantaneous frequency will be dependent on the message m(t), which will set the phase of the cosine.

$$s(t) = A \cdot \cos\left(\omega_c t + \theta(t)\right) \tag{2.5}$$

The phase θ will be set by equation 2.7.

$$m(t) = M \cdot \cos(\omega_c t) \tag{2.6}$$

$$\frac{d\theta(t)}{dt} = P \cdot m(t) \tag{2.7}$$

$$s(t) = A \cdot \cos(\omega_c t + P \cdot M \cdot \int \cos(\omega_m t)\, dt) = A \cdot \cos\left(\omega_c t + \frac{P \cdot M}{\omega_m} \cdot \sin(\omega_m t)\right) \tag{2.8}$$

The instantaneous frequency of the resulting modulated signal is varying in a sine like fashion in the interval $[\omega_c - A \cdot P, \omega_c + A \cdot P]$.

$$\omega_s(t) = \frac{d\theta_s(t)}{dt} = \omega_c + A \cdot P \cdot \cos(\omega_m t) \tag{2.9}$$

The FM spectrum can be found by Fourier transform and the use of Bessel functions. The interested reader could for example see [1].

2.3 Phase Modulation (PM)

Phase Modulation uses different phase states to carry information. PM in the simplest form has never been used much. It requires more advanced hardware to be used, and if for example two phase positions are used there is hard to see the difference between 0 and 180 degrees phase shift.

2.4 Fading

Fading is a multipurpose name for mathematical models of the distortion when sending over various channels.

2.5 Multipath propagation

Whenever a wireless RF signal is sent (ground wave) the multipath propagation phenomenon appears. The signal takes multiple paths from the transmitter to the aerial, see figure 2.2. These different signals interfere at the aerial causing the amplitude of the received signal to fluctuate. Signals can be reflected and phase disturbed by terrestrial objects such as mountains and buildings among other things. Ionospheric reflection and refraction, and atmospheric ducting are other things causing multipath propagation. OFDM is a technique (explained later in this report) to get rid of the artifacts of multipath propagation. This is done by sending small information packets with delays in between. The reflected signals can then pass by the aerial before the next information packet is sent, thus getting around the problem of multipath propagation.

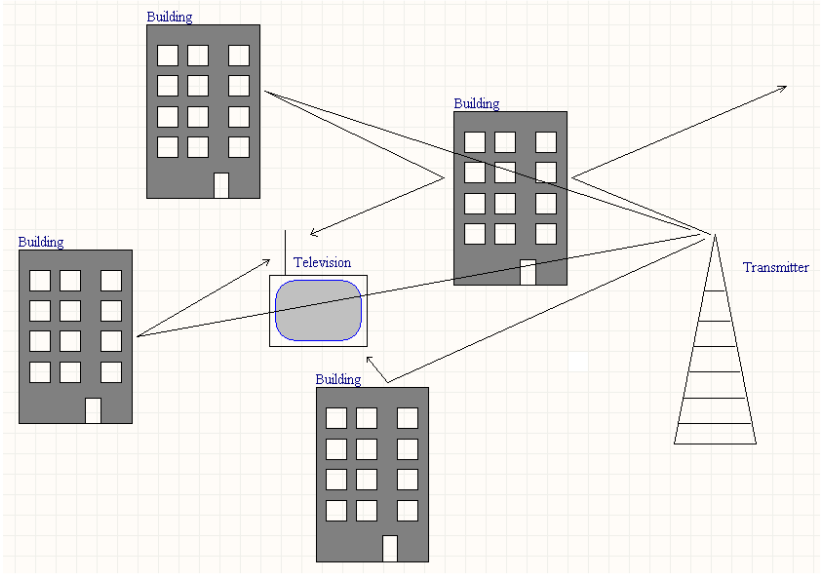

Figure 2.2 - Multipath propagation

3 Digital modulation techniques

3.1 Amplitude Shift Keying (ASK)

Amplitude Shift Keying is the digital counterpart of analog AM. As the name implies the envelope of the modulated signal is varied. Especially on radio channels the damping is of great concern when using ASK. Big and fast variations of the total channel damping affect the amplitude of the transmitted signal and can in the worst case lead to a false symbol received. The symbol rate has an upper limit that varies with the bandwidth of the channel. The preceding symbol must have time to decay to a low level before the next symbol is sent. If the time allowed for decay is too short an effect called inter symbol interference will make it hard to separate symbols following each other. With the use of several discrete amplitudes, for example 8 levels, more information can be sent at the same time as three bits can be coded as one level. This is for example done in 8-VSB used by the ATCS digital television system [14].

3.2 Frequency Shift Keying (FSK)

Frequency Shift Keying is the digital counterpart of analog FM. The frequency is shifted between two or more predetermined values. Minimum Shift Keying (MSK) is a subgroup of FSK where the frequencies used differs by half the data bit rate. This will assure that the transitions between the different frequencies will be smooth. FSK is used by many of all the worlds' telephone companies.

3.3 Phase Shift Keying (PSK)

Phase Shift Keying is a modulations technique that shifts period of the wave, the so called wave carrier. There are three major examples of PSK, Binary Phase Shift Keying (BPSK) which uses two phases, Quadrature Phase Shift Keying (QPSK) and Differential Phase Shift Keying (DPSK) which depends on the difference between successive phases. There are also extended versions of PSK, such as Offset QPSK (OQPSK) and $\pi/4$–QPSK.

The modulation schemes are representing digital data by using a finite number of distinct signal constellations. Every single phase is made by a unique pattern of binary bits; where usually each phase encodes an equal number of bits. The symbol that is formed by a certain bit pattern is then represented by a particular phase. The demodulator, which is an electronic circuit that recovers information content from the carrier wave of the signal, determines the phase and decodes the symbol it represents so that the original data is recovered. This system is termed coherent, meaning the receiver needs to be able to compare the phase of the received signal to a reference signal.

There are various examples of PSK applications in several existing technologies. The most popular is wireless Local Area Network (LAN) that uses a variety of different PSK depending on the required data-rate. If the data rate is 1 Mbit/s, DBPSK is used. Should the data rate increase to 2 Mbit/s, it would be appropriate to use DPSK. At data rates over 5.5 Mbit/s to 11 Mbit/s QPSK is employed, but with some complementary code keying. Higher speed wireless LAN use other coding techniques.

Radio Frequency Identification (RFID), a small tag, which is used in credit cards, passports, product tracking and automotive, is using BPSK because of its simplicity for low-cost passive transmitters. The Bluetooth technique is using π/4–QPSK for low data rates and 8-DPSK for higher data rates when the link between the two devices is satisfactorily robust. ZigBee also relies on PSK, but operates in only two frequency bands: 868–915 MHz where it employs BPSK and at 2.4GHz where it uses OQPSK.

3.4 Binary Phase Shift Keying (BPSK)

BPSK is the easiest form of PSK, which uses two phases separated by 180 degrees. The coding can be pictured as constellation points in the complex plane. In BPSK the constellation points are positioned on the real axis, see figure 3.1. Because of the 180 degree phase difference it has robust characteristics which make decoding easy. It's not suitable for high data rate applications for the reason that is only able to send 1 bit/symbol.

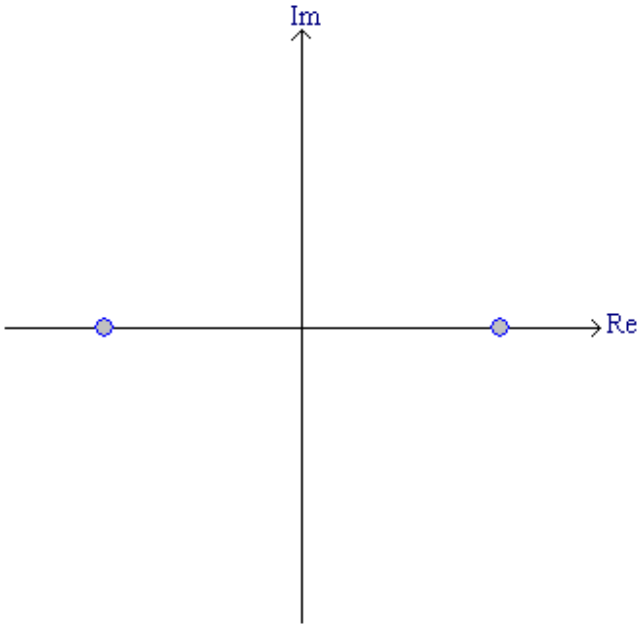

Figure 3.1 - Illustration of the BPSK constellation

3.5 Quadrature Phase Shift Keying (QPSK)

In QPSK there are four constellation points placed with equal distance to center, see figure 3.2. QPSK enables the use of either double data rate, compared to a BPSK system, while maintaining the same bandwidth, or the same data rate as BPSK but with less bandwidth.

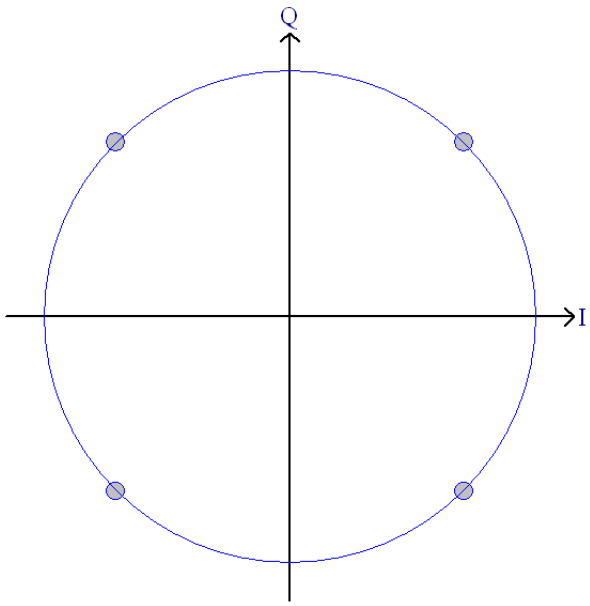

Figure 3.2 - Illustration of the QPSK constellation

3.6 Differential Phase Shift Keying (DPSK)

This method is an alternative method of demodulation and it is used for signals that have been encoded differentially. By ignoring carrier-phase ambiguity and demodulating, the phase between two received signals is compared and used to decode the data.

3.7 Offset QPSK (OQPSK)

This method is another variant of QPSK which uses 4 different phase values for coding. In QPSK there is a possibility for the phase to jump 180 degrees at a time. When the signal is low pass filtered, as it is in for example transmitters, this causes large amplitude fluctuations. In OQPSK this phenomenon is prevented by offsetting the changes in the I- and Q-channels by one bit-period, which results in a maximum phase jump of 90 degrees.

3.8 Quadrature Amplitude Modulation (QAM)

QAM uses both phase shift and amplitude modulation. By using the amplitude as an extra degree of freedom every symbol can contain more information. Information is thus stored both in the phase and length of the transferred vector. There are several types of QAM modulation, such as 16-QAM that can assume 12 phases and three amplitude sizes, see figure 3.3. The most common type used for digital TV is 64-QAM which can transfer 64 different symbols, each containing 6 bits. Distribution of the 6-bits is done with Gray Coding, changing only one bit at a time for adjacent symbols. Should the decoder miss one bit group, the error would probably only be one misread bit [2], [3].

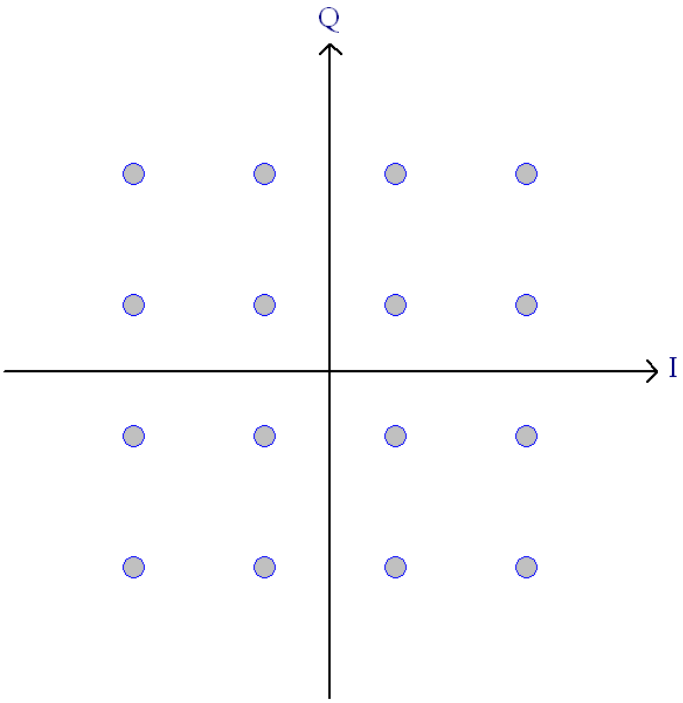

Figure 3.3 - 16-QAM (4x4) constellation pattern

3.9 Code Division Multiplexing (CDM)

CDM is one of the techniques used in the ISDB standard for frequencies at 2.6 GHz and it is used as an access technology named Code Division Multiple Access (CDMA). Its main application is in the Universal Mobile Telecommunications System (UMTS) which is the standard for third generation mobile phone systems. Another field is within Global Positioning Systems (GPS) where it is regularly used. Other multiple access techniques are Time Division Multiple Access (TDMA) and Frequency Division Multiple Access (FDMA).

CDM transmits bits in each channel as a coded channel specific sequence of pulses. The coding is accomplished by transmitting a certain time-dependent series of short pulses, which later are placed in a chip within larger bit time, see figure 3.4. Each channel has a different code and can be sent on the same fiber and be asynchronously de-multiplexed.

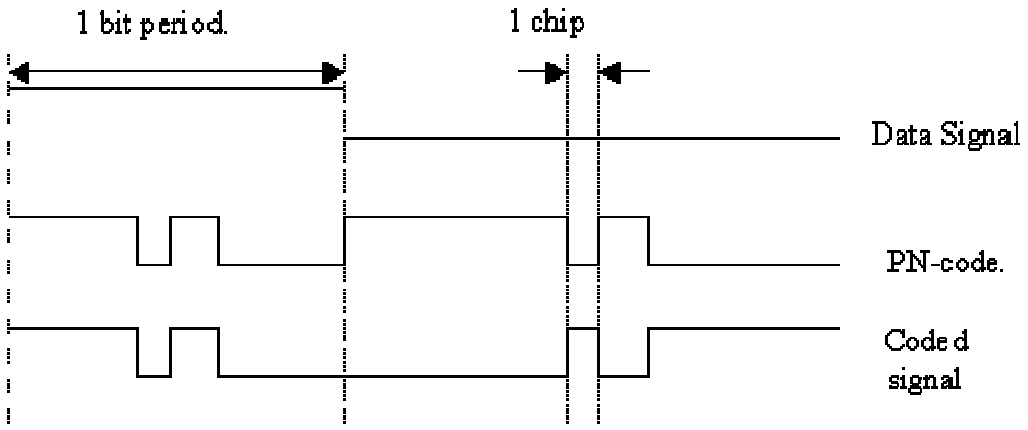

Figure 3.4 - Code Division Multiplexing

3.10 Orthogonal Frequency Division Multiplexing (OFDM)

OFDM is mainly used in digital communications transmitting data on multiple carriers over one single communications channel. This technique is used in wireless applications, such as cable modems, digital radio, Digital Subscriber Line (DSL), power line technology, terrestrial digital radio and television, wireless LAN and many more.

In OFDM, the stream of bits to be transmitted is split up into multiple data streams and is transmitted using multiple data BPSK carriers at a certain frequency over the same wired or wireless communications channel. However, any digital modulation method can be used for the data stream subcarriers. The available frequency spectrum is split up into several sub channels in form of cosine and sine waves and each symbol is transmitted over one sub-channel by converting a sub-carrier using a modulation technique such as PSK, QAM. The frequencies are chosen so the modulated data streams are orthogonal to each other, which results in the ability to send several signals over the same medium without any interference [3].

4 Digital television systems

Digital television transmission systems differ around the world. In Japan the Integrated Service Digital Broadcasting (ISDB) system is standard [15]. In USA, Advanced Television Systems Committee (ATSC) is the main standard [14] and in Europe the Digital Video Broadcasting (DVB) standard [16] is most widespread. The next few chapters will compile a survey of the mentioned standards.

4.1 ISDB

ISDB were created to transmit signals from radio and television stations in the new digital format era. The ISDB standards are ISDB-S (satellite), ISDB-T (terrestrial), ISDB-C (cable), ISDB-Tsb (terrestrial digital sound broadcasting) and a mobile broadcasting standard for the 2.6 GHz band. For mobile reception in TV bands ISDB-S and ISDB-Tsb formats are often used. This concept allows multiple channels of data to be transmitted at the same time, which is very similar to the digital radio system Eureka 147, which calls each group of stations on a transmitter an ensemble [15]. This system is also similar to European multi channel digital TV standard DVB-T.

Compression of video and audio in ISDB is done with MPEG-2. The same compression system is used in some of the American and European standards. Other compression methods which are used in both DVB and ISDB are Joint Picture Experts Group (JPEG) and Moving Pictures Experts Group (MPEG-4). ISDB is split up in different modulations, due to different requirements of different frequency bands and media. PSK-modulation is used in the satellite standard ISDB-S for the 12 GHz band. CDM-modulation is used in the 2.6 GHz band for digital sound broadcasting and the terrestrial standard ISDB-T is using COFDM modulation with PSK/QAM. The most used interaction that ISDB uses, besides audio and video, is with Internet as a return channel over several other medias, such as mobile phones, wireless LAN, telephone line modem etc.

4.1.1 ISDB-Satellite

Japan has been using the DVB-S standard since 1996, but some of the Japanese broadcasters were not satisfied. The requirements were HTDV capability, interactive services, network access and effective frequency utilization. The DVB-S standard can only transmit 34 Mbit/s with a single satellite transponder, which means the transponder only can send one High Definition Television (HDTV) channel. The Japanese satellite has four vacant transponders. The unused transponders were used to try out new transmitter techniques which led to the development of ISDB-S, a standard that can transmit as much as 51Mbit/s with a single transponder. That means the efficiency is increased 1.5 times and that one transponder can transmit two HDTV channels, which would be a groundbreaking achievement for future companies and businesses.

Satellite digital broadcasting is using phase shift keying modulations such as QPSK and BPSK. For audio and video coding and multiplexing, MPEG-2 encoding technology is applied. The frequency range for BS digital broadcasting is 11.7 to 12.2 GHz and for wide band CS digital broadcasting the frequency is between 12.2 and 12.75 GHz. Transmission bit rate are 51 Mbit/s and 40 Mbit/s respectively. However, the 34.5MHz transmission bandwidth is the same.

4.1.2 ISDB-Terrestrial

HDTV began its journey and development around 1960s but the standard was suggested around mid 1970s. The television camera, high definition Cathode-Ray Tube (CRT), video tape receiver and other editing equipment came at 1980s. At the same time a company named Nippon Hōsō Kyōkai (NHK) had developed MUltiple sub-nyquist Sampling Encoding (MUSE), which was the first HDTV video compression and transmission system. MUSE implements a digital video compression system, but one of the drawbacks is that the digital signal must be converted by a digital-to-analog converter in order to modulate the signal. Both Europe and USA were impressed by the technology which led to the development of the ATSC standard for USA and the DVB standard for Europe.

There are several characteristics that distinguish ISDB-T from other standards. For example both a HDTV channel and a mobile phone channel can be transmitted within the 6 MHz bandwidth usually reserved for standard TV. The bandwidth is enough for sending one HDTV channel or two, maybe three, multiplexed Standard Definition Television (SDTV) channels. It provides interactive services with data broadcasting and Electronic Program Guides (EPG). ISDB-T also provides robustness to multipath interference called “ghosting”, co-channel analog television interference and to impulse noises coming from power lines and motor vehicles in suburbs.

ISDB-T first commercial use was adopted in Japan at the end of 2003, taking over a market of about 100 millions television sets. Brazil has also transferred from the analogue TV system (PAL-M) to the ISTB-T standard, calling it SBTVD-T. For development of technology in Latin America, other countries such as Argentina, Venezuela are thinking of cooperating with Brazil in order to prevent import from other standards and countries. In addition, reception tests have shown better results using ISDB-T compared to both ATSC and DVB. The tests showed that ISDB was the most flexible solution for better answering the necessities of mobility and portability.

Terrestrial digital broadcasting uses amplitude modulation like 64QAM-OFDM, 16QAM-OFDM, 16QAM-OFDM and DQPSK-OFDM. For audio coding, video coding and multiplexing, MPEG-2 encoding technology is mostly used, but MPEG-4 is used for some mobile phone segments [15].

4.2 ATSC

The ATSC group [14] helped develop the new digital television standard for the United States of America. Several other countries such as Canada, Korea and Mexico have adapted to this standard. The ATSC standard covers both terrestrial, cable and satellite transmissions. For terrestrial use the 8-VSB modulation form is applied. When using cable the signal-to-noise ratio is higher, and more advanced forms of modulation can be used, such as 16-VSB and 256-QAM, to capsule more information on the same channel bandwidth. As the ATSC terrestrial standard is almost identical to the cable standard just ATSC-T will be described in greater depth in this text. Generally the video content is digitalized by MPEG-2 encoding, error correction added and finally the modulation form and RF up-converter are used to transmit the information.

4.2.1 ATSC-Terrestrial

Digital information in VSB is transmitted exclusively in the amplitude envelope unlike other modulation formats where also the phase can contain information. 8-VSB used by standard ATSC handles eight amplitude levels. The spectrum of digital 8-VSB is contained in a 6 MHz channel as in the National Television Standard Committee (NTSC) television standard. With the use of data encoders the data is transformed and will get almost noise-like characteristics. Therefore the digital spectrum is, in contradiction to the NTSC spectrum, flat throughout most of the band, making efficient use of the channel bandwidth.

From the MPEG-2 video output stream to the data stream it is required to add error correction codes among other things, see figure 4.1. Every block in the figure will be explained in the following text.

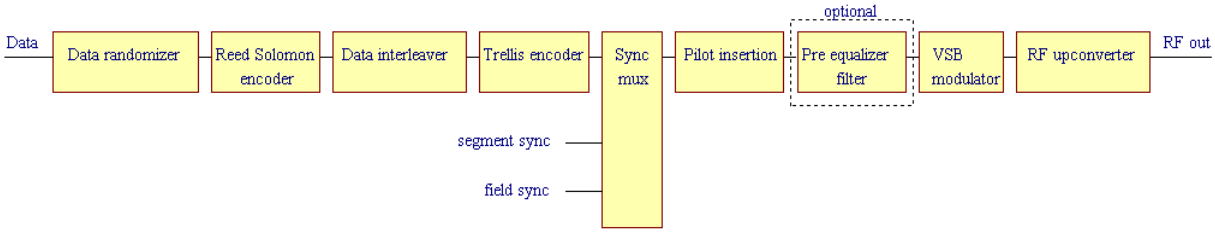

Figure 4.1 - Functional block diagram of the ATSC-T modulator and encoder

The MPEG-2 package from the video converter contains 187 bytes plus a packet sync byte. The packet sync byte is removed and the data is further processed. The *Data randomizer* is used to get a random data stream that will be almost noise-like to make efficient use of the channel space. For example, if our data contained repetitive patterns some of the parts of the spectrum would be overused, leaving holes in other parts of the spectrum. The data randomizer is built up by a Pseudo Random Binary Sequence (PRBS) generator. The code used for randomization is also stored in the receiver for proper recovery of the data values. The *Reed-Solomon encoder* adds redundant information for error correction purposes. Adding redundant information in this way is in general terms called Forward Error Correction (FEC). The extra information is used if the data stream sent in any way is corrupted by for example atmospheric noise, multipath propagation, signal fades and transmitter nonlinearities. The error correction bits can compensate for this up to a certain point. All the 187 bytes from the MPEG-2 packet is used by the Reed-Solomon encoder. The encoder adds an extra 20 parity bytes to the tail of the packet. The receiver compares the MPEG-2 packet with the parity bytes in order to determine the validity of the received data. Up to 10 error bytes can be found and corrected before the entire packet must be discarded. The *Data interleaver* incorporates a buffer and combines bytes from different packages (according to a specified pattern, which is known to the receiver) to account for burst-type interference effects in the channel. If a sent segment is lost due to burst interference this means that only a part of the original packet is lost and this can often be restored by the Reed-Solomon correction code. The *Trellis code* is an evolving error correction code and as the Reed-Solomon code it is another FEC. Every incoming 2-byte word is compared to the past history of 2-byte words to generate a 3-byte word describing the changes from the foregoing transitions.

The receiver can correct potential errors by looking at the past history of received 3-byte words. Help signals such as ATSC pilot, segment sync and frame sync signal must be applied before modulation, helping the receiver to place the received packets in the correct order. In the *8-VSB modulator* the 3-byte words from the Trellis encoder are converted to an 8-level discrete amplitude and modulated according to AM-VSB. The signal is amplified and adjusted for the used channel and sent to the receivers.

4.2.2 ATSC-Satellite

The modulation forms used in the satellite standard are QPSK, 8PSK and 16QAM. With the use of more advanced modulation techniques the consumed bandwidth is less, for a constant bit rate, than for QPSK. The bit rate is increased as well as overall performance. The main drawback is the use of more power to achieve the same level of performance. For a functional block diagram, see figure 4.2.

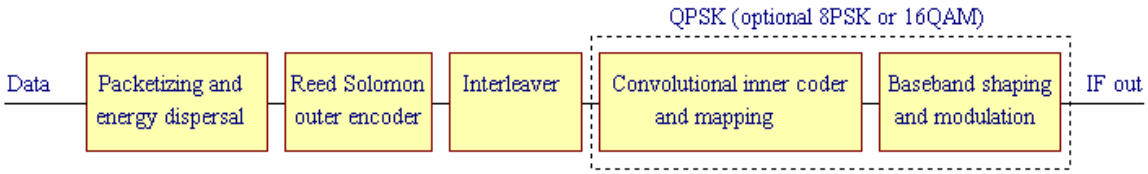

Figure 4.2 - Functional block diagram

The standard relies on previous work done within the DVB project, especially [21] and [22]. The main distinction between DVB-S and the ATSC-S system is the use of arbitrary data streams. The ATSC-S system can use MPEG data streams or an arbitrary constant rate data stream. In the case of the arbitrary data stream, the modulator packetizes 187 bytes together with a 0x47hex sync byte to form a MPEG-like package. In the demodulator end this sync byte is discarded to deliver the arbitrary data stream to the output. Modulation and coding is done in the same way according to the DVB standards [21] and [22]. See the DVB-S section for more information.

4.3 DVB

The DVB project is a cooperation of about 250-300 companies worldwide. It is an open standard of European origin but now spreading over the world. The specifications proposed by the DVB alliance are passed on to the European Broadcasting Union (EBU/GENELEC/ETSI) Joint Technical Committee for approval and later standardization. With the close cooperation with the industry the DVB specifications has been market driven and the development has been done with the finished product in mind. This has probably contributed greatly to the DVB success.

There are several digital television standards developed by the DVB project group, among which are:

- DVB-Satellite
- DVB-Cable
- DVB-Terrestrial
- DVB-Handheld
- DVB-Satellite 2nd Generation

4.3.1 DVB-Satellite

The DVB-S standard was published in 1993 by the EBU commission and it became standard for broadcasting of digital television over satellite. Its main purpose is to prepare a digital MPEG transport for satellite transmission. The standard for DVB-S is similar to the standard for DVB-T, except from using the modulation technique QPSK instead of COFDM. Quaternary PSK modulations technique is more suitable for satellite transmission due to higher bandwidth with small and weak noise transferring channel. The key features in DVB-S are: Changing encoding parameters in real time, Variable Coding and Modulation (VCM) and Adaptive Coding and Modulation (ACM). For a functional block diagram, see figure 4.3.

Figure 4.3 – DVB-S functional block diagram

4.3.1.1 Signal coding and channel adaption

Video, audio and data information, so called bit waves, are received in the program MUltipleXer (MUX). Different packages form a transport stream together with Program Specific Information (PSI). Then the transportation MUX combines the different TV-channels transportation streams to a common Transport Stream (TS), where each stream is supplied with its own identification, a transport- ID, “TS-id”. A device for energy spread is used for evening out the sequences with binary ones and zeros, evening out the energy located in the transmission channel. The signal move on to the device called Reed-Solomon encoder. This type of encoding is called RS (204, 188 t=8), meaning 16 additional bytes is added to the 188 bit package which can correct up to eight incorrect bytes. Burst type interference can be managed with the interleaving encoder, where streams permute byte by byte into 12 different streams. The first has no delay time; the second is delayed with 17 bytes, the third with 34 etc. Viterbi encoding, which is a FEC, gives protection against random noise. Least safety is given by 7/8 which adds 1 extra control bit for every 7 bits. Highest safety gives 1/2 which doubles the number of bits. In satellite-TV context a FEC with value of 1/2 is very unusual. After Viterbi encoding the data stream is sent for encoding into Gray coded QPSK, where only one bit is changed between adjacent pair of bits.

4.3.1.2 Applications and Market

The DVB-S standard is mostly used in broadcasting applications, but has other purposes like point-to-point transmission. The reason why it became such a great success in the broadcasting market is due to inexpensive silicon used in the receivers. The market for DVB-S is divided in to

two segment, DTH (Direct-to-home) and Contribution and Distribution. The DTH-segment is referred to TV for home reception, Satellite Master Antenna Television (SMATV), Internet Access/Content delivery, Interactive TV and many more. Contribution-and-Distribution-segment includes Satellite News Gathering (DSNG), cable feeds, flight entertainment and Internet content distribution/trunking.

4.3.2 DVB-Satellite 2nd generation

DVB-S2 was developed in the DVB Project in 2003 and became the second generation specification for satellite broadcasting. Combining a variety of modulation formats such as QPSK, 8PSK, 16APSK and 32APSK with the latest developments in channel coding, it became a great benefit in interactive applications. Broadcasting services are managed with DVB-S and with the flexible VCM. Broadcasting Services (BS) offers great levels of protection for both robust SDTV and less robust HDTV. Along with the existing DVB Return Channel Standard (DVB-RCS), Interactive Services (IS) is designed to operate in both CCM and ACM modes. ACM mode is here used to enable receiving station to control the protection around the traffic addressed around it. DTV and DSNG uses either CCM or ACM modes for facilitating point-to-point or point-to-multipoint communications of single or multiple MPEG transport streams. ACM is implemented for optimization of transmission parameters for each individual user depending on the path conditions. Even backwards-compatible modes are used for DVB-S Set-Top-Boxes (STB) for continuous work during the transitional period.

There are three concepts in the DVB-S2 standard: best transmission performance, total flexibility and reasonable receiver complexity. Using the recent techniques in channel coding and modulation, DVB-S2 can achieve the best performance complexity trade-off, 30 % gain capacity over DVB-S. Due to its flexibility, DVB-S2 can cope with any existing satellite transponder characteristics with a large variety of spectrum efficiency and associated C/N requirements. Being not limited to MPEG-2 video and audio coding, it is designed to handle a variety of advanced audio-video formats. It can accommodate any input stream format, single and multiple Transport Streams, continuous bit-streams, ACM and IP packets.

4.3.2.1 Modulation

DVB-S2 is using an advanced FEC as the key subsystem for achieving excellent performance, in the presence of high levels of noise and interference. Low Density Parity Check (LDPC) is selected as a coding technique, and offers a minimum distance from Shannon limit on the linear AWGN channel. QPSK in combination with some additional codes have shown that the signal can be retrieved even when the level is below the noise floor. Avoiding the error floors at low Bit Error Rates (BER) is done by concatenated Bose-Chaudhuri-Hocquenghem (BCH) outer codes.

Four different modulations modes are used for the transmitted payload, as shown in figure 4.4. QPSK and 8PSK are used in broadcasting applications due to its constant envelopment and usage in non-linear satellite transponders driven near saturation. 16APSK and 32APSK which mainly are used at professional applications can be used for broadcasting, but needs a higher level of available C/N and adoption of advanced pre-distortion methods. The spectrum efficiency is much greater, whilst the power-efficient modes are not. By placing the constellations points on circles it optimizes the constellation to operate over a non-linear transponder, even though their performance on a linear channel is comparable with performances of both 16QAM and 32QAM.

Spectrum efficiencies from 0.5 to 4.5 bit/symbol are available by selecting specific modulation and code rates, and can be chosen dependent on the capabilities and restrictions of the satellite transponder used [7]. To determine the spectrum shapes DVB-S2 can choose from three “roll-off-factors”, 0.35 as in DVB-S or 0.25 and 0.20 for tighter bandwidth restrictions.

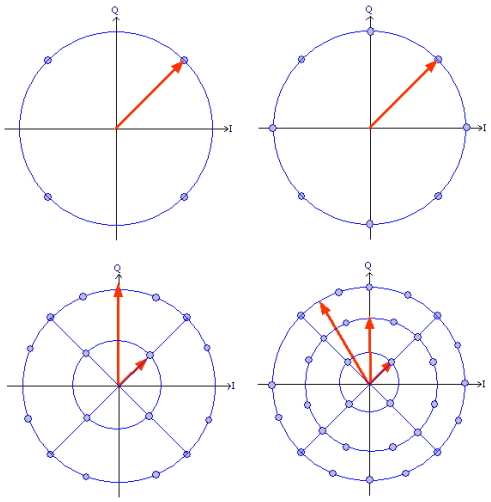

Figure 4.4 - Four possible modulation constellations.

From left to right and up to down: QPSK, 8PSK, 16APSK and 32APSK.

DVB-S already installed receivers are giving some major problems for many broadcaster, especially where the receivers are subsidiary and for free-to-air public service. In that case, DVB receivers need to be backward compatible in order to allow receivers to continue operating while still providing additional capacity and services to new, advanced receivers. After the migration process when most users have migrated to DVB-S2, the transmitted signal can be modified to a non-backward compatible mode, exploiting the full potential of DVB-S2. Backwards compatibility is implemented by high priority and low priority transport streams. They are combined at modulation symbol level on a non-uniform 8PSK constellation. The low priority signal is coded with BCH and LDPC. The high priority signal is defined by QPSK modulation, where the single bit from the DVB-S2 LDPC encoder sets an additional rotation before transmission. The result of having quasi-constant envelopment makes it possible to transmit on a single transponder driven near saturation.

4.3.2.2 ACM

ACM is used in wireless communication to decide the matching of modulation, coding, signal- and protocol-parameters, especially in radio links. That includes interference caused by signals coming from other transmitters, the sensitivity of the receiver and the available transmitter power margin. Considering interference distribution, ACM uses the entire C/I range. The interference together with other channels, noise and background effects have a direct influence in the quality of the received signal. In atmospheric conditions, ACM maximizes instantaneous data-rate as a function of time versus location. Depending on the location and modulation, such as 8PSK, QPSK, 16APSK or 32APSK, the system can on its own select which optimum couple is most

convenient. ACM render it possible for a return channel to be available from each receiving site to the transmit site, making it possible to modify the coding rate and modulation scheme for every single frame according to the measured channel conditions where the frame must be received. The return channel dynamically reports the receiving conditions at each receiving site. All depends on the weather. Should the probability of clear weather be 95 %, the C/No-ratio will vary between 84.3 and 88.1 dBHz. These values give information on which modulation and coding will be used, such as 16APSK 3/4 or 16APSK 5/6. These coding and modulations are ranged from 8PSK 3/4 to 16APSK 5/6. Compared with DVB-S, efficiency is improved with 130 % with ACM in the DVB-S2 system [8].

4.3.2.3 VCM

VCM transmits different services on the same carrier using their own modulations scheme and coding rate. VCM is stronger when protection levels of other services are not needed, for example in case of fade rain it is acceptable to lose a secondary channel. The same principle can be used when different services are intended for different stations with different average receiving conditions. If the probability of clear weather is 99.85 %, the Co/No-ratio will be between 6.0 and 10.6 dB. These coding and modulations are ranged from QPSK 5/6 to 16APSK 2/3. Compared with DVB-S, efficiency is improved by 65.7 % with VCM in DVB-S2 system [8].

4.3.2.4 CCM

In CCM all frames are modulated and coded with fixed parameters and it is the simplest mode in DVB-S2. LDPC code is used as inner error correction code, compared to DVB-S which uses Reed Solomon. In comparison with DVB-S, the efficiency is improved by 29 % with CCM in a DVB-S2 system [8].

4.3.2.5 Performance of the DVB-S2 system

The system has the characteristics to operate at C/N-ratios from -2.4 dB (using QPSK 1/4) to 16 dB (using 32APSK), depending on the selected code rate and modulation. The distance from the Shannon limit is 0.7 dB to 1.2 dB. Under the same transmission conditions as for DVB-S, DVB-S2 has 2-2.5 dB more robust reception for the same spectrum. A DVB-S2 system can be used in both “single-carrier-per-transponder” and “multi-carriers-per-transponder” FDM configurations.

4.3.3 DVB-Cable

After a year, in 1994, specifications for digital cable networks system were proposed. It uses the more sophisticated modulation technique QAM to squeeze in more information at a specified bandwidth.

The carriers can be modulated according to the following constellations:

- 16-QAM
- 32-QAM
- 64-QAM
- 128-QAM
- 256-QAM

In Sweden the 16-QAM and 64-QAM modulation forms are mostly used. None or very few receivers are equipped with modulators that can decode 128- or 256-QAM.

When comparing different channels, transportation of information in a cable is least prone to addition of errors. Noise, damping and reflections are the main problem areas when transmitting over a cable network. The Viterbi algorithm, used in for example DVB-T and DVB-S, is therefore excluded from the DVB-C standard, see figure 4.5. The use of randomization, Reed-Solomon encoding, and interleaving fulfills the need for protection of the data stream. Protection of burst errors is achieved by byte interleaving. Differential encoding of the modulation constellations is used to get rotational invariant reception of the phase differences used in QAM.

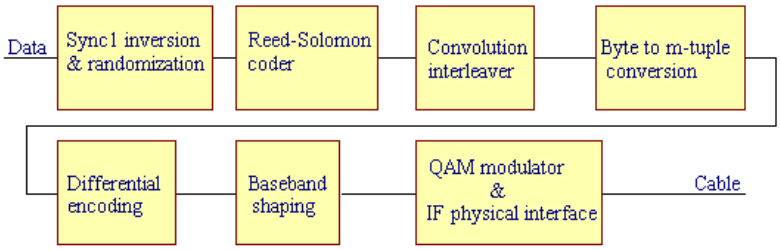

Figure 4.5 - DVB-C functional system block diagram

4.3.4 DVB-Terrestrial

In 1998 the terrestrial system was standardized. Due to harder environment, like multipath propagation and different noise characteristics, the terrestrial system needed to be more complex. The use of the existing VHF and UHF spectrum allocation used by the old analogue system places constraints on bandwidth and protection against Co-Channel Interference (CCI) and Adjacent Channel Interference (ACI) with the existing analogue transmissions of PAL/SECAM/NTSC. To cope with multipath propagation, COFDM is used with a guard interval, chosen such that the interference from multiple terrestrial signal paths are of less concern. The guard interval can be flexible chosen to allow for different network topologies and frequency efficiency. For a functional block diagram, see figure 4.6.

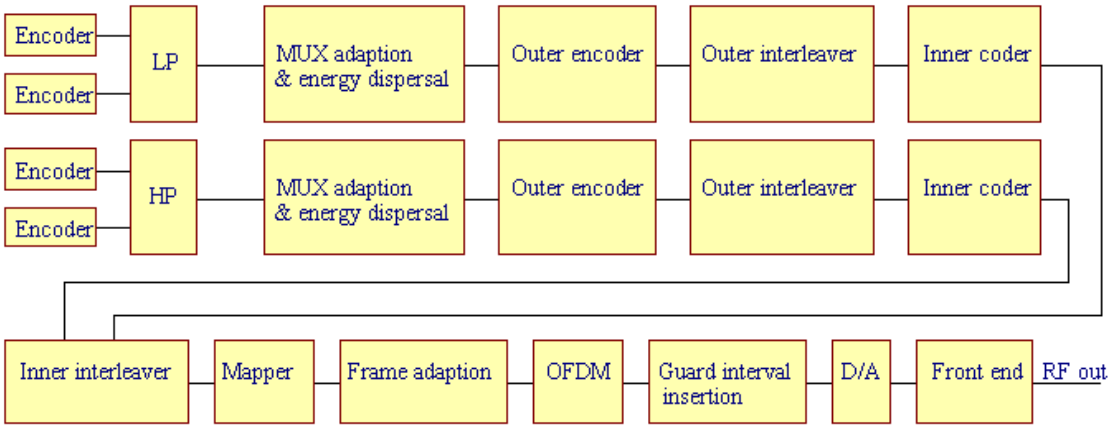

Figure 4.6 - DVB-T functional block diagram

The transmission system has two modes of operation, either the 2K mode or the 8K. The two modes actually specify the FFT length of the modulator, and thus the number of carriers used by COFDM. The 2K mode uses 1705 carriers and the 8K mode 6817 carriers. For synchronization purposes some carrier positions always contain pilot carriers. Other pilot carriers are also present but are scattered in frequency and time in a predefined way. Some carriers are Transmission Parameter Signaling (TPS) carriers. The TPS carriers are always modulated by differential 2-PSK, and these convey information on:

- Modulation used, including the α (spacing of the different QAM "points") value of the QAM constellation pattern
- Hierarchy information
- Guard interval
- Inner code rates
- 2K or 8K transmission mode
- Frame number in super-frame (one super-frame contains $4 \cdot 68$ COFDM frames)
- Cell identification

Several different modulation forms can be chosen for the video transport, trading between bit rate and ruggedness.

Carriers can be modulated in the following constellations:

- QPSK
- 16-QAM ($\alpha = 1$), non-hierarchical and hierarchical
- 64-QAM($\alpha = 1$), non-hierarchical and hierarchical
- Non-uniform 16-QAM ($\alpha = 2, 4$)
- Non-uniform 64-QAM ($\alpha = 2, 4$)

α is the minimum distance separating two constellation points carrying different HP-bit values divided by the minimum distance separating any two constellation points.
With the use of 16-QAM or 64-QAM additional information can be buried in QPSK like fashion, shown in figure 4.7.

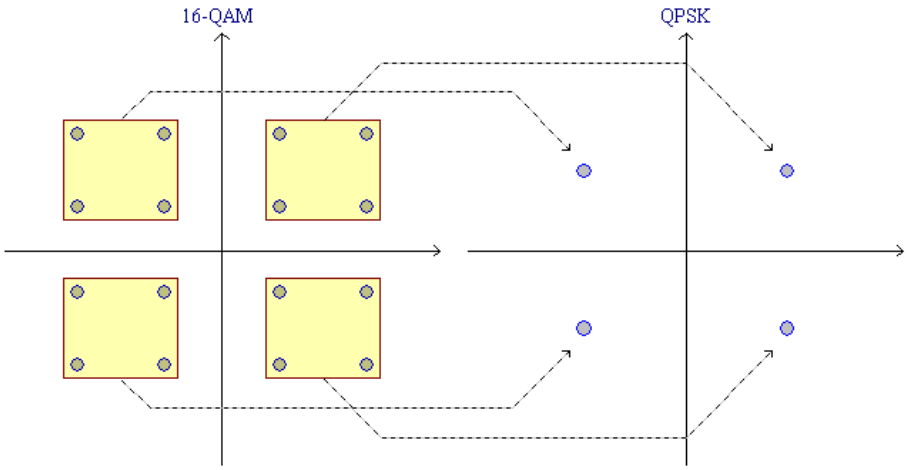

Figure 4.7- QPSK information buried in QAM

Two MPEG streams can be sent simultaneously, one low- and one high priority stream. The high priority stream (low bit rate) is mapped as QPSK on the low priority stream modulated as either 16-QAM or 64-QAM. The high priority stream is thus more rugged against noisy environments and the broadcaster can choose to send the same program with both a high and a low bit rate. A receiver in very noisy environments, which has problem receiving the low priority stream, allows switching to the high priority stream. The drawback of this implementation is found on the receiver end. The receiver must adapt to the different transmissions by the broadcaster. The adaption to new coding and mapping when switching between one layer and another takes some time to complete and thus instantaneous switching cannot be done. Usually video and sound freezes a short amount of time (around 0.5s) before lock on the new data stream have been accomplished.

4.3.4.1 Comparisons between ATSC-T and DVB-T in Taiwan

The standard for analog television in Taiwan has been NTSC. They originally planned to directly adapt to the new ATSC-T standard but when Sinclair Broadcasting demonstrated COFDM (DVB-T) vs. 8-VSB (ATSC) reception in USA 1999, this raised deep concerns about the qualities of the ATSC system. In-door, out-door and mobile reception was tested in Taiwan and in almost all cases the DVB-T system outperformed ATSC-T. After the test trials, the Taiwanese Directorate General of Telecommunications proposed the DVB-T as the new DTV system, and this was adopted by all terrestrial broadcasters in 2001. The main reason for the excellent reception of DVB-T originates from the fact that it uses OFDM and resists multipath propagation [9].

4.3.5 DVB-Handheld

DVB-H is essentially the same as DVB-T, but a 4K transmission mode is added. The 4K mode offers a trade-off between transmission cell size and mobile reception capabilities. DVB-H uses the exceptional features of the DVB-T standard, as the possibility to receive broadcasting services with portable devices and even in cars. The standard was published by ETSI in November 2004.

One of the biggest problems with handhelds is the limited available power. Low power consumption is therefore necessary to obtain reasonable usage and standby cycles. Another fact which makes transmission to handhelds a very demanding task is the high mobility of the handheld. Access to services must be possible whether located indoor, outdoor or in a moving vehicle. The high mobility, small antenna and interference from for example GSM mobile radio signals transmitted and received from within the same device, places hard constraints on the transmission/receiver. The close affinity between DVB-T and DVB-H makes re-use of the same transmission equipment an attractive possibility.

The power-saving technique used is called time slicing. The algorithm is based on time-multiplexed transmission of different services, which can be used to turn off the front end in time slots where no relevant data are sent, see figure 4.8. The power saving may be more than 90 %, compared with conventional DVB-T front ends [10]. Another advantage of time-slicing is the ability to seamlessly move between different adjacent radio-cells, which can be done in the power-saving period.

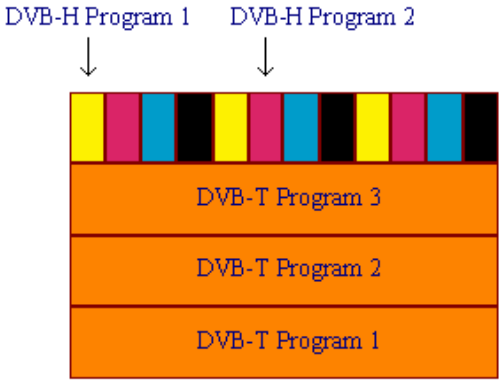

Figure 4.8 - DVB-H time slicing compared to DVB-T transmissions

An enhanced error-protection scheme, Multi-Protocol Encapsulation – Forward Error Correction (MPE-FEC), is used for reliable transmission in poor reception conditions. To be backwards compatible with DVB-T (for transmission purposes) time slicing and MPE-FEC is put on the protocol layer above the DVB transport stream. The system is based on the Internet Protocol (IP). The IP data are embedded in the MPEG-2 transport stream used as the base layer by means of the Multi-Protocol Encapsulation (MPE). This makes effortless migration to other IP-based networks.

5 Satellite reception

To use the available frequency spectrum in satellite transmissions in a more effective way, several satellites transmit at the same frequencies. This places constraints on the reception tool, the aerial, on earth. The aerial must have a high directivity to receive just the right signal. This is achieved by using a parabolic reflector, often called dish, concentrating the received signal to one point. To properly retrieve the signal in the focal point a Low Noise Block down-converter (LNB) is used [2].

Satellites transmit at fairly high frequencies (in the multiple gigahertz regions). When receiving radio signals at this high frequencies it must be done out-doors as the signal is easily damped out when sent through different materials. Coaxial cables are used for transportation from the dish to the set-top-box. Because of the high attenuation of gigahertz frequencies in coaxial cables the received signal must be down-converted to a lower Intermediate Frequency (IF). This also has the effect that the Radio Frequency (RF) front end of the STB is easier to construct. The LNB serves multiple purposes:

- Collect the signal at the focal point
- Amplify the received signal
- Down-convert the received spectrum to lower frequencies

The satellite transponder can transmit at two different frequency bands with either horizontal or vertical polarization of the microwaves. This means that one LNB can receive four different signals placed in the same position. In the early beginning of satellite transmissions one LNB could just receive one band and polarization switching had to be done with an outer mechanical or electrical switch. Nowadays there exist a so called universal LNB that has all these features built in. Switching between the different modes can easily be done with the universal LNB by varying a voltage applied on the same coaxial cable that transports the content to the set-top-box. The different frequency bands and the polarization are switched according to table 5.1.

Voltage applied	13V	18V	13V + 22kHz	18V + 22kHz
Low band, vertical. pol.	X			
Low band, horizontal pol.		X		
High band, vertical pol.			X	
High Band, horizontal pol.				X

Table 5.1 - LNB switch modes

6 Receiver functions

The Radio Frequency (RF) converted to Intermediate Frequency (IF) by the LNB must be processed in some way to decode the channel adapted signal. In most receiver systems this is done by a front-end tuner converting the IF to I- and Q-baseband channels. The I- and Q-channels are then decoded in the demodulator and converted to the transport stream known by the MPEG video processor. In figure 6.1, a general overview of a receiver is presented.

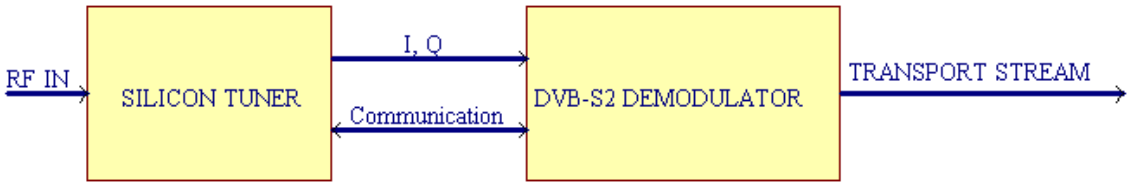

Figure 6.1 - General receiver overview

6.1 Tuner

The main purpose of the tuner circuit is to lock on a frequency of interest and transmit I- and Q-channels to the demodulator. The tuner has a LNA with Automatic Gain Control (AGC) to amplify the weak signal to a level suitable to the mixers and output circuitry. The tuner communicates with the demodulator and outer world, often through an I^2C interface. Through the interface common settings such as frequency band, gain, filtering or lock detect can be sent or read.

6.2 Demodulator

To cope with noise, signal strength loss and other channel artifacts the transmitter added lots of coding to the data stream. The task of the demodulator is to decode the data stream and forward the MPEG transport stream to the MPEG video and applications processor. The LDPC decoder used in DVB-S2 is a highly complex design taking up lots of area and computational effort which can be seen in the current consumption.

6.3 LNB Driver

The LNB receives the signal that is gathered with the parabola liked antenna and focused into the LNB. Inside the LNB the converter takes the incoming signal with high frequency, approximately 12 GHz, and converts it to about 1.5 GHz, called the first signal conversion. The signal is carried to the receiver where the signal is improved by a low noise amplifier. The other purpose of the LNB is to change polarization type, either horizontal or vertical, or change operative band by command signals controlled by the receiver. Other ways to steer the LBN is by use of the bidirectional DiSEqC standard which is a communication protocol for frequency and motor position adjustment. The DiSEqC signal is a pulse width modulated 22 kHz signal with amplitude between 0.3 and 0.6V aligned to the supply voltage. The LNB driver is a component or system that handles the communication and powering of the LNB.

7 Available chipsets for DVB-S2 reception

To make a cost efficient and physically small design the needs for integrated circuits apply. In this chapter the available chipsets for DVB-S2 reception (spring 2007) is presented in short form.

7.1 ST STB6100

The STB6100 is an 8PSK/QPSK direct conversion tuner Integrated Circuit (IC) which is a highly integrated, low-cost tuner for DVB-S2 broadcasting satellite applications. The device has an LNA, down-converting mixers, gain control, on-chip VCO and a low noise Phase Locked Loop (PLL). The tuner is controlled by two interfacing wires designed to minimize external Bill Of Material (BOM) to reduce manufacturing costs and simplify board layout. The reduced number of components gives system stability and reliability. The capacity is increased with 30% by the DVB-S2 standard and renders possible high data rate applications such as HDTV and broadband Internet.

7.1.1 Features

- Direct conversion
- Input range 950 to 2150 MHz
- 2-wire I^2C serial interface
- Low power consumption
- Differential I/Q outputs
- 8PSK/QPSK support

7.2 ST STB0899

The STB0899 is an advanced demodulator which enables set-top boxes to produce base-band DVB-S2 signals into digital video transport stream data. The demodulator supports QPSK in DIRECTV and DVB-S up to 45 Msymbols/s in legacy transmission, plus 8PSK in DVB-S2 transmissions (up to 30 Msymbols/s). The demodulator is using the modulation technique 8PSK with LDPC/BHC and Reed-Solomon/Viterbi decoding. The FEC has integrated BER and Package Error Rate (PER) computation to evaluate reception quality. It accepts both baseband differentials I and Q signals using AD-converters.

7.2.1 Features

- Compatible with direct conversion tuners
- QPSK, 8PSK, 16 and 32 APSK
- Legacy DVB-S and DVB-S2
- I^2C serial bus interface
- Multi-tap equalizer for RF reflection removal
- Power-saving features
- DiSEqC 2.0 22 kHz to 100 kHz interface

7.3 Conexant CX24118A

The CX24118A is digital satellite tuner RF IC which is used for high-volume digital video, audio and data receiving. The device increases phase noise performance, has low implementation loss and is also using the modulation techniques required for DVB-S2.

7.3.1 Features

- Single-chip RF-to-baseband satellite receiver
- Zero-IF architecture
- Variable baseband filters
- Low power consumption
- Auto-tuning machine for elimination of software calibration
- Lead-free package

7.4 Conexant CX24116

The CX24116 is used both for demodulation and FEC decoding. The demodulator is using the modulation technique 8PSK with LDPC/BHC forward error decoding. It can demodulate and decode transmitted signals with both the new DVB-S2 and old DVB-S specification. It automatically searches and acquires the carrier within a 10MHz range during initial acquisition and performs a smart search to reacquire under fade condition. The CX24116 has integrated Signal-to-Noise Ratio (SNR) and BER monitors for performance measurements.

7.4.1 Features

- 8PSK/H-8PSK/QPSK/BPSK
- Internal microcontroller
- DiSEqC 2.x compliant
- DVB-S/DSS backward compatible
- Power-down mode
- 1.2-V core voltage, 3.3-V I/O voltage

7.5 Intel® CE 5038

All Intel front-end chips originally come from Zarlink Semiconductor Limited, acquired by Intel in 1995. Since this is a single tuner chip, it must be combined with some kind of DVB-S2 demodulator chip for correct function.

7.5.1 Features

- Supports 8PSK and 16QAM modulations by high signal-to-noise and inter-modulation performance
- Low power modes for saving energy
- RF loop-through
- Guaranteed maximum of 2 degrees integrated phase jitter over the full operational temperature range
- Automatic and manual tuner modes
- Consumes less than 1.5 W
- Excellent immunity for adjacent channel interference

7.6 Broadcom BCM4501

This is a fully integrated single-chip solution for DVB-S and S2 reception. The single-chip solution reduces the external component count and increases performance.

7.6.1 Features

- Single-chip solution
- I^2C interface
- Dual tuner and demodulator sections
- Supports QPSK and 8PSK modulation
- Demodulators DVB-S and S2 compliant
- 208-pin MQFP package

7.7 Selected chipset

The ST microelectronics companion chip solution (STB0899 [17], STB6100 [18]) was selected with the aid of our supervisor. The availability, price and contacts with ST made the choice easy. Interfacing the chips is done with the I^2C communication protocol, with the demodulator chip forwarding the commands to the tuner chip. This way the communication with the tuner chip can be turned off when not used thus reducing the risk of interference. There are in addition several registers available for BER, Modulation Error Ratio (MER) and Carrier-to-Noise Ratio (CNR) estimates, making tuning and reception quality evaluation of new satellites easy.

8 Circuit design considerations

Before the design start there are several considerations that must be taken into account. Are there RF sections where RF design methods must be addressed?

The following chapters present issues to consider when working with RF. The main issues are:

- EMC- Electromagnetic Compliance

  EMC refers to the ability of a product to coexist in its intended electromagnetic environment without causing or suffering functional degradation or damage.

- EMI – Electromagnetic Interference

  EMI is the process where electromagnetic energy is transferred from one electronic device to another in a non wanted manner.

Unintentional radiation is regulated by international EMC requirements and the PCB with components must fulfill these requirements for product certification. To avoid redesign of the PCB, EMC requirements must be thought of under the whole design phase.

8.1 RF component selection

When dealing with RF design there are numerous new parameters to take into account. The nearly ideal passive component behavior at DC will transform to new behavior at high frequencies. For example, lead length inductance, which is not recognized when dealing with DC or low frequencies will greatly alter a capacitors behavior. Every component contains hidden parasitic elements such as inductance and capacitance. In figure 8.1 the RF behavior, in terms of ideal circuit elements, of some of the most used passive components are listed.

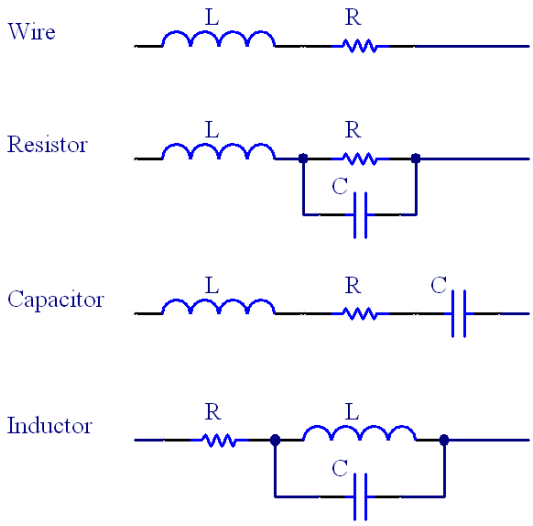

Figure 8.1 - Component RF characteristics

To successfully complete a RF design without having to redesign for EMC compliance one must have these component behaviors in mind under the whole design process.

8.1.1 Capacitors

Capacitance is defined as the measure of the amount of electrical charge stored for a given electric potential.

$$C = \frac{Q}{V} \tag{8.1}$$

Negative and positive charges attract each other. Two metal plates, separated with an insulating material (dielectric), connected in a circuit, will accumulate charge as a result of charge attraction. This will result in a capacitance between these metal plates, as defined in equation 8.1. The closer the metal plates get to each other more and more capacitance will appear. This will also apply if the area of the plates is enlarged. As such capacitance will appear between every conductor where charges freely can move. Even if there is just a tiny capacitance between for example two leads of an inductor this will influence the behavior at high frequencies. As seen in equation 8.2 the reactance of the capacitor will affect the circuit more and more as frequency rise.

$$X_c = \frac{1}{\omega \cdot C} \tag{8.2}$$

Even if the capacitance is very low it can affect circuit behavior if the frequency is high enough. Designing RF circuits including capacitors is a more delicate art than choosing capacitors for DC circuits. Different dielectric materials and capacitor sizes must be chosen for correct circuit behavior. In a forthcoming chapter the materials used for the capacitors in this design is presented, listed with their respective characteristics. Several characteristics within a capacitor are temperature dependent, such as capacitance, ESR (Equivalent Series Resistance) and leakage current (sometimes called insulation resistance). To describe losses in a capacitor the dielectric loss $\tan\delta$ is often listed.

$$\tan\delta = \frac{ESR}{X_c} \tag{8.3}$$

In the capacitor body leads and electrodes inductance is found. As the inductance and capacitance are in series a series resonance occur at a frequency where the two reactances are equal. At this frequency the impedance of the capacitor is equal to ESR. As seen in figure 8.2 the capacitor only works as a capacitor up to the series resonance frequency. This means that capacitors must be chosen carefully for the application they are meant to be in.

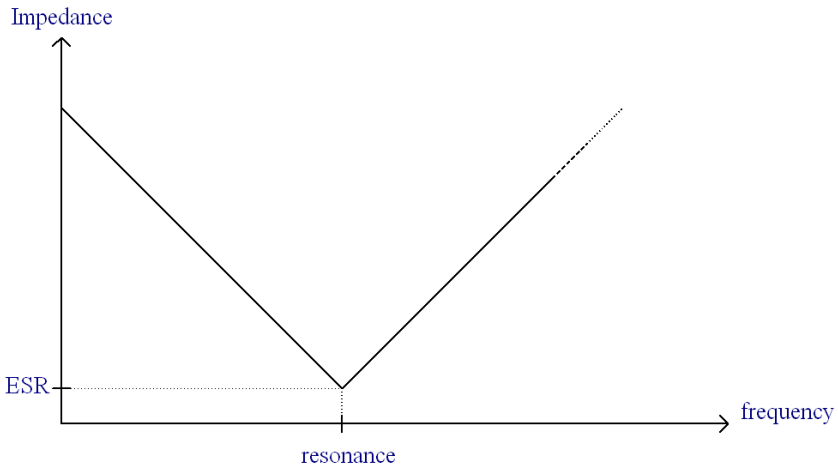

Figure 8.2 - Capacitor behavior as frequency rise

As the size of the capacitors shrink the lead inductance is lowered so therefore smaller surface mount capacitors are useful at higher frequencies then bigger. This is also one of the reasons that surface mount components are used.

8.1.1.1 Dielectrics

There are quite a few different dielectrics that can be used for capacitor design. There are tradeoffs between for example capacitance per area, loss and stability. The capacitors used in the design in this report use ceramic and electrolytic dielectrics.

Electrolytic capacitors have large capacitance per area ratio. They are therefore used where the need for a big reservoir and small footprint are the main objectives. The main drawbacks are low stability and large leakage current. Ceramic capacitors often have better characteristics but can't be made with as large capacitance values.

Ceramic capacitors are divided into three different classes [13]:

Class 1 materials have low dielectric constant but are highly stable and have very low losses at high frequencies. Because of the low dielectric constant these capacitors cannot be made with high capacitance. They are often manufactured with capacitance values in the range 0.47 pF (single layer) – 0.1uF (multi layer). Capacitors of class 1 used in this design are of dielectric type NP0.

Class 2 materials have higher dielectric constant but have nonlinear temperature, frequency and voltage dependencies. They are often manufactured with capacitance values in the range 10 pF (single layer) – 10uF (multi layer). Capacitors of class 2 used in this design are of dielectric type X7R and X5R. For comparison NPO has a dielectric constant ε_r of 60 and X7R a constant of 1500. Class 2 capacitors are used as output capacitors for the buck converter later described in this report.

Class 3 materials have almost the same or slightly poorer specifications as class 2 materials. The voltage ratings are rather low but as the dielectric constant of these materials are in the range 10000 – 50000 it is possible to make small capacitors with large capacitance. Class 3 dielectrics are not used in this report.

8.1.1.2 Capacitor ripple current

Ripple current capability for capacitors has it origin in the losses accompanied with charge and recharge. The charge and recharge currents dissipate power in the ESR of the capacitor, which in turn generates heat and temperature rise in the capacitor. High temperatures reduce the capacitor reliability, and could lead to failure. ESR decreases with frequency thus increasing the current capability of the capacitor. The reliability of capacitors depends mostly on applied voltage and core temperature. For good reliability it is therefore mandatory keeping the capacitor voltage and temperature down [11].

8.1.2 Inductors

Whenever a current is conveyed in a conductor a proportional magnetic field forms around the conductor. A current change will then create a change in the magnetic field that, in turn, will try to oppose the current change by introducing an electromotive force in the inductor. Inductance is a measure that tells us how much the current change will be opposed by the inductor. To increase the inductance, materials that make the magnetic field coupling more confined to the windings are introduced. This approach has the drawback that the material has a certain point when it can't handle more magnetic flux (in a linear way) and the material goes into saturation. At the saturation point and beyond the inductor changes it's approximately linear relationship in a highly non linear manner which in most applications is a not wanted characteristic. Therefore the current, that creates the magnetic flux in the core material, must be held below the saturation point specified by the manufacturer.

Most of the inductors used in this design are situated in connection with rather low frequency, high current circuits, such as DC/DC converters. Therefore the capacitance that occurs between the windings of the inductor is of less importance then if it would be situated in a complex RF environment. The parameters that are of great importance are the losses in the core and leads, and the saturation current of the core material.

Small inductors may be etched right onto the printed circuit board. In prototypes as in this report this can be rather dumb as the designer can have been making a mistake calculating the inductor, or some properties not fully known at the design phase may alter the behavior of the circuit. Therefore the only RF inductor included in this design is made up of a physical component.
EMI filters are also placed on the input power lines to suppress RF and noise interference picked up on the lines from the regulators to the circuit board.

8.1.3 Wires

In DC circuits the primary wire characteristic is resistance. At higher frequencies other characteristics will play an important role. Parasitic elements, such as inductance and capacitance, can in special cases interact with other components and self resonance can occur. If the PCB trace that this resonance phenomenon occurs in is long enough, it can form an efficient

radiating antenna. Even if active components aren't driving the trace into resonance, incoming radiation may do so, thus injecting unwanted RF energy into components. The physical dimensions of the traces are also of great concern when the wavelength becomes short in relation to the trace length. Analysis with lumped circuit parameters cannot be used anymore. The trace assumes the characteristic of a transmission line and for optimal signal transfer transmission lines must be terminated in their characteristic impedance. The primary concern is to preserve signal integrity but it also helps to control EMI [4].

8.2 RF energy developed in PCB

One of the main problems in PCB design is the unwanted RF energy developed by both passive and active digital components [5]. To understand this phenomenon it is required to have some basic knowledge of Maxwell's equations. Based on the physics of electromagnetics they describe the relationship of electric and magnetic fields. These equations express the root cause for how EMI is developed, i.e. time varying currents. Static charge distributions create static electric fields, but not magnetic fields. Constant current sources create magnetic fields, but not electric fields. Time varying currents produce both electric and magnetic fields. For deeper insight, Maxwell's equations are related to Ohm's law. In time domain Ohm's law is expressed as

$$V = I \cdot R \tag{8.4}$$

where V is voltage, I is current and R is resistance. Switching to the frequency domain transforms the equation to

$$V_{rf} = I_{rf} \cdot Z \tag{8.5}$$

where Z is impedance (R+jX) and subscript *rf* refers to radio frequency. If RF current is present in a PCB trace with some impedance value, an RF voltage is created proportional to the RF current present. R is substituted by Z, a quantity containing both resistance (DC-real component) and reactance (AC-complex component). The quantity is the impedance in both time and frequency domains, which is resistance to the flow of energy. There are several different ways to describe impedance. For a wire or a trace in PCB, the impedance can be expressed as

$$Z = R + jX_L + \frac{1}{jX_C} = R + j\omega L + \frac{1}{j\omega C} \tag{8.6}$$

where $X_L = \omega L$, $X_C = \frac{1}{(\omega C)}$ and $\omega = 2\pi f$. The magnitude change of impedance versus frequency in equation 8.7 must be taken in consideration, when a component with known inductance, capacitance and resistance is applied.

$$|\mathrm{Z}| = \sqrt{R^2 + jX^2} = \sqrt{R^2 + j(X_L - X_C)^2} \tag{8.7}$$

For higher frequencies the inductive reactance exceeds R, forcing the current to take the path of least impedance. The path for low frequencies is resistive and for higher the path of least reactance is dominant. The correct current path for RF currents is always through the smallest impedance. For the reason that most circuits operate at frequencies higher than a few kHz, the

idea that current takes the path of smallest amount of resistance, provides an wrong theory of how current flow occurs within a transmission line structure.

Each PCB trace has some impedance and that is the reason why RF energy is developed inside the PCB. A connection between silicon dies and mounting pads also develop RF energy. Traces on a PCB can be highly inductive, especially traces that are electrically long. Traces which don't return fast edge events to the source before the next edge-trigged event are called electrically long. In the frequency domain this occurs when the length exceed approximately λ/10 of the frequency present inside the trace.

A circuit must be closed in order to function otherwise the RF current will take the path through any accessible impedance and emit electromagnetic energy. Both a signal- and return-path is needed, otherwise the signal would never travel through the trace from source to load. The absence of a path between load and source would force RF current to return through an alternative return path causing EMI to occur and develop RF energy, which disturbs other adjacent components.

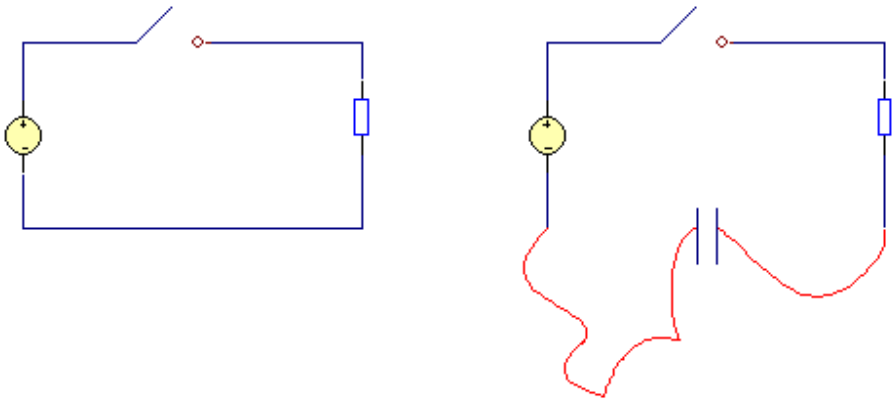

Figure 8.3 -Closed and open circuitry

In figure 8.3, the left picture shows the path direct for both signal and return current, where total impedance is small. In the right picture, the return path is non-existing. Since current needs to obey Ampere's law, the RF energy will return through the lowest impedance path present. When the impedance of the return path is greater than 377 ohms, free space becomes the return channel and is seen as radiated EMI.

8.2.1 Magnetic flux and cancellation

Why is the Ampere's law so important in PCB design?

It is because a magnetic field is created around the transmission line whenever there is a closed loop present and current is flowing freely from one point to another. These fields are radiated through free space as unwanted electromagnetic energy and are the main source of electromagnetic disturbance. To prevent RF energy inside the PBC, the concept of flux minimization needs to be considered. By bringing the RF return path adjacent and parallel to its source trace, magnetic flux lines in the return path (clockwise field), relative to the source path

(counterclockwise) will be in the opposite direction. Cancelation of magnetic flux will be achieved by combining the clockwise magnetic field caused by the forward propagating current with the counterclockwise magnetic field caused by the return current. The trace forming a small loop or a turn will cancel out the magnetic flux if the traces are positioned close to each other. Unwanted magnetic flux between the source and the return path will be cancelled or minimized. Regardless how great the design is, magnetic and electric fields will always be present. There are several different techniques for flux minimization. Some techniques [5] are listed below:

- Proper PCB layer stack up assignment and impedance control
- Routing a clock trace adjacent to a RF return path
- Reducing RF currents by decreasing RF voltage
- Reducing ground noise voltage in the power and ground plane structure
- Proper termination of clock and signal traces to prevent ringing, over- and undershoot

8.2.2 Common-mode and differential-mode currents

Common mode (CM) and differential mode (DM) currents exist in every circuit. These currents determine how much of the RF energy that propagates. The differential mode signals are carriers of data or signal of information. The common mode current is just a side effect of differential mode currents and is the EMC compliance problem cause. Common-mode signals can produce great levels of radiated electric fields, despite their smaller size compared to differential mode currents. Even small sizes of wires can produce significant radiated emission levels. The troubling part is that small amounts of common mode current will produce the same amounts of RF energy as a larger amount of differential mode current because common mode currents do not cancel out magnetic flux.

The origin of common and differential mode current comes from erroneous grounding and current loops. Two sources aligned in series with each other providing power for example to an amplifier makes it possible for both currents to exist, shown in figure 8.4.

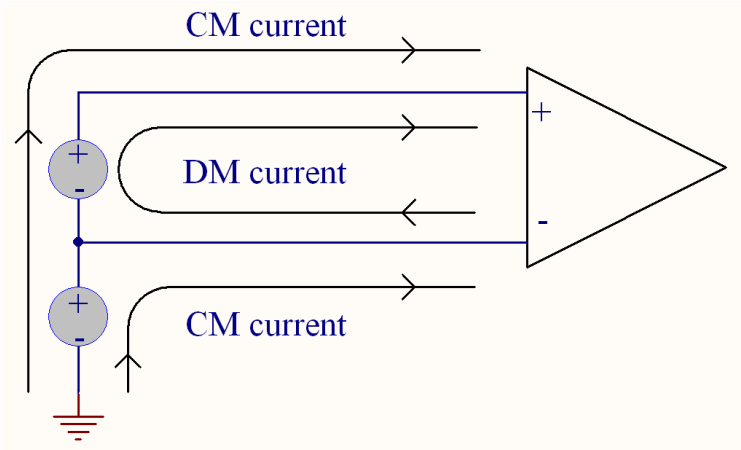

Figure 8.4 - Common mode and differential mode currents

Usually there are some small resistors and ground inside the amplifier where the current flow through. In picture 8.4, common mode currents propagate in two separate directions, in the upper- and lower-side of the amplifier. The current propagating in the upper and the lower side of the amplifier is called differential mode current. Differential mode current is always present if the path of the current is forming a loop. Common mode current propagates in a one-way direction. The common mode current is created by poor differential mode cancelation. The best way to reduce common mode current is proper grounding and to avoid having too many loops.

Another important aspect that needs consideration is the differential mode radiation caused by the flow of RF current loops with in a system structure. In PCBs, emission sources are created from currents flowing between components and in the power and 0V planes. These sources can be seen as small loop antenna carrying interference RF currents. A small loop is defined as one whose dimension is smaller than a quarter wavelengths ($\lambda/4$) at a particular frequency.

Common mode radiation comes from unintentional voltage drops in circuits which cause some ground parts to rise above the real ground potential. Radiation of common mode potential comes from cables connected to the affected ground system where they act as an antenna. With a constant current and antenna length, the electric field is proportional to the frequency. Common mode radiation is a more difficult issues to solve, unlike to differential mode radiation which is easy to reduce using proper design techniques. The common path impedance for common mode current is the only variable available to the designer. Elimination of common mode radiation is done forcing the common mode fields to approach zero, which is made by using a sensible grounding scheme.

8.2.3 Input power consumption

One major contribution to noise generation on the board is power supply transition currents to a transistor gate, which is either conveyed by a power- or ground-plane. The ground reference refers to the source that is at ground potential relative to the power source. It is usually referred to as 0V reference or the power return plane, image plane or ground plane. The main source of differential currents and RF energy are transition currents, which is causing an EMI spectral profile to exist if the transmission time is short or edge rate is fast. The power supply transition current demands during component switching can be quite large. These currents have no relationship with the same current needed to establish a “1” or “0” signal state in digital logic. The inrush of surge current is created due to partial conduction overlap of output drive transistors for TTL and some CMOS technologies. The power bus is virtually shorted to ground through two partially saturated transistors during the crossover time from logic high to logic low.

Manufacturers provide Schottky barrier diodes to prevent the output transistors from going into saturation in order to avoid crossover conduction currents. There are other techniques for fabrication of the component that includes “output edge rate control”. This is done by replacing one big output transistor with several smaller ones. Only when voltage swing is between logic high and logic low RF voltages and capacitive crosstalk can exists. The current that is needed to change logic state from low to high and opposite is larger than the quiescent current and it can be estimated to be

$$I_t = C\frac{dV}{dt} \tag{8.8}$$

where C is the sum of distributed capacitance of the load and trace capacitance to ground. Single-sided boards have 0.1 to 0.3 pF/cm and multilayer boards have values from 0.3 to 2pF/cm [5]. The peak current combines nonsymmetrical current usage with the power supply transition current.

Other problems related to radiated EMI emissions is the difference between manufacturers' active components. Differences do exist in the manufacturing process even though digital devices are form, fit and function compatible. Not every manufacturers design the components in the same way, since they don't assume the same problems from similar components related to functionality of EMC.

8.2.4 Component packaging

Placement of the components on a PCB must be considered to their interconnect traces, bus structures and decoupling. The designers do not always consider design parameters like how digital components are packaged or if their functionality is correct. Its often speed to get to the market that is important in high-technology designs. What they do forget is that the component packaging plays an important role in the development or suppression of RF currents. One of the major problems is the lead-length inductance, which allows several abnormal operating conditions to exist. These conditions concern creations of small loop antenna and ground bounce that may radiate RF currents that exist between source and load. Whenever the devices output switches from one logic state to another ground bounce causes glitches to occur in logic input circuitry.

The loop area of the die, the bonding wire and components leads to the PCB can become great contributors to the creation of EMI. In components like VLSI components and high speed components mounted on multilayer PCB's, radiating loops become small which causes IC leads to become relatively large and being equivalent to a radiating antenna. As mentioned in previous chapters, differential mode currents generate radiated emission. These currents are set up by the existence of the loop between components and a plane on a multi-layer board. For inductance to exist, a loop must exist, and for minimization of inductance the loop area must be kept small. These inductances include everything from the lengths of the bond wires internal to components, internal bond leads for capacitors, resistors and other passive components.

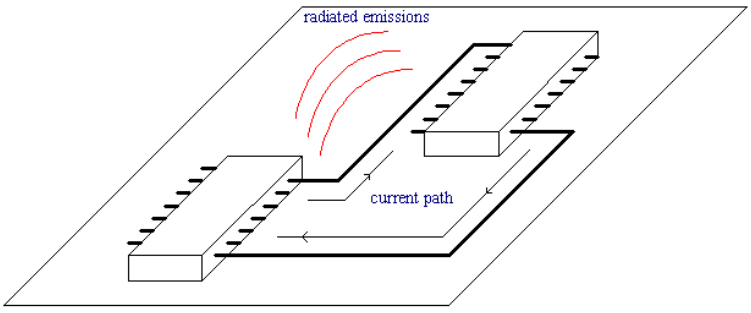

Figure 8.5 - Loop areas between components

Major emissions sources are established from currents flowing between components. As seen in the figure 8.5, radiated emissions can be seen as a small-loop antenna carrying interference current. If dimensions are smaller than λ/4, a small loop is present and it exist for frequencies up to several hundred Mhz. Common mode currents are harder to manage and control. They usually are observed from cables affixed noise to the unit, where the RF energy is determined by common mode potential. The common mode current can be seen as a monotonic antenna driven by ground–noise voltage.

The best way to control differential mode radiated emissions is in the design and layout of the PCB. That is done by minimizing loop areas, where logic components are selected with power and ground pins located in the center of the package or physically adjacent to each other. Power pins in the center gives optimal placement of decoupling capacitors. This configuration also minimizes trace length connections between the device and decoupling capacitor. It also minimizes the inductance from the power and ground pins internal to the silicon wafer of the package. Since vias are needed to bring power and ground to the device, these same vias can be used for heat removal when placed around the active components.

Looking at the creation of RF currents, surface mount technology components has an advantage over through-hole components due to a smaller loop area. By minimizing loop areas of adjacent power and 0V reference it can prevent RF currents to develop and allow for improved flux cancellation between power and ground. Large RF currents exist on power input pins due to differential-mode switching currents created by switching all pins under maximum capacitive load. The RF flux must find an alternative path to cancel out internally generated RF currents by minimizing differential ground noise voltage. Knowing this, it can be established that surface-mount technology is preferred to through-hole technology for minimized RF emissions. The characteristic difference is due to shorter lead-length inductance from the die of the component to the circuit trace on the PCB, where Surface Mount Technology (SMT) has smaller loop size areas. RF currents can also be created by lead length inductance, which cause induced RF currents.

Another important issue concerning RF emissions is how IC package leads are bonded to the PCB. Even though the loop areas are small, bonding wires along the interconnect leads permit RF paths to be developed. The RF currents can be minimized by keeping the loop area of the traces in multilayer PCB's smaller than the lead-length inductance. Even bond wires become small antennas at high frequencies, making it possible for RF path to exits and interfere with electromagnetic compliance. In today´s high technology products there are great problems with bond wiring, for example Dual In-Line Package (DIP) components is one to mention. By choosing SMT components over DIP components performance is increased and package size is reduced by approximately 40%. Lead-length inductance is decreased between the die and the mounting pad because of the smaller board space with less trace length in between SMT components.

8.2.5 Inductance reduction

One of the important issues in PCB design is to reduce inductance. Traces inside the PCB can produce a large amount of EMI depending on the size and frequency. Designers who prefer

smaller width of the traces have to cope with inductance, voltage ripples and high voltage drops. Using separate power and ground planes can also reduce inductance, where the inductance of a plane is much lower than a PCB trace. This solution reduces the parasitic elements because the parasitic inductance is very small due to a very large contour and a good magnetic coupling factor. For higher frequencies, the plane technique is efficient if the distance between the source and the load is short. These planes are inefficient at lower frequencies because of the small equivalent capacitor and the impedance existing across the circuit.

Another technique in reducing inductance is selecting a proper and small package for the components. Impedance and resistance are present inside the package where pins are connected to dies. The die has some internal impedance and the package is in series with the die, and can be seen as an RLC circuit which has some resonance frequency. Even the quality factor can be reduced by selecting the smallest package.

8.2.6 Transmission line analysis

A transmission line is a material medium that form a path for directing transmission of energy, such as electromagnetic waves or acoustic waves. It can include wires, coaxial cables, dielectric stubs, micro strips or optical fibers. In this particular design micro strips were used as transmission line. Important characteristics when designing a transmission line is the characteristic impedance, dielectric constant, operating frequency, height of the substrate, width of the strip and the thickness of the strip metallization. Characteristic impedance, Z_0, is the ratio of the complex voltage of a given wave to the complex current of the same wave at any point on the line and it is defined by equation 8.9.

$$Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{8.9}$$

The importance of Z_0 will be comprehended due to Kirchhoff's laws no longer can be applied. Should impedance be present in the circuit and the average size of discrete components is more than a tenth of the wavelength, transmission line theory must be applied.

$$l_A \geq \frac{\lambda}{10} \tag{8.10}$$

At this length the phase delay and the interference of any reflections on the line become important and can lead to unpredictable behavior in the system. Traveling voltages and current waves expressed as exponential functions are used instead of Kirchhoff laws. The voltage wave can be expressed as in equation 8.11

$$V(z) = V^+ e^{-kz} + V^- e^{+kz} \tag{8.11}$$

and the current wave as in equation 8.12.

$$I(z) = I^+ e^{-kz} + I^- e^{+kz} \tag{8.12}$$

Another important thing is to decide whether the transmissions line is lossless or not. When the elements R and G are relatively small, the transmission line is considered as an idealized lossless structure. For lossless transmissions lines characteristic impedance is

(8.13)

The design requirement for the characteristic impedance is 75Ω. Other characteristics are determined due to characteristic impedance, such as width, height and thickness. The dielectric constant for frequencies over 1 GHz is approximately 4.34. To determine the width of the trace, wave impedance in free space, Z_f, is needed and a factor A given by equation 8.14 [6].

(8.14)

where $Z_f = 377\Omega$ and factor A = 2.1862. Substituting A in equation 8.15

(8.15)

with the knowledge from the PCB manufacturer that both thickness of trace and height of the substrate needs to be h = 1.6mm and t = 35µm, see figure 8.6. Solving equation 8.15 gives the required value of width, which is 1.47mm.

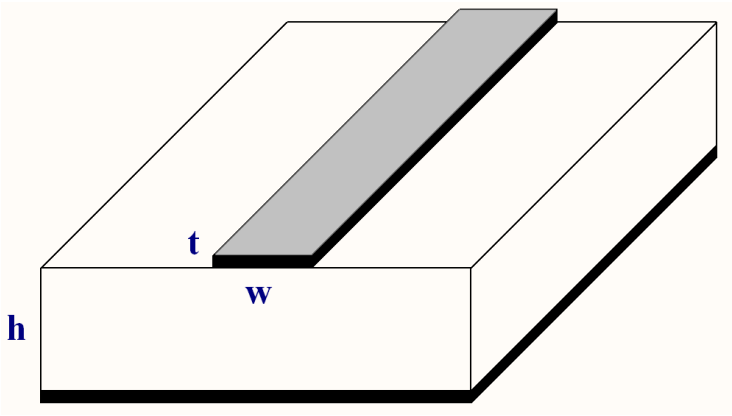

Figure 8.6 - Microstrip line

When all these parameters are determined the PCB design can begin to take form.

8.3 Power supply design elements

8.3.1 DC/DC converters

Traditionally used linear regulators are often made up of a more or less sophisticated linear circuit that tries to keep the output voltage at a desired value. When the load draws large amounts

of current and the voltage drop over the regulator is high the power loss in the regulator is large. High power loss generates heat which in turn must be conveyed off the regulator to prevent malfunction. The regulator will be destroyed because of the too much heat.

A DC/DC converter takes care of two of the main drawbacks of linear regulators. The first is that the converter can be made highly efficient thus radically reducing the power loss in the converter. The second advantage is that voltage can be converted in a large number of ways, for example both down- (Buck) and up-converted (Boost). Only voltage down-conversion can be made with linear regulators. The main drawback of DC/DC converters is the less well regulated output voltage and the noise emissions due to the high switching frequency. In comparison linear regulators have well regulated output voltage and low noise.

DC/DC converters uses the fact that transistors can be used as switches and that these when switched in either position (on or off) have very low power dissipation. High voltage and low current in off position makes low power dissipation. In the on position the current is high and the saturation voltage low which again give low power dissipation. In the design in this report both Buck and Boost converters are used. First the function of the down-converting buck topology is presented.

8.3.1.1 Buck down-converter

If the waveform, with 50% duty cycle, in figure 8.7 would be time averaged the value would be half the top voltage.

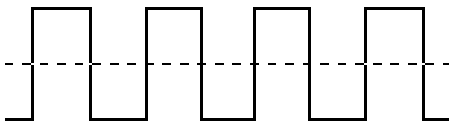

Figure 8.7 - Solid line input voltage, dotted line time averaged voltage.

If the duty cycle (D) is varied, the time averaged voltage will vary as in equation 8.16.

$$V_{OUT} = V_{IN} \cdot D \tag{8.16}$$

The time averaging of a Buck down-converter is done as in figure 8.8. When the transistor is fully on then current is flowing through the inductor, partly to the load and partly to capacitor. When the transistor is turned off, the current through the inductor cannot suddenly disappear, due to the energy accumulated in the magnetic field. The current continue to flow, transferring energy to the capacitor and the load. As the transistor is cut off the current therefore takes the way through the diode. This goes on several times per second, called the switching frequency.

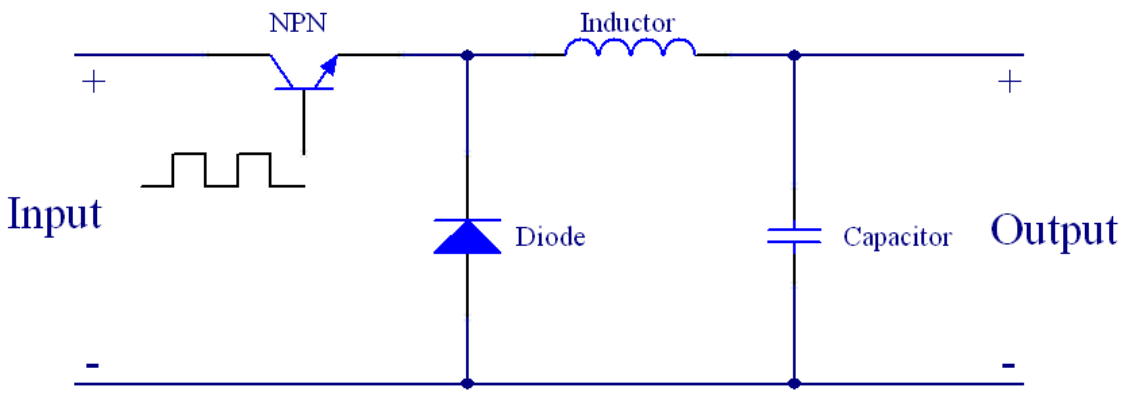

Figure 8.8 - Buck step down converter

The ripple current of the output capacitor is small compared with the input capacitor. As the inductor obstructs changes in current, it facilitates the task for the output capacitor. The capacitor current has small deviations from the load current. The input capacitor has a more demanding job delivering more current in portions determined by the switch frequency. It must be capable of more ripple current, and thus a more expensive capacitor must be selected. The opposite applies to a Boost converter, where the output capacitor has the more demanding job.

8.3.1.2 Boost step-up converter

The principle for Boost step-up conversion, see figure 8.9, is similar as the principle for the Buck converter. Energy is stored in the inductor magnetic field when the transistor conducts. When the transistor is turned off, the current continues to flow through the diode to the load and the capacitor. The input voltage and the inductor induced electromotive force are also in series resulting in a higher output voltage then input voltage. Equation 8.17 relates input voltage and duty cycle to output voltage.

$$V_{OUT} = V_{IN} \cdot (1 + \frac{D}{1-D}) \tag{8.17}$$

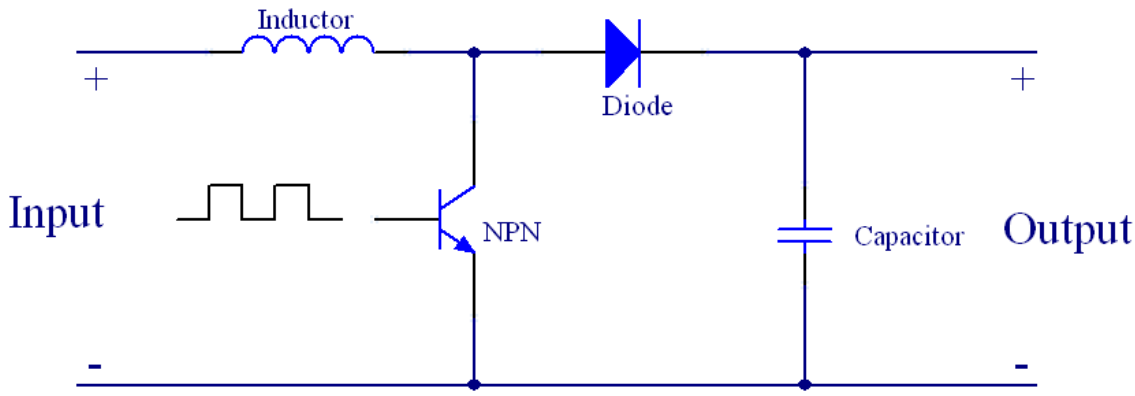

Figure 8.9 - Boost step-up converter

As the input current is filtered through the inductor, sudden changes in input current cannot occur. The smoothing function of the inductor makes the task for the input capacitor easier than for the output capacitor. When the switch is turned on, current is flowing through the inductance to ground. The output capacitor is then the only load current supplier, and no current flows through the diode. When the transistor is turned off, the output capacitor is recharged through the diode. This means that the output ripple is proportional the load current consumption. More load current means more ripple current and thus affects the selection of output capacitor. In other words, a more expensive capacitor with greater ripple current capability must be used.

8.4 Power loss

Theoretically, the conversion between voltages with the two switching topologies can be made 100 % efficient. Some converters come close with efficiencies of 96-97% at low currents but the efficiency gets lower when load current increases. The main power loss factors are the series resistance of the inductor, losses in the switching transistor and the diode. The transistor can't switch off and on infinitely fast and thus there is power loss at the moment of every switching. The saturation voltage of a bipolar transistor is also a limiting factor. One solution to get higher efficiency is to replace the bipolar transistor with a MOSFET with low on resistance. However, with such an advantage there is always a drawback. The gate of the MOSFET acts as a capacitor and at every switching instant charge must be moved to or removed from the capacitor. This charge transport introduces new power losses. This can in fact also be found in the bipolar case but not in the same order of magnitude.

Theoretically, a Boost step-up converter could step-up the voltage as high as wanted. Unfortunately power loss and the forward voltage of the diode set stop and limit the available up-conversion factor to a few times. Sometimes the diode is replaced with a MOSFET transistor, which makes the forward diode voltage problem disappear. If the MOSFET doesn't switch at the right time the electromotive force from the inductor can increase dramatically. Fortunately the MOSFET has a parallel body diode, and often a built in Schottky diode, conducting for a short period of time before the switching has occurred. In other case, the transistor could easily break down by the high reverse voltage applied by the inductor.

8.5 Heat removal

As virtually all components heat up, some more than others, this heat must be removed for correct functionality, or to maintain a low component temperature. If the temperature is not held within specification, the increased temperature can break or potentially decrease the component length of lifetime. All of the chips in this design needs more or less cooling. As these chips are situated on top and near the PCB one easy way to remove heat is to put a copper plane right under the chip, reaching out on the sides, which will aid temperature removal. Some of the chips have an exposed thermal pad right under the chip package. This pad is soldered to the PCB, and with the aid of thermal vias to the underlying ground plane this makes a rather efficient heat sink, see figure 8.10. More information about thermal via size and solder mask techniques for efficient heat removal and soldering can be found in [12].

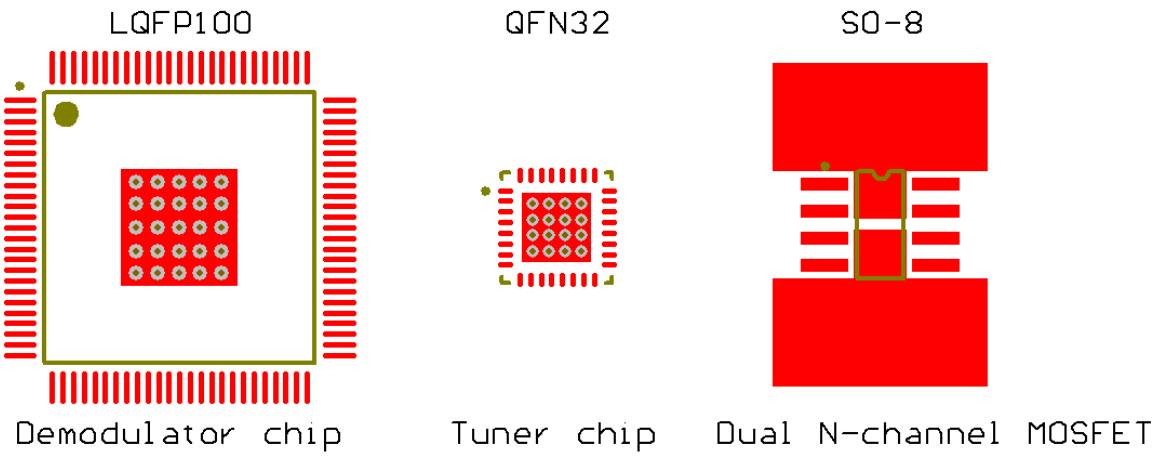

Figure 8.10 - Thermal pads for heat removal

9 Circuit design

The tuner, demodulator and LNB driver are only a small part of a complete STB, see figure 9.1. The transport stream comes out of the demodulator and must be processed to filter the needed packets that belong to a certain TV-channel, text-TV or maybe subtitling. Afterwards the filtered data must be decoded by a MPEG decoder if there is a video content and an audio decoder if there is audio content. A great part of all the processing is done in a special STB processor. The processor contains special hardware for most of the task which implies much computational effort.

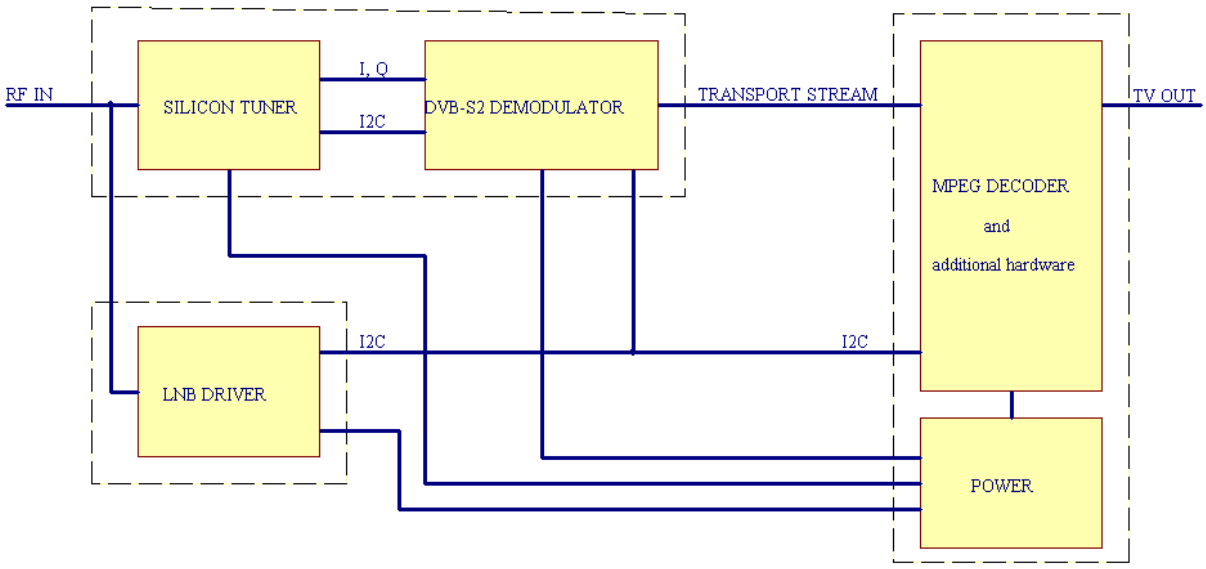

Figure 9.1 - System overview

A working system for terrestrial DVB were given with the task of rebuilding it for the second generation satellite DVB-S2 standard. This might seem like an easy task but rebuilding a system for new functionality without altering the existing base hardware can make things difficult. The constraints on the new design were:

1. Use the existing base hardware as far as possible
2. Fit the new front end at the same place as the old
3. If possible, do not make the new front end larger than the old (44 x 70 mm)
4. To make manufacturing easy, do not place components on the back side on the PCB
5. Power the new front-end on the same power supply as the old (5.7V, 3.3V, 2.5V, 1.1V)

Some things that made the conversion difficult were the fact that the tuner and demodulator were on different PCBs. The original system had a stand-alone tuner on a separate shielded PCB which was soldered to the main PCB. The demodulator chip was soldered right on the main PCB. Packaging and pin configuration of the new and old demodulator was not equal and therefore the new demodulator was forced to be on the tuner PCB. By making this decision the base hardware had to be altered with a contact for the transport stream. This was interfering with

constraint 1 but as the main PCB was under revision the contact could easily be added in. At this point the tuner, demodulator and LNB driver were planned to reside on the same PCB at the old tuner position. Trying to fit all this functionality on such a small space as 44 x 70 mm without interfering with constraint 4 could not be done. The decision was then to lift out the LNB driver, placing this on an own PCB, and see if the remaining components could fit.

A power converter for the demodulator had to be added to cope with the current consumption. This was placed on the same PCB as the demodulator (see figure 9.2) as the feedback loop had to be held small and the response fast. Unfortunately the size constraint could not be held anymore and the PCB had to be prolonged form 70 to 110 mm. This was just 10 mm less than the hard 'fit-in-the-box' constraint and the PCB could not be much longer.

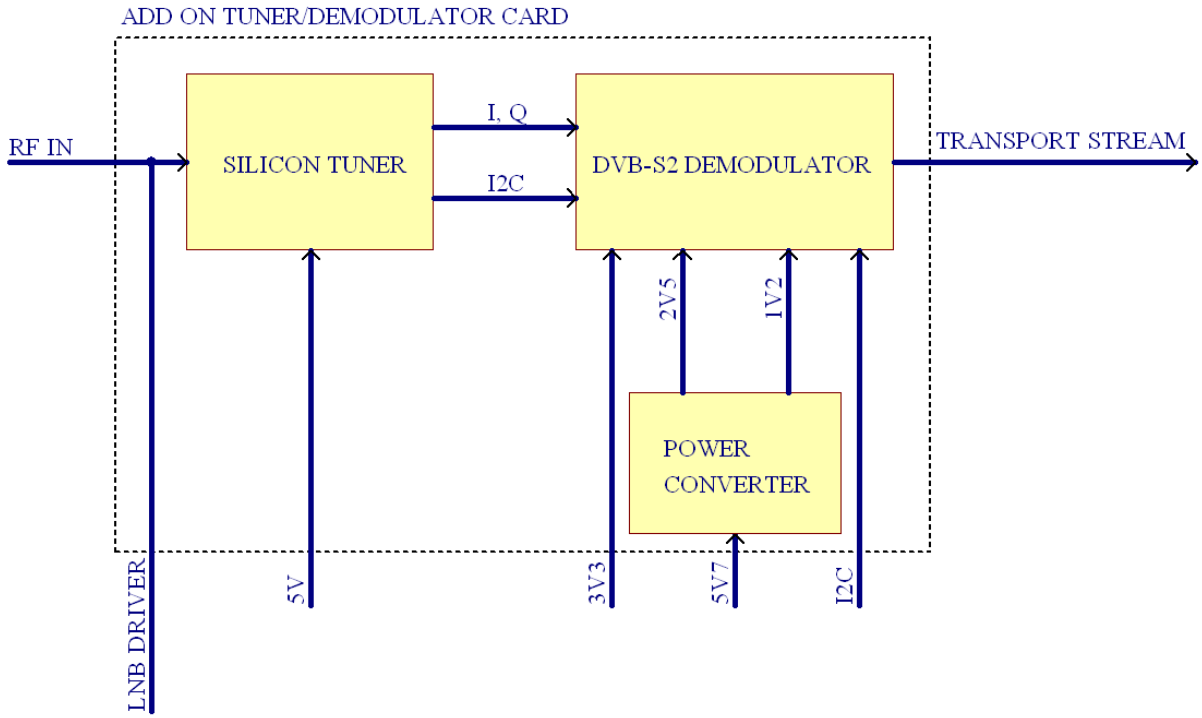

Figure 9.2 - Front-end PCB overview

An overview of the LNB PCB functionality can be seen in figure 9.3. As can be seen the LNB driver must be powered by around 12V. This interfered with constraint 5 but could be solved by switching wall socket ac/dc adapter.

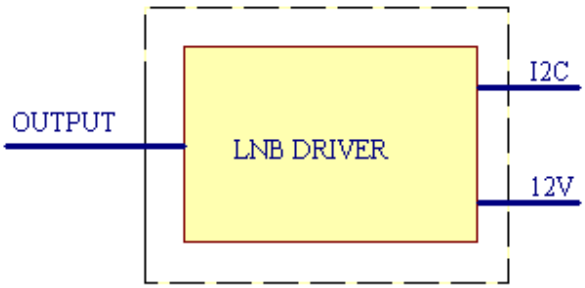

Figure 9.3 - LNB driver PCB overview

9.1 LNB driver and interface

The integrated circuit LNBH21 [19] from ST Microelectronics were chosen to control and power the LNB. It has a built in DC/DC converter that generates 13 and 18 V from a single supply source and a continuous 22 kHz tone for selection of the high frequency band.

9.2 The LNB boost converter

The rectifying diode in the DC/DC converter dissipates a lot of power. For a normal diode the power loss can be quite large. The reverse recovery, or charge removal, will also add some loss. Schottky diodes will partly solve this problem, as they have a relatively low forward voltage and good reverse recovery. For the LNB driver circuit a Schottky diode is thus selected. A dual MOSFET switch would have been even better but the LNBH21 IC is not equipped with dual driver circuits, and is therefore forced to use a Schottky diode. For cost and area efficiency an integrated Schottky and MOSFET combo in a SO-8 package has been selected. Thermal pads have been applied as in chapter *Heat removal* to maintain a low chip temperature. A compromise between switch loop area and thermal pad area has been made in order to keep both EMI and temperature down. As this is a Boost converter the ripple current at the output is larger than at the input. This places constraints on the output capacitor ripple current capability. Load current measured with several different LNBs shows a maximum of 200mA steady state current. At the low 13V output the DC/DC converter must keep an output value of 13+2.2V. The 2.2V voltage drop has its origin in the post regulator within the LNBH21. The post regulator is used to get an almost ripple free output. To calculate the rms ripple current before the regulator, the mode in which the converter works must be determined. The inductor value 22µH used in the design is chosen according to the recommendation in the LNBH21 documentation. To maintain continuous mode operation the average ripple current through the inductor must equal the mean output current, see figure 9.4.

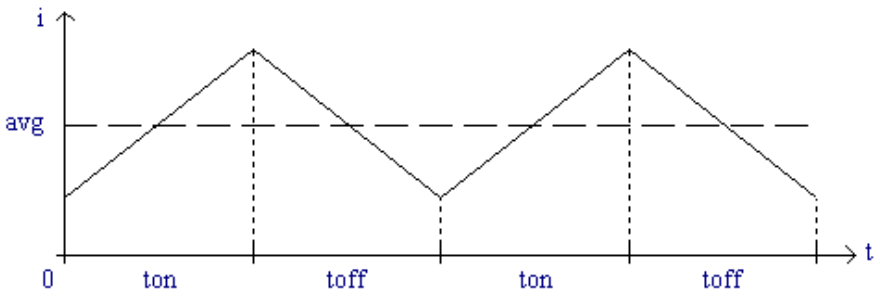

Figure 9.4 - Current waveform for continuous mode operation

The minimum output current for continuous mode operation is then

$$I_{min,avg} = \frac{\Delta I_L}{2} \tag{9.1}$$

Disregarding losses in the circuit, the current increase during t_{on} is

$$\Delta I_L += \frac{V_{IN}}{L} \cdot t_{on} \tag{9.2}$$

During t_{off} the decrease in current must match the prior increase in current

$$\Delta I_L -= \frac{V_{OUT} - V_{IN}}{L} \cdot t_{off} \tag{9.3}$$

Combining these two equations leads to equation 9.4.

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT}}{V_{IN}} - 1 = \frac{15.2}{12} - 1 = 0.27 \tag{9.4}$$

The off- and on-time at the typical switch frequency 220 kHz lead to

$$t_{on} + t_{off} = \frac{1}{220 \cdot 10^3} \quad \xrightarrow{yields} \tag{9.5}$$

$$(0.27 + 1) \cdot t_{off} = \frac{1}{220 \cdot 10^3} \quad \xrightarrow{yields} \tag{9.6}$$

$$t_{off} = \frac{1}{1.27 \cdot 220 \cdot 10^3} \approx 3.58\mu s \quad \xrightarrow{yields} \tag{9.7}$$

$$t_{on} = 0.27 \cdot t_{off} \approx 0.97\mu s \tag{9.8}$$

By combining the equations above the minimum average current can be calculated, see equation 9.9.

$$I_{min,avg} = \frac{1}{2} \cdot \frac{V_{IN}}{L} \cdot t_{on} = 265mA \quad (9.9)$$

The minimum current for continuous operation is thus larger than the maximum measured current drawn by the LNB, and the converter will work in discontinuous mode. It can easily be seen from the equation that the minimum current increases with increasing on-time (corresponds to a larger output voltage), and the converter will thus never be in continuous mode with the 200mA load.

9.2.1 Output capacitor ripple current

As the inductor current will reach zero during t_{off}, due to the discontinuous mode operation, this will alter the previous equations. The off-time can be divided into two different parts, t_{off1} with inductor current and t_{off2} when current has decreased to zero, see figure 9.5.

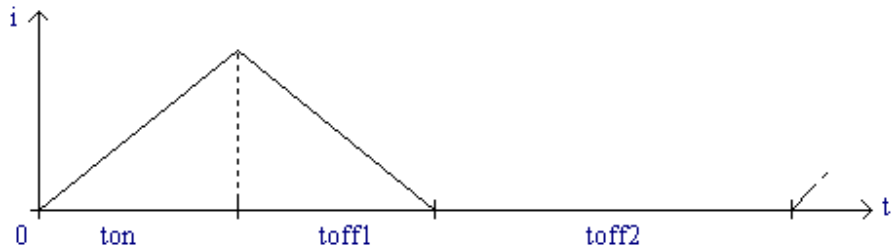

Figure 9.5 - Discontinuous mode operation

The current increase during t_{on} is the same as before but equation 9.3 is altered slightly and become

$$\Delta I_L -= \frac{V_{OUT} - V_{IN}}{L} \cdot t_{off1} \quad (9.10)$$

Setting the two inductor current equations equal yields

$$t_{off1} = \frac{V_{IN}}{V_{OUT} - V_{IN}} \cdot t_{on} \quad (9.11)$$

The charge supplied to the load during t_{on}, t_{off1} and t_{off2} must equal the charge supplied by the inductor at t_{off1}.

$$I_{out} \cdot T = \frac{V_{IN}}{2 \cdot L} \cdot t_{on} \cdot t_{off1} \quad (9.12)$$

Combining equations 9.11 and 9.12 creates an expression for the output voltage.

$$V_{OUT} = V_{IN} + \frac{V_{IN}^2 \cdot t_{on}^2}{2 \cdot L \cdot I_{OUT} \cdot T} \quad (9.13)$$

Recombining the variables also leads to an expression for t_{on},

$$t_{on,13V} = \sqrt{\frac{I_{OUT}\cdot(V_{OUT}-V_{IN})\cdot 2\cdot L}{V_{IN}^2\cdot f_{switch}}} = 0.94\mu s \tag{9.14}$$

and with the use of equation 9.11, t_{off1} can be calculated for a output current of 200mA.

$$t_{off1} = 3.54\mu s \tag{9.15}$$

By knowing t_{on} the peak inductor current can be calculated.

$$I_{L,peak} = \frac{V_{IN}}{L}\cdot t_{on} = 514mA \tag{9.16}$$

During t_{off1} this current decreases according to

$$I_L = I_{L,peak} - \frac{(V_{OUT}-V_{IN})}{L}\cdot t \tag{9.17}$$

The inductor current refills the capacitor with charge through the diode until the inductor current has decreased to 200mA. Thereafter the capacitor current reverses and adds with the inductor current to sum to the 200mA output current, see figure 9.6. The equation for I_L can therefore be used to calculate the rms current flowing through the capacitor if I_{OUT} is subtracted to account for the output current.

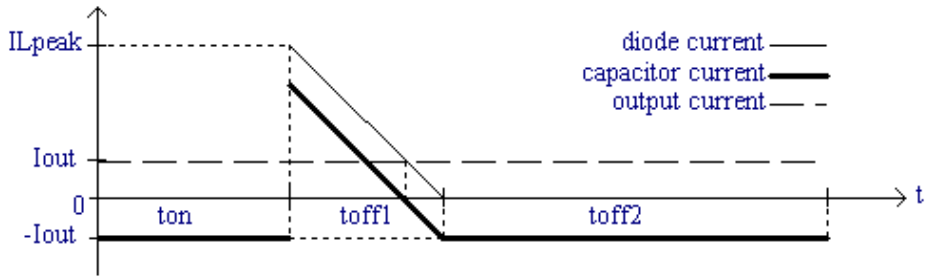

Figure 9.6 - Current waveform for discontinuous mode operation

With all this information the output capacitor rms current can be calculated.

$$I_{rms} = \sqrt{f_{switch}\cdot\left(\begin{array}{c}\int_0^{t_{off1}}\left(I_{L,peak} - I_{OUT} - \frac{(V_{OUT}-V_{IN})}{L}\cdot t\right)^2 dt \\ + \\ \int_0^{t_{on}+t_{off2}} I_{out}^2 dt\end{array}\right)} = 227mA \tag{9.18}$$

Due to the fact that the design uses two capacitors this value is halved and the rms current capability of each capacitor must be at least 113mA for the low voltage level. The calculations for the high level are not showed but results in an rms ripple current of 276mA and thus 138mA for each of the capacitors.

9.2.2 Output ripple voltage

As the LNBH21 IC is equipped with a linear regulator after the Boost converter the ripple voltage at the output is of less importance. However, if the ripple is big there is a chance of malfunction as the linear regulator has a 2.2V voltage drop. By the well known equation $= C \cdot \frac{dV}{dt}$, the drop due to current supplied to the load can be calculated. By using the equations in the previous chapter t_{on}, t_{off1} and t_{off2} can be calculated for the high voltage output. Then the output voltage drop can be calculated as

$$\Delta V- = \frac{I_{OUT} \cdot (t_{on} + t_{off2})}{C} + \frac{1}{C} \int_{\Delta t}^{t_{off1}} \left(\frac{V_{OUT} - V_{IN}}{L} \cdot t \right) dt \tag{9.19}$$

$$\Delta t = \frac{L \cdot (I_{L,peak} - I_{OUT})}{V_{OUT} - V_{IN}} \tag{9.20}$$

Where Δt is the time from when the capacitor begins to recharges to the time where it starts to supply current over again.

Increasing the output current or time where the capacitor supplies all the current, increase the output voltage ripple. Increasing the capacitance helps lowering the ripple and thus for a specified output voltage and maximum ripple voltage a minimum capacitance value can be calculated. Recommendations in the datasheet suggest a 220µF and a 100µF with a ferrite bead filter in between. The ferrite bead is almost a short for dc current and therefore the ripple voltage can be calculated by adding the capacitance values. A 320µF value corresponds to around 1,6mV output voltage ripple. Unfortunately this is not the only voltage ripple source. The voltage $I \cdot ESR$ in the capacitor adds to the final ripple. When the capacitor discharges with 200mA the ESR voltage is 6.8mV (for an ESR of 34mΩ). Thus the negative peak value is 8.3mV. The positive peak ripple value can be determined by

$$\Delta V+ = \frac{1}{C} \int_0^{\Delta t} I_L dt = \frac{1}{C} \int_0^{\Delta t} \left(I_{L,peak} - I_{OUT} - \frac{V_{OUT} - V_{IN}}{L} \cdot t \right) dt = 1.6mV \tag{9.21}$$

As can be seen the delta voltages are exactly the same. This is no surprise since the same amount of charge is added or subtracted from the capacitor plates. From the definition of capacitance $C = \frac{Q}{V}$ it can be seen that a charge change corresponds to a direct proportional voltage increase or decrease.

The final peak-to-peak voltage ripple thus become 10mV (equation 9.22) which is acceptable as the linear regulator makes the output voltage almost ripple free.

$$V_{ripple,p-p} = 2 \cdot \Delta V + I_{OUT} \cdot ESR = 10mV \tag{9.22}$$

9.2.3 Input capacitor ripple current

The converter exhibits a triangular waveform at the input. The main function of the input capacitor is to smoothen out the current supplied by the input power circuitry. This also leads to minimized areas of high frequency currents which reduce RFI. As most of the current is directly supplied by the input power circuitry the ripple current of the input capacitor will be several times less than for the output capacitor. With unknown powering circuit the rms ripple current for the capacitor is impossible to calculate with acceptable accuracy. However, a good estimate or guess might be a calculation of the rms current with subtracted mean current value.

$$I_{in,mean} = f_{switch} \cdot \left(\int_0^{t_{on}} \frac{V_{IN}}{L} \cdot t \, dt + \int_0^{t_{off1}} \left(\frac{V_{IN}}{L} \cdot t_{on} - \frac{(V_{OUT} - V_{IN})}{L} \cdot t \right) dt \right) \tag{9.23}$$

$$I_{in,rms-est} = \sqrt{f_{switch} \cdot \begin{pmatrix} \int_0^{t_{on}} \left(\frac{V_{IN}}{L} \cdot t - I_{in,mean} \right)^2 dt \\ + \\ \int_0^{t_{off1}} \left(\frac{V_{IN}}{L} \cdot t_{on} - \frac{(Vout - Vin)}{L} \cdot t - I_{in,mean} \right)^2 dt \end{pmatrix}} \tag{9.24}$$

Calculating the input capacitor rms current estimate shows a lower current, as expected. For comparison, table 9.1 shows input and output rms ripple currents for the LNB Boost converter with a 200mA load.

Output voltage	Input capacitor rms ripple current (estimate)	Output capacitor rms ripple current (estimate)	Input/output rms current ratio
15.2V (13+2.2V)	147mA	227mA	0.65
20.2V (18+2.2V)	225mA	276mA	0.82

Table 9.1 - Capacitor ripple current

As the converter works in discontinuous mode the input/output ripple current ratio is quite high. This ratio would have been much lower in continuous mode as the inductor ripple current would not have been so high.

9.3 Voltage requirements by the demodulator chip

The LDPC FEC in the demodulator chip consumes lots of power when activated. According to the demodulator datasheet [17] the maximum current consumption is 1.7A. To keep power dissipation on a low level the LDPC runs at a voltage of 1.2V. See table 9.2 for a complete overview of the required voltages and current consumption.

Supply voltage	Maximum current consumption	Power dissipation
3.3V	30mA	99mW
2.5V	100mA	250mW
1.2V	1.7A	2.04W

Table 9.2 - Supply voltage, current consumption and power dissipation of the demodulator chip

As the available voltage at the input of the STB is 5.7V the use of a linear regulator for the 1.2V would result in a voltage drop of 4.5V over the regulator. A power dissipation of 7.65W in the regulator would then be the result. This requires a special package and lots of PCB heat sink area in order to maintain a relatively cool chip. As there are restrictions on the dimensions of the PCB, and so much power dissipation would be a waste of energy, another voltage conversion method must be considered. A DC/DC Buck converter could do an excellent job of voltage conversion. With an efficiency of 90%, the power dissipation in the converter decreases to around 0.8W which is more manageable with the area restrictions of the design.

The demodulator chip requires two more voltages, 2.5V and 3.3V. The hardware driven by these voltages draws considerable less current than the LDPC and thus the use of linear regulators will easily accomplish the goal. The use of linear regulators has the advantage of low noise and a well regulated voltage, needed by for example the ADC converter for I- and Q-channel decoding. Linear regulators also keep the price and complexity of the design down. The regulator can often be made with a single integrated circuit and two additional capacitors. In comparison a DC/DC converter often need at least one or two more, quite bulky components.

The 2.5V digital and analog sections share the same supply but are separated by an EMI filter. The more sensitive analog section is thus isolated from the more noisy digital section.

9.4 The 1.2V Buck Controller

The TPS40190 is a synchronous buck controller which operates from 4.5V to 15V and implements fixed frequency voltage mode power supply [20]. By using an adaptive anti-cross conduction scheme it prevents both the high side and rectifier MOSFET to be turned on at the same time. In that manner it prevents shoot through current in the two MOSFET´s. The controller is also protected against short circuit with a threshold that is selectable between one of three values. Should the controller sense an output short circuit, both MOSFETs will be turned off and a timeout period would be observed before attempting to restart. It also provides drivers to minimize switching losses in the power stage, reducing heat building up in the MOSFETs and permitting larger MOSFETs to be used without undue switching time penalty. In figure 9.7, a simplified application diagram is presented. Values for the inductor and capacitors have been determined by iteration of the equations in the next chapters. The inductor was set to 10µH and the output capacitor to 2x22µF + 10µF in near proximity to the demodulator chip. The input capacitor was chosen to be 100µF.

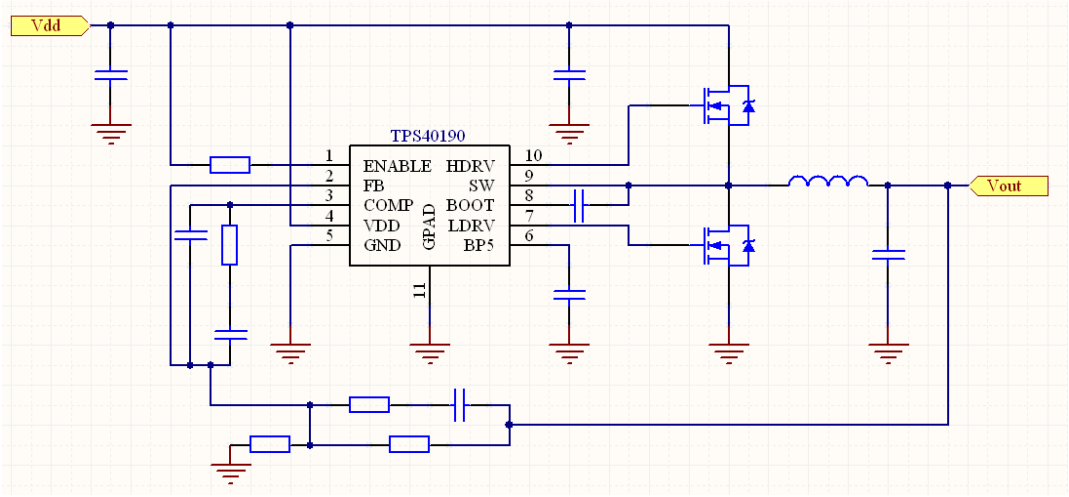

Figure 9.7 - TPS40190 simplified application diagram

9.4.1 Output capacitor ripple current

To calculate the currents the on- and off-periods must be determined. It is assumed that the converter operates in continuous mode. The following calculations will determine if this is true.

Disregarding losses in the circuit, the current increase during t_{on} is

$$\Delta I_L += \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{on} \tag{9.25}$$

During t_{off} the decrease in current must match the prior increase in current

$$\Delta I_L -= \frac{V_{OUT}}{L} \cdot t_{off} \tag{9.26}$$

Combining these two equations leads to

$$\frac{t_{on}}{t_{off}} = \frac{V_{OUT}}{V_{IN} - V_{OUT}} = \frac{1.2}{(5.7 - 1.2)} \approx 0.27 \tag{9.27}$$

The off- and on-time at the typical switch frequency 300 kHz lead to

$$t_{on} + t_{off} = \frac{1}{300 \cdot 10^3} \quad \xrightarrow{yields} \tag{9.28}$$

$$(0.27 + 1) \cdot t_{off} = \frac{1}{300 \cdot 10^3} \quad \xrightarrow{yields} \tag{9.29}$$

$$t_{off} = \frac{1}{1.27 \cdot 300 \cdot 10^3} \approx 2.63 \mu s \quad \xrightarrow{yields} \tag{9.30}$$

$$t_{on} = 0.27 \cdot t_{off} \approx 0.7\mu s \tag{9.31}$$

The peak delta current is then

$$I_{Lpeak\Delta} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{on} \approx 316mA \tag{9.32}$$

As can be seen in equation 9.32 the mean delta peak current is much lower than the load current. The assumption that the converter worked in continuous mode was true. With this knowledge the input- and output-rms current can be calculated. The inductor current for continuous mode operation is depicted in figure 9.8.

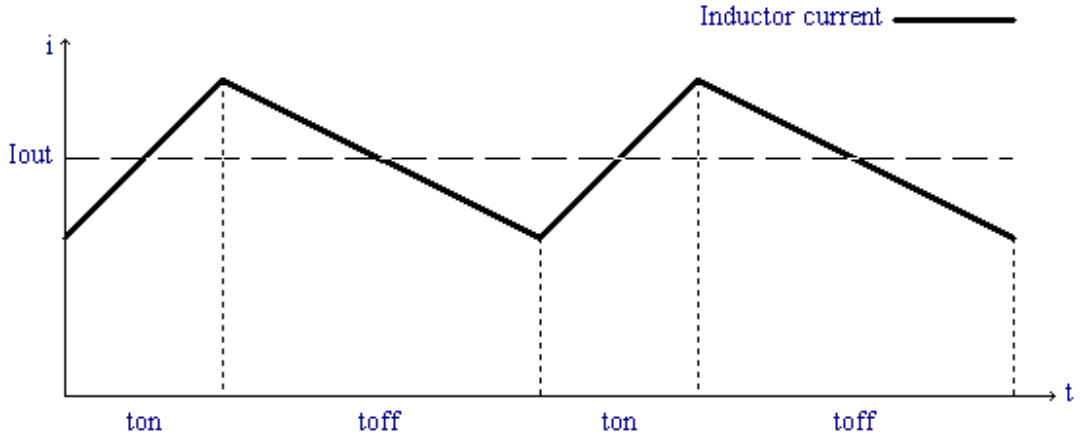

Figure 9.8 - Inductor current for continuous mode operation

The output capacitor will deliver current when the inductor current is less than I_{OUT} and be refilled when the current is higher than I_{OUT}. The rms capacitor current can thus be calculated as in equation 9.33.

$$I_{rms} = \sqrt{f_{switch} \cdot \left(\begin{array}{c} \int_0^{t_{on}} \left(\frac{(V_{IN} - V_{OUT})}{L} \cdot t - \frac{I_{Lpeak\Delta}}{2} \right)^2 dt \\ + \\ \int_0^{t_{off}} \left(\frac{V_{OUT}}{L} \cdot t - \frac{I_{Lpeak\Delta}}{2} \right)^2 dt \end{array} \right)} \approx 91mA \tag{9.33}$$

As this is an estimate of the output capacitor rms current, measurements of the real implementation will most probably be a bit higher. The equation would still help to pick a capacitor as the rms current would be in the same order of magnitude.

9.4.2 Output voltage ripple

As the inductor current, the capacitor will exhibit a triangular current waveform. The waveform mean value is zero as depicted in figure 9.9.

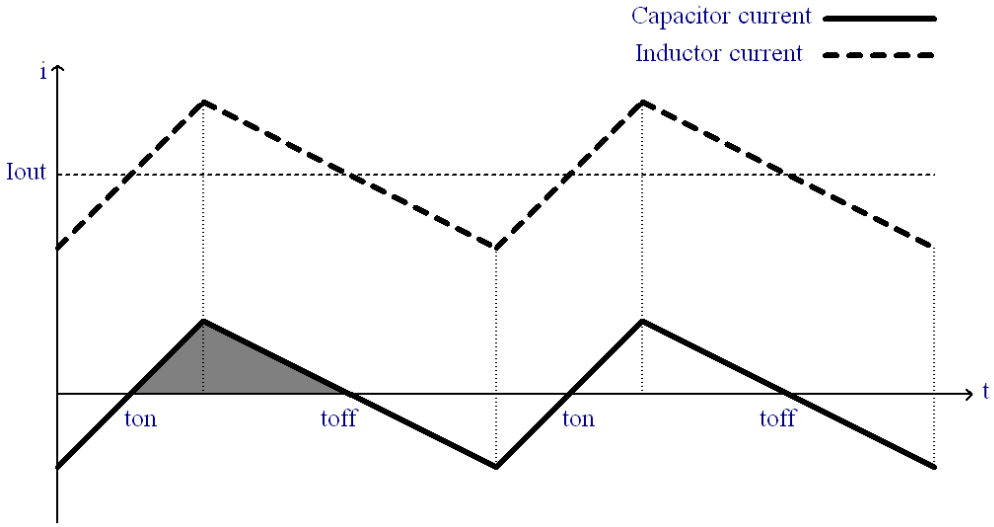

Figure 9.9 - Inductor- and output capacitor-current

At the instances when the current reverses direction the voltage drop caused by the capacitor ESR is at its maximum value. The voltage drop can be calculated with the already determined delta peak current in equation 9.32.

$$V_{ESR,peak} = \frac{I_{Lpeak\Delta}}{2} \cdot ESR \approx 0.8mV \tag{9.34}$$

The ESR of the output capacitor will ultimately set the limit on how low the output ripple can be. Increasing the capacitance beyond a certain level will not be of any use since the ESR voltage ripple always will be there. The ESR voltage ripple will be at its peak value when the capacitor current is at its maximum, as in equation 9.34. The capacitor contribution can be calculated by integration of the current in the grey area in figure 9.9. The charge accumulated will raise the voltage level as described in equation 9.35.

$$V_{peak} = \frac{1}{C} \cdot \left(\int_0^{\frac{t_{on}}{2}} \left(\frac{(V_{IN}-V_{OUT})}{L} \cdot t\right) dt + \int_0^{\frac{t_{off}}{2}} \left(\frac{V_{OUT}}{L} \cdot t\right) dt\right) \approx 3mV \tag{9.35}$$

The capacitor ripple voltage is a few times higher than the ESR voltage ripple. This means that the ESR ripple voltage is only a small part of the total ripple and the capacitor ripple can be taken as a measure of the total ripple. The capacitor ripple peak will also occur at a different time instant and if the capacitor is large enough and the ESR is small enough, the capacitor ripple peak is the true peak.

9.4.3 Input capacitor rms current

As the converter is powered through long interconnects with intrinsic inductance there is no way for the power supply to deliver current as fast as the converter needs. The input current can then be assumed nearly constant. Therefore the input capacitor has to act as a supply during these moments.

During ton the total input current must be the same as the inductor current in steady state. The current supplied to the input capacitor during t_{off} must then be (assuming constant input current):

$$I_{IN} = \frac{t_{on}}{t_{off}} \cdot I_{OUT} \tag{9.36}$$

Figure 9.10 depicts the behavior of the input current, the capacitor current and the inductor current.

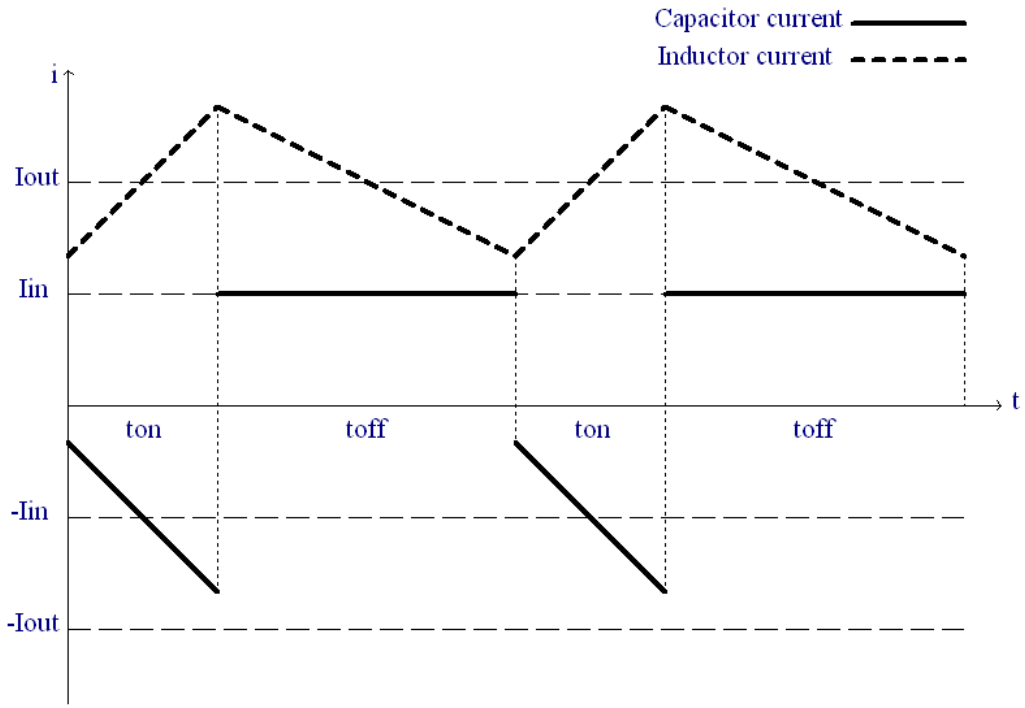

Figure 9.10 – Input capacitor current, input current and inductor current

Positive capacitor current is defined as flowing into the capacitor. During ton the input current and capacitor current therefore adds up to the total inductor current during the same instance. With this information an estimate of the capacitor rms current can be calculated.

$$I_{rms} = \sqrt{f_{switch} \cdot \left(\begin{array}{c} \int_0^{t_{on}} \left(\frac{(V_{IN}-V_{OUT})}{L} \cdot t + (I_{IN} - \frac{I_{Lpeak\Delta}}{2}) \right)^2 dt \\ + \\ \int_0^{t_{off}} I_{IN}^2 dt \end{array} \right)} \approx 455mA \tag{9.37}$$

The true input capacitor rms current will differ from the calculated values but equation 9.37 presents an indication of how to select the input capacitor with regards to the current capability. Most probably will the RMS current be smaller as the real input current is not constant.

9.5 Voltage requirements by the tuner chip

The tuner [18] power supply could be made less sophisticated than for the demodulator chip. One single, low current, 5V power supply is all that is needed but care has to be taken when placing bypass capacitors. The voltage regulation could therefore be made by a simple linear regulator.

10 PCB layout

The PCB layout has been made with a trial version of Altium designer as both of us had a little experience from earlier software releases from the same company. As there were size constraints on the finished tuner and demodulator PCB it had to be made with four layers. The first and the fourth layer were chosen as signal layers, the second layer as a dedicated ground plane and the third layer as a power plane for the different voltage levels.

In figure 10.1, the finished tuner and demodulator card can be seen. At the left, with predrilled holes for a shield, is the tuner chip located. The zero IF baseband I- and Q-channels are transferred from the tuner chip to the demodulator chip which is located in the low center of the card. This chip handles all the tasks required to put out a decoded transport stream to the white PFC contact to the right. In the upper right the 1.2V buck converter is located, as can be seen by the bulky input capacitor and the inductor. There is also a 2.5V linear regulator located in the same area.

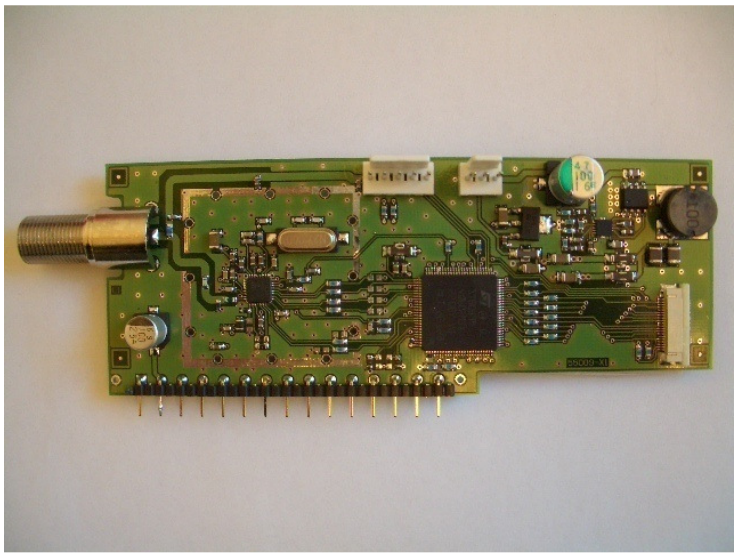

Figure 10.1 - Populated tuner and demodulator PCB, top side

Decoupling capacitors for the demodulator chip are located right below the power pins, on the back side, to make the connection length as small as possible, see figure 10.2.

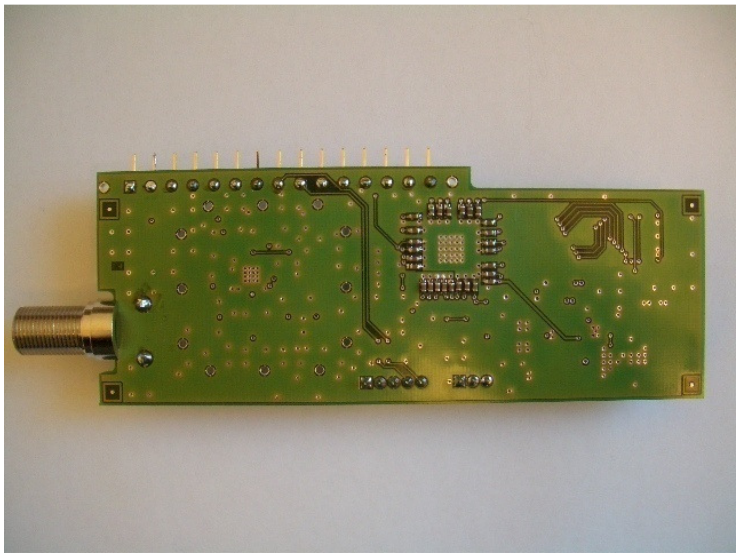

Figure 10.2 - populated tuner and demodulator PCB, back side

The LNB driver was originally planned to reside on the same PCB as the tuner and demodulator but there was not enough room and the solution was to do one more PCB. The size (44x100mm) was chosen so that it could easily be attached to some unused area in the finished STB. In figure 10.3, the two layer LNB driver PCB is depicted.

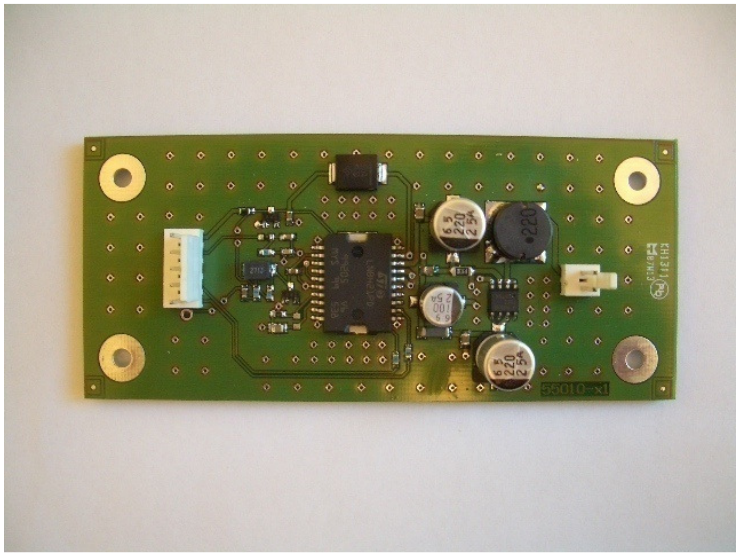

Figure 10.3 - Populated LNB driver PCB

11 Drivers

To get anything useful out of the hardware some software drivers were needed. As the base platform with the st7100 CPU/MPEG-decoder was running STLinux, drivers for the Linux system had to be written.

The hardware was also tested on the PC with a ST developed Graphic User Interface (GUI) with their own drivers. All measurements in the next chapter have been done with the aid of the ST GUI in figure 11.1 to lock on different frequencies. In the GUI all demodulator and tuner registers can be read and programmed.

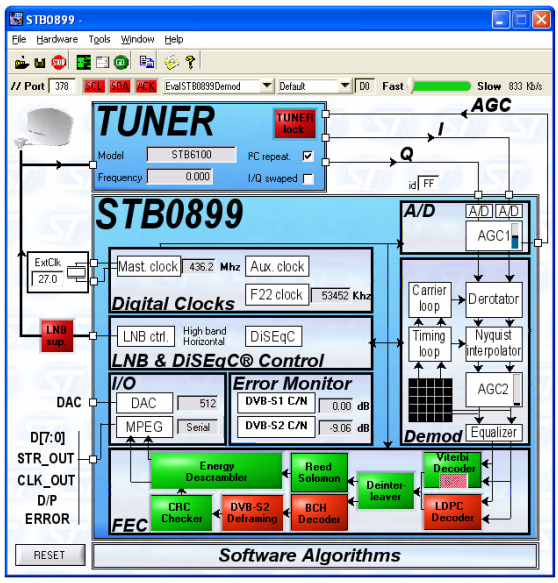

Figure 11.1 - ST GUI for front-end measurements

Communication between the PC and the front-end has been done with an I^2C-interface. The measurement setup can be seen in figure 11.2.

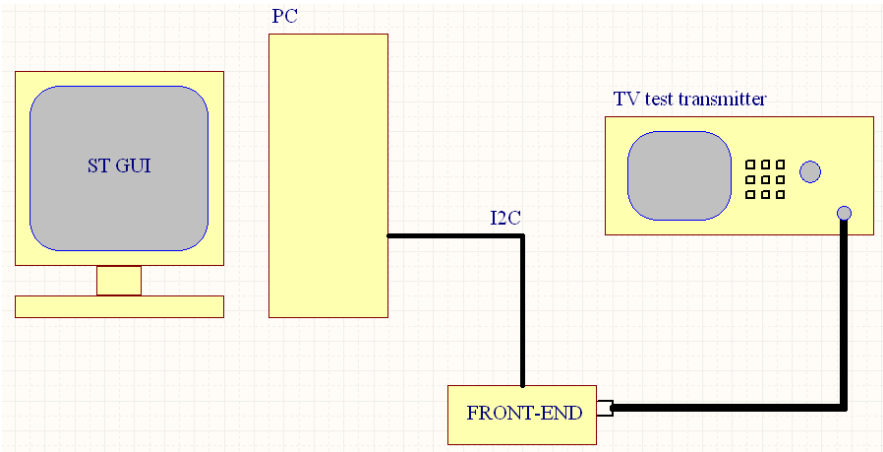

Figure 11.2 – Front-end measurement setup

12 Measurements and testing

In order to check compliance with specifications some basic measurements had to be performed. The measurement equipment used was an Agilent digitizing oscilloscope, DSO6034A, and a DVB-S and S2 digital television test transmitter from Rhode & Schwarz. As discussed earlier the ST GUI was used to read valuable data from the tuner and demodulator registers.

12.1 Front-end

In this section the most basic performance measurements for correct function of the front-end is presented. Of course there are several more measurements that have to be done in order to fulfill a full test plan for the finished product, but as the time were running short only the most important measurements were finished.

12.1.1 Voltage levels and ripple measurements

When the LDPC FEC starts there is a sudden current surge from the power supply. ST specifies a voltage drop limit of 40mV for correct functionality at this instant. As can be seen in figure 12.1 this requirement is fulfilled by a margin of approximately 10mV. When the LDPC stops working the voltage rises (the left yellow top) but soon settles down on 1.2V. It can be seen on the lower MOSFET drive voltage that the converter stops switching until the output voltage has decreased before continuing switching. Then the FEC starts and the voltage dips for a short while (the right yellow dip). At this instance the upper MOSFET is turned on for a longer period in order to supply more current.

Figure 12.1 – LDPC supply voltage dip (yellow) and low MOSFET drive voltage (green)

The 1.2V output voltage ripple can be seen in figure 12.2. It is around 5 - 10mV as predicted in the calculations and satisfactory for our application. All other voltage levels are within the tolerances of specification.

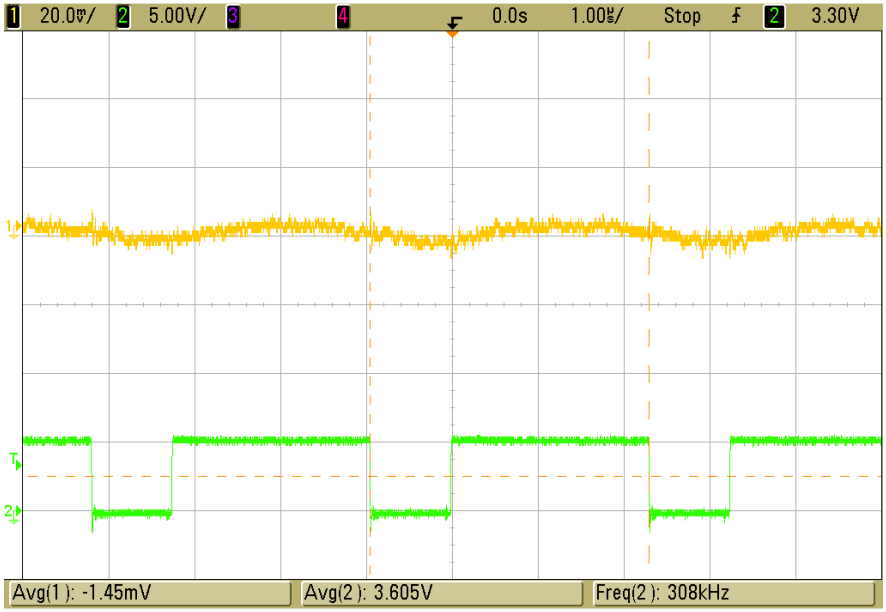

Figure 12.2 - 1.2V buck converter output ripple voltage (yellow) and lower MOSFET switch voltage (green)

For a basic input capacitor current test a 0.1 ohms resistance was connected in series with the input capacitor. In this way the voltage over the resistance could be measured and an indication on how great the ripple current was could be determined. One of the measurements could be seen in figure 12.3.

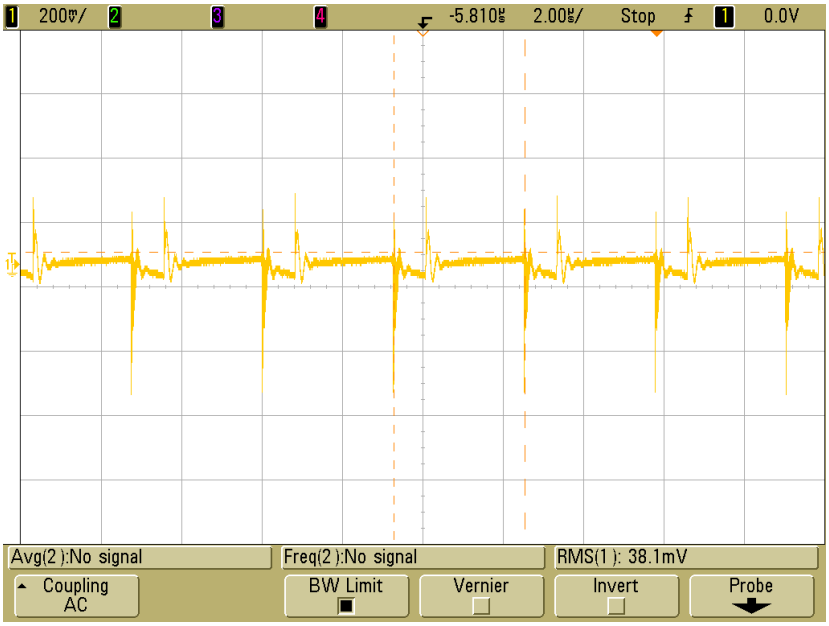

Figure 12.3 - basic input capacitor ripple current measurement

The measurement is not exact but it can be seen by the RMS voltage that the current is smaller than the calculated in chapter 9.4. The ripple is still high for a normal electrolytic capacitor. For the purpose of reducing the ripple current of the big input capacitor a small ceramic capacitor had been added in the schematic design phase. This capacitor was placed as close to the switching MOSFET input as possible to reduce inductance. In figure 12.4 the difference with the ceramic capacitor can be seen. The RMS current ripple was reduced by approximately three times, and the electrolytic capacitor could now be replaced with a less ripple current capable capacitor (cheaper).

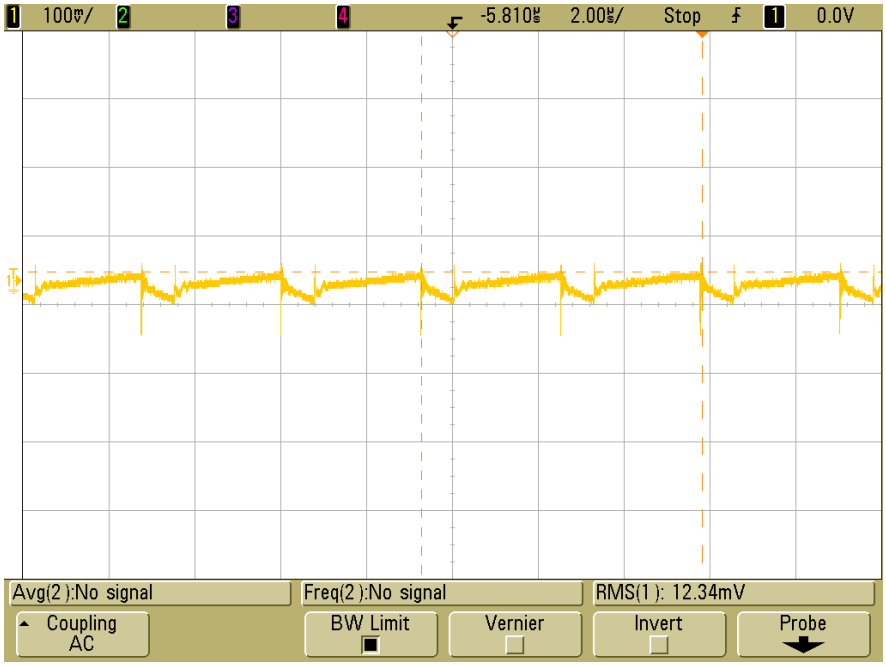

Figure 12.4 - basic measurement of input current with both electrolytic and ceramic capacitor

12.1.2 Tuner and demodulator functionality tests

Quasi Error Free (QEF) is a term in DVB context which defines a post-Viterbi BER (DVB-S) or PER (DVB-S2) threshold for acceptable performance. For DVB-S, BER values higher than the QEF limit of 2E-4 is defined as unacceptable. In table 12.1, the theoretical and measured C/N ratios for QEF operation are presented. In the DVB-S case the acceptable implementation loss is 0.8 dB [23]. As the DVB-S2 FEC doesn't use Viterbi, direct comparisons between DVB-S and S2 is impossible. For DVB-S2 the QEF is defined as a PER of 1E-7. The DVB-S2 measurements are presented in table 12.2.

	Theory	Measured
Code rate	C/N (dB)	C/N (dB)
1/2	3,3	3,3
2/3	5,1	5,1
3/4	6,1	6,13
5/6	7,1	7,1
7/8	7,7	7,79

Table 12.1 - DVB-S performance measurements

	Measured QPSK	Measured 8PSK
Code rate	C/N (dB)	C/N (dB)
1/2	1,05	-
3/5	2,5	5,7
2/3	3,09	6,7
3/4	4,04	7,96
4/5	4,67	-
5/6	5,2	9,41
8/9	6,23	10,78
9/10	6,45	11,09

Table 12.2 - DVB-S2 performance measurements

The DVB-S measurements show exemplary performance. All measurements are within the 0.8 dB implementation loss limit, and some even touch the theoretical limit. The DVB-S2 measurements, see table 12.2, show a much better performance for a given code rate making it possible to send data on even noisier channels. Two 8PSK code rate values could not be output with the instrument so they were not measured. With 8PSK the data rate is doubled while the C/N limit is roughly deteriorated by 3 dB in comparison to DVB-S. With the increased data rate it is possible to send several more TV channels on the same frequency.

12.2 LNB driver

At first the chip was unable to put out the high voltage level. Fairly quick an error was found in the schematic. One pin that should be AC coupled to the output had mistakenly been directly coupled to the output. This made the chip go into current protection mode. After correcting the mistake the design worked as planned.

12.2.1 Measurements

In the following text measurements on the design are presented. The LNB driver must handle two voltage levels with and without 22 kHz added (tabulated in chapter 6). As can be seen in picture 12.5 the driver handles the crossing between no tone and tone smoothly. The tone frequency is also within specification.

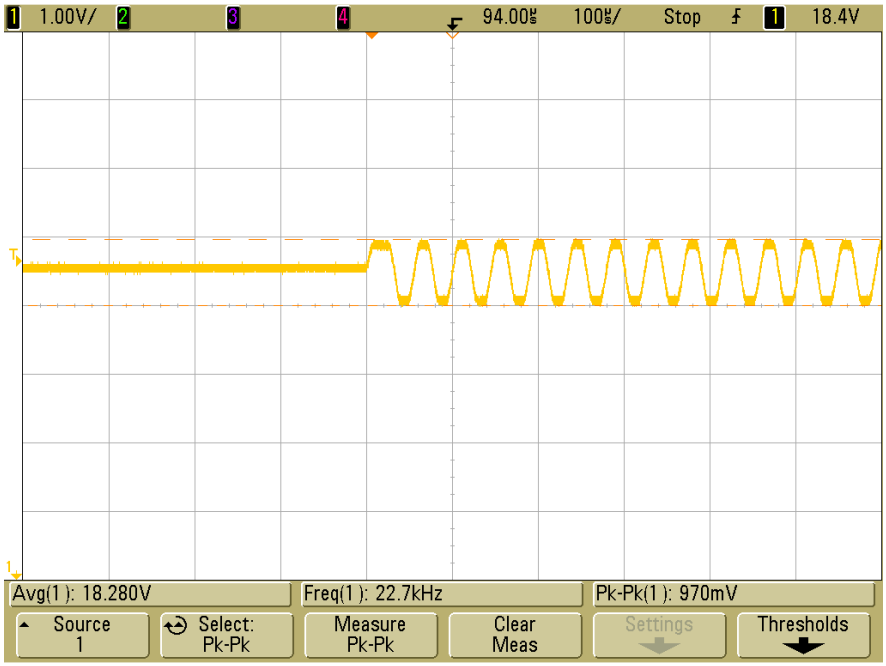

Figure 12.5 - LNB driver, right; high voltage, left; high voltage (22 kHz added)

Figure 12.6 show switching between the high and low voltage output while the tone is on. The slope becomes a bit jagged but this is a consequence of the chip design (when the 22 kHz is on) and nothing that will alter the driver function.

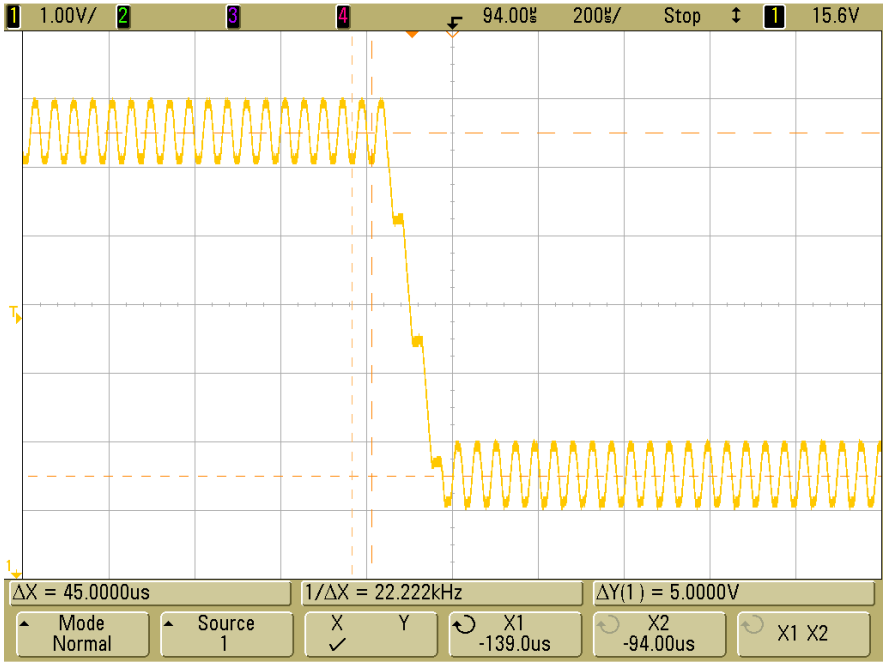

Figure 12.6 - LNB driver, switching between high and low voltage (22 kHz added)

In figure 12.7 the switching behavior from high to low without tone can be seen. The transition is smooth and there are no real remarks.

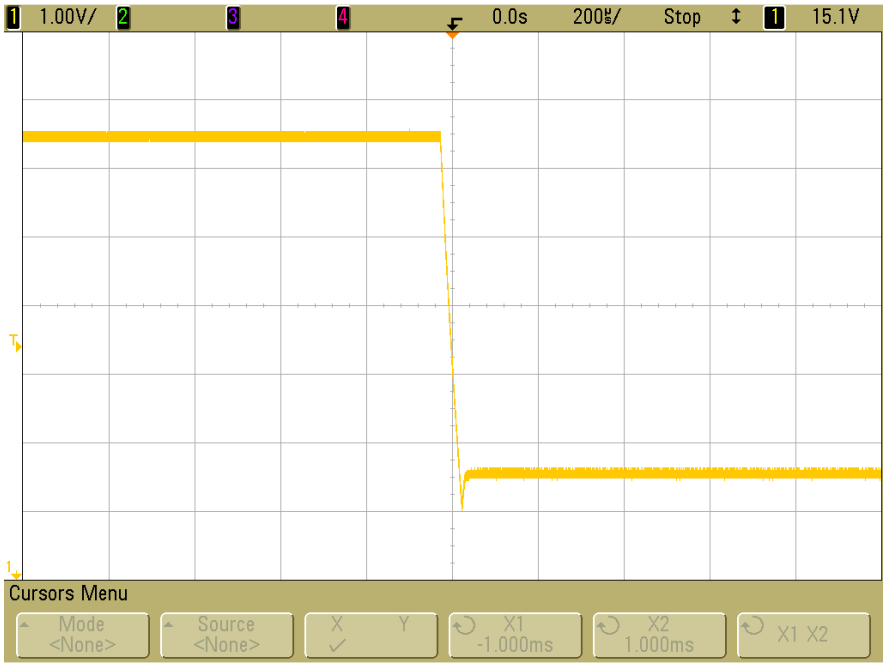

Figure 12.7 - LNB driver, switching between high and low voltage

The transition from low to high takes a great deal more time than from high to low. This can be seen in picture 12.8 and 12.9. The behavior is a consequence of the step up converter that takes some time to get the voltage up to the high level.

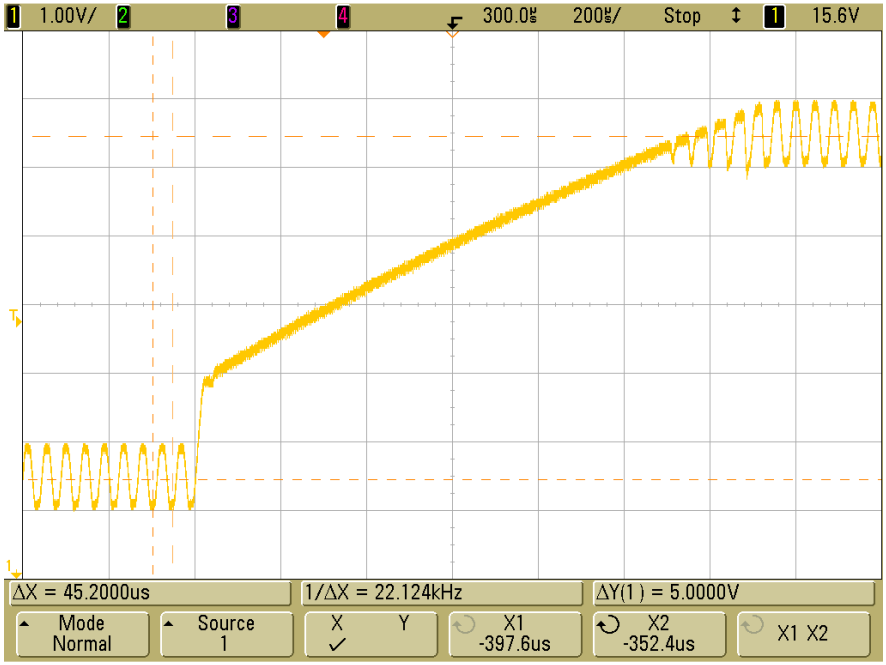

Figure 12.8 - LNB driver, switching between low and high voltage (22 kHz added)

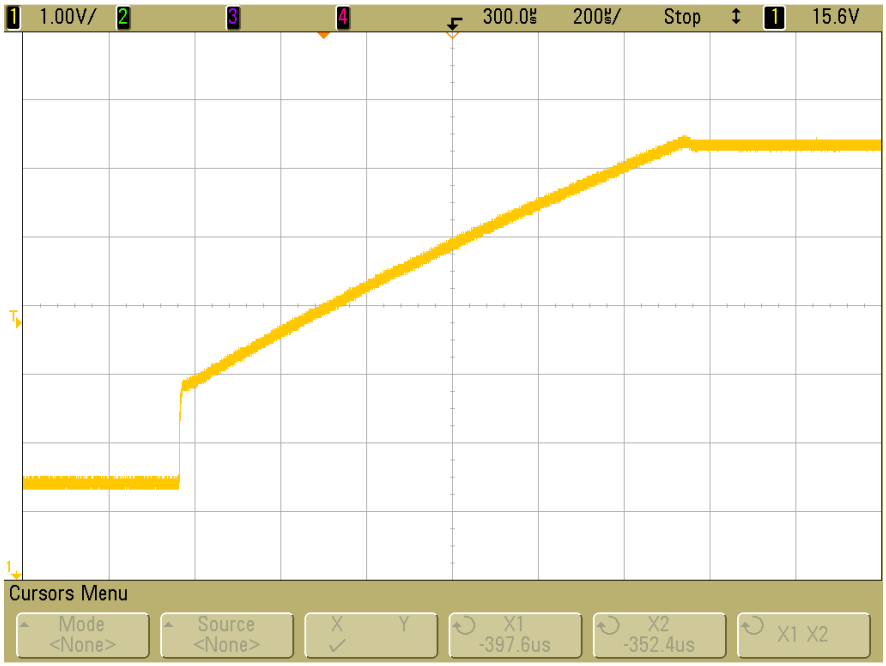

Figure 12.9 - LNB driver, switching between low and high voltage

The measurements on the LNB driver card show good behavior with no remarks. The output ripple was also measured but is not shown as this is almost immeasurable with the equipment available and therefore nothing to worry about.

13 Result

The purpose that was set up in the beginning of this report has been fulfilled. The result of this thesis is a fully functionally DVB-S2 system. The advantages of the DVB-S2 system, is the best transmission performance, total flexibility and reasonable receiver complexity. The disadvantages are pretty obvious because of the systems short age. The conversion from DVB-S to DVB-S2 will take approximately 10 – 15 years like the entrance of HDTV. The testing and measurements that has been made during this master thesis has strengthened the thesis and the theories about the DVB-S2 system. The measurements performed on the DVB-S sections of the chip gave exemplary results. Comparing these results with corresponding measurements performed on the DVB-S2 section showed much better performance with the same coding rates, which made our expectations from the literature study fulfilled. Applications of the DVB-S2 system can be found in broadcasting television programs, interactive services, data content distribution and Internet trunking.

The future seems pretty bright for the DVB-S2 standard. Many companies are manufacturing their products according to the DVB-S2 standard. The sought-after characteristic on the market is HDTV where high data-rate is a requirement. The higher data-rate, the greater quality will HDTV have. Separate set-top-boxes are soon going to be taken off the market. Placing them into the television set, forces the manufacturers to come up the new solutions for media entertainment, which is an important aspect we find our self in the information era. People are getting more and more aware of television and entertainment. Almost every household have a desire to one day own a HDTV with a built in set-top-box, where the receiver might be a DVB-S2 receiver.

14 Conclusion

This report has gradually been developed to the present version, part by part from different scientific areas. From the beginning this thesis was said to be too difficult to even be a master thesis due to several difficult moments. All these moments could be structured down to own fields and give base for several master theses. The literature study was the most important part since both of us had limited experience and knowledge of digital television. Studying all the modulation techniques, both analogue and digital gave us an idea what was expected from us, and how much effort and time this thesis would require.

The second part of the literature study was to understand how digital television works and why different standards are needed for different broadcast media. Most important was to understand the differences between the first and second generation of the satellite DVB standard. The following moments were the most challenging and the most enjoyable to do, the actual design of both schematics and PCB layout. Even though neither of us had much previous experience in design; one could say that it went pretty well. The knowledge and experience we got after the prototypes were made was priceless. Now we know how much effort and knowledge that are needed in order to come even close to a functioning prototype. Fortunately the errors in the design were few.

When the components were mounted, the testing of the prototype appeared to be the easy part since there were not many mistakes in the design. One critical error of the LNB driver design was found during the measurement phase but could be temporarily corrected. In the future, a smart thing would be to have extra control checkpoints on the schematics level before PCB layout. This will prevent small and annoying errors.

14.1 The future of digital television

Looking at the past evolution of radio and television the next area of exploration will most certainly be DTV reception among handhelds. With the DVB-H standard already set, field trials have been performed in 2006 and several more countries will begin in 2007. Mobile media of different forms has seen an up going trend and many new service providers will eventually pop up, making handhelds more and more attractive to the consumers. There are a few more standards for mobile purposes but DVB-H is the most used so far.

15 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ACI	Adjacent Channel Interference
ACM	Adaptive Coding and Modulation
AM	Amplitude Modulation
ATSC	Advanced Television Systems Committee
BCH	Bose-Chaudhuri-Hocquenghem
BER	Bit Error Rate
BOM	Bill Of Material
BS	Broadcasting Services
CCI	Co-Channel Interference
CCM	Constant Coding and Modulation
C/I	Carrier to Interference
CM	Common mode
C/N	Carrier to Noise ratio
CNR	Carrier-to-Noise Ratio
COFDM	Coded Orthogonal Frequency Division Multiplex
CRT	Cathode-Ray Tube
CS	Communication Satellite
DM	Differential mode
DTH	Direct-to-home
DSB	Double Sideband
DSL	Digital Subscriber Line
DSGN	Digital Satellite News Gathering
DTV	Digital Television
DVB	Digital Video Broadcasting
DVB-RCS	DVB-Return Channel Standard
EBU	European Broadcasting Union
EMC	Electro-Magnetic Compliance
EHF	Extremely High Frequency
EPG	Electronic Program Guides
ETSI	European Telecommunications Standards Institute
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FM	Frequency Modulation
FSK	Frequency Shift Keying
GUI	Graphic User Interface
HDTV	High Definition Television
IC	Integrated Circuit
IF	Intermediate Frequency
IP	Internet Protocol
IS	Interactive Services
ISDB	Integrated Services Digital Broadcasting
JPEG	Joint Picture Experts Group
LAN	Local Area Network

LNB	Low Noise Block down converter
LDPC	Low Density Parity Check
MER	Modulation Error Ratio
MPEG	Motion Pictures Experts Group
MPE-FEC	Multi-Protocol Encapsulation – Forward Error Correction
MSK	Minimum Shift Keying
MUSE	MUltiple sub-nyquist Sampling Encoding
MUX	Multiplexer
NHK	Nippon Hōsō Kyōkai
NTSC	National Television Systems Committee
PAL	Phase Alternation Line
PCB	Printed Circuit Board
PER	Package Error Rate
PLL	Phase Locked Loop
PRBS	Pseudo Random Binary Sequence
PSI	Program Specific Information
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QEF	Quasi Error Free
QPSK	Quaternary Phase Shift Keying
RF	Radio Frequency
RFID	Radio Frequency Identification
SBTVD	Sistema Brasileiro de Televisão Digital
SECAM	Séquentiel couleur à mémoire
SDTV	Standard Definition Television
SHF	Super High Frequency
SMT	Surface Mount Technology
SSB	Single Sideband
S/N	Signal to Noise ratio
SMATV	Satellite Master Antenna Television
TPS	Transmission Parameter Signaling
TS	Transport Stream
UHF	Ultra High Frequency
VCM	Variable Coding and Modulation
VHF	Very High Frequency
VSB	Vestigial Sideband

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