Data Converters In VLSI Systems

A

Project Report

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Abstract

TRANSISTOR LEVEL IMPLEMENTATION OF PHASE LOCKED LOOP (PLL)

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Keywords:
Data Converters, VLSI Systems, Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC), Successive Approximation Register (SAR), Sigma-Delta ADC, Signal Processing, Electronic Systems.

In this report, we endeavor to understand Data Converters in VLSI Systems, focusing on the theoretical aspects of the Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC). We explore the principles of operation, design considerations, and performance metrics of these converters. The report also delves into the different architecture of ADCs and DACs, including their working principles, advantages, and disadvantages. We discuss the various types of ADCs, such as Successive Approximation Register (SAR) and Sigma-Delta ADCs, and their applications in modern VLSI systems. The report highlights the importance of data converters in bridging the gap between analog and digital domains, enabling efficient signal processing and communication in electronic systems.

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Chapter 1

Introduction

Data conveters are systems that convert analog signals to digital signals and digital signals to analog signals. These converters are termed as DACs (Digital to Analog Converters) and ADCs (Analog to Digital Converters). The conversion of signals is essential in modern days as most of the systems are digital in nature. The conversion from Analog to Digital is majorly done by Quantizaion and Sampling. The quantization is the process of mapping a large set of input values to a smaller set of output values. The sampling is the process of converting a continuous signal into a discrete signal by taking samples at regular intervals. The conversion from Digital to Analog is done by reconstructing the signal from the digital values. The reconstruction is done by using various techniques such as interpolation, filtering, etc

$$\phi_{\text{out}}(t) = \phi_{\text{in}}(t) + \text{const.} \tag{1.1}$$

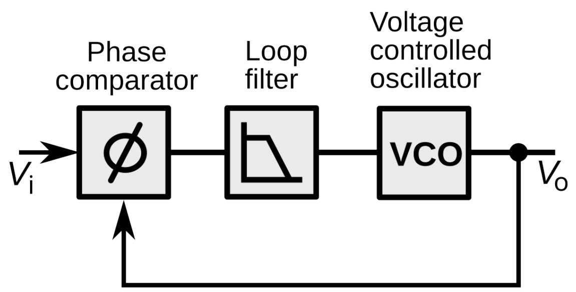

Figure 1.1: Simple analog phase locked loop

1.1 Motivation

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1.5 PLL Terminologies

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- **Digital PLLs (DPLLs):**
- **All-Digital PLLs (ADPLLs):**

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- **Microprocessors:**
- **Power Electronics:**

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