2017-2018

**DCS-2**

**EC-407**

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SERIAL IN PARALLEL OUT SHIFT REGISTER

# CODE

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity sipo\_code is

Port ( ip : in STD\_LOGIC;

clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

q : inout STD\_LOGIC\_VECTOR(0 to 5));

end sipo\_code;

architecture Behavioral of sipo\_code is

begin

one:process(ip,rst,clk)

begin

if(rst='1')

then

q<="000000";

else if(clk='1' and clk'event)

then

q(0)<=ip;

q(1)<=q(0);

q(2)<=q(1);

q(3)<=q(2);

q(4)<=q(3);

q(5)<=q(4);

--q(6)<=q(5);

end if;

end if;

end process;

end Behavioral;

# TEST BENCH

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY sipo\_tb IS

END sipo\_tb;

ARCHITECTURE behavior OF sipo\_tb IS

COMPONENT sipo\_code

PORT(

ip : IN std\_logic;

clk : IN std\_logic;

rst : IN std\_logic;

q : INOUT std\_logic\_vector(0 to 5)

);

END COMPONENT;

--Inputs

signal ip : std\_logic := '0';

signal clk : std\_logic := '0';

signal rst : std\_logic := '0';

--BiDirs

signal q : std\_logic\_vector(0 to 5);

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: sipo\_code PORT MAP (

ip => ip,

clk => clk,

rst => rst,

q => q

);

-- -- Stimulus process

stim\_proc: process

begin

-- hold reset state for 100 ns.

ip<='1';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='0';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='0';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='0';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='1';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='1' ;

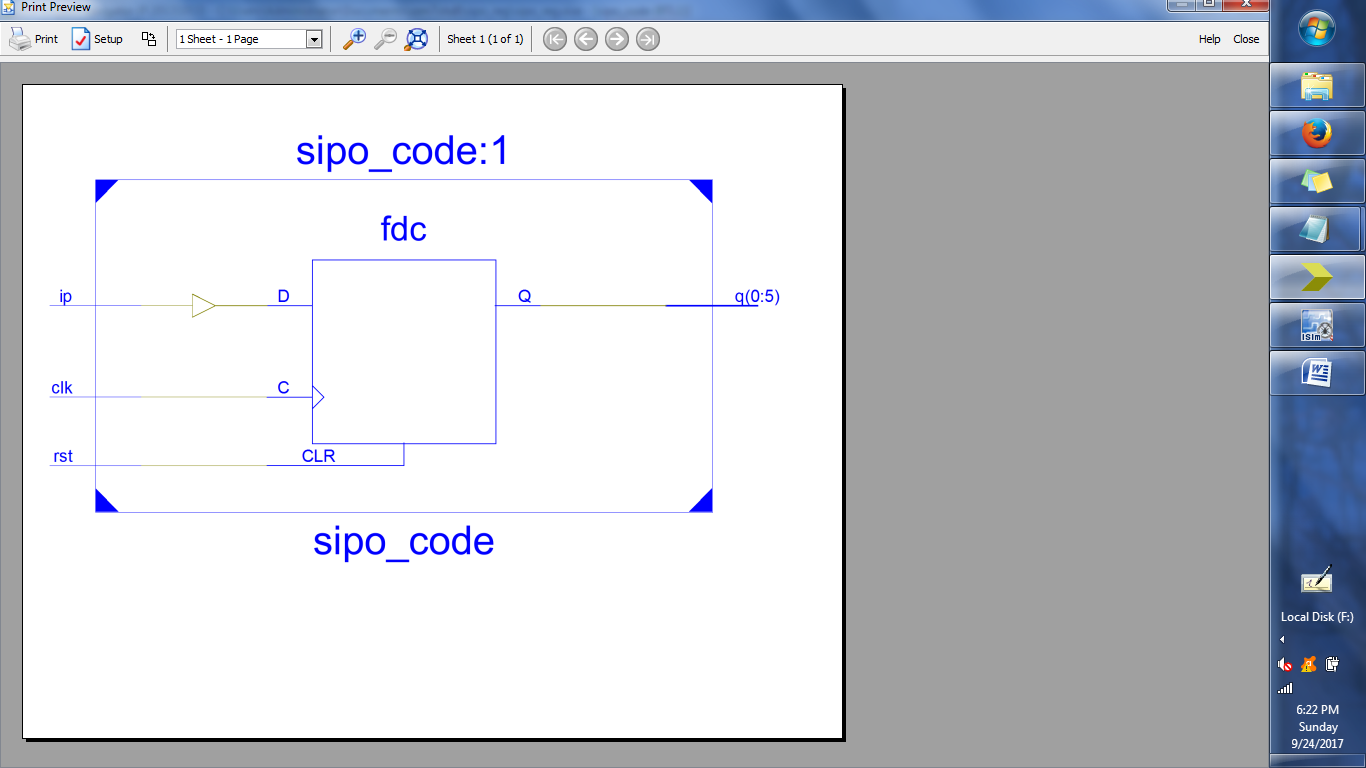
clk<='1 ';

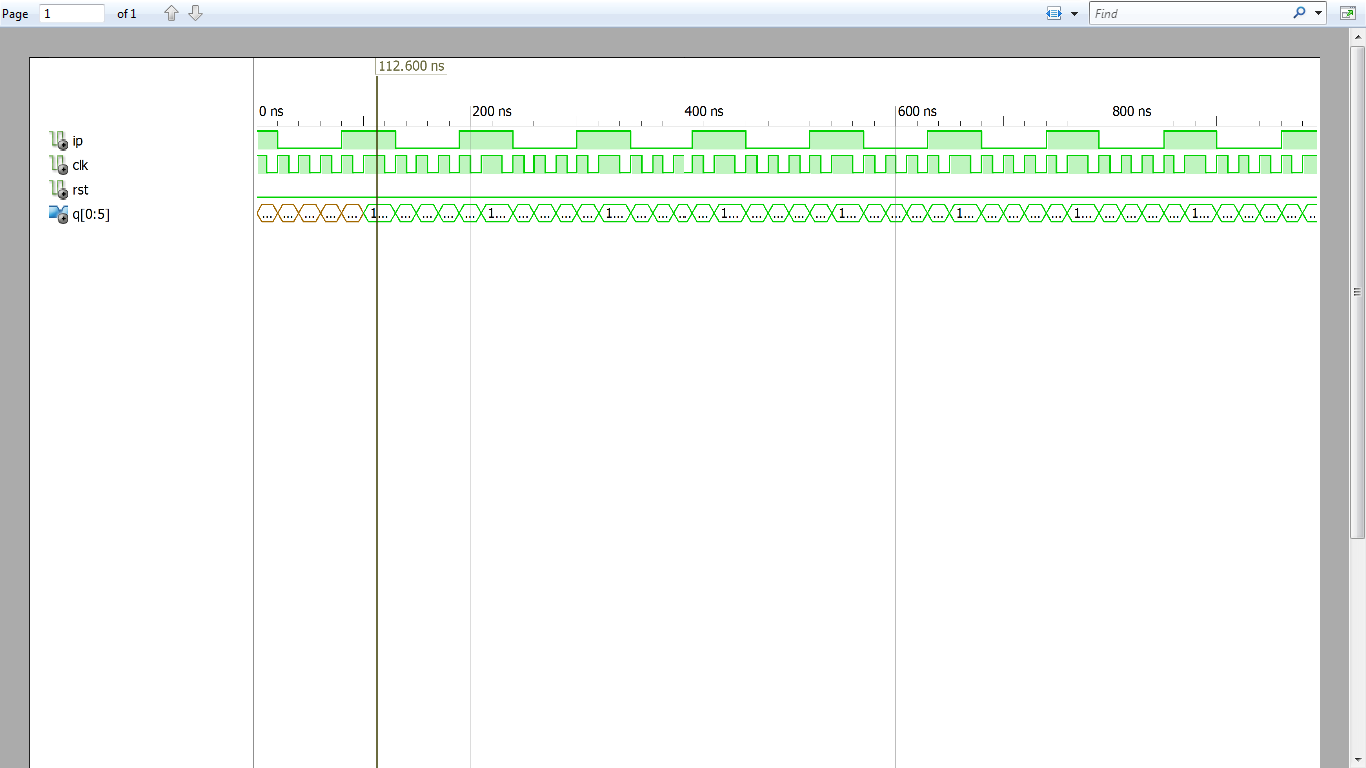
wait for 10 ns;

end process;

END;

## OUTPUT





INTRODUCING A DELAY OF 1 AND 2 CYCLES

## CODE

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity delay\_code is

Port ( ip : in STD\_LOGIC;

rst : in STD\_LOGIC;

clk : in STD\_LOGIC;

d : inout STD\_LOGIC\_vector(0 to 2);

q : inout STD\_LOGIC\_vector(0 to 2));

end delay\_code;

architecture Behavioral of delay\_code is

begin

process(ip,clk,rst)

begin

if (rst='1')

then

q<="000";

else if(clk='1' and clk'event)

then

d(0)<=ip;

q(0)<=d(0);

d(1)<=q(0);

q(1)<=d(1);

d(2)<=q(1);

q(2)<=d(2);

end if;

end if;

end process;

end Behavioral;

# TEST BENCH

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY delay\_tb IS

END delay\_tb;

ARCHITECTURE behavior OF delay\_tb IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT delay\_code

PORT(

ip : IN std\_logic;

rst : IN std\_logic;

clk : IN std\_logic;

d : INOUT std\_logic\_vector(0 to 2);

q : INOUT std\_logic\_vector(0 to 2)

);

END COMPONENT;

--Inputs

signal ip : std\_logic := '0';

signal rst : std\_logic := '0';

signal clk : std\_logic := '0';

--BiDirs

signal d : std\_logic\_vector(0 to 2);

signal q : std\_logic\_vector(0 to 2);

-- Clock period definitions

--constant clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: delay\_code PORT MAP (

ip => ip,

rst => rst,

clk => clk,

d => d,

q => q

);

stim\_proc: process

begin

-- hold reset state for 100 ns.

--wait for 100 ns;

ip<='1';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='0';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='0';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='0';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='1';

clk<='1';

wait for 10 ns;

clk<='0';

wait for 10 ns;

ip<='1' ;

clk<='1';

wait for 10 ns;

end process;

END;

OUTPUT

