16-Mb RADIATION-HARDENED SRAM

Check for Samples: SMV512K32-SP

FEATURES

- **20-ns Read, 13.8-ns Write Through Maximum Access Time**
- **Functionally Compatible With Commercial 512K x 32 SRAM Devices**
- **Built-In EDAC (Error Detection and Correction) to Mitigate Soft Errors**
- **Built-In Scrub Engine for Autonomous Correction**
- **CMOS Compatible Input and Output Level, Three State Bidirectional Data Bus**
  - **3.3 ±0.3-V I/O, 1.8 ±0.15-V CORE**
- **Radiation Performance** (1)
  - **Uses Both Substrate Engineering and Radiation Hardened by Design (HBD)** (2)
  - **TID Immunity > 3e5 rad (Si)**
  - **SER < 5e-17 Upsets/Bit-Day (Core Using EDAC and Scrub)** (3)
  - **Latch up immunity > LET = 110 MeV (T = 398K)**
- **Available in a 76-Lead Ceramic Quad Flatpack**
- **Engineering Evaluation (/EM) Samples are Available** (4)

(1) Radiation tolerance is a typical value based upon initial device qualification. Radiation Data and Lot Acceptance Testing is available – contact factory for details.
(2) *HardSIL*™ technology and memory design under a license agreement with Silicon Space Technology (SST).
(3) SER calculated using CREME96 for geosynchronous orbit, solar minimum.
(4) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. no burn-in, etc.) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of -55°C to 125°C or operating life.

DESCRIPTION

The SMV512K32 is a high performance asynchronous CMOS SRAM organized as 524,288 words by 32 bits. It is pin selectable between two modes: master or slave. The master device selection provides user defined autonomous EDAC scrubbing options. The slave device selection employs a scrub on demand feature that can be initiated by a master device. Three read cycles and four write cycles (described below) are available depending on the user needs.

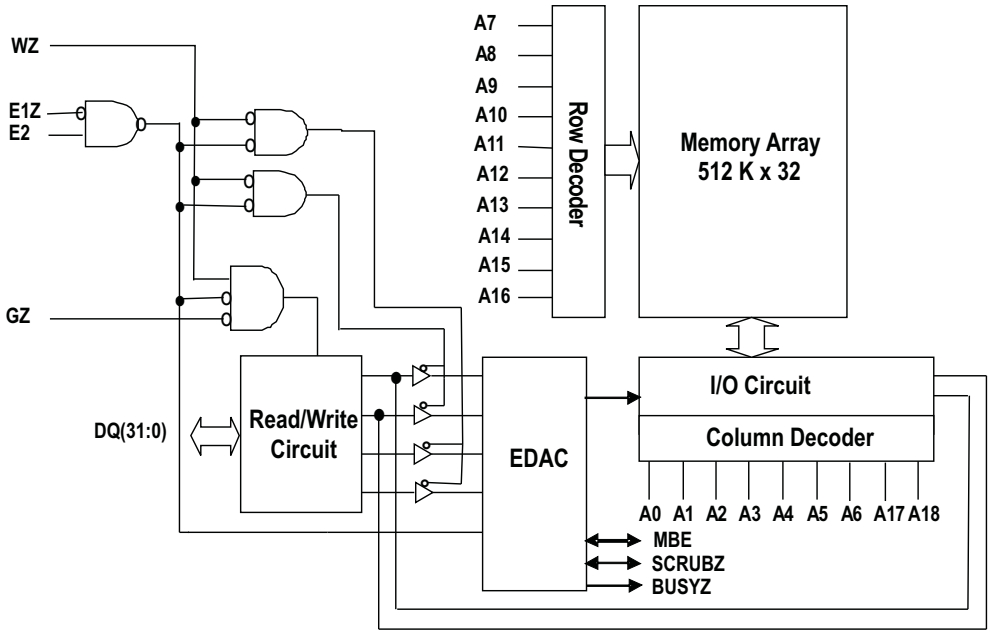
SILICON SPACE TECHNOLOGY

HardSIL™ is a trademark of Silicon Space Technology (SST).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Figure 1. SMV512K32 Block Diagram



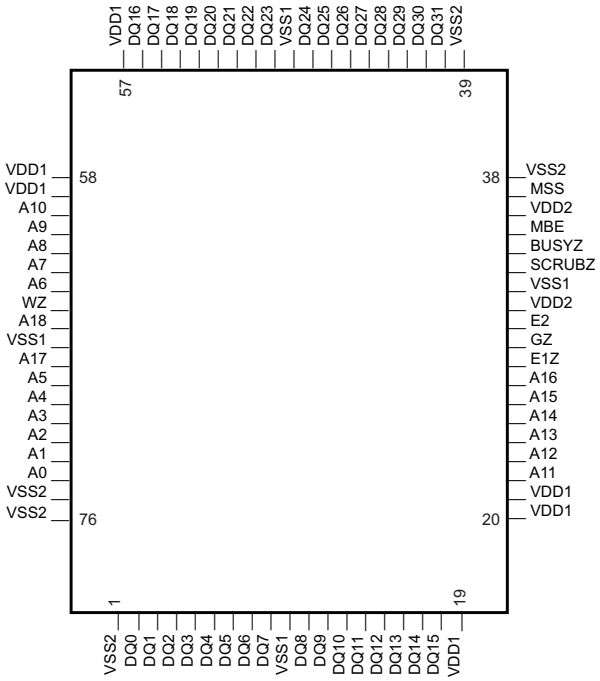


Figure 2. SMV512K32 Pin Out

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

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TERMINAL FUNCTIONS

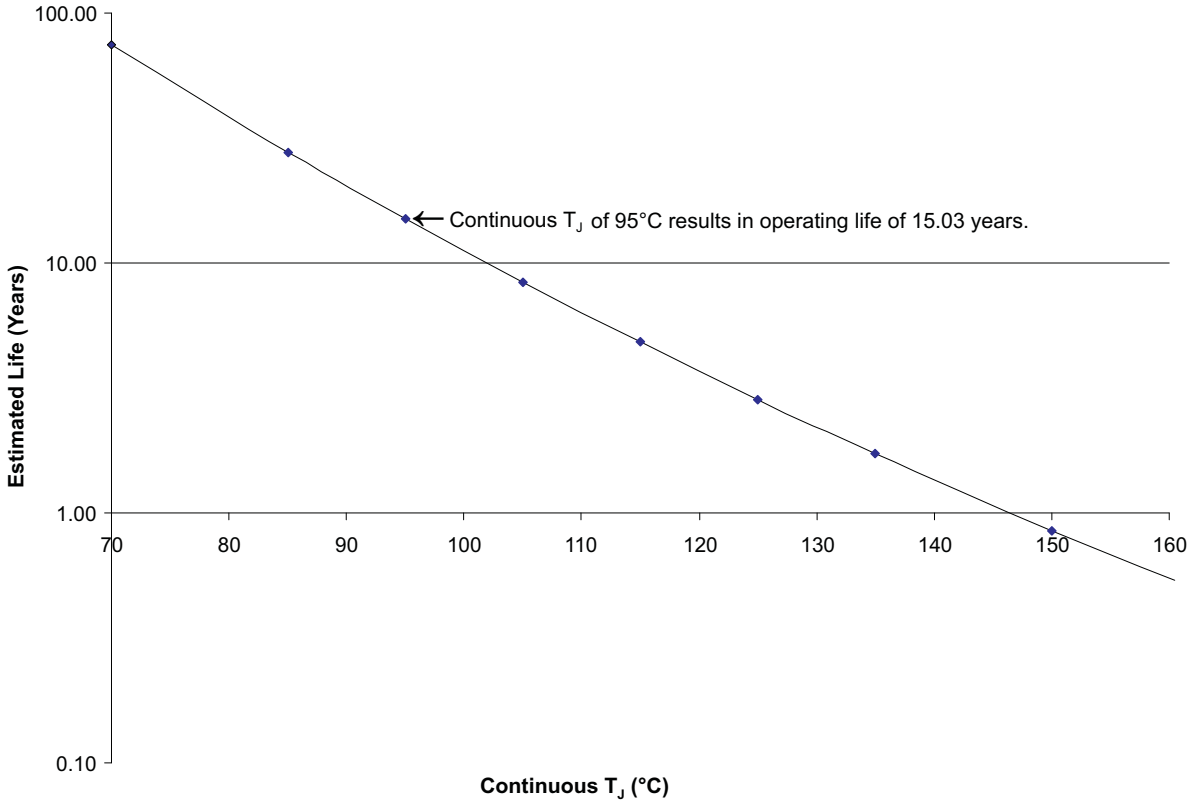
PIN NAME	TYPE	ACTIVE	DESCRIPTION
A[18:0]	Input	N/A	Address
DQ[31:0]	Bidirectional	N/A	Data input/output
E1Z	Input	Low	Chip enable - 1
E2	Input	High	Chip enable - 2
WZ	Input	Low	Write enable
GZ	Input	Low	Output enable for bidirectional input/output
VDD1	Power	N/A	Power supply (1.8 V)
VDD2	Power	N/A	Power supply (3.3 V)
VSS1	Power	N/A	Ground (core)
VSS2	Power	N/A	Ground (I/O)
MSS	Input	N/A	Used for setting master/slave selection. Connect to VSS2 for master operation and VDD2 for slave operation.
MBE	Bidirectional	High	Multiple bit or single bit error indicator (output - user programmable) EDAC function select (input)
SCRUBZ	Bidirectional	Low	Master SCRUBZ (output) Slave SCRUBZ (input)
BUSYZ	Output	Low	Master BUSYZ (output) Slave (do not use)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted). (1)

		VALUE	UNIT
V_{DD1}	DC supply voltage(core)	–0.3 to 2.0	V
V_{DD2}	DC supply voltage (I/O)	–0.3 to 3.8	V
$V_{I/O}$	Voltage on any pin	–0.3 to 3.8	V
T_{STG}	Storage temperature	–65 to 150	°C
P_D	Maximum power dissipation	1.2	W
T_J	Maximum junction temperature	150	°C
θ_{JC}	Thermal resistance, junction-to-case	5	°C/W
I_I	DC input current	±5	mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



Notes:

(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Mil-Prf 38535, appendix B, section B.3.4 targets a 15 year operating life at 65°C ≤ T_J ≤ 95°C.

(3) Above derating is based upon a worse-case power supply current condition for continuous $I_{DD1}(OP_2)$ write operation at 50 MHz and may not reflect actual usage.

Figure 3. SMV512K32 Operating Life Derating Chart (Electromigration Fail Mode)

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	TYP	MAX	UNIT
V_{DD1}	DC supply voltage (core)	1.7	1.8	1.9	V
V_{DD2}	DC supply voltage (I/O)	3.0	3.3	3.6	V
T_C	Case temperature range	–55		125	°C
V_{IN}	DC input voltage	0		V_{DD2}	V

ELECTRICAL CHARACTERISTICS

T_C = -55°C to 125°C, V_{DD1} = 1.7 V to 1.9 V, V_{DD2} = 3 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IH}	HIgh-level input voltage				0.7 x V_{DD2}		V
V_{IL}	Low-level input voltage					0.3 x V_{DD2}	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, V_{DD2} = V_{DD2}(min)				0.2 x V_{DD2}	V
V_{OH}	High-level output voltage	I_{OH} = -4 mA, V_{DD2} = V_{DD2}(min)			0.8 x V_{DD2}		V
C_{IN} (1)	Input capacitance	f = 1 MHz at 0 V				4.5	pF
C_{IO} (1)	Bidirectional I/O capacitance	f = 1 MHz at 0 V				4.5	pF
I_{IN}	Input leakage current	V_{IN}=V_{DD2} and V_{SS}			–500	500	nA
I_{OZ}	Tri-state output leakage current	V_O= V_{DD2} and V_{SS} V_{DD2} = V_{DD2}(max), GZ=V_{DD2}(max)			–500	500	nA
I_{OS} (2) (3)	Short-circuit output current	V_{DD2} = V_{DD2}(max), V_O = V_{DD2} V_{DD} = V_{DD2}(max), V_O = V_{SS}			–46	46	mA
$I_{DD1}(OP_1)$	V_{DD1} supply operating current at 1 MHz	Input: V_{IL} = V_{SS} + 0.2 V, V_{IH} = V_{DD2} - 0.2 V, I_{OUT} = 0 A, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	Write	–55°C to 25°C		18	mA
				125°C		31	
			Read	–55°C to 25°C		13	
				125°C		27	
$I_{DD1}(OP_2)$	V_{DD1} supply operating current at 50 MHz	Input: V_{IL} = V_{SS} + 0.2 V, V_{IH} = V_{DD2} - 0.2 V, I_{OUT} = 0 A, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	Write	–55°C to 25°C		635	mA
				125°C		460	
			Read	–55°C to 25°C		365	
				125°C		315	
$I_{DD2}(OP_1)$	V_{DD2} supply operating current at 1 MHz	Input: V_{IL} = V_{SS} + 0.2 V, V_{IH} = V_{DD2} - 0.2 V, I_{OUT} = 0 A, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	Write	–55°C to 25°C		255	µA
				125°C		255	
			Read	–55°C to 25°C		5.2	mA
				125°C		5.1	
$I_{DD2}(OP_2)$	V_{DD2} supply operating current at 50 MHz	Input: V_{IL} = V_{SS} + 0.2 V, V_{IH} = V_{DD2} - 0.2 V, I_{OUT} = 0 A, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	Write	–55°C to 25°C		5.9	mA
				125°C		1.2	
			Read	–55°C to 25°C		275	
				125°C		120	
$I_{DD1}(SB)$ (4)	Supply stand-by current at 0 MHz	CMOS inputs, I_{OUT} = 0 A E1Z = V_{DD2} - 0.2 V, E2 = GND, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	–55°C to 25°C			0.375	mA
			125°C			17	
$I_{DD2}(SB)$ (4)	Supply stand-by current at 0 MHz	CMOS inputs, I_{OUT} = 0 A E1Z = V_{DD2} - 0.2 V, E2 = GND, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	–55°C to 25°C			330	µA
			125°C			330	
$I_{DD1}(SB)$ (4)	Supply stand-by current A[16:0] at 50 MHz	CMOS inputs, I_{OUT} = 0 A E1Z = V_{DD2} - 0.2 V, E2 = GND, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	–55°C to 25°C			4.4	mA
			125°C			21	
$I_{DD2}(SB)$ (4)	Supply stand-by current A[16:0] at 50 MHz	CMOS inputs, I_{OUT} = 0 A E1Z = V_{DD2} - 0.2 V, E2 = GND, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)	–55°C to 25°C			1.6	mA
			125°C			0.8	

(1) Measured for initial qualification and after process or design changes that could affect input/output capacitance.
(2) Provided as a design limit but not guaranteed or tested.
(3) No more than one output may be shorted at a time for maximum duration of one second.
(4) V_{IH} = V_{DD2}(max), V_{IL} = 0 V

OPERATIONS

SMV512K32 has four control inputs called chip enable-1 (E1Z), chip enable-2 (E2), write enable (WZ) and output enable (GZ); 19 address inputs A[18:0] and a 32-bit bidirectional data bus DQ[31:0]. E1Z and E2 enable control device selection, active and stand-by modes (with and without scrub). WZ controls read and write operations. During read operation, GZ must be asserted to enable the outputs.

Table 1. SRAM Device Control Operation Truth Table

E1Z	E2	GZ	WZ	MBE	I/O MODE	MODE
H	X	X	X	X	DQ[31:0] 3-State	Standby without EDAC scrub enable
L	L	X	X	X	DQ[31:0] 3-state	Standby with EDAC scrub enable(1)
L	H	L	H	X	DQ[31:0] Data out	Word read
L	H	X	L	X	DQ[31:0] Data in	Word write
L	H	H	H	L	DQ[31:0] 3-state	3-state
L	H	H	H	H	DQ[31:0] Data in/out	EDAC function select (see Table 6)(2)

(1) During SCRUB mode, MBE is 3-state if GZ is high and indicates multiple or single bit error if GZ is low.
(2) Special precautions must be observed to prevent accidental over-writing of the Control Register in the memory after a bit error is detected and the memory drives MBE high (please refer to the next section).

Procedures for Controlling the MBE Pin

A 1-kΩ resistor must be attached from the MBE pin to ground to insure that MBE cannot float high during time intervals when it is not actively driven HIGH by the memory or actively driven by the external memory control.

During normal EDAC operation, the control registers are set as shown by Sequence 1 in Table 2. Whenever the EDAC circuit encounters either a multiple-bit error or single-bit error (depending on user configuration), the MBE pin is driven high by the memory as shown by Sequence 2 in Table 2 . Following this the MBE will need to be reset (low) to restore the detection circuit for the next bit error event. The MBE pin will be pulled low by the 1-kΩ resistor when GZ is switched to high state. However, to accomplish the MBE reset properly and avoid an accidental write to the control register, the memory must first be disabled by switching either E1Z to high or E2 to low (Sequence 3) before switching GZ from low to high (Sequence 4). Note however, that if E1Z is switched to high this will disable scrub during the interval that GZ is being set high after the memory is disabled.

The memory must remain disabled long enough to insure that MBE is pulled low before the memory is enabled again. During the time the memory is disabled the address at which the MBU was detected must also be changed to access the last known error free address. After the address is changed the memory can be enabled with GZ high. Then an Output Enable-controlled read operation can be performed using the last known error free address. This turns off the MBE error flag in the memory and causes the memory to drive MBE low after the GZ-controlled output data valid time, t_{GLMV}.

This procedure resets the memory back into its normal EDAC read state in which the memory will drive MBE low sequentially for each read operation until the next bit error is encountered. This avoids accidental over-writing of the Control Register in the memory. After this procedure is completed the system protocol for responding to bit errors can be executed.

Table 2. Example Control Settings for Resetting MBE

SEQUENCE	E1Z	E2	GZ	WZ	MBE	I/O MODE	MODE
1	L	H	L	H	L	DQ[31:0] Data out	Normal read mode with EDAC enabled
2	L	H	L	H	H	DQ[31:0] Data out	MBE driven high when single bit or multiple bit error (depending on user configuration) is detected during read
3	H	L	L	H	H	DQ[31:0] Data out	Memory disabled
4	H	L	H	H	H → L	DQ[31:0] Tri-state	Outputs tri-stated and MBE pulled low by load R
5	L	H	H	H	L	DQ[31:0] Tri-state	Read at a last known error free address (1)
6	L	H	L	H	L	DQ[31:0] Data out	Output enable-controlled read (2)

(1) During this operation MBE drive circuitry in the memory is tri-stated but MBE is held low by the 1-kΩ resistor to ground.
(2) During this operation MBE is actively driven low by the MBE drive circuitry in the memory after a time, t_{GLMV}, and the memory is back to the original state corresponding to normal read mode with EDAC enabled.

Read Operations

A combination of E1Z low, E2 high and WZ high defines a read cycle. GZ low enables the outputs to drive read data to the DQ pins. Read access time is measured from the latter of device enable, output enable or valid address to valid data output.

- SRAM read cycle 1 (Figure 4): Address controlled access is initiated by a change in address inputs while device is selected with WZ high and GZ low. Valid data appears on DQ[31:0] after a specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as the device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time t_{AVAV}.
- SRAM read cycle 2 (Figure 5): Chip-enable controlled access is initiated by the latter of either E1Z or E2 going active while GZ is low, WZ is high, and address remains stable for the entire cycle. After the specified time t_{ETQV}, the 32-bit word addressed by A[18:0] is accessed and appears at DQ[31:0].
- SRAM read cycle 3 (Figure 6): Output-enable controlled access is initiated by GZ going active while E1Z and E2 are asserted, WZ is de-asserted, and address is stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

  If EDAC is turned on during read operation:

  - If MBE is low, data is valid.
  - If MBE is high, data is corrupted (dependent on EDAC programming configuration on A[12], MBE can indicate a single bit or double bit error). Single bit error is correctable by EDAC.

Table 3. AC Characteristics Read Cycle (1)

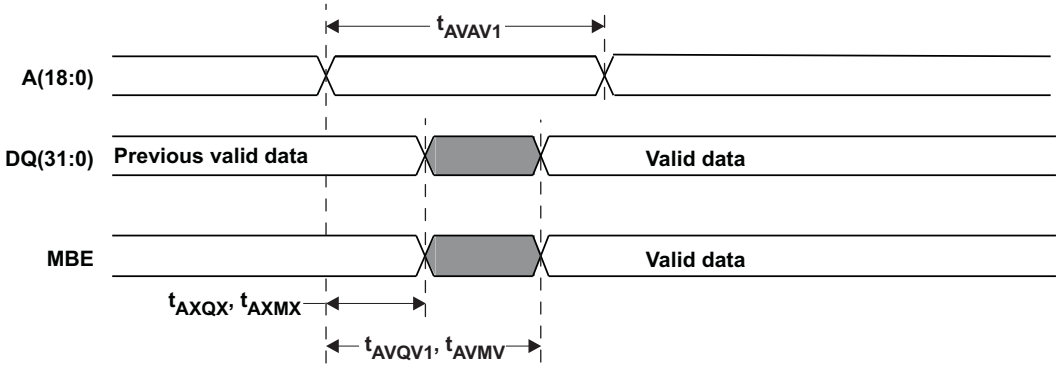
SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{AVAV1}	Read cycle time	20		ns	Figure 4
t_{AVQV1}	Address to data valid from address change (2)		20	ns	Figure 4
t_{AXQX}	Output hold time	7.5		ns	Figure 4
t_{GLQX1}	GZ-controlled output enable time	3.5		ns	Figure 6
t_{GLQV}	GZ-controlled output data valid		8.6	ns	Figure 6
t_{GHQZ1}	GZ-controlled output enable tri-state time	3.5	5	ns	Figure 6
t_{ETQX}	E-controlled output enable time	3.5		ns	Figure 5
t_{ETQV}	E-controlled access time		20	ns	Figure 5
t_{EFQZ}	E-controlled tri-state time	3.5	5	ns	Figure 5
t_{AVMV}	Address to error flag valid		20	ns	Figure 4
t_{AXMX}	Address to error flag hold time from address change	7.5		ns	Figure 4

(1) T_C = -55°C to 125°C, V_{DD1} = 1.7 V to 1.9 V, V_{DD2} = 3 V to 3.6 V (unless otherwise noted).
(2) 20 ns at 5-pF load.

Table 3. AC Characteristics Read Cycle (1) (continued)

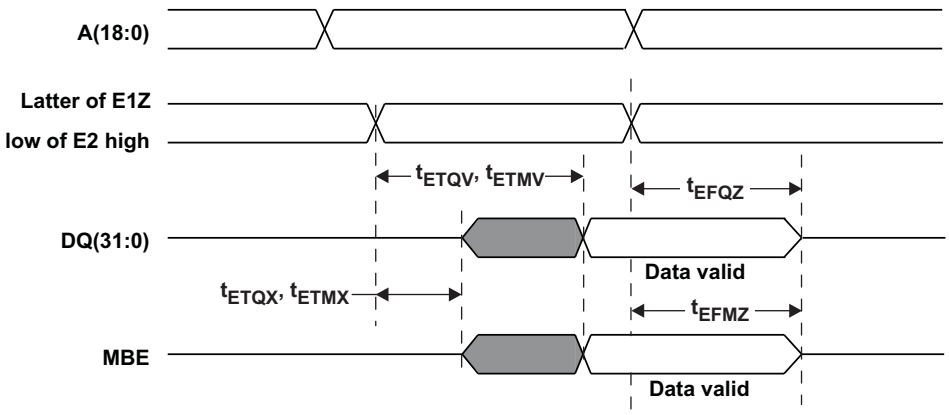
SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{GLMV}	GZ-controlled error flag valid		8.6	ns	Figure 6
t_{GLMX}	GZ-controlled error flag enable time	3.5		ns	Figure 6
t_{ETMX}	E-controlled error flag enable time	3.5		ns	Figure 5
t_{ETMV}	E-controlled error flag time		20	ns	Figure 5
t_{GHMZ} (3)	GZ-controlled error flag tri-state time	3.5	5	ns	Figure 6
t_{EFMZ} (3)	Chip enable change to MBE tri-state	3.5	5	ns	Figure 5

(3) Parameters ensured by design and/or characterization if not production tested.



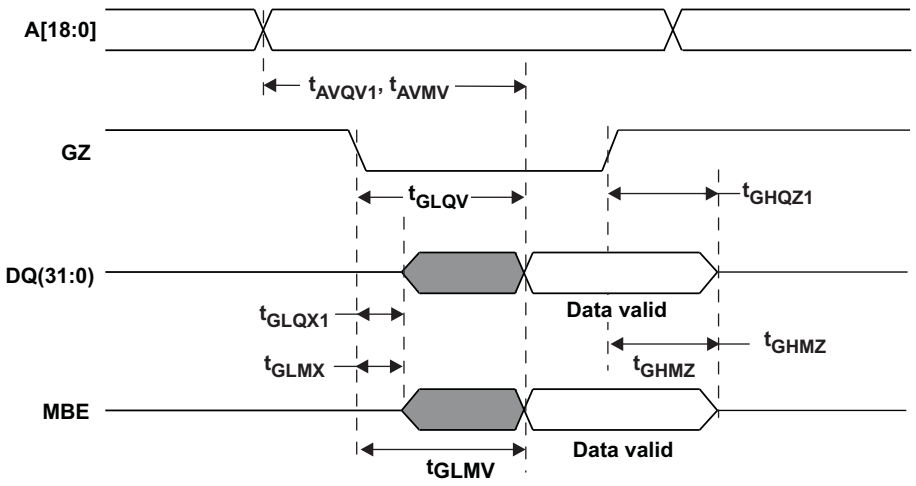
Assumptions: E1Z low, E2 high, WZ high, GZ low and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

Figure 4. SRAM Read Cycle 1, Address-Controlled Access



Assumptions: GZ low, WZ high and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

Figure 5. Read Cycle 2, Chip Enable-Controlled Access



Assumptions: E1Z low, E2 high, WZ high and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

Figure 6. Read Cycle 3, Output Enable-Controlled Access

Write Operation With Write-Through Support

A combination of WZ and E1Z low with E2 high defines a write cycle. The state of GZ is “don’t care” for a write cycle although it may be necessary to set GZ high for convenient setup of new data for some system operation modes in order to avoid data bus contention. During a write operation, data just written will be sent to the outputs. When the write operation has been completed, the output data bus will be updated by controlling either GZ going low or WZ goes high while GZ low. The outputs are placed in a high impedance state when GZ is high or WZ is low during standard read and write cycles.

- **Write cycle 1** (Figure 7): Access and data write through controlled by WZ is initiated when WZ goes low and is terminated by WZ going high while E1Z and E2 remain active. The write pulse width is determined by t_{WLWH} and t_{ETWH}. To avoid bus contention, t_{WLQZ} must be satisfied before write data is applied to the DQ[31:0] pins. In addition, at the end of the write operation write data must be removed from the DQ[31:0] pins after t_{WHDX} is met, but before t_{WHQX}. The output access time is determined by t_{WHQV} as long as GZ remains low.
- **Write cycle 1a** (Figure 8): WZ controlled write cycle with GZ high is similar to write cycle 1 but with GZ fixed high so data outputs remain in high impedance state.
- **Write cycle 2** (Figure 9): WZ controlled write access with data write through controlled by GZ is similar to write cycle 1 with the difference being that the output data comes out when GZ goes low with WZ high. The output access time is determined by t_{GLQV}. The GZ high pulse is used to keep the DQ[31:0] outputs in a high impedance state during the write operation to avoid bus contention.
- **Write cycle 3** (Figure 10): Chip enable controlled write access with data write through controlled by WZ is initiated when E1Z or E2 goes active, and the data write operation is terminated by WZ going high. The write pulse width is defined by t_{ETWHZ} from the latter of E1Z or E2 going active to WZ high. The output access time is determined by t_{WHQV} as long as GZ remains low. As with write cycle 1, the write data must be removed from the DQ[31:0] pins after the input data hold time, t_{WHDX}, but before t_{WHQX}.
- **Write cycle 3a** (Figure 11): chip enabled controlled write cycle with GZ high is similar to write cycle3, but with GZ fixed high so the data outputs remain in a high impedance state.
- **Write cycle 4** (Figure 12): Chip enable controlled write access with data write through controlled by GZ is similar to Write cycle 3 with the difference that the data output is controlled by GZ going low. The output access time is determined by t_{GLQV}. The GZ high pulse is used to keep the DQ[31:0] pins in a high impedance state during the write operation to avoid bus contention.

Table 4. AC Characteristics Write Cycle (1)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{AVAV}	Write-through cycle time	20		ns	Figure 7 Figure 9 Figure 10 Figure 12
t_{AVAV2} (2)	Write cycle time with GZ always high	13.8		ns	Figure 8 Figure 11
t_{ETWH}	Device enable to end of write (WZ-controlled)	12		ns	Figure 7 Figure 8 Figure 9
t_{ETWH2} (3)	Device enable to end of write (E-controlled)	11		ns	Figure 10 Figure 12
t_{AVET}	Address setup time for write (E-controlled)	1.4		ns	Figure 10 Figure 11 Figure 12
t_{EFQZ}	E-controlled tri-state time	3.5	5	ns	Figure 7 Figure 9 Figure 10 Figure 12
t_{AVWL}	Address setup time for write (WZ-controlled)	3.6		ns	Figure 7 Figure 8 Figure 9
t_{WLWH}	Write pulse width	7.9		ns	Figure 7 Figure 8 Figure 9
t_{WHAX} (3)	Address hold time for write-through (WZ-controlled)	8.5		ns	Figure 7 Figure 9
t_{WHAX1} (2)	Address hold time for write (WZ-controlled) with GZ always high	2.3		ns	Figure 8
t_{EFAX}	Address hold time for device enable (E-controlled)	0.1		ns	Figure 10 Figure 11 Figure 12
t_{ETEF} (3)	Device enable pulse width (E-controlled)	19.5		ns	Figure 10 Figure 12
t_{ETEF1} (2)	Device enable pulse width (E-controlled) with GZ always high	12.3		ns	Figure 11
t_{DVWH}	Data setup time	8.2		ns	Figure 7 Figure 8 Figure 9 Figure 10 Figure 12
t_{WHDX}	Data hold time	0.2		ns	Figure 7 Figure 8 Figure 9 Figure 10 Figure 12
t_{WHEF}	Write disable time to device disable for write-through	8.5		ns	Figure 7 Figure 9 Figure 10 Figure 12
t_{WHEF1} (2)	Write disable time to device disable with GZ always high	2.3		ns	Figure 8
t_{WHWL}	Write disable time. Write pulse width high for write-through.	12.1		ns	Figure 7 Figure 9
t_{WHWL1} (2)	Write disable time. Write pulse width high with GZ always high.	2.6		ns	Figure 8
t_{WHQX}	WZ-controlled tri-state end time	3		ns	Figure 7 Figure 10
t_{WHQV}	WZ-controlled output data valid		10	ns	Figure 7 Figure 10
t_{WLQZ}	WZ-controlled tri-state time	2	3.3	ns	Figure 7

(1) T_C = -55°C to 125°C, V_{DD1} = 1.7 V to 1.9 V, V_{DD2} = 3 V to 3.6 V (unless otherwise noted).
(2) Write-only operations with GZ fixed high (no write-through).
(3) Parameters ensured by design and/or characterization if not production tested.

Table 4. AC Characteristics Write Cycle (1) (continued)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{GLQX}	GZ-controlled output enable time	1.3		ns	Figure 9 Figure 12
t_{GLQV}	GZ-controlled output data valid		8.6	ns	Figure 9 Figure 12
t_{GLMX}	GZ-controlled error flag enable time	3.5		ns	Figure 9 Figure 12
t_{GLMV}	GZ-controlled error flag valid		8.6	ns	Figure 9 Figure 12
t_{WHMX} (4)	WZ-controlled error flag enable time	4		ns	Figure 7 Figure 10
t_{WHMV} (4)	WZ-controlled error flag valid		8.5	ns	Figure 7 Figure 10
t_{EFMZ} (4)	Chip enable change to MBE tri-state	3.5	5	ns	Figure 7 Figure 9 Figure 10 Figure 12
t_{WLMZ} (4)	WZ-controlled output MBE tri-state time	2	3.3	ns	Figure 7

(4) Parameters ensured by design and/or characterization if not production tested.

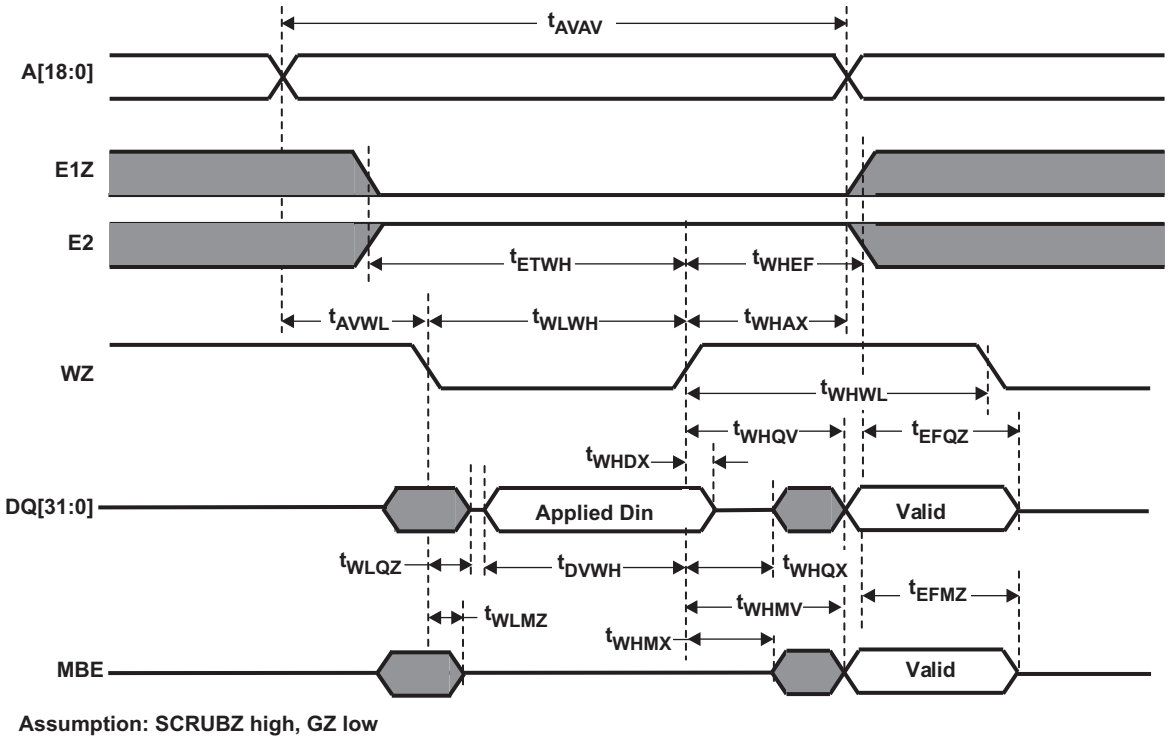
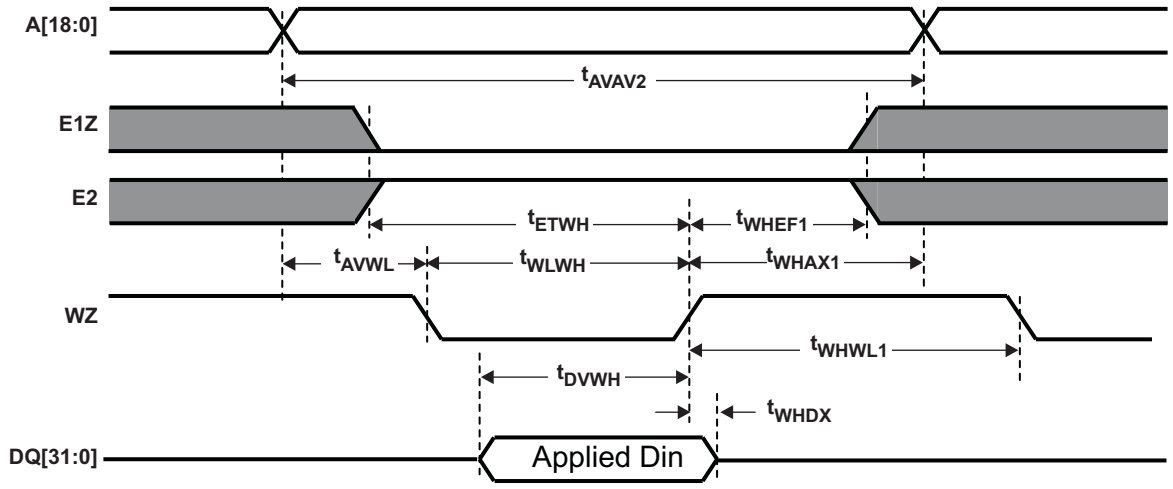
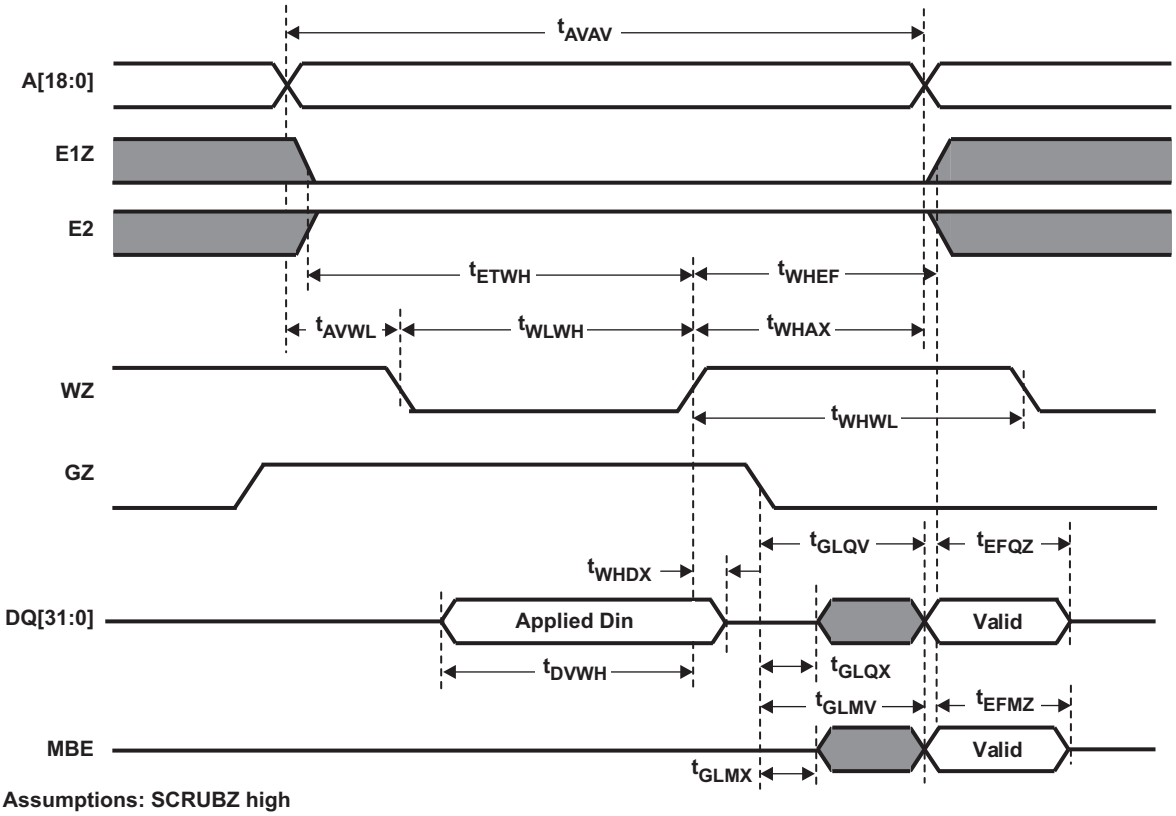


Figure 7. SRAM Write Cycle 1, WZ Controlled Access



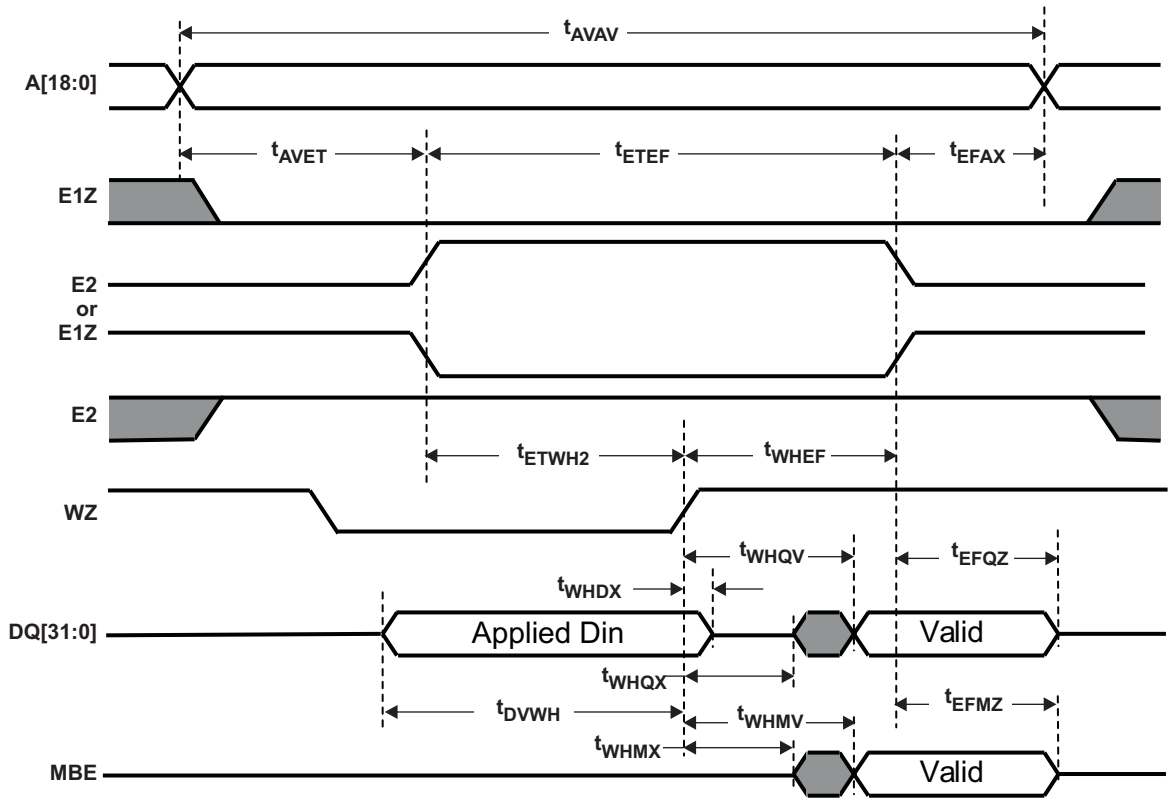
Assumptions: SCRUBZ high, GZ high

Figure 8. SRAM Write Cycle 1a, WZ-Controlled Write Only With GZ Fixed High



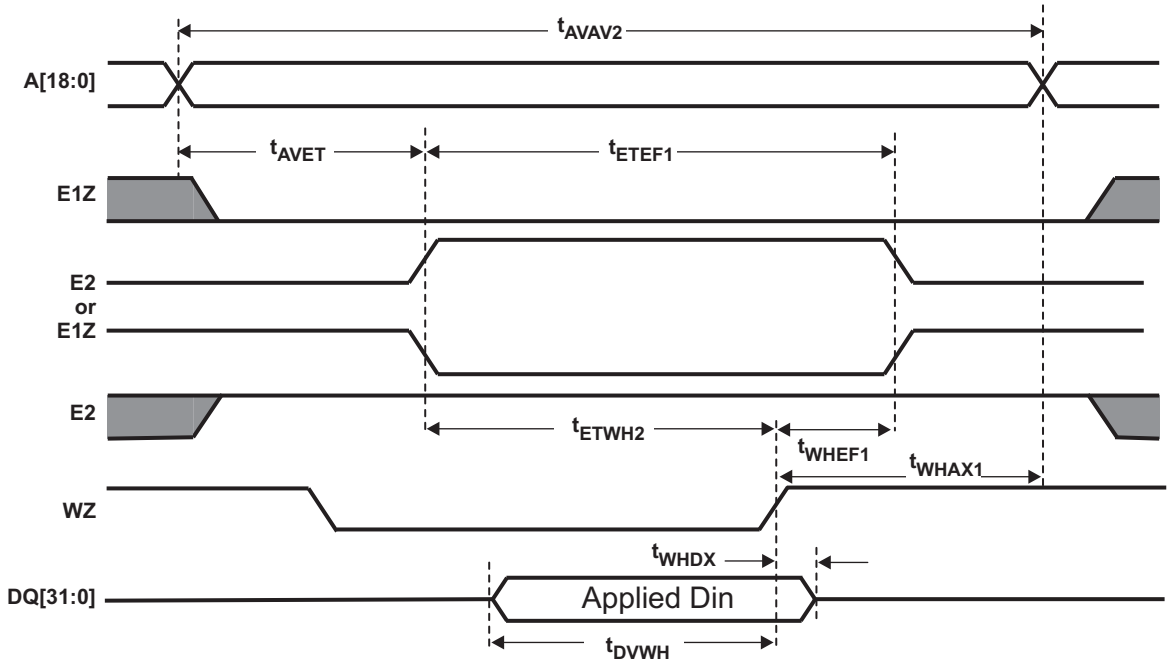
Assumptions: SCRUBZ high

Figure 9. SRAM Write Cycle 2, WZ Controlled Write With Data Write Through Controlled by GZ



Assumptions: Either E1Z,/E2 scenario can occur, SCRUBZ high, GZ low

Figure 10. SRAM Write Cycle 3, Enable Controlled Write With Data Write Through Controlled by WZ



Assumptions: Either E1Z,/E2 scenario can occur, SCRUBZ high, GZ High

Figure 11. SRAM Write Cycle 3a, Enable Controlled Write Only With GZ Fixed High

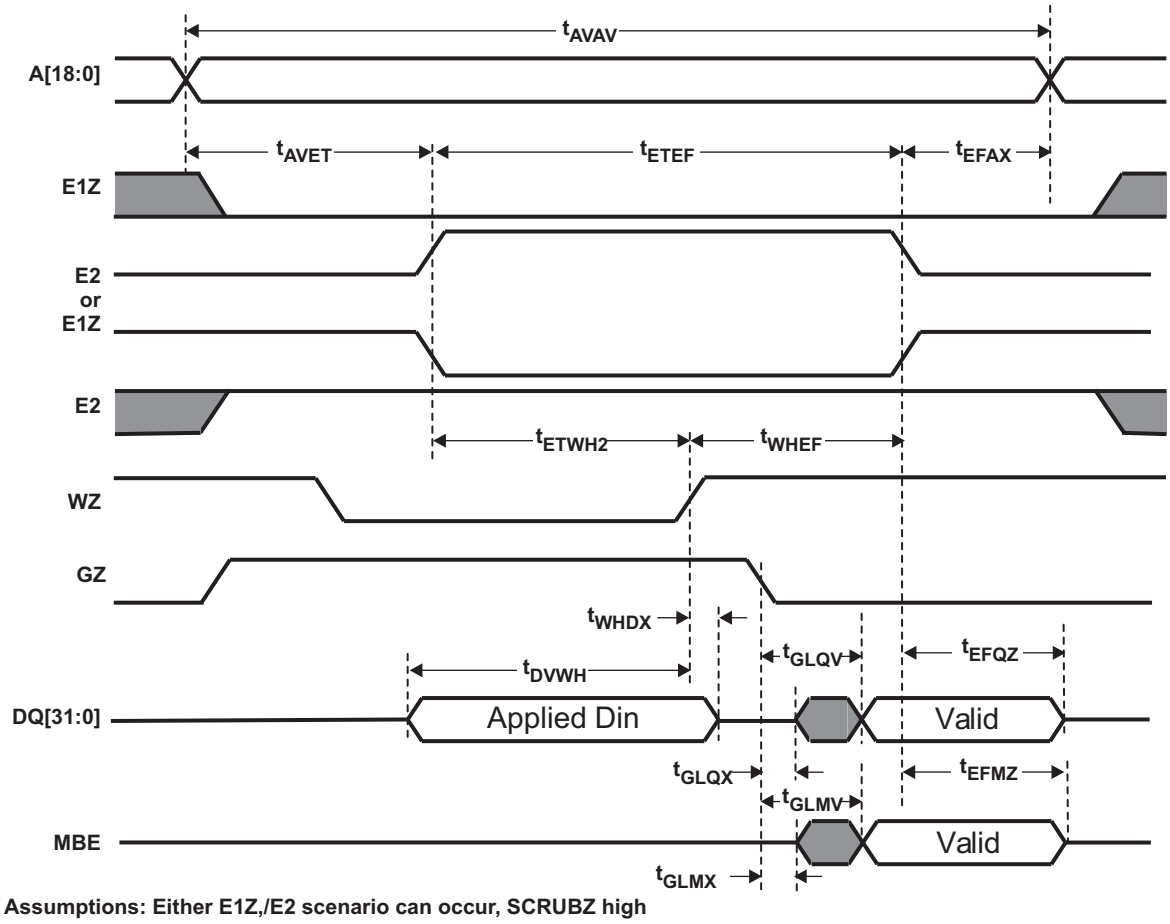


Figure 12. SRAM Write Cycle 4, Enable Controlled Write With Data Write Through Controlled by GZ

Scrub Operation

The SMV512K32 uses embedded error detection and correction (EDAC) to correct single bit upset of each 32-bit word. The device pins BUSYZ and SCRUBZ are used differently depending on whether the device is operated as a slave device (MSS pin connected to VDD2) or as a master device (MSS pin connected to VSS2). The BUSYZ pin is an output for the master device and is driven low to indicate that a scrub cycle is about to be initiated. The BUSYZ signal can be used to generate wait states by the memory controller. The BUSYZ pin should should be left unconnected for slave devices. The SCRUBZ pin is an output on the master device and an input on slave devices. The master SCRUBZ pin is driven low when a scrub cycle initiates and can be used to trigger scrub cycles for slave units by connecting their respective SCRUBZ pins to the SCRUBZ master output.

The EDAC operation truth table is shown in Table 5.

Table 5. EDAC Control Operation Mode Truth Table

MBE (OUTPUT)	SCRUBZ	BUSYZ	I/O MODE	MODE
H	H	H	Read	Data error detected(1)
L	H	H	Read	Valid data out(1)
X	H	H	X	Device ready
X	H	L	X	Device ready/early scrub request coming
X	L	X	Not accessible	Device busy (scrub in progress)

(1) MBE is only valid in EDAC operation modes (Read with EDAC enable or scrub).
MBE indicates Multiple Bit Error if A[12] bit in the control register is '0'.
MBE indicates Single Bit Error if A[12] bit in the control register is '1'.

To allow system design flexibility, the time delay between falling edges of BUSYZ and SCRUBZ as well as the scrub rate are user programmable (see the control register programming description below). Depending on environment and usage, some users may want a high scrub rate to minimize error rate at the sacrifice of reduced data throughput, while others may want a lower scrub rate to increase the throughput and accept a higher error rate.

Data errors are detected and corrected not only during scrub cycles, but also during normal read cycles.

EDAC Configuration and Scrub Address Polling (Master Device Only)

The user can program the scrub rate and the edge relationship between BUSYZ and SCRUBZ by writing configuration data to the control register. The value recorded in the control register determines scrub rate, SCRUBZ to BUSYZ delay, EDAC bypass selection, scrub enable/disable and single bit or multiple bit error detection. See Table 7 for more detail.

Table 8 and Table 9 give typical timing characteristics for various configuration options. Table 10 gives the AC characteristics for EDAC functions.

The following EDAC control operations are defined by Table 6.

- Control register write (Figure 15): This mode is used to write configuration values to the EDAC control register.
- Control register read (Figure 16): This mode is used to read the contents of the EDAC control register.
- Scrub address counter read (Figure 17): This mode is to read out the address counter which is used as a pointer for scrub operations. The address counter is reset to all '1' when the configuration register is written. It is then automatically incremented for each scrub cycle. In the event of a single or multiple bit error detected during a scrub cycle, the address can be polled to determine the location of the data error. During the address counter read, the 19 bits of the counter are output on data bits DQ[18:0]. The value of the other data bits DQ[31:19] are ignored.

Table 6. EDAC Function Select Truth Table(1)

E1Z	E2	GZ	WZ	MBE	A7	A8	A9	A10	MODE
L	H	H	H	H	X	X	L	L	Write control register
L	H	H	H	H	X	X	H	L	Read control register
L	H	H	H	H	H	X	X	H	Address counter read

(1) All other combinations of A7-A10 are reserved and should be avoided.

Table 7. EDAC Control Register Programming (1) (2)

ADDRESS BIT	PARAMETER	VALUE	FUNCTION
A[3:0]	Scrub rate – Rates are approximate and will vary with temperature and voltage conditions as well as process parameters	0–15	As scrub rate changes from 0 to 15, then the interval between scrub cycles, t_{BLBL}, will change as follows: 0 = N/A 6 = 222 kHz 11 = 7 kHz 1 = N/A 7 = 111 kHz 12 = 3.5 kHz 2 = N/A 8 = 55 kHz 13 = 1.75 kHz 3 = N/A 9 = 28 kHz 14 = 0.875 kHz 4 = 888 kHz 10 = 14 kHz 15 = 0.433 kHz 5 = 444 kHz See Table 8.
A[7:4]	BUSYZ to SCRUBZ – Delays are approximate and will vary with temperature and voltage conditions as well as process parameters	0–15	If A[7:4] changes from 0 to 15, the interval t_{BLSL} between falling edges of BUSYZ and SCRUBZ will change as follows: 0 = 80 ns 6 = 480 ns 11 = 820 ns 1 = 160 ns 7 = 560 ns 12 = 880 ns 2 = 220 ns 8 = 620 ns 13 = 960 ns 3 = 280 ns 9 = 680 ns 14 = 1020 ns 4 = 360 ns 10 = 760 ns 15 = 1080 ns 5 = 420 ns See Table 9.
A[8]	EDAC bypass bit	0/1	0: Enable EDAC 1: Disable EDAC including scrub
A[11]	Scrub enable bit	0/1	0: Enable scrub 1: Disable scrub
A[12]	SE/DE indication bit	0/1	0: MBE indicates multiple-bit error 1: MBE indicates single-bit error

(1) A(10:9) must be '00' during control register programming according to Table 6.
(2) A(18:13) are don't care.

NOTE

During power up, states of all registers are random so it is imperative that the user execute Write Control Register and preferably Read Control Register to affirm desired operations. The following values are recommended to set for initial use:

1. Scrub rate is 111 kHz.
2. t_{BLSL} is 760 ns.
3. EDAC bit is 0 (enabled).
4. Scrub enable bit is 0 (enabled).
5. SE/DE indication bit is 0 (multiple bit).

Table 8. Scrub Rate Variation (Voltage = 1.8 V, Temperature = –55°C to 125°C)

VALUE	MAX (ns)
0000	N/A
0001	N/A
0010	N/A
0011	N/A
0100	1,500
0101	3,100
0110	6,100
0111	12,200
1000	24,200
1001	48,300
1010	96,400
1011	192,500
1100	384,500
1101	770,000
1110	1,500,00
1111	3,200,00

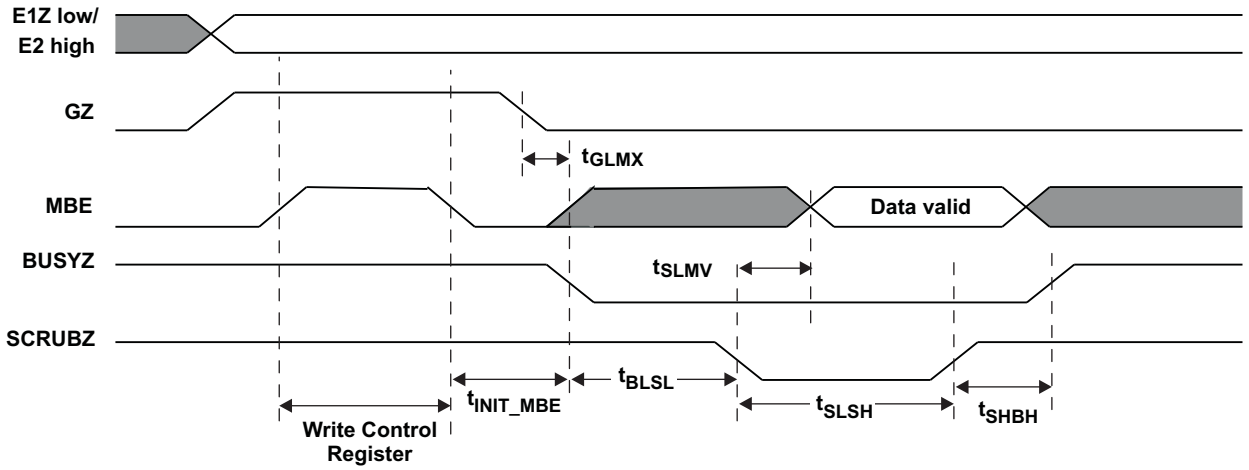
Table 9. BUSYZ Low to SCRUBZ Low Delay Variation (Voltage = 1.8 V, Temperature = –55°C to 125°C)

VALUE	MAX (ns)
0000	80
0001	180
0010	270
0011	370
0100	460
0101	600
0110	650
0111	800
1000	900
1001	1000
1010	1200
1011	1300
1100	1400
1101	1500
1110	1600
1111	1600

Table 10. AC Characteristics for EDAC Function (1)

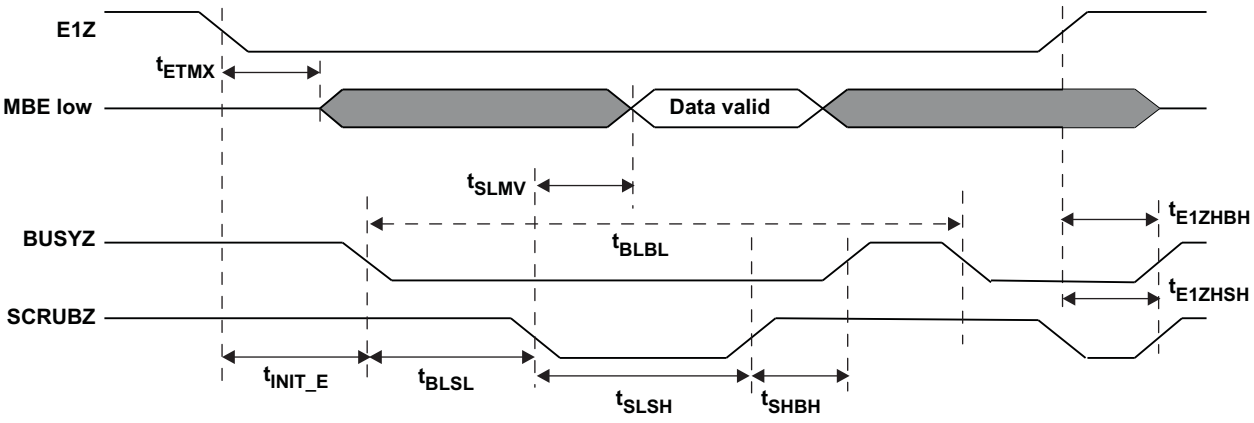
SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{BLSL}	User programmable, BUSYZ low to SCRUBZ low	See Table 9		ns	Figure 13 Figure 14
t_{BLBL}	User programmable, BUSYZ low to BUSYZ low	See Table 8		ns	Figure 14
t_{SLSH}	SCRUBZ low to SCRUBZ high	200	504	ns	Figure 13 Figure 14
t_{SHBH}	SCRUBZ high to BUSYZ high	50	120	ns	Figure 13 Figure 14
t_{ETMH}	Device enable to MBE high	5.5		ns	Figure 15 Figure 16 Figure 17
t_{GHMH}	GZ high to MBE high	6.5		ns	Figure 15 Figure 16 Figure 17
t_{AVMH}	Address valid to MBE high	0.9		ns	Figure 15 Figure 16 Figure 17
t_{MHML}	MBE high to MBE low	12.8		ns	Figure 15 Figure 16 Figure 17
t_{MLEF}	MBE low to device disable	0.4		ns	Figure 15 Figure 16 Figure 17
t_{MLGL}	MBE low to GZ low	1.8		ns	Figure 15 Figure 16 Figure 17
t_{MLAX}	MBE low to address change	0.1		ns	Figure 15 Figure 16 Figure 17
t_{MHQX}	MBE high to data change	4.5		ns	Figure 16 Figure 17
t_{MHQV}	MBE high to data valid		8.2	ns	Figure 16 Figure 17
t_{EFQZ}	Memory enable change to output data tri-state	3.5	5	ns	Figure 16 Figure 17
t_{EFMZ} (2)	Memory enable change to MBE tri-state	3.5	5	ns	Figure 14
t_{GLMX}	GZ-controlled error flag enable time	3.5		ns	Figure 13
t_{ETMX}	E-controlled error flag enable time	3.5		ns	Figure 14
t_{INIT_E}	E1Z low to BUSYZ low		160	ns	Figure 14
t_{INIT_MBE}	MBE low to BUSYZ low		160	ns	Figure 13
t_{SLMV}	SCRUBZ low to MBE valid		146	ns	Figure 13 Figure 14
t_{E1ZHSH}	E1Z high to SCRUBZ high		20	ns	Figure 14
t_{E1ZHBH}	E1Z high to BUSYZ high		20	ns	Figure 14
t_{MHBH}	MBE high to BUSYZ high		20	ns	Figure 15

(1) T_C = -55°C to 125°C, V_{DD1} = 1.7 V to 1.9 V, V_{DD2} = 3 V to 3.6 V (unless otherwise noted).
(2) Parameters ensured by design and/or characterization if not production tested.



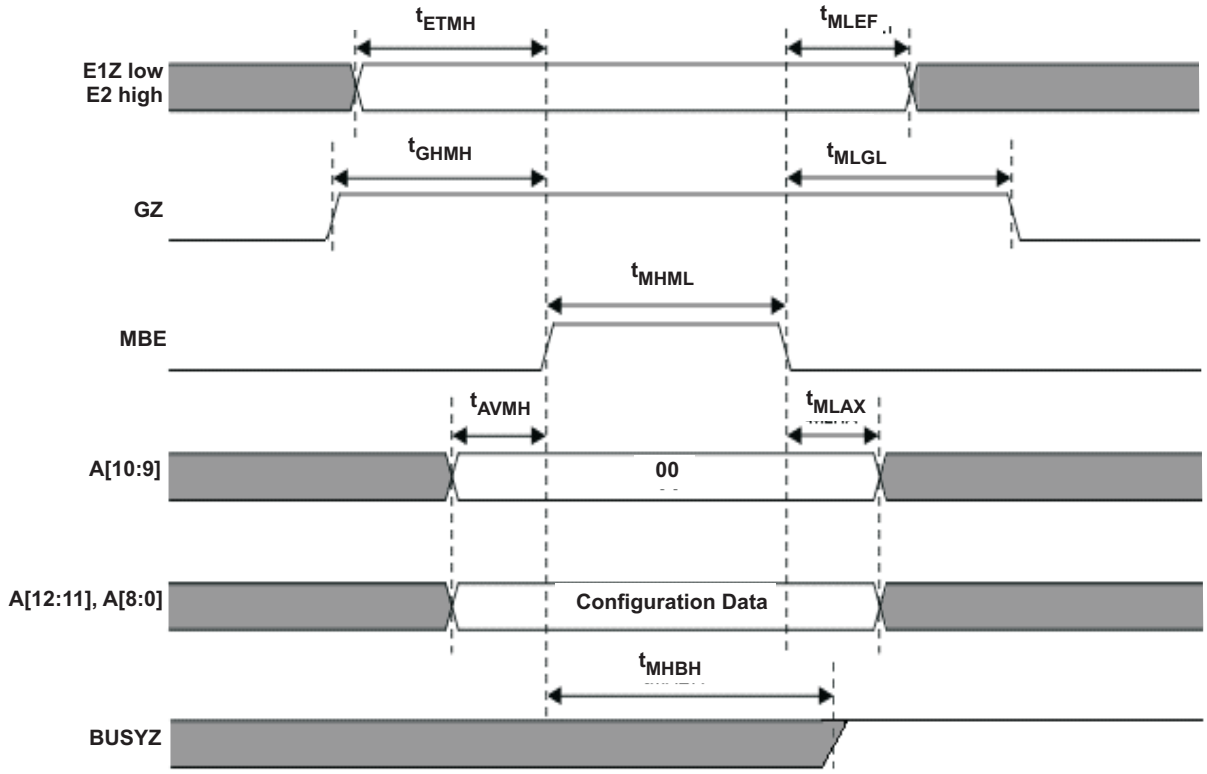
Assumption: WZ is high

Figure 13. Scrub Cycle Controlled by MBE



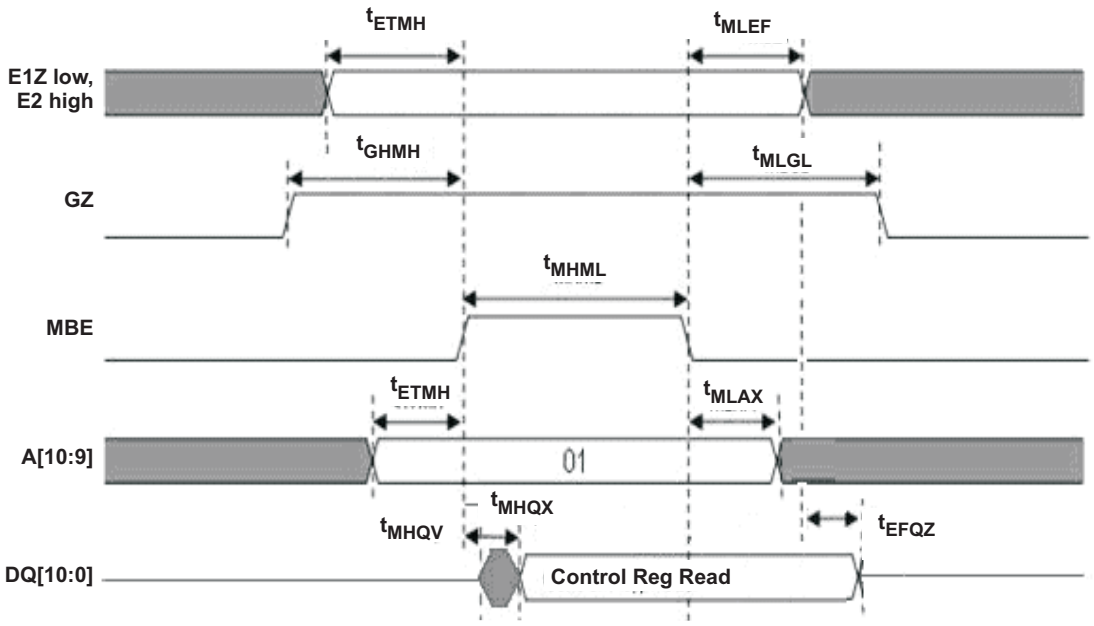
Assumptions: E2 and GZ are low, WZ is high

Figure 14. Scrub Cycle Controlled by E1Z



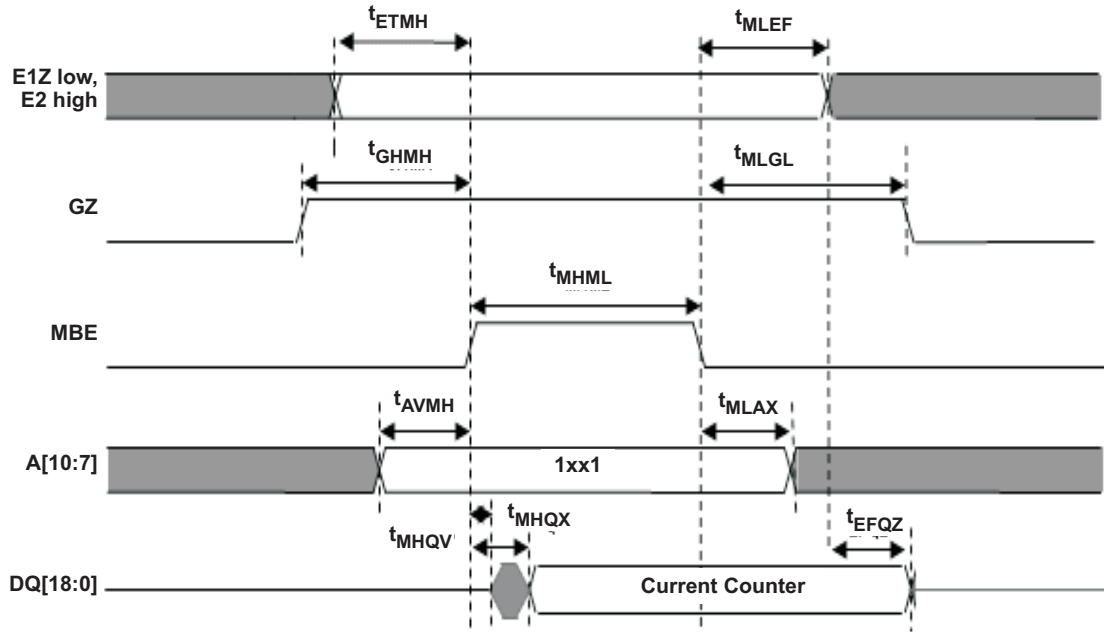
Assumptions: SCRUBZ and WZ are high

Figure 15. Control Register Write Cycle



Assumptions: SCRUBZ and WZ are high

Figure 16. Control Register Read Cycle



Assumptions: SCRUBZ and WZ are high

Figure 17. Address Counter Read

REVISION HISTORY

Changes from Revision H (July 2013) to Revision I	Page
• Added /EM bullet to FEATURES	1
• Deleted Ordering Information table	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1123701VXC	ACTIVE	CFP	HFG	76	1	RoHS & Green	AU	N / A for Pkg Type	-55 to 125	SMV512K32HFG 5962-1123701VXC	Samples
SMV512K32HFG	ACTIVE	CFP	HFG	76	1	RoHS & Green	AU	N / A for Pkg Type	-55 to 125	SMV512K32HFG 5962-1123701VXC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

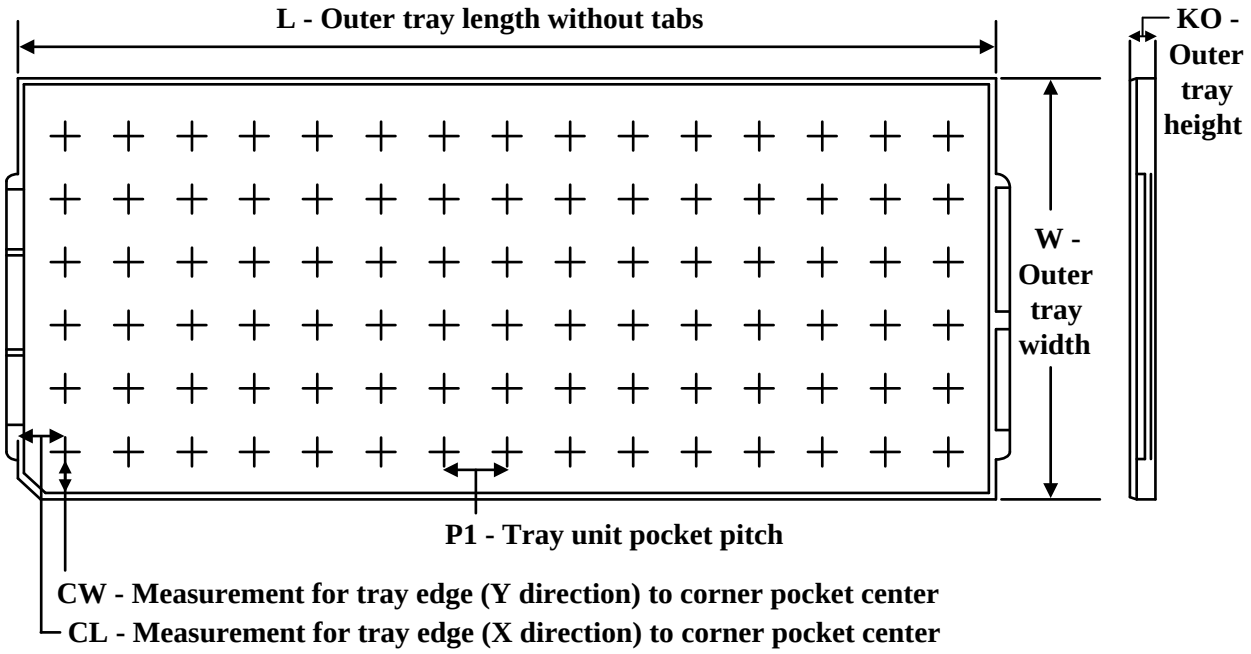
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

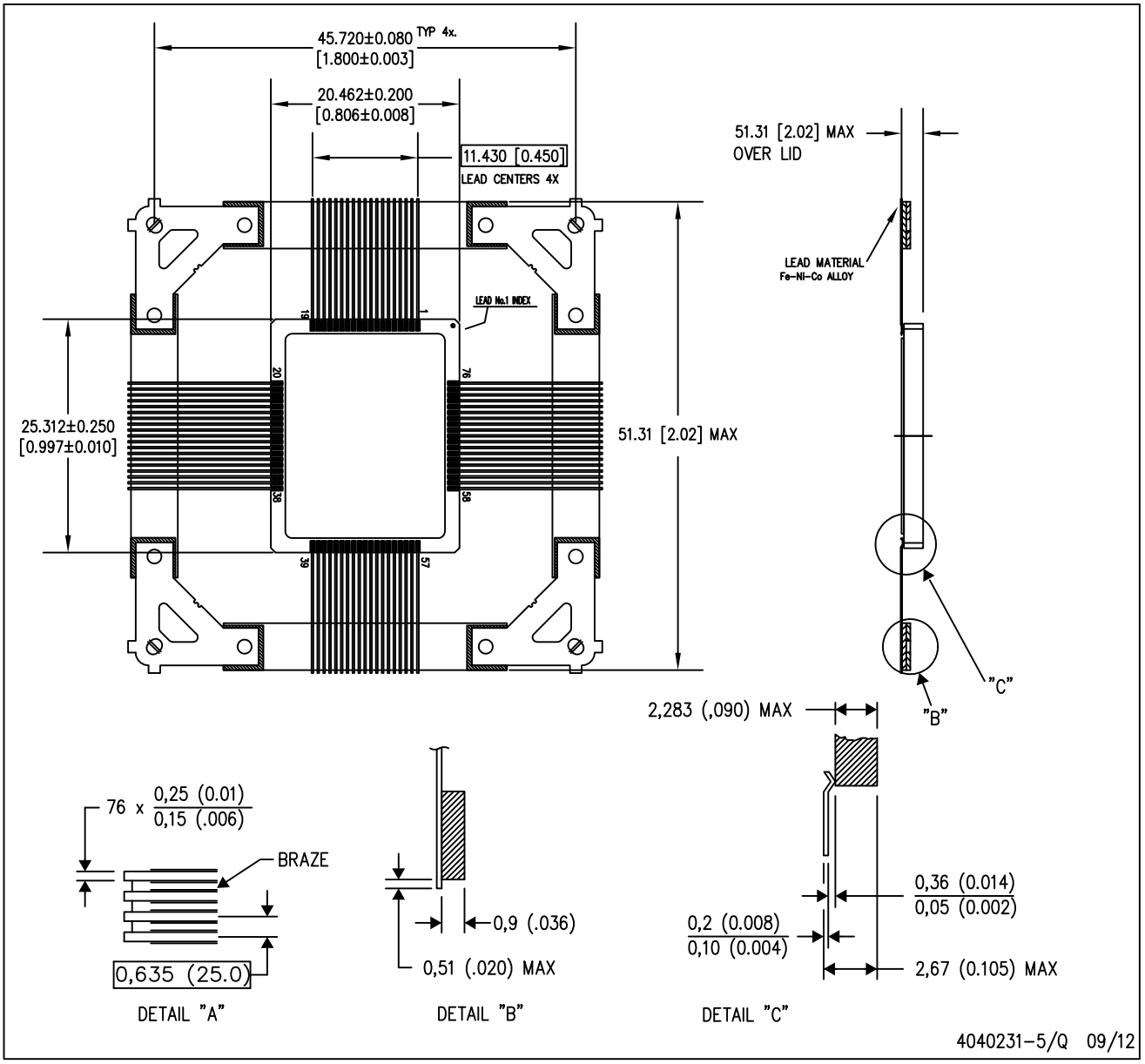


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-1123701VXC	HFG	CFP	76	1	2 x 5	150	315	135.9	7620	57	43.5	39.45
SMV512K32HFG	HFG	CFP	76	1	2 x 5	150	315	135.9	7620	57	43.5	39.45

HFG (S–CQFP–F76) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Lid is connected to GND leads (see data sheet).

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