Designing JK Flip-Flop using 28nm Architecture

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***Abstract*— In this paper I'm going to design and implement JK flip-flop using CMOS transistor technology. I'll also be using Openlane and Skywater for this. Designing will be done with the help of eSim. JK flip-flop is a very well known device in the electronics industry and the backbone of all microprocessors and microcontrollers. JK flip-flop is improvised version of its predecessor SR flip-flop. It's truth table is mostly similar but distinguishes when both the inputs are logic high.**

Keywords—digital logic, electronics, vlsi

1. Reference Circuit Details

Digital circuits are composed of logic functions which are then implemented using building blocks. AND, OR and NOT are basic building blocks of every digital logic. Many different modules are created using combination of these gates to achieve various functionality. One of such modules is JK flip-flop. This flip-flop is one of the most used flip-flop over every digital electronics. The inputs to this flip flop are 'J' and 'K'. The JK flip flop work in the same way as the SR flip flop. The only difference between JK flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flop are set to 1. The JK flip flop is a gated SR flip flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. The JK flip flop is an improved clocked SR flip flop, but it still suffers from "race around" condition. We have to keep short timing pulse for avoiding this condition.

Same as for SR Latch	Clock	Input		Output		Description
	Clk	J	K	Q	Q'	
	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	¯↓_	0	1	1	0	Reset Q>>0
	X	0	1	0	1	
	¯↓_	1	0	0	1	Set Q>>1
	X	1	0	1	0	
Toggle action	¯↓_	1	1	0	1	Toggle
	¯↓_	1	1	1	0	

Figure 1: Truth table of a typical clock JK flip flop

2. Reference Circuit Design

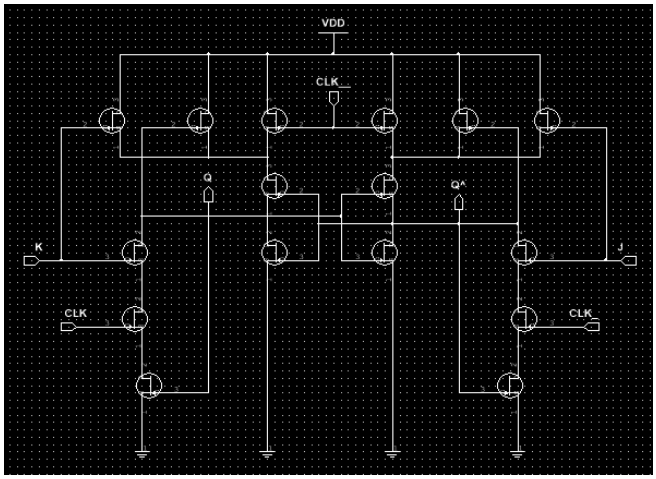

Figure 2: CMOS realization of JK flip flop

3. Reference Waveforms

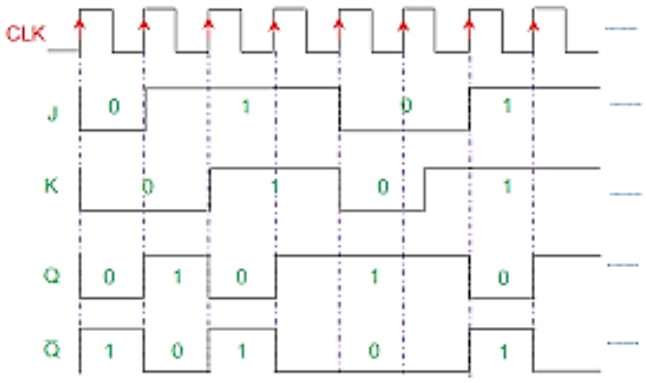

Figure 3: Reference waveform of JK flip flop

4. References

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