Design and Implementation of a Function Generator

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34	Documentation	Keshav Rai	2022MT61968	mt6221968@maths.iitd.ac.in	1.0

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45	Software	Niranjan Rajeev	2022EE11766	ee1221766@ee.iitd.ac.in	1.0
46	Software	Nobin Kidangan Benny	2022EE11154	ee1221154@ee.iitd.ac.in	1.0
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52	Software	Praveen Lakhara	2022MT11280	mt1221280@maths.iitd.ac.in	1.0
53	Software	Priyansh Prakash Mayank	2022MT11954	mt1221954@maths.iitd.ac.in	1.0
54	Hardware Design and Fabrication	Priyanshu Jindal	2022EE11668	ee1221668@ee.iitd.ac.in	1.0
55	Software	Punit Meena	2022EE11184	ee1221184@ee.iitd.ac.in	1.0
56	Testing and Debugging (Hardware)	Rahul Rajoria	2022MT11947	mt1221947@maths.iitd.ac.in	1.0
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66	Documentation	Shashwat Kasliwal	2022MT11915	mt1221915@maths.iitd.ac.in	1.0
67	Documentation	Shivang Goyal	2022MT11269	mt1221269@maths.iitd.ac.in	1.0
68	Software	Siddharth Saini	2022MT11283	mt1221283@maths.iitd.ac.in	1.0
69	Market Research and Survey	Siya Gupta	2022MT11274	mt1221274@maths.iitd.ac.in	1.0
70	Testing and Debugging (Hardware)	Sparsh Jain	2022MT11917	mt1221917@maths.iitd.ac.in	1.0
71	Hardware Design and Fabrication	Suhani Soni	2022MT61981	mt6221981@maths.iitd.ac.in	1.0
72	Software	Sumit Sonowal	2022MT11296	mt1221296@maths.iitd.ac.in	1.0
73	Software	Suneel Masarapu	2022MT11942	mt1221942@maths.iitd.ac.in	1.0
74	Hardware Design and Fabrication	Sushil Kumar	2022EE31765	ee3221765@ee.iitd.ac.in	1.0
75	Hardware Design and Fabrication	Syna Rajvanshi	2022MT61974	mt6221974@maths.iitd.ac.in	1.0
76	Market Survey and Research	Tanya Jain	2022MT11935	mt1221935@maths.iitd.ac.in	1.0
77	Testing and Debugging (Hardware)	Taru Singhal	2022MT11922	mt1221922@maths.iitd.ac.in	1.0
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80	Hardware Design and Fabrication	Tushar Goyal	2022MT11266	mt1221266@maths.iitd.ac.in	1.0
81	Hardware Design and Fabrication	Umang Agarwal	2022EE11692	ee1221692@ee.iitd.ac.in	1.0
82	Documentation	Utkarsh Dubey	2022MT61045	mt6221045@maths.iitd.ac.in	1.0
83	Hardware Design and Fabrication	Vatsal Manish Sejpal	2022MT11926	mt1221926@maths.iitd.ac.in	1.0
84	Hardware Design and Fabrication	Viha Singla	2022MT61972	mt6221972@maths.iitd.ac.in	1.0
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Table 3: **List of Team Members with IF $<$ 1**

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Glossary

AC	Alternating Current	27
AM	Amplitude Modulation	26
DC	Direct Current	27
EMC	Electromagnetic Compatibility	27
EMI	Electromagnetic Interference	27
FM	Frequency Modulation	26
IEC	International Electrotechnical Commission	28
LCD	Liquid Crystal Display	26
MTBF	Mean Time Between Failures	28
PCB	Printed Circuit Board	26
PM	Phase Modulation	26
THD	Total Harmonic Distortion	26

1. Introduction

1.1 Definitions

ATmega328P: A microcontroller from the AVR family, commonly used in embedded systems, including Arduino platforms, known for its flexibility and ease of use in controlling various digital and analog devices.

Chassis: The outer protective housing of the device, made of durable recycled plastic.

Coleman Liau Index: A readability test that uses characters per word and sentences per text to compute a U.S. school grade level.

Crystal Oscillator: An electronic component that generates a stable frequency signal by utilizing the mechanical vibrations of a crystal. It is widely used for clock generation in microcontrollers, communication devices, and timing circuits.

DC Offset: A shift in the waveform along the voltage axis, allowing the signal to have a constant voltage added or subtracted from the waveform.

Electromagnetic Compatibility: The capability of electrical devices and systems to operate efficiently within their electromagnetic environment without generating or experiencing disruptive interference from other electronic sources.

Electromagnetic Interference: A disturbance caused by electromagnetic radiation that disrupts the operation of electrical or electronic equipment, potentially leading to degraded performance or malfunction.

Frequency Modulation: A technique where the frequency of a carrier signal is continuously altered based on the amplitude of the input message signal, allowing for efficient transmission of audio and data signals with reduced noise interference.

Flesch Reading Ease and Flesch-Kincaid Grade Level: Formulas that evaluate the readability of text, with higher scores indicating easier readability.

Gunning Fog Index: A readability metric that predicts the level of education needed to comprehend a text upon first reading.

International Electrotechnical Commission (IEC): An international standards organization that creates and publishes international standards for all electronic, electrical, and related technologies.

Liquid Crystal Display (LCD): A flat-panel display technology that utilizes liquid crystals and polarized light to produce images, widely used in screens for televisions, monitors, digital clocks, and other electronic devices.

Modular Design: A design feature that allows for easy replacement of individual components, improving serviceability.

Mean time between Failures(MTBF): A reliability measure indicating that the product is expected to operate for at least 10,000 hours before failure.

Phase Modulation: A method of modulation in which the phase of the carrier signal is shifted in direct response to the variations in the amplitude of the message signal.

Potentiometer: A three-terminal adjustable resistor that regulates voltage levels in a circuit by changing its resistance, often used for fine adjustments in settings like volume or brightness.

Printed Circuit Board: A non-conductive substrate with embedded copper traces that interconnect electronic components, enabling circuit functionality in electronic devices.

Readability Score (WebFx): A metric used to measure the readability of a text. A lower score indicates that the text is harder to read.

Service Level Agreement(SLA): Formal agreements that ensure customers receive timely technical support.

Signal Stability: The degree to which the output frequency remains constant, with drift limited to no more than 0.01

Total Addressable Market(TAM): The overall revenue potential for function generators.

Total Harmonic Distortion (THD): It quantifies the distortion in a signal due to the presence of harmonics, expressed as a percentage of the original signal's amplitude.

Unique Selling Proposition(USP): The key distinguishing feature of the product.

Vpp (Peak-to-Peak Voltage): A measure of the amplitude of an alternating current (AC) signal, indicating the voltage difference between the highest and lowest points in the waveform.

1.2 Mind Map

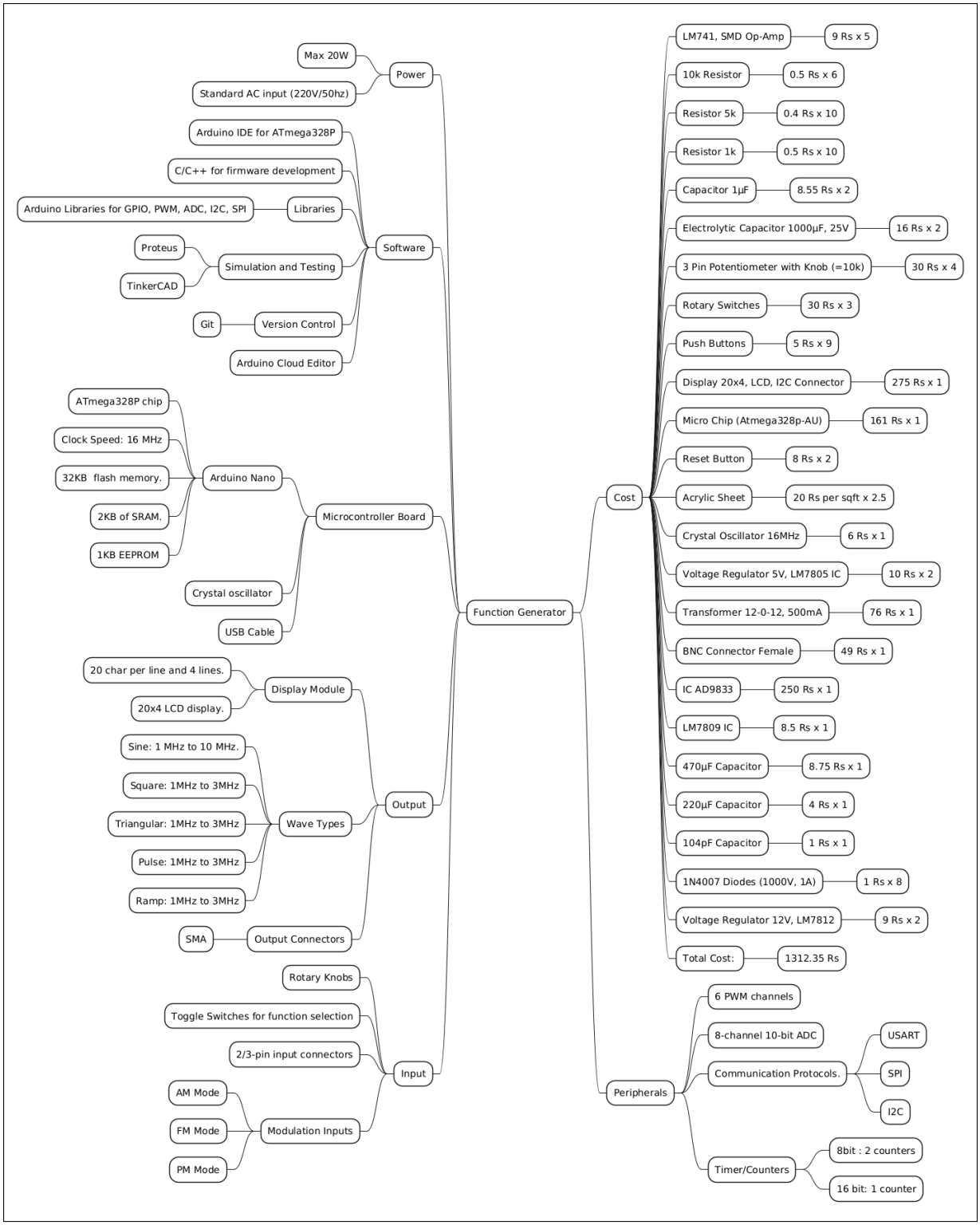


Figure 1.1: Mind Map of the Project

1.3 Project Management

The outputs from ProjectLibre include the **Gantt chart** (Fig. 1.6), **network charts** (Figs. 1.2–1.5), and **resource breakdown** (Figs. 1.7–1.9), each playing a crucial role in project planning and execution.

The **Gantt chart** (Fig. 1.6) provides a timeline-based view of tasks, detailing their start and finish dates, durations, and dependencies. It aids in tracking progress, managing resources, and identifying potential bottlenecks.

The **network charts** (Figs. 1.2–1.5) focus on task dependencies and workflow, highlighting their sequence and identifying the **critical path**, which determines the shortest completion time. Together, these charts enhance project visibility, streamline coordination, and ensure timely execution.

The **resource breakdown** (Figs. 1.7–1.9) ensures clear task allocation, preventing workload imbalances and delays. By defining team roles, responsibilities, and timelines, it optimizes efficiency, improves coordination, and enhances accountability, ensuring a smooth and conflict-free workflow.

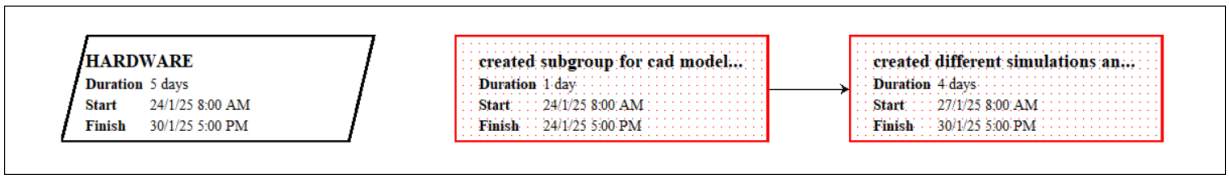


Figure 1.2: Hardware Test and Debugging Process

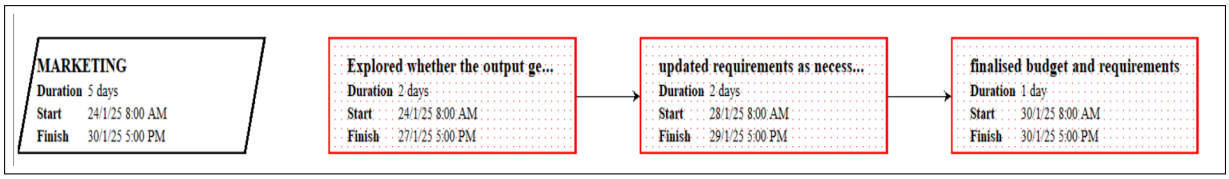


Figure 1.3: Market Research Analysis Workflow

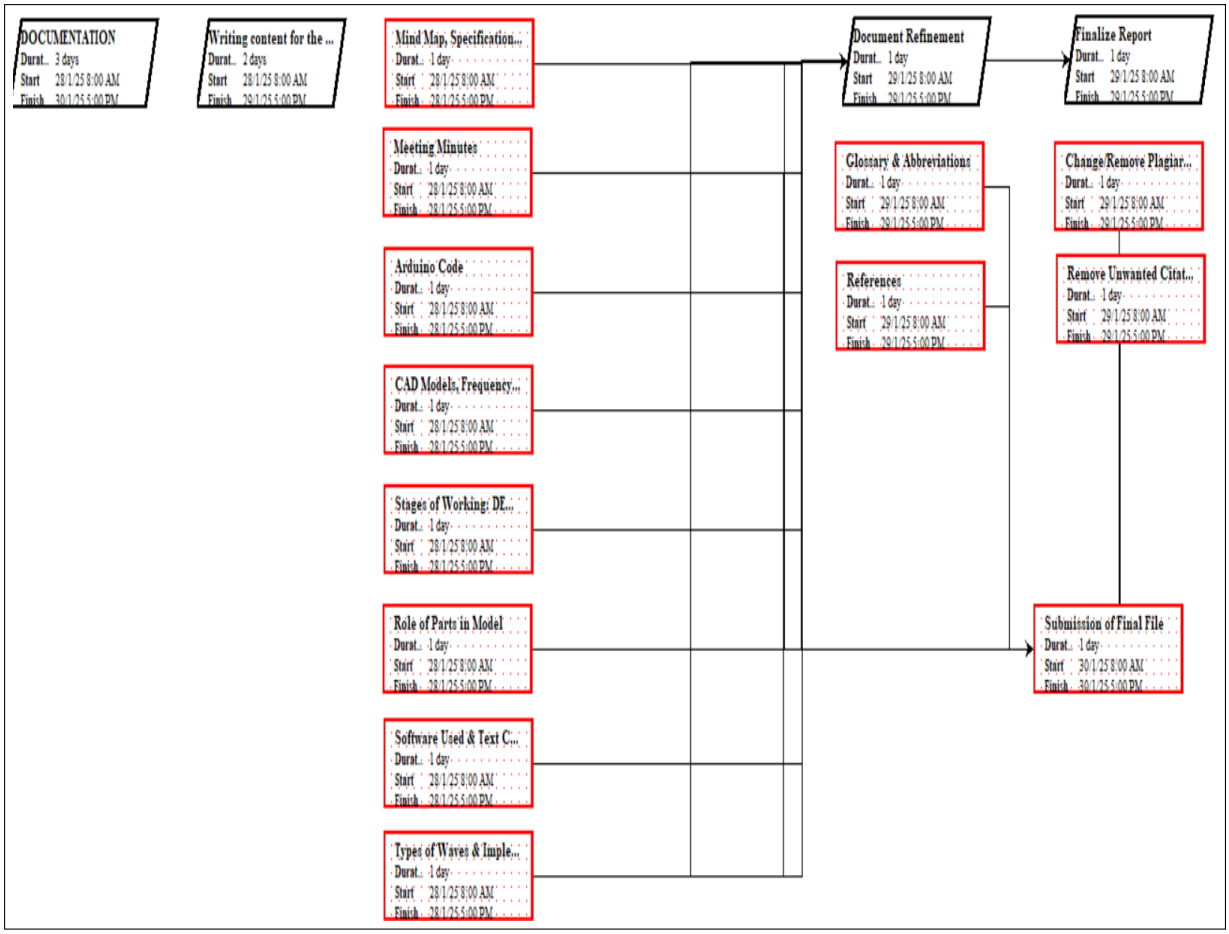


Figure 1.4: Documentation and File Writing Steps

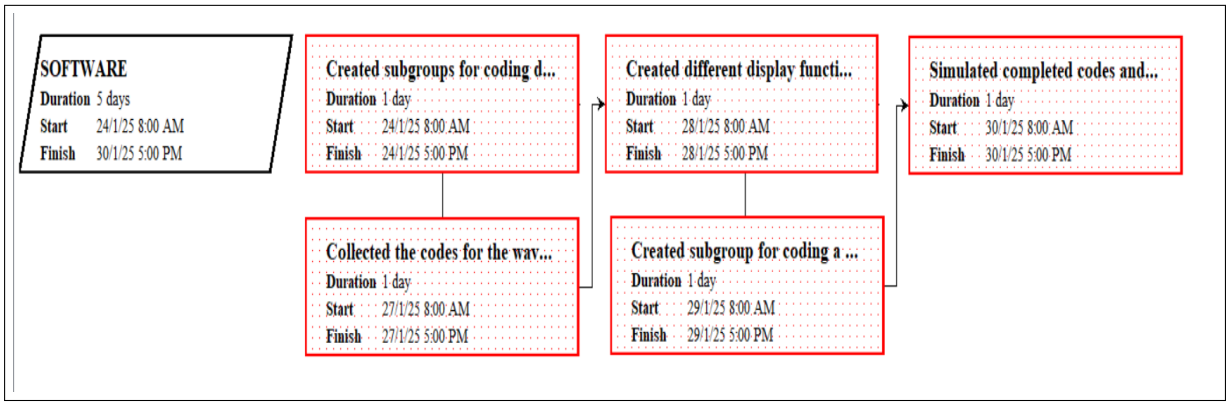
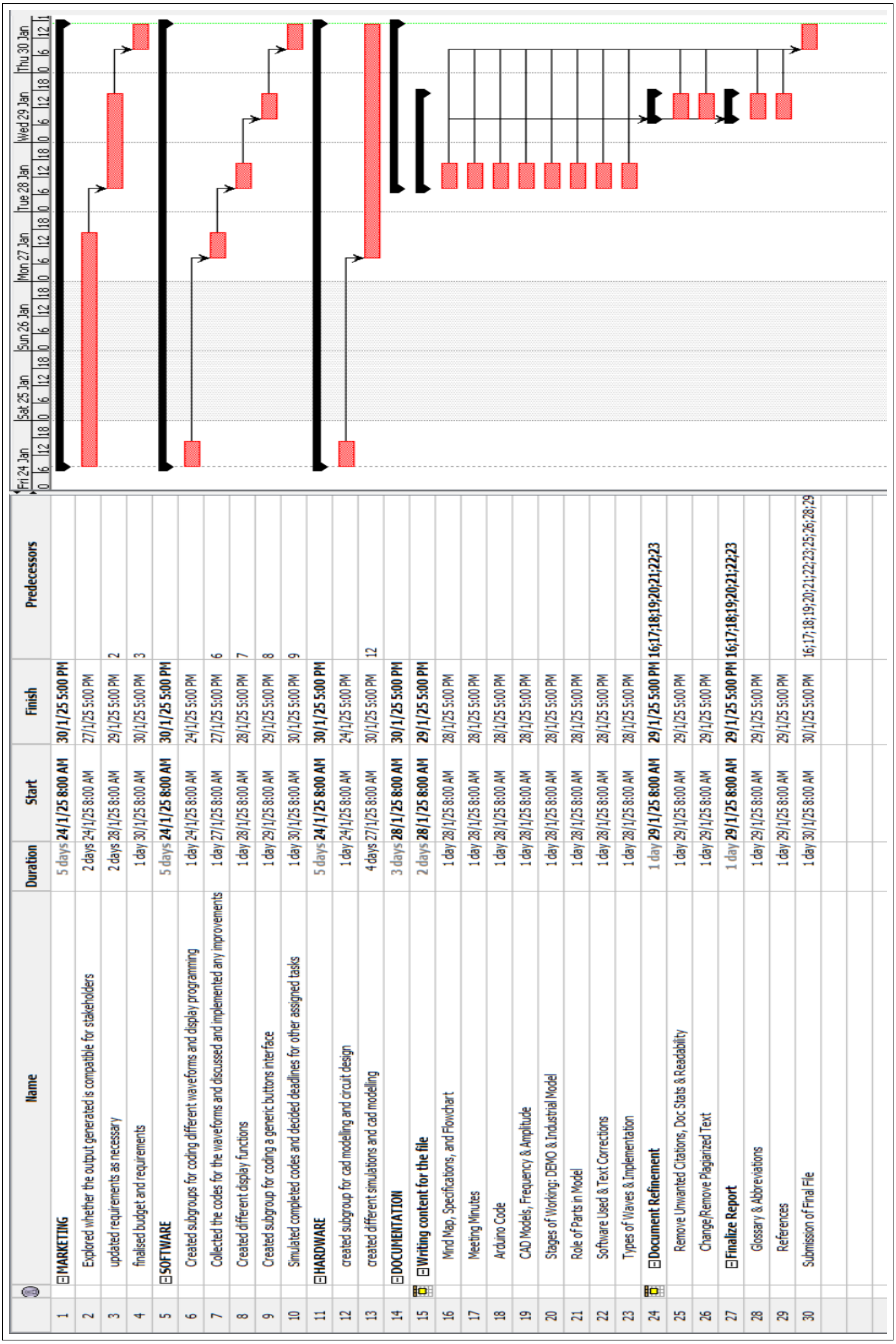


Figure 1.5: Flowchart of Software Development Process



	Name	Duration	Start	Finish	Predecessors
1	⊟MARKETING	5 days	24/1/25 8:00 AM	30/1/25 5:00 PM	
2	Explored whether the output generated is compatible for stakeholders	2 days	24/1/25 8:00 AM	27/1/25 5:00 PM	
3	updated requirements as necessary	2 days	28/1/25 8:00 AM	29/1/25 5:00 PM	2
4	finalised budget and requirements	1 day	30/1/25 8:00 AM	30/1/25 5:00 PM	3
5	⊟SOFTWARE	5 days	24/1/25 8:00 AM	30/1/25 5:00 PM	
6	Created subgroups for coding different waveforms and display programming	1 day	24/1/25 8:00 AM	24/1/25 5:00 PM	
7	Collected the codes for the waveforms and discussed and implemented any improvements	1 day	27/1/25 8:00 AM	27/1/25 5:00 PM	6
8	Created different display functions	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	7
9	Created subgroup for coding a generic buttons interface	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	8
10	Simulated completed codes and decided deadlines for other assigned tasks	1 day	30/1/25 8:00 AM	30/1/25 5:00 PM	9
11	⊟HARDWARE	5 days	24/1/25 8:00 AM	30/1/25 5:00 PM	
12	created subgroup for cad modelling and circuit design	1 day	24/1/25 8:00 AM	24/1/25 5:00 PM	
13	created different simulations and cad modelling	4 days	27/1/25 8:00 AM	30/1/25 5:00 PM	12
14	⊟DOCUMENTATION	3 days	28/1/25 8:00 AM	30/1/25 5:00 PM	
15	⊟Writing content for the file	2 days	28/1/25 8:00 AM	29/1/25 5:00 PM	
16	Mind Map, Specifications, and Flowchart	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
17	Meeting Minutes	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
18	Arduino Code	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
19	CAD Models, Frequency & Amplitude	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
20	Stages of Working: DEMO & Industrial Model	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
21	Role of Parts in Model	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
22	Software Used & Text Corrections	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
23	Types of Waves & Implementation	1 day	28/1/25 8:00 AM	28/1/25 5:00 PM	
24	⊟Document Refinement	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	16;17;18;19;20;21;22;23
25	Remove Unwanted Citations, Doc Stats & Readability	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	
26	Change/Remove Plagiarized Text	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	
27	⊟Finalize Report	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	16;17;18;19;20;21;22;23
28	Glossary & Abbreviations	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	
29	References	1 day	29/1/25 8:00 AM	29/1/25 5:00 PM	
30	Submission of Final File	1 day	30/1/25 8:00 AM	30/1/25 5:00 PM	16;17;18;19;20;21;22;23;25;26;28;29

Figure 1.6: Project Timeline in Gantt Chart

		Name	Type	Text2	Text1
1		**⊟HARDWARE**	**Work**	**DAYSTOFINISH**	
2		Abhishek Singh	Work	3	Laser cutting
3		Adarsh Singh	Work	3	Laser cutting
4		Ajaypal Kulhari	Work	3	pcbdesign(LTM)
5		AmbhoreSohamBhaskar	Work	3	pcbdesign(LTM)
6		Arpit Mourya	Work	3	pcbdesign(LTM)
7		Deevyansh Khadria	Work	2	circuit design
8		Jenit Jain	Work	2	circuit design
9		Khushi Gupta	Work	3	Laser cutting
10		Nagure Kalyani Paraman...	Work	3	Laser cutting
11		Priyanshu Jindal	Work	2	circuit design
12		SakshamKumarRohilla	Work	2	circuit design
13		Suhani Soni	Work	2	RDworks
14		Sushil Kumar	Work	2	circuit design
15		Syna Rajvanshi	Work	2	RDworks
16		Tirth Punit Golwala	Work	2	RDworks
17		Tushar Goyal	Work	2	RDworks
18		Umang Agarwal	Work	3	pcbdesign(LTM)
19		Vatsal Manish Sejpal	Work	2	RDworks
20		VihaSingla	Work	2	RDworks
21		Madhav	Work	1	FreeCAD
22		Dev Singh	Work	1	FreeCAD Modelling
23		Aditya Raj	Work	1	FreeCAD Modelling
24		Krish Singh	Work	1	FreeCAD Modelling
25		Ayush Raj	Work	1	Review of FreeCAD Models
26		Naman Kale	Work	1	Review of FreeCAD Models
27		**⊟SOFTWARE**	**Work**	**DAYSTOFINISH**	
28		Punit	Work	2	Waveform coding
29		Nobin	Work	2	Waveform coding
30		Sumit	Work	2	Waveform coding
31		Lakshaya	Work	2	Waveform coding
32		Praveen	Work	2	Waveform coding
33		Dhruv	Work	2	Waveform coding

Figure 1.7: Resource Breakdown, generated from ProjectLibre

		Name	Type	Text2	Text1
34		Manas	Work	2	Waveform coding
35		Yashwant	Work	2	Waveform coding
36		Suneel	Work	2	Waveform coding
37		Srinivasa	Work	3	Waveform coding
38		Shrenik	Work	2	Waveform coding
39		Arnav	Work	2	Waveform coding
40		Rijul	Work	2	Buttons interface programming
41		Niranjan	Work	2	Buttons interface programming
42		Niraj	Work	2	Buttons interface programming
43		Siddharth	Work	2	Buttons interface programming
44		Abhinav	Work	2	Display Programming
45		Priyansh	Work	2	Display Programming
46		Mukul	Work	2	Display Programming
47		Sarthak	Work	2	Display Programming
48		Devansh	Work	2	Display Programming
49		**⊟MARKETING**	**Work**	**DAYS TO FINISH**	
50		Rahul Athipatla	Work	3	Cost Analysis & Research fo...
51		Siya Gupta	Work	2	Cost Analysis
52		Ayush Nayak	Work	2	Cost Analysis
53		Satvik Prasad	Work	3	Cost Analysis
54		Ashmit Nangia	Work	2	Output Quality Assurance f...
55		Gauri Agarwal	Work	2	Output Quality Assurance f...
56		Tanya Jain	Work	3	Cost Analysis
57		Kaneesha Jain	Work	2	Cost Analysis
58		Sanya Sachan	Work	2	Output Quality Assurance f...
59		Pratyush Shrivastava	Work	2	Output Quality Assurance f...
60		Aahna Jain	Work	2	Output Quality Assurance f...
61		**⊟DOCUMENTATION**	**Work**	**DAYS TO FINISH**	
62		Utkarsh	Work	2	Project Libre
63		Kabir	Work	2	"Mind map, correcting specif...
64		Keshav	Work	2	"Parts of model

Figure 1.8: Resource Breakdown (contd.)

		Name	Type	Text2	Text1
65		Ishant	Work	2	Sofwares used
66		Shivaani	Work	2	References
67		Nilay	Work	2	Glossary and Abbreviations
68		Shivang	Work	2	Doc stats, ID, readability
69		Sachin	Work	2	CAD Models,frequency and ...
70		Pratyush	Work	2	Glosaary and abbreviations
71		Madhav	Work	2	Stages of working (DEMO d...
72		Ojas	Work	2	Stages of working (Industria...
73		Om	Work	2	MoM
74		shashwat	Work	2	Types of wave and their imp...
75		Yuvraj	Work	2	Arduino codes and Simulations

Figure 1.9: Resource Breakdown (contd.)

1.4 Project Statement

Design and development of a function generator that, within a Rs 1000 budget, replicates the features, specifications, and layout of the generator used in ELP101.According to the requirements of our stakeholders the FG must support the same frequency range, waveform types, amplitude control, and other essential features as the "Scientech 4064S".

1.5 Abstract

As part of Project 1, we are creating a **Function Generator**—a highly adaptable electronic device designed to produce various periodic waveforms, including sine, square, triangular, and sawtooth waves. Our goal is to replicate some of the functionalities of the **Scientech 4064S Function Generator** that is used in the lab. This device allows users to adjust frequency, amplitude, and duty cycle, making it a perfect tool for tasks like electronics testing, debugging, and circuit design.

Key features of the Function Generator:

1. Precise frequency adjustments for accurate signal output.
2. Multiple waveform options to suit diverse testing needs.
3. A user-friendly interface for quick and efficient operation.

Function Generator is an essential tool for any electronics lab, offering flexibility and precision for a wide range of applications. The employment of cheap parts providing sufficient performances is foreseen within the frame of this project. The resulting design becomes a means of instruction for hands-on awareness of techniques of waveform generation in lab work.

1.6 Motivation

An affordable and adequately engineered Function Generator is a major requirement for electronic experiments in general and elp101 in specific. While the broader electronics market is substantial, our initial focus is on equipping educational institutions, specifically those conducting introductory electronics laboratory courses similar to **ELP101.** These labs form the bedrock of electronics education, introducing students to fundamental circuit concepts and signal manipulation. Currently, many institutions rely on **older, less versatile** equipment or face budget constraints when acquiring modern function generators.

Our product aims to bridge this gap by offering a **cost-effective solution** with comparable capabilities compared to commonly used, basic function generators. While alternatives like the XR2206 exist, our product offers **a superior frequency range (10 MHz vs. 1 MHz) at a comparable or lower price point**, directly benefiting institutions with limited budgets. This improved performance allows students to explore a wider range of experiments and gain a deeper understanding of signal behavior.

This targeted approach to the educational market allows for efficient development and production scaling appropriate for the initial demand. While we acknowledge the potential for wider applications in hobbyist communities and small businesses in the long term, our primary objective is to provide a reliable and capable tool for foundational electronics education, starting with institutions conducting courses akin to **ELP101.** This focused strategy allows us to establish a strong foothold in a key segment before considering expansion into other markets. The product will still deliver multiple waveform generations **(sine, square, triangle, ramp, and pulse)**, adjustable output signal amplitude (Vpp), and DC offset capabilities, meeting the core requirements of these educational labs. Our maintenance strategy will prioritize rapid support for these educational institutions, ensuring minimal disruption to lab schedules.

2. Requirements

2.1 Functional Requirements

2.1.1 Input Requirements

1. **Control Interfaces**:
   - Physical rotary knobs for coarse adjustments.[17]
   - Additional knob for finer adjustment of frequency values.[17]
2. **Modulation Inputs**:
   - Supports Amplitude Modulation (AM), Frequency Modulation (FM), and Phase Modulation (PM) modulation modes.
3. **Additional Inputs**:
   - Toggle switches for function selection.[34]
   - 2/3-pin input connectors for external components.
   - A Printed Circuit Board (PCB), onto which components would be soldered.[14]

2.1.2 Output Requirements

1. **Display Module (20x4 Liquid Crystal Display (LCD))**: [3]
   - HD44780 Compatible 20x4 LCD.
   - Capable of displaying 20 characters per line and 4 lines.
   - Allows clear visualization of frequency, amplitude, and waveform type.
   - Contrast adjustable via a 10kΩ potentiometer.[31]
2. **Waveform Types**: Sine, square, triangular, pulse, ramp, TTL.
3. **Output Impedance**: Configured to 50 Ω for compatibility with standard test equipment.
4. **Waveform Accuracy**: Less than 1% Total Harmonic Distortion (THD) for sine waves.
5. **Waveform Symmetry**: Adjustable from 1% to 99% (duty cycle).

6. **Voltage Offset**: Programmable Direct Current (DC) offset adjustable between -5 V and +5V.
7. **Frequency Precision**: Accuracy within 0.01% of the programmed value.
8. **Frequency Resolution**: Fine adjustments of the order of 1 mHz.
9. **Signal Stability**: Output frequency drift not exceeding 0.01%.
10. **Amplitude Range**: Adjustable output from 0 to 5 V (peak-to-peak) with a resolution of 0.01V.
11. **Output Connectors**:
    - BNC(Female) connectors for high-quality signal output.
    - Optional backlight connection via a 220Ω resistor for current limiting.

2.1.3 Power Requirements

1. **Power Consumption**: Maximum 20 W under full load.
2. **Voltage Compatability**: Requires a standard Alternating Current (AC) input (220 V/50 Hz).

2.1.4 Logistical Requirements

1. **Accessories**: Supplied with BNC cables, probes, knobs, and a user manual.
2. **Carry Case**: Optional carry case for portability.

2.1.5 Environmental Requirements

1. **Operating Temperature**: Functional from 0°C to 50°C.
2. **Storage Temperature**: Safe storage from -20°C to 70°C.
3. **Humidity Resistance**: Operates in environments with up to 80% relative humidity (non-condensing).
4. **Electromagnetic Interference (EMI)/Electromagnetic Compatibility (EMC) Compliance**: Meets regulatory standards such as FCC and CE compliance.

2.1.6 Site (Usage Site) Requirements

1. **Laboratory Use**: Designed for standard electronics laboratories with clean and stable workbenches.
2. **Power Outlet Compatibility**: Supports both EU and US power outlet standards with adapters.

2.1.7 Structural Requirements

1. **Chassis**: Durable recycled plastic enclosure with heat resistance.
2. **Control Panel**:
   - Intuitive layout with labeled controls.
   - Backlit buttons for visibility in low-light conditions.
3. **Protective Measures**:
   - Fuse for circuit protection.
   - Shielding to minimize interference and protect internal components.

2.1.8 Time Requirements

1. **Design Time Requirement**: Development and testing to be completed within 6 months.
2. **Time to Market Requirement**: Ready for commercial launch within 9 months from project initiation.
3. **Lifetime Requirements**: Guaranteed operational life of at least 5 years with proper maintenance.
4. **End of Life Requirements**: Must support recycling and environmentally safe disposal of components.

2.2 Non-Functional Requirements

2.2.1 Aesthetic Design

1. **Aesthetic Design**: Modern, sleek appearance with an ergonomic design.

2.2.2 Safety

1. **Safety**: Certified for safety under International Electrotechnical Commission (IEC) 61010-1 standards.

2.2.3 Serviceability

1. **Serviceability**: Modular design for easy part replacement.

2.2.4 Reliability

1. **Reliability**: Mean Time Between Failures (Mean Time Between Failures (MTBF)) of at least 10,000 operational hours.

3. Specifications

3.1 Hardware Specifications

The project utilizes the ATmega328P microcontroller, a widely used 8-bit microcontroller known for its efficiency and versatility. The key hardware specifications are as follows:

- **Processor:** ATmega328P, a high-performance, low-power 8-bit AVR microcontroller.
- **Memory:**
  - 32KB of in-system programmable flash memory.
  - 2KB of SRAM.
  - 1KB of EEPROM with 100,000 write/erase cycles.
- **Architecture:** Advanced RISC architecture with 131 instructions, most executed in a single clock cycle, enabling up to 16 MIPS throughput at 16 MHz.
- **Clock Speed:** Supports up to 16 MHz clock frequency.
- **Power Consumption:**
  - Active mode: 1.5mA at 4 MHz and 3V.
  - Power-down mode: As low as 1µA.
- **Operating Voltage Range:** 2.7V to 5.5V, suitable for automotive and industrial applications.
- **Peripherals:**
  - 6 PWM channels.
  - 8-channel 10-bit ADC.
  - USART, SPI, and I^2C communication protocols.
  - Three Timer/Counters: Two 8-bit and one 16-bit.
  - Interrupt and wake-up on pin change.
- **I/O Pins:** 23 programmable I/O lines.
- **Temperature Range:** Operates between -40°C and +125°C.
- **Programming:** In-system programming with onboard bootloader and SPI interface.

- **Quality Standards:** Manufactured according to ISO-TS-16949 and verified with AEC-Q100 Grade 1 standards [9].

3.2 Software Specifications

The software specifications for the project include:

- **Development Environment:** Arduino IDE for programming and uploading sketches to the ATmega328P microcontroller.
- **Programming Language:** C/C++ for firmware development.
- **Libraries:**
  - Standard Arduino libraries for GPIO, PWM, ADC, I^2C, and SPI.
  - Additional custom libraries for specific project needs.
- **Simulation and Testing Tools:**
  - Proteus or TinkerCAD for circuit simulation and debugging.
- **Version Control:** Git for source code management and collaboration.
- **Additional Features:** Integration with Arduino Cloud Editor for remote programming and debugging.

3.3 Comparative Analysis: Arduino Uno vs. Arduino Nano

For our **function generator project**, we selected the **Arduino Uno** over the Nano due to its beginner-friendly features, better stability, and ease of expansion. A comparison of key factors is provided below: [8]

- **Beginner-Friendly Design:** The Uno features a **USB Type-B** connector, avoiding driver issues common with the Nano's micro-USB. It also has a **barrel jack** for stable power input, making it easier to use.
- **Easy Hardware Integration:** Unlike the Nano, the Uno supports **plug-and-play shields**, reducing wiring complexity and making hardware expansion easier.
- **Better Stability & Debugging:** While both have a USB-to-serial converter, the Uno is more reliable and requires fewer driver installations. Its **larger PCB** also improves heat dissipation and durability.

3.4 Comparative Analysis: Sine Wave using Arduino Uno vs Using RC Filter

Analysis is being done in the context of application in ELP101 laboratory experiments.

3.4.1 Function Generator & Amplifier Performance

Objective

- Analyze whether amplifiers generate the expected functionality using a function generator.

Voltage Follower

- A voltage follower (buffer) ideally produces an output identical to the input.
- It has high input impedance and low output impedance.
- Real-world performance is affected by the op-amp's finite slew rate.

Effect with Step Wave Input

- The op-amp lags behind rapid input changes due to slew rate limitations.
- Overshoot and ringing may occur if the input step changes too quickly.
- This effect is critical in high-speed applications where signal integrity is a concern.

Effect with RC Filtered Input

- The RC filter smooths transitions, reducing abrupt input changes. [26]
- The output follows the input more closely, ensuring better signal isolation.
- However, at high frequencies, RC filters introduce:
  - Attenuation
  - Phase shifts
  - Distortions that may affect the op-amp's behavior

Comparison

- In low-frequency applications, RC filtering provides a more stable and predictable output than a step wave.

Inverting and Non-Inverting Amplifiers

- Op-amp amplifiers in inverting and non-inverting configurations react differently based on the input waveform.

Effect with Step Wave Input

- Fast transitions in the step signal can exceed the op-amp's slew rate, causing:
  - Distortion or incomplete output steps
  - Reduced accuracy in signal reproduction

3.4.2 Effect with RC Filtered Input

- The smoother signal is easier for the amplifier to process.
- However, attenuation and phase shifts can still alter the signal's characteristics.

Slew Rate

- The slew rate of an op-amp is the maximum rate at which the output voltage changes in response to a fast input signal.
- Expressed in volts per microsecond (V/µs), it determines how well an op-amp can handle high-frequency or fast-transient signals.

3.4.3 Effect of Step or RC Signals Instead of Sinusoids

- Sinusoidal signals allow steady-state operation, while step or RC signals disrupt it.

Key Effects

- The circuit won't settle, making it difficult to measure steady voltages or phases.[37]
- Phasor diagrams won't apply as they are only valid for sinusoidal signals.
- Capacitor & inductor response changes produce:
  - Sudden voltage/current spikes
  - Oscillations instead of smooth behavior
- The oscilloscope will show fluctuating signals, making comparisons with theoretical predictions challenging.

3.4.4 Effects of Non-Sinusoidal Signals in Rectifiers & Clippers

- **Rectifier (Diode):** [23]
  - Only positive (or negative) half-cycles of the stepped waveform appear in the output.
  - The steps remain in the waveform since the rectifier does not smooth them.
  - Amplitude alternates between rectified and zero regions.
- **Clipper (Diodes):**
  - Clips signal at set levels, removing portions beyond a threshold.
  - The remaining waveform still exhibits jitter and irregularities from the original signal.
- **Clamper:**
  - Shifts the waveform vertically while preserving its shape.
  - The sharp step transitions remain unchanged as the clamper only affects the DC level.

3.5 Space specifications

- **Outer casing:** The outer body of the function generator has dimensions of 20 cm x 7.5 cm x 27.5 cm.
- **Display:** The area occupied by the display screen is 7.5 cm x 2.5 cm on the front panel of the function generator.

3.6 Cost specifications

Component	**Quantity**	**Price per Unit (Rs)**	**Total (Rs)**
LM741, SMD Opamp	5	9	45
Resistor 5k	10	0.4	4
Resistor 1k	10	0.5	5
Capacitor 1μF	2	8.55	17
3-Pin Potentiometer (10k)	4	30	120
Rotary Switches	3	30	90
Push Buttons	9	5	45
20x4 LCD Display with I2C Connector	1	275	275
Atmega328P Chip	1	161	161
Reset Button	2	8	16
Acrylic Sheet	2.5 sqft	20	50
Crystal Oscillator 16MHz	1	6	6
Voltage Regulator 5V, LM7805	2	10	20
Transformer 12-0-12, 500mA	1	76	76
BNC Connector (Female)	1	49	49
IC AD9833	1	250	250
LM7809 IC	1	8.5	9
470μF Capacitor	1	8.75	9
220μF Capacitor	1	4	4
104pF Capacitor	1	1	1
10k Resistor	6	0.5	3
1N4007 Diodes (1000V,1A)	8	1	8

Component	Quantity	Price per Unit (Rs)	Total (Rs)
1000μF, 25V Capacitor	2	16	32
Voltage Regulator 12V, LM7812	2	9	18

Table 3.1: Components and Pricing

Total cost = Rs. 1312.35

3.7 Performance specifications:

- **Waveforms:**
  - Sine wave: Frequency range of 1 MHz to 10 MHz.
  - Square wave: Frequency range of 1 MHz to 3 MHz.
  - Triangular wave: Frequency range of 1 MHz to 3 MHz.
  - Pulse wave: Adjustable duty cycle (1% –99%), frequency up to 3 MHz.
  - Ramp wave: Frequency range of 1 MHz to 3 .
  - TTL wave: Frequency range of 1 MHz to 3 MHz.
- **Front panel:** Contains knobs and switches to alternate between modes, and set the parameters of the wave to be generated, through both coarse and fine tuning.

3.8 Milestone Specifications

Table 3.2: CAD Milestones and Sub tasks

Milestone	Description	Subtasks	Weightage	Total Weightage	Date
CAD	Outer casing of dimensions 20 cm x 7.5 cm x 27.5 cm	in (.CAD extension file)	3		
		Isometric view	0.5		
		Top view	0.5		
		Front view	0.5		
		Right view	0.5	5	
	Display of 7.5 cm x 2.5 cm	in (.CAD extension file)	3		
		Isometric view	0.5		
		Top view	0.5		
		Front view	0.5		
		Right view	0.5	5	
	4 poles for support, to provide an elevated platform for the function generator	in (.CAD extension file)	3		
		Isometric view	0.5		
		Top view	0.5		
		Front view	0.5		
		Right view	0.5	5	
	Buttons and knobs for setting frequency modes, fine and coarse tuning of wave parameters	in (.CAD extension file)	3		
		Isometric view	0.5		
		Top view	0.5		

Milestone	Description	Subtasks	Weightage	Total Weigh-tage	Date
		Front view	0.5		
		Right view	0.5	5	
	Consolidated CAD file	in (.CAD extension file)	5	5	04/02/25
			Total Weightage	**25**	

Table 3.3: Software Simulations Milestones and Sub tasks

Milestone	Description	Sub tasks	Weightage	Total Weigh-tage	Date
Software simulations	Chip programming	Code for generating different types of waves		14	
		Sine wave	4		
		Square wave	2		
		TTL wave	2		
		Triangle wave	2		
		Pulse wave	2		
		Ramp wave	2		
	Display programming	Programming the display to show details of the set waveforms	5	5	
	Achieving milestones	Compilation of results from past weeks	6	6	05/02/25
			Total weightage	**25**	

Table 3.4: Fabrication Milestones and Sub tasks

Milestone	**Description**	**Sub tasks**	**Weightage**	**Total Weigh-tage**	**Date**
Fabrication	Container as described in the final CAD model, along with 4 poles at the bottom to stabilize the function generator body, having power supply ports and other ports for connection purposes.	Required size	4	16	
		Poles	4		
		Stable	4		
		Ports	4		
	The front panel has buttons and knobs for switching on, changing waveform, adjusting frequency, amplitude, and overall display.	Buttons	3	9	
		Knobs	3		
		Display	3		06/02/25
			Total Weightage	**25**	

Table 3.5: Demo Milestones and Sub tasks

Milestone	**Description**	**Sub tasks**	**Weightage**	**Total Weigh-tage**	**Date**
DEMO	Similar display and front panel of FG as that in the lab		4	4	
	Button presses work as intended		4	4	
	All types of waves are generated of required frequencies and alternate on button press	Sine wave	2	12	
		Square wave	2		
		Triangular wave	2		
		Pulse wave	2		
		Ramp wave	2		
		TTL wave	2		
	Milestones 1, 2, and 3 are completed		5	5	07/02/25
			Total Weightage	**25**	

3.9 Man-hour specifications

3.9.1 Man-hours

Table 3.6: Man-hours invested

S.no	Role	Name	Entry No	Man-hours invested
1	Tribe Coordinator and Hardware Design and Fabrication	Saiyam Jain	2022MT11962	16.0
2	Deputy Tribe Coordinator and Documentation	Shivaani Hari	2022MT11273	16.0
3	Activity Coordinator-Hardware Design and Fabrication	Vagesh Mahajan	2022MT11260	14.0
4	Activity Coordinator-Software	Shrenik Mohan Sakala	2022MT11920	14.0
5	Activity Coordinator-Testing and Debugging (Hardware)	Madhav Maheshwari	2022MT61975	10.0
6	Activity Coordinator-Market Survey and Research	Rahul Athipatla	2022MT11277	9.0
7	Activity Coordinator-Documentation	Nilay Sharma	2022MT12007	16.0
8	Market Survey and Research	Aahna Jain	2022MT11930	8.0
9	Testing and Debugging (Hardware)	Abhishek Kumar Singh	2022MT11276	8.0
10	Hardware Design and Fabrication	Abhishek Singh	2022MT11934	11.0
11	Hardware Design and Fabrication	Adarsh Singh	2022MT11285	9.0
12	Testing and Debugging (Hardware)	Aditya Goyal	2022EE31761	7.0
13	Testing and Debugging (Hardware)	Aditya Raj	2022MT61980	7.0
14	Hardware Design and Fabrication	Ajaypal Kulhari	2022EE11711	10.0
15	Testing and Debugging (Hardware)	Aman Divya	2022MT11293	7.0

Table continues on the next page

S.no	Role	Name	Entry No	Man-Hours
16	Hardware Design and Fabrication	Ambhore Soham Bhaskar	2022EE11713	10.0
17	Software	Arnav Tiwari	2022MT11267	10.0
18	Hardware Design and Fabrication	Arpit Mourya	2022EE11728	10.0
19	Market Survey and Research	Ashmit Nangia	2022EE11989	7.0
20	Market Survey and Research	Ayush Nayak	2022MT11958	8.0
21	Testing and Debugging (Hardware)	Ayush Raj	2022MT11944	7.0
22	Software	Chintada Srinivasarao	2022MT11924	9.0
23	Hardware Design and Fabrication	Deevyansh Khadria	2022EE31883	9.0
24	Testing and Debugging (Hardware)	Dev Singh	2022MT11143	8.0
25	Software	Devansh Upadhyay	2022MT11931	8.0
26	Software	Dhruv Chaurasiya	2022MT11172	9.0
27	Software	Galla Yaswant Venkata Ramana	2022EE11687	8.0
28	Market Survey and Research	Gauri Agarwal	2021EE10715	7.0
29	Testing and Debugging (Hardware)	Ishan Bankal	2022EE31779	7.0
30	Documentation	Ishant Yadav	2022MT11397	9.0
31	Hardware Design and Fabrication	Jenit Jain	2022EE11690	14.0
32	Documentation	Kabir Uberoi	2022MT61202	12.0
33	Market Survey and Research	Kaneesha Jain	2022MT11929	10.0
34	Documentation	Keshav Rai	2022MT61968	9.0
35	Hardware Design and Fabrication	Khushi Gupta	2022MT61973	9.0
36	Testing and Debugging (Hardware)	Krish Singh	2022MT61303	8.0
37	Software	Lakshaya Jain	2022MT11933	8.0
38	Documentation	Madhav Biyani	2022EE11321	9.0

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S.no	Role	Name	Entry No	Man-Hours
39	Software	Manas Goyal	2022MT11918	11.0
40	Software	Mukul Sahu	2022MT11939	10.0
41	Hardware Design and Fabrication	Nagure Kalyani Paramanand	2022MT61983	9.0
42	Testing and Debugging (Hardware)	Naman Kale	2022MT11960	9.0
43	Software	Nimkar Abhinav Yashwant	2022MT11943	10.0
44	Software	Niraj Agarwal	2022MT11921	10.0
45	Software	Niranjan Rajeev	2022EE11766	8.0
46	Software	Nobin Kidangan Benny	2022EE11154	10.0
47	Documentation	Ojas Sharma	2022EE31746	8.0
48	Documentation	Om Goel	2022MT12071	10.0
49	Testing and Debugging (Hardware)	Parth Bhardwaj	2022MT11257	8.0
50	Documentation	Pratyush Sharma	2022MT61970	9.0
51	Market Survey and Research	Pratyush Shrivastava	2022EE11660	8.0
52	Software	Praveen Lakhara	2022MT11280	9.0
53	Software	Priyansh Prakash Mayank	2022MT11954	10.0
54	Hardware Design and Fabrication	Priyanshu Jindal	2022EE11668	9.0
55	Software	Punit Meena	2022EE11184	11.0
56	Testing and Debugging (Hardware)	Rahul Rajoria	2022MT11947	9.0
57	Testing and Debugging (Hardware)	Raman Jakhar	2022MT11941	7.0
58	Testing and Debugging (Hardware)	Ranjan Kumar Singh	2022MT61304	9.0
59	Software	Rijul Rudrax Barot	2022EE11664	8.0
60	Testing and Debugging (Hardware)	Rudranil Naskar	2022MT11287	6.0

Table continues on the next page

S.no	Role	Name	Entry No	Man-Hours
61	Documentation	Sachin Hiren Trivedi	2022EE11190	8.0
62	Hardware Design and Fabrication	Saksham Kumar Rohilla	2022EE11709	10.0
63	Market Survey and Research	Sanya Sachan	2022MT11286	9.0
64	Software	Sarthak Gangwal	2022MT11275	8.0
65	Market Survey and Research	Satvik Prasad S	2022MT11279	8.0
66	Documentation	Shashwat Kasliwal	2022MT11915	9.0
67	Documentation	Shivang Goyal	2022MT11269	9.0
68	Software	Siddharth Saini	2022MT11283	9.0
69	Market Research and Survey	Siya Gupta	2022MT11274	7.0
70	Testing and Debugging (Hardware)	Sparsh Jain	2022MT11917	9.0
71	Hardware Design and Fabrication	Suhani Soni	2022MT61981	8.0
72	Software	Sumit Sonowal	2022MT11296	10.0
73	Software	Suneel Masarapu	2022MT11942	9.0
74	Hardware Design and Fabrication	Sushil Kumar	2022EE31765	9.0
75	Hardware Design and Fabrication	Syna Rajvanshi	2022MT61974	10.0
76	Market Survey and Research	Tanya Jain	2022MT11935	9.0
77	Testing and Debugging (Hardware)	Taru Singhal	2022MT11922	8.0
78	Testing and Debugging (Hardware)	Tatsam Ranjan Sharma	2022MT61969	9.0
79	Hardware Design and Fabrication	Tirth Punit Golwala	2022MT11967	10.0
80	Hardware Design and Fabrication	Tushar Goyal	2022MT11266	10.0
81	Hardware Design and Fabrication	Umang Agarwal	2022EE11692	8.0
82	Documentation	Utkarsh Dubey	2022MT61045	10.0

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S.no	Role	Name	Entry No	Man-Hours
83	Hardware Design and Fabrication	Vatsal Manish Sejpal	2022MT11926	9.0
84	Hardware Design and Fabrication	Viha Singla	2022MT61972	9.0
85	Documentation	Yuvraj Singh	2022EE11715	7.0

3.9.2 Skillset

Table 3.7: Skillset acquired

S.no	Role	Name	Entry No	Skillset
1	Tribe Coordinator and Hardware Design and Fabrication	Saiyam Jain	2022MT11962	LaTeX, soldering
2	Deputy Tribe Coordinator and Documentation	Shivaani Hari	2022MT11273	LaTeX, Zotero, soldering
3	Activity Coordinator-Hardware Design and Fabrication	Vagesh Mahajan	2022MT11260	RDWorks
4	Activity Coordinator-Software	Shrenik Mohan Sakala	2022MT11920	Arduino programming using TinkerCAD, SimulIDE
5	Activity Coordinator-Testing and Debugging (Hardware)	Madhav Maheshwari	2022MT61975	FreeCADweb
6	Activity Coordinator-Market Survey and Research	Rahul Athipatla	2022MT11277	Stakeholder Analysis, Cost Optimisation
7	Activity Coordinator-Documentation	Nilay Sharma	2022MT12007	LaTeX, Zotero
8	Market Survey and Research	Aahna Jain	2022MT11930	Cost analysis from different websites
9	Testing and Debugging (Hardware)	Abhishek Kumar Singh	2022MT11276	FreeCADweb and LaTeX
10	Hardware Design and Fabrication	Abhishek Singh	2022MT11934	RDWorks, Laser Cutting

Table continues on the next page

S.no	Role	Name	Entry No	Skillset
11	Hardware Design and Fabrication	Adarsh Singh	2022MT11285	RDWorks, Laser Cutting
12	Testing and Debugging (Hardware)	Aditya Goyal	2022EE31761	FreeCADweb
13	Testing and Debugging (Hardware)	Aditya Raj	2022MT61980	Circuit building
14	Hardware Design and Fabrication	Ajaypal Kulhari	2022EE11711	Circuit Design
15	Testing and Debugging (Hardware)	Aman Divya	2022MT11293	FreeCADweb
16	Hardware Design and Fabrication	Ambhore Soham Bhaskar	2022EE11713	Arduino functions like Analogwrite().RC Filters
17	Software	Arnav Tiwari	2022MT11267	TinkerCAD,SimulIDE
18	Hardware Design and Fabrication	Arpit Mourya	2022EE11728	PCB software LTM
19	Market Survey and Research	Ashmit Nangia	2022EE11989	Market Analysis
20	Market Survey and Research	Ayush Nayak	2022MT11958	Stakeholder Analysis, Cost Optimisation
21	Testing and Debugging (Hardware)	Ayush Raj	2022MT11944	Market base analysis
22	Software	Chintada Srinivasarao	2022MT11924	Circuit Simulation in TinkerCAD and SimulIDE
23	Hardware Design and Fabrication	Deevyansh Khadria	2022EE31883	Circuit Simulation in SimulIDE
24	Testing and Debugging (Hardware)	Dev Singh	2022MT11143	Circuit Analysis
25	Software	Devansh Upadhyay	2022MT11931	Circuit Design
26	Software	Dhruv Chaurasiya	2022MT11172	Circuit Simulations in TinkerCAD
27	Software	Galla Yaswant Venkata Ramana	2022EE11687	Basics of TinkerCAD
28	Market Survey and Research	Gauri Agarwal	2021EE10715	Stakeholder Analysis

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S.no	Role	Name	Entry No	Skillset
29	Testing and Debugging (Hardware)	Ishan Bankal	2022EE31779	Circuit Analysis, GitHub
30	Documentation	Ishant Yadav	2022MT11397	LaTeX
31	Hardware Design and Fabrication	Jenit Jain	2022EE11690	Circuit simulation in LTspice
32	Documentation	Kabir Uberoi	2022MT61202	LaTeX, PlantText
33	Market Survey and Research	Kaneesha Jain	2022MT11929	Cost analysis and optimization
34	Documentation	Keshav Rai	2022MT61968	LaTeX
35	Hardware Design and Fabrication	Khushi Gupta	2022MT61973	RDWorks, Laser Cutting
36	Testing and Debugging (Hardware)	Krish Singh	2022MT61303	Circuit Analysis
37	Software	Lakshaya Jain	2022MT11933	Circuit Simulations in TinkerCAD
38	Documentation	Madhav Biyani	2022EE11321	LaTeX
39	Software	Manas Goyal	2022MT11918	Arduino programming using TinkerCAD, SimulIDE
40	Software	Mukul Sahu	2022MT11939	Circuit Simulations in TinkerCAD, Wokwi, Basic Display Programming
41	Hardware Design and Fabrication	Nagure Kalyani Paramanand	2022MT61983	RDWorks, Laser Cutting
42	Testing and Debugging (Hardware)	Naman Kale	2022MT11960	FreeCADweb
43	Software	Nimkar Abhinav Yashwant	2022MT11943	TinkerCAD,WOKWI circuit simulations for display programming using LiquidCrystal I2C
44	Software	Niraj Agarwal	2022MT11921	TinkerCAD
45	Software	Niranjan Rajeev	2022EE11766	TinkerCAD
46	Software	Nobin Kidangan Benny	2022EE11154	TinkerCAD, Wokwi

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S.no	Role	Name	Entry No	Skillset
47	Documentation	Ojas Sharma	2022EE31746	LaTeX
48	Documentation	Om Goel	2022MT12071	LaTeX, PlantText
49	Testing and Debugging (Hardware)	Parth Bhardwaj	2022MT11257	LaTeX
50	Documentation	Pratyush Sharma	2022MT61970	LaTeX
51	Market Survey and Research	Pratyush Shrivastava	2022EE11660	Cost Optimization, LaTeX
52	Software	Praveen Lakhara	2022MT11280	Circuit Simulations in TinkerCAD
53	Software	Priyansh Prakash Mayank	2022MT11954	Circuit simulation in WOKWI and TinkerCAD for LiquidCrystal I2C display programming
54	Hardware Design and Fabrication	Priyanshu Jindal	2022EE11668	Altium, LtSpice Simulations
55	Software	Punit Meena	2022EE11184	TinkerCAD, Wokwi
56	Testing and Debugging (Hardware)	Rahul Rajoria	2022MT11947	TinkerCAD
57	Testing and Debugging (Hardware)	Raman Jakhar	2022MT11941	TinkerCAD
58	Testing and Debugging (Hardware)	Ranjan Kumar Singh	2022MT61304	using tools and techniques to find and fix problems in hardware and software.
59	Software	Rijul Rudrax Barot	2022EE11664	TinkerCAD
60	Testing and Debugging (Hardware)	Rudranil Naskar	2022MT11287	FreeCADweb, LaTeX
61	Documentation	Sachin Hiren Trivedi	2022EE11190	LaTeX
62	Hardware Design and Fabrication	Saksham Kumar Rohilla	2022EE11709	Circuit Design
63	Market Survey and Research	Sanya Sachan	2022MT11286	Selecting the best market option based on quality, price, and specific needs

Table continues on the next page

S.no	Role	Name	Entry No	Skillset
64	Software	Sarthak Gangwal	2022MT11275	Circuit Simulations in TinkerCAD, Wokwi, Basic Display Programming
65	Market Survey and Research	Satvik Prasad S	2022MT11279	Analyzing components and It's evaluating market value .
66	Documentation	Shashwat Kasliwal	2022MT11915	LaTeX
67	Documentation	Shivang Goyal	2022MT11269	LaTeX
68	Software	Siddharth Saini	2022MT11283	TinkerCAD
69	Market Research and Survey	Siya Gupta	2022MT11274	Cost analysis
70	Testing and Debugging (Hardware)	Sparsh Jain	2022MT11917	FreeCADweb
71	Hardware Design and Fabrication	Suhani Soni	2022MT61981	RDWorks, Laser Cutting
72	Software	Sumit Sonowal	2022MT11296	Circuit Simulations in TinkerCAD
73	Software	Suneel Masarapu	2022MT11942	Circuit Simulations in SimulIDE
74	Hardware Design and Fabrication	Sushil Kumar	2022EE31765	Circuit Design
75	Hardware Design and Fabrication	Syna Rajvanshi	2022MT61974	RDWorks, Laser Cutting
76	Market Survey and Research	Tanya Jain	2022MT11947	Optimal cost estimation techniques, research
77	Testing and Debugging (Hardware)	Taru Singhal	2022MT11922	LaTeXand FreeCADweb
78	Testing and Debugging (Hardware)	Tatsam Ranjan Sharma	2022MT61969	3-D Modelling
79	Hardware Design and Fabrication	Tirth Punit Golwala	2022MT11967	RDWorks, Laser Cutting
80	Hardware Design and Fabrication	Tushar Goyal	2022MT11266	TinkerCAD

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S.no	Role	Name	Entry No	Skillset
81	Hardware Design and Fabrication	Umang Agarwal	2022EE11692	Circuit analysis
82	Documentation	Utkarsh Dubey	2022MT61045	LaTeX, Project Libre
83	Hardware Design and Fabrication	Vatsal Manish Sejpal	2022MT11926	RDWorks
84	Hardware Design and Fabrication	Viha Singla	2022MT61972	RDWorks, Laser Cutting
85	Documentation	Yuvraj Singh	2022EE11715	

3.9.3 How Assignment was Done

We divided the assignments among the team members based on their individual strengths and preferences. This was achieved by documenting each member's skillset and areas of interest. We strategically assigned tasks, such as delegating the majority of hardware and debugging responsibilities to Electrical Engineering students, and assigning documentation and software development to Mathematics students respectively. This approach fostered a highly coordinated and efficient team where each member effectively contributed to the project's timely completion.

3.9.4 Surplus Manpower

To date, the project has progressed smoothly without encountering any instances of surplus manpower. Proactive resource allocation and regular progress reviews have ensured that team members are effectively utilized and their skills are aligned with the project's evolving needs. This proactive approach minimizes the risk of under utilization and allows for efficient and timely task completion.

3.9.5 TRL Description

Our design of the function generator is currently at Technology Readiness Level (TRL) 2. This indicates that the concept and application have been formulated but the technology is still in the early research and development stage. The design has not yet been prototyped or validated through testing and evaluation, and further research, prototyping and optimization is required to move it towards a more advanced prototype.

4. Design

4.1 Model

4.1.1 Parts of Model

The function generator model consists of various parts that play a crucial role in its operation and usability:

Outer Casing

The outer casing provides structural support and protection for internal components. It ensures durability and safeguards the internal circuitry from external damage.

Display

The display shows waveform details, frequency, and amplitude settings for user interaction. It allows users to monitor and adjust parameters effectively.

Support Poles

Support poles elevate the function generator body, providing stability and ensuring the device remains securely positioned during operation.

Buttons and Knobs

Buttons and knobs allow users to switch modes, change waveforms, and adjust parameters. They form the primary means of manual control over the function generator.

Ports

Ports facilitate power input and connectivity with external devices for signal transmission. They enable integration with other electronic equipment for various applications.

Front Panel

The front panel serves as the main user interface, integrating all buttons, knobs, and the display. It provides an organized layout for user-friendly operation.

4.2 Demo Function Generator Design and Working

Our function generator is designed to replicate some of the essential features of an industrial function generator while maintaining cost-effectiveness and simplicity.

4.2.1 Design

The demo function generator features a simplified yet effective design:

- **Plastic outer casing** for lightweight portability and cost efficiency.
- **20x4 LCD display** for showing frequency, waveform type, and amplitude settings.
- **ATmega328P microcontroller** for generating and controlling waveform outputs.
- **Rotary knobs and push buttons** for adjusting frequency, waveform type, and amplitude.
- **BNC output connector** for interfacing with oscilloscopes and other test equipment.
- **Power supply module** that converts 220V AC to 12V DC for stable operation.

4.2.2 Working

The demo function generator operates through a structured process:

1. The user selects the waveform type and frequency using **rotary knobs and buttons**.
2. The **ATmega328P microcontroller** processes the input and generates the corresponding waveform digitally.
3. The waveform is passed through a **low-pass filter** to smooth out digital artifacts.
4. The processed signal is amplified and made available through the **BNC output port**.
5. The LCD display continuously updates with real-time information about the selected waveform and settings.

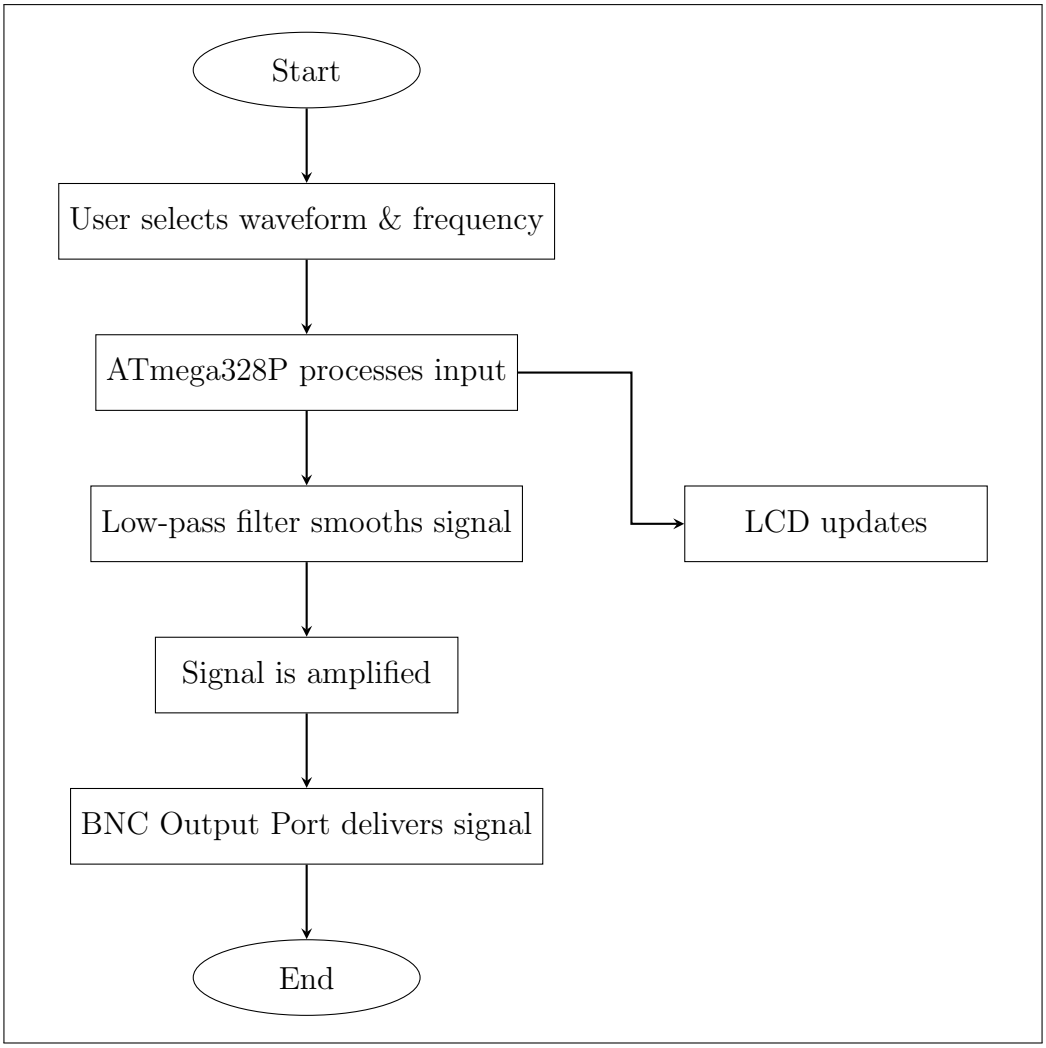

Figure 4.1: Flowchart of the Function Generator Working

This demo function generator provides a cost-effective yet functional alternative to industrial models, making it suitable for educational and small-scale testing applications.

4.3 CAD Models

4.3.1 Outer Casing

The outer casing provides structural support and protection for internal components. It ensures durability and safeguards the internal circuitry from external damage.

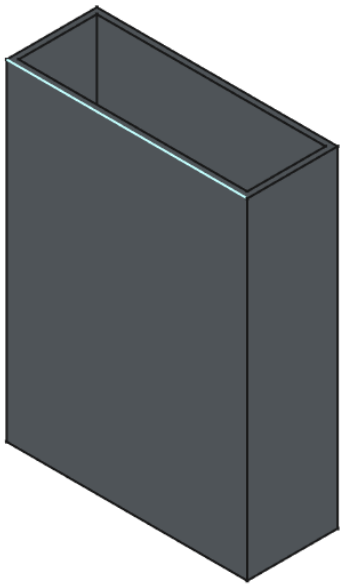

Figure 4.2: Isometric view of Outer Casing(Produced using FreeCADweb)

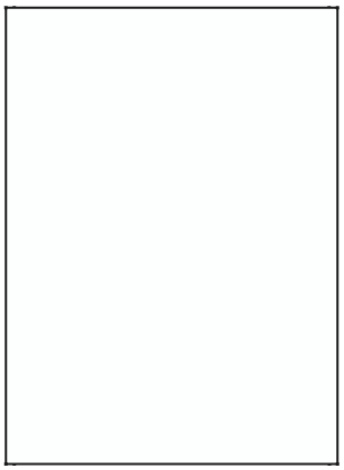

Figure 4.3: Top view of Outer Casing(Produced using FreeCADweb)

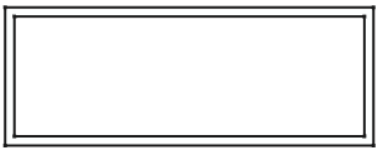

Figure 4.4: Front view of Outer Casing(Produced using FreeCADweb)

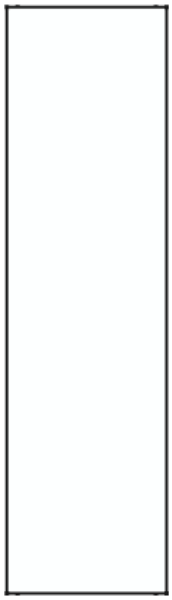

Figure 4.5: Right view of Outer Casing(Produced using FreeCADweb)

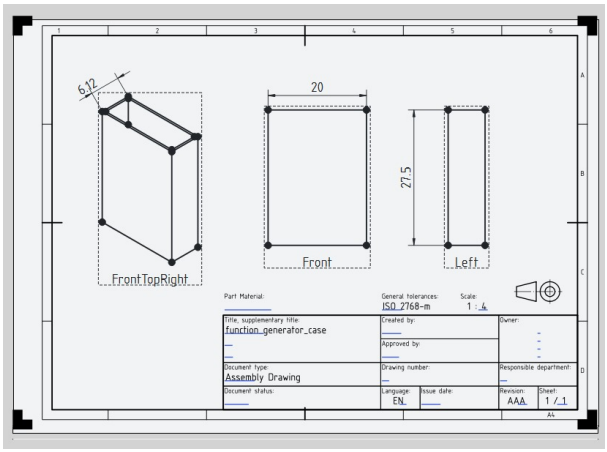

Figure 4.6: Drawing of Outer Casing(Produced using FreeCADweb)

4.3.2 Display

The display shows waveform details, frequency, and amplitude settings for user interaction. It allows users to monitor and adjust parameters effectively.

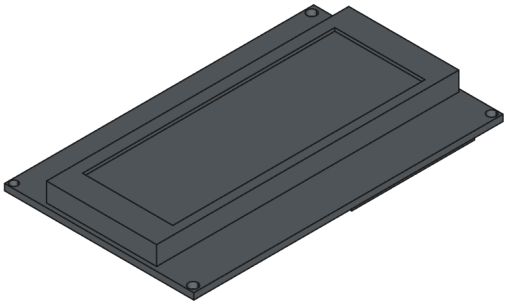

Figure 4.7: Isometric view of Display(Produced using FreeCADweb)

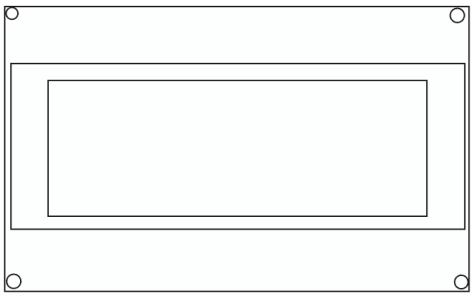

Figure 4.8: Top view of Display(Produced using FreeCADweb)

Figure 4.9: Front view of Display(Produced using FreeCADweb)

Figure 4.10: Right view of Display(Produced using FreeCADweb)

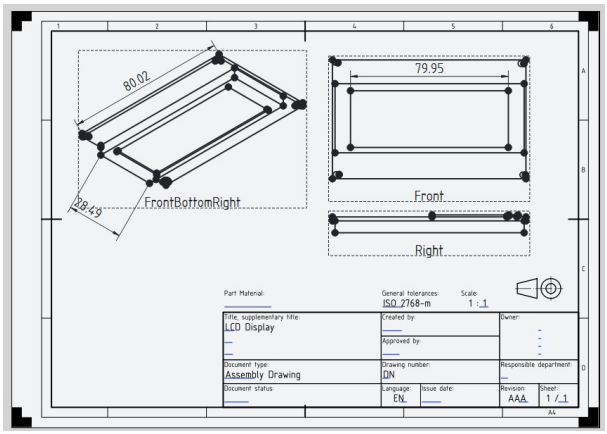

Figure 4.11: Drawing of Display(Produced using FreeCADweb)

4.3.3 Support Poles

The support poles elevate the function generator body, providing stability and ensuring the device remains securely positioned during operation.

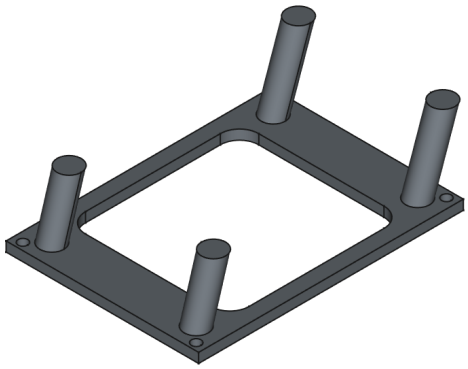

Figure 4.12: Isometric view of Support Poles(Produced using FreeCADweb)

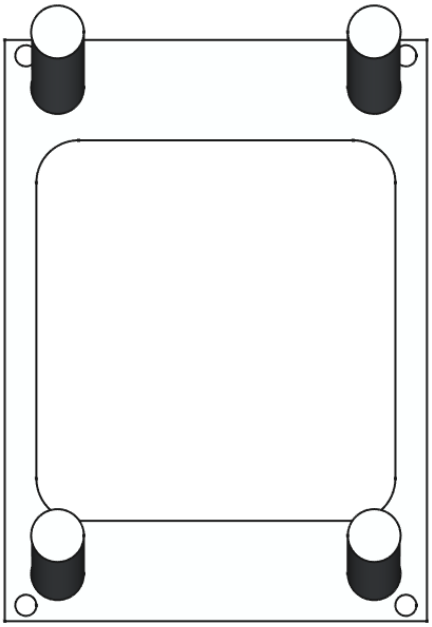

Figure 4.13: Top view of Support Poles(Produced using FreeCADweb)

Figure 4.14: Front view of Support Poles(Produced using FreeCADweb)

Figure 4.15: Right view of Support Poles(Produced using FreeCADweb)

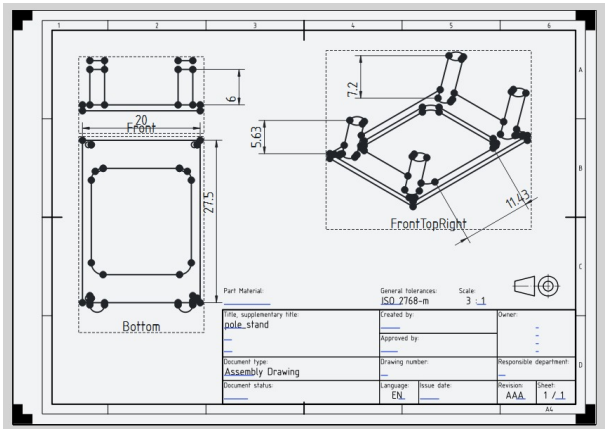

Figure 4.16: Drawing of Support Poles(Produced using FreeCADweb)

4.3.4 Body

The buttons allow users to switch modes and interact with the function generator. They form a crucial part of the manual control system.

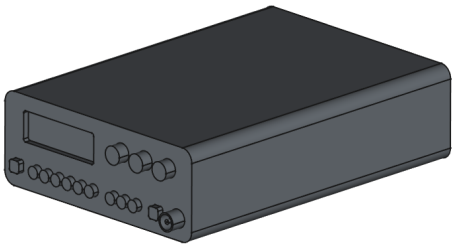

Figure 4.17: Isometric view of Body(Produced using FreeCADweb)

Figure 4.18: Top view of Body(Produced using FreeCADweb)

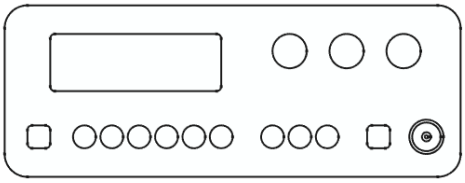

Figure 4.19: Front view of Body(Produced using FreeCADweb)

Figure 4.20: Right view of Body(Produced using FreeCADweb)

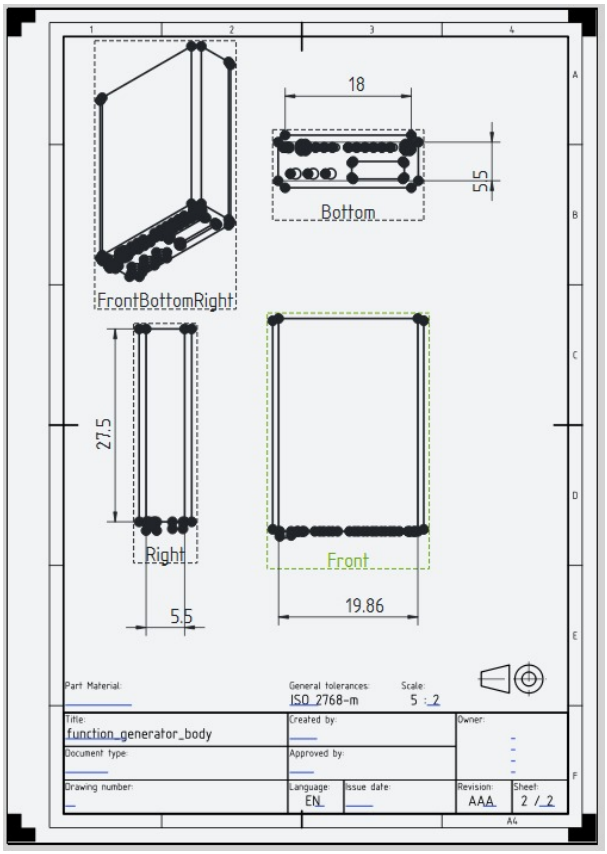

Figure 4.21: Drawing of Body(Produced using FreeCADweb)

4.3.5 Potent Knobs

The knobs allow users to adjust parameters such as amplitude and frequency. They provide precise control over waveform settings.

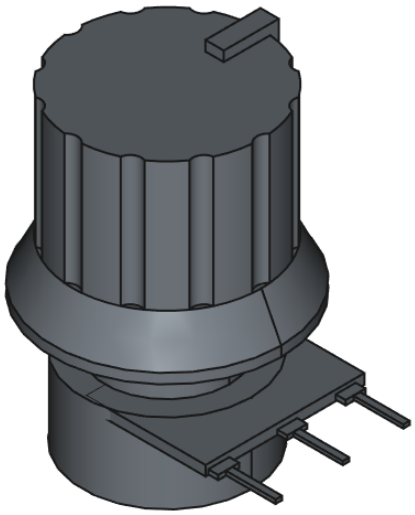

Figure 4.22: Isometric View of Potent knob(Produced using FreeCADweb)

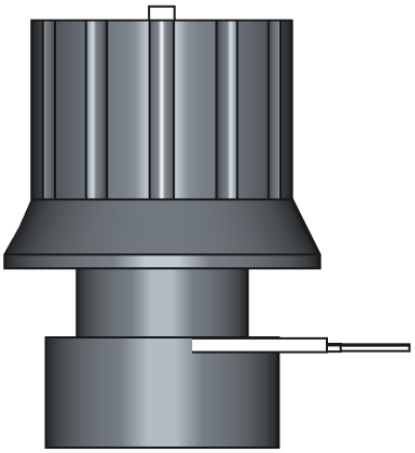

Figure 4.23: Top View of Potent knob(Produced using FreeCADweb)

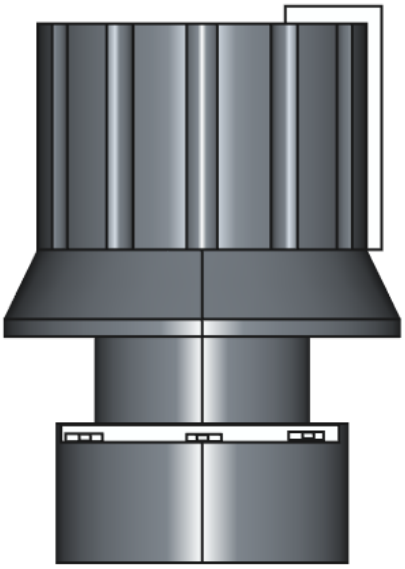

Figure 4.24: Front view of Potent knob(Produced using FreeCADweb)

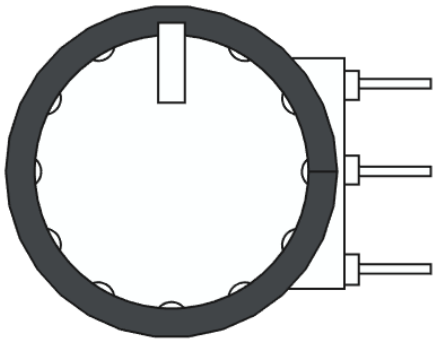

Figure 4.25: Right View of Potent knob(Produced using FreeCADweb)

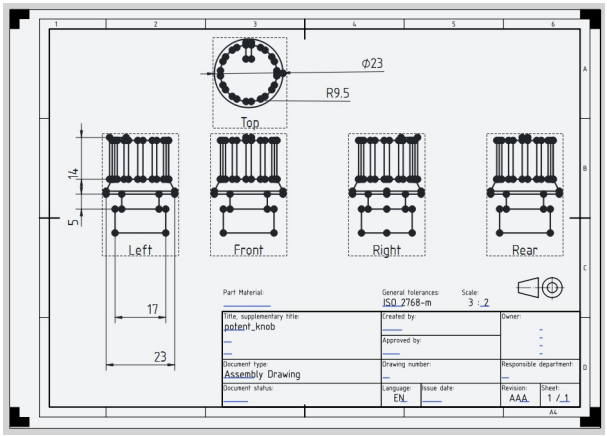

Figure 4.26: Drawing of Potent knob(Produced using FreeCADweb)

4.3.6 Push button

The knobs allow users to adjust parameters such as amplitude and frequency. They provide precise control over waveform settings.

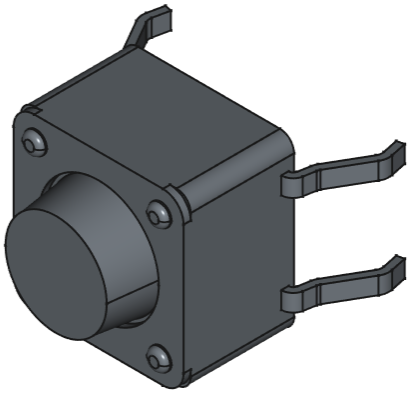

Figure 4.27: Isometric View of Push Button(Produced using FreeCADweb)

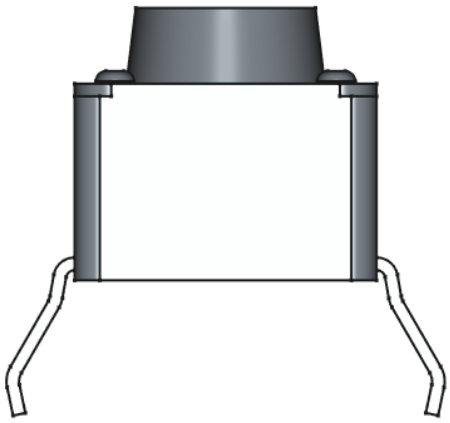

Figure 4.28: Top View of Push Button(Produced using FreeCADweb)

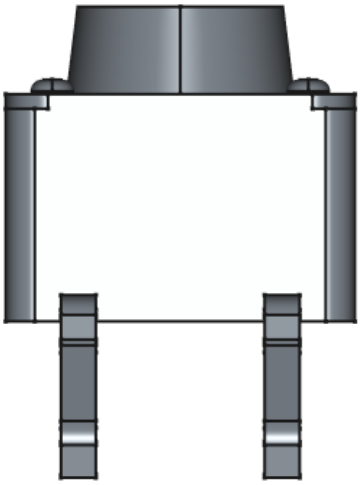

Figure 4.29: Front View of Push Button(Produced using FreeCADweb)

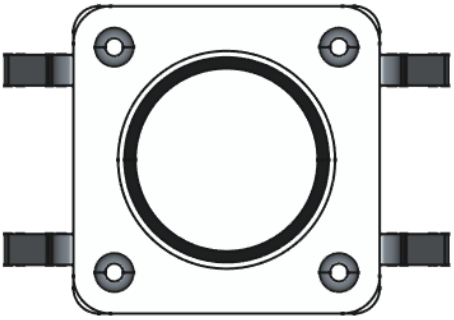

Figure 4.30: Right View of Push Button(Produced using FreeCADweb)

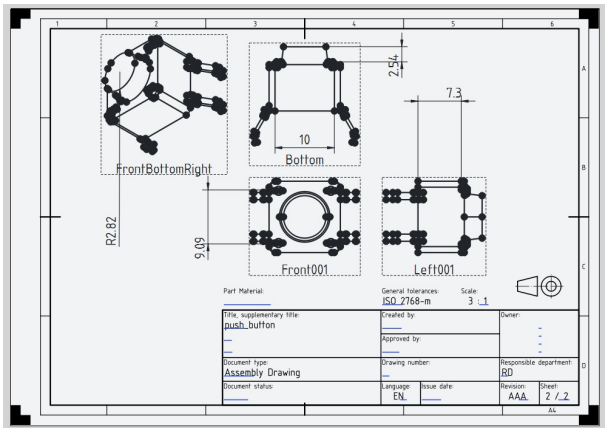

Figure 4.31: Drawing of Push Button(Produced using FreeCADweb)

4.3.7 Reset button

The knobs allow users to adjust parameters such as amplitude and frequency. They provide precise control over waveform settings.

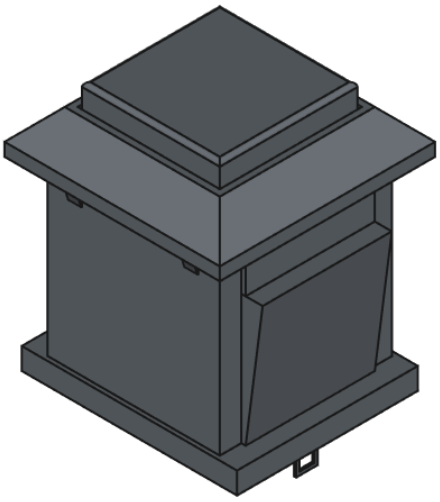

Figure 4.32: Isometric View of Reset Button(Produced using FreeCADweb)

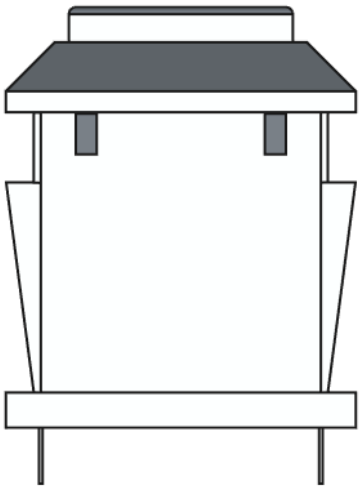

Figure 4.33: Top View of Reset Button(Produced using FreeCADweb)

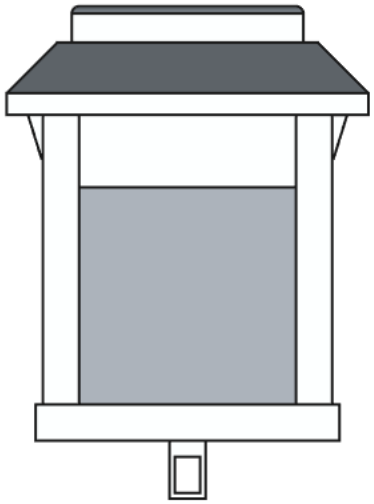

Figure 4.34: Front View of Reset Button(Produced using FreeCADweb)

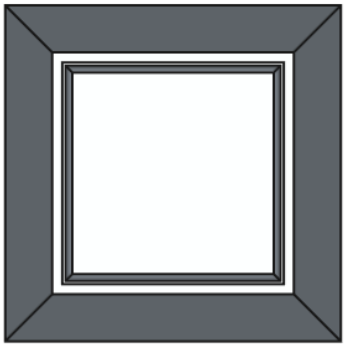

Figure 4.35: Right View of Reset Button(Produced using FreeCADweb)

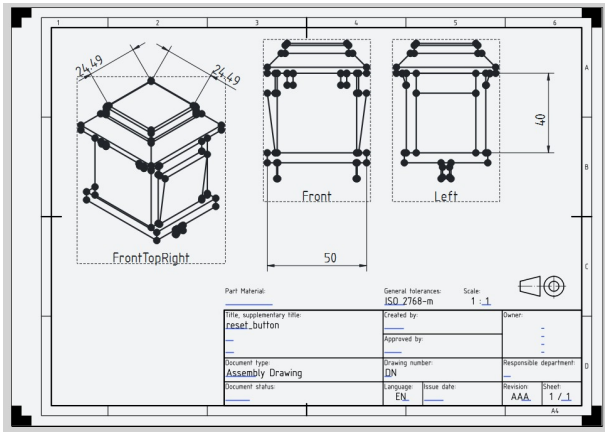

Figure 4.36: Drawing of Reset Button(Produced using FreeCADweb)

4.4 Types of Waveform & their Generation

4.4.1 Square Wave

The square wave is generated by toggling a digital pin between HIGH and LOW states based on a delay controlled by user input, such as a potentiometer. This delay determines the frequency of the output waveform. Square waves are fundamental in digital systems, where they are used to represent binary logic, generate clock signals, and test digital circuits. The ATmega328P microcontroller processes the input, updates the LCD to reflect changes, and sends the waveform through the output port for testing or control applications.

4.4.2 Ramp Wave

The ramp wave is created by charging and discharging a capacitor in a controlled manner, producing a voltage that linearly decreases over time. The slope of the waveform is determined by the input provided to the microcontroller, which manages the timing for the charging and discharging cycle. Ramp waves are commonly used in analog signal processing, oscilloscopes, and radar systems. However, care must be taken to avoid distortion caused by exceeding the bandwidth limitations of the circuit.

4.4.3 Sine Wave

The sine wave is generated using a predefined lookup table of sine values stored in memory, which the microcontroller outputs periodically using a timer interrupt. This approach ensures smooth and continuous waveforms, with the frequency adjustable via user input. Sine waves are widely used in signal analysis, testing analog filters, and generating carrier signals for communication systems. The low-pass filter smooths the output, and the waveform is delivered through an amplified port.

4.4.4 Triangular Wave

The triangular wave is formed by linearly increasing and then decreasing the signal's voltage using pulse-width modulation (PWM). The duty cycle is incremented and decremented systematically, creating a waveform with a consistent rise and fall. This waveform is ideal for audio signal processing, testing linear circuit responses, and controlling motors. The ATmega328P processes the input, adjusts the waveform parameters, and delivers the signal through the output port for various applications.

4.4.5 Pulse Wave

The pulse wave is generated by toggling a digital output pin based on a duty cycle, which is defined by the load factor. Instead of using traditional delay-based methods, this program utilizes the millis() function to calculate elapsed time, allowing the program to remain responsive to other tasks or inputs. The load factor determines the proportion of time the signal stays in the HIGH state during a complete time period. This method provides precise control over the waveform's duty cycle and frequency without interrupting the microcontroller's functionality. Pulse waves are widely used in applications such as PWM-based motor speed control, LED dimming, and signal modulation. By relying on a non-blocking approach, the program ensures accurate and flexible pulse generation while maintaining overall system responsiveness.

4.5 Voltage Amplitude Control

Figure 4.23 focuses on a simplified circuit for amplitude control.

- The 1 k potentiometer directly controls the amplitude of the square wave signal from the function generator.
- By increasing or decreasing resistance, it modifies how much of the input signal is passed to the output.

The graph shows how adjusting the potentiometer changes the amplitude of the square wave without affecting its frequency.

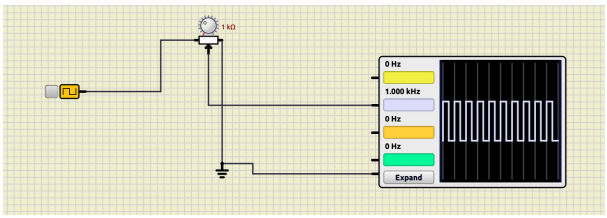

Figure 4.37: Voltage Amplitude Variation(Produced using TinkerCAD)

4.6 DC Offset Control

Figure 4.24 demonstrates how a function generator produces a waveform with adjustable DC Offset. Key components include:

- **Operational Amplifier (Op-Amp):** The op-amp is configured as an amplifier to amplify the offset signal. The amplification is controlled by the feedback resistor and input resistor ratio.
- **Voltage Divider (Potentiometer):** The 1 k potentiometer adjusts the input voltage to the op-amp. By varying the potentiometer, the input signal's amplitude changes, which is reflected in the output waveform.
- **Resistor:** Fixed resistors (10 k) set the gain of the op-amp and stabilize the circuit.
- **Output:** The output waveform's amplitude is directly proportional to the input voltage adjusted by the potentiometer.

The waveform displayed on the right confirms that changing the potentiometer alters the amplitude of the generated signal by changing the DC offset.

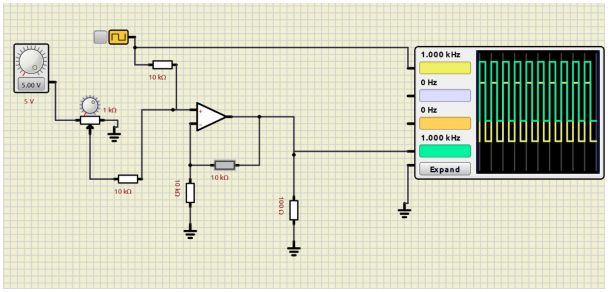

Figure 4.38: DC Offset Control(Produced using TinkerCAD)

4.7 Arduino Code

Our function generator is programmed using Arduino to generate different waveforms, including square, ramp, sine, and triangular waves. The following sections provide the Arduino code for each waveform.

4.7.1 Code for Square Wave

```
void setup(){
  pinMode(A0, INPUT);
  pinMode(7, OUTPUT);

}

void loop(){
  int d = analogRead(A0); // the reading from the potetiometer
  digitalWrite(7,HIGH);
  delay(d);
  digitalWrite(7, LOW);
  delay(d);
}
```

4.7.2 Code for Ramp Wave

```
/*Negative Slope Ramp.
In this case not all range of frequencies
gives appropriate ramp cause of the
filtering nature of the cap in this circuit.

Limit in bandwidth of input!

Sometimes during change in frequency or amplitude
the output gets distored. Our guess is due to cap overloading
when going beyond the bandwidth limit.

Stopping and running the simulation
does seem to solve the problem for the sake of observation.
*/

void setup(){
  pinMode(A1, INPUT);
  pinMode(4, OUTPUT);

}

void loop(){
  int input = analogRead(A1);
  digitalWrite(4,HIGH);
  delay(0.5);
  digitalWrite(4, LOW);

  delay(input);
}

```

4.7.3 Code for Sine Wave

```
1
2  #include <avr/interrupt.h>
3  #include <stdlib.h>
4
5
6  char sinetable [32];
7  int  i ;
8  int val = 0;
9
10
11 void ioinit (void)
12 {
13
14   DDRD  = B11111111;
15   pinMode(A5, INPUT);
16
17
18
19 }
20
21 void timer_setup(){
22   TCCR2A = 0;
23   TCNT2= 455;    //455 outputs 1.007khz
24   TCCR2B = B00000010;
25   //Timer2 Overflow Interrupt Enable
26   TIMSK2 = 1<<TOIE2;
27 }
28 void setup(){
29
30   Serial.begin(9600);
31   ioinit();
32   arraysetup();
33   cli();
34   timer_setup();
35   i = 0;
36   sei();
37
38
39
40
41 }
42
43
44 ISR(TIMER2_OVF_vect) {
45
46
```

```
47    PORTD=(sinetable[i++]);
48    TCNT2= val / 4;
49
50    if(i==32){
51      i=0;
52  }
53  }
54  void arraysetup(void){
55    sinetable[0]=127;
56    sinetable[1]=152;
57    sinetable[2]=176;
58    sinetable[3]=198;
59    sinetable[4]=217;
60    sinetable[5]=233;
61    sinetable[6]=245;
62    sinetable[7]=252;
63    sinetable[8]=254;
64    sinetable[9]=252;
65    sinetable[10]=245;
66    sinetable[11]=233;
67    sinetable[12]=217;
68    sinetable[13]=198;
69    sinetable[14]=176;
70    sinetable[15]=152;
71    sinetable[16]=128;
72    sinetable[17]=103;
73    sinetable[18]=79;
74    sinetable[19]=57;
75    sinetable[20]=38;
76    sinetable[21]=22;
77    sinetable[22]=10;
78    sinetable[23]=3;
79    sinetable[24]=0;
80    sinetable[25]=3;
81    sinetable[26]=10;
82    sinetable[27]=22;
83    sinetable[28]=38;
84    sinetable[29]=57;
85    sinetable[30]=79;
86    sinetable[31]=103;
87  }
88  void loop()
89  { val = analogRead(A5);
90   Serial.println(val);
91
92
93
94
```

```
}
```

4.7.4 Code for Triangular Wave

```
#define OUTPUT_PWM_PIN 3

int x;

void setup()
{
  pinMode(OUTPUT_PWM_PIN, OUTPUT);
}

void loop()
{
  for (x = 0; x <= 255; x++)
  {
    analogWrite(OUTPUT_PWM_PIN, x);
    delay(2);
  }

  for (x = 255; x >= 0; x--)
  {
    analogWrite(OUTPUT_PWM_PIN, x);
    delay(2);
  }
}
```

4.7.5 Code for Pulse Wave

```
void setup()
{
  pinMode(10, OUTPUT);
}

double load_factor = 0.4;
int time_period = 1000;
int prev_time = 0;
bool signal_high = false;

void loop()
{
  int curr_time = millis();
  if (signal_high){
    if (curr_time - prev_time >= time_period*load_factor){
      digitalWrite(10, LOW); signal_high = false;
      prev_time = curr_time;
```

```
    }
  }
  else {
    if (curr_time - prev_time >= time_period*(1 - load_factor)){
      digitalWrite(10, HIGH); signal_high = true;
      prev_time = curr_time;
    }
  }

}
```

4.8 Software Simulations

4.8.1 Simulation for Square Wave

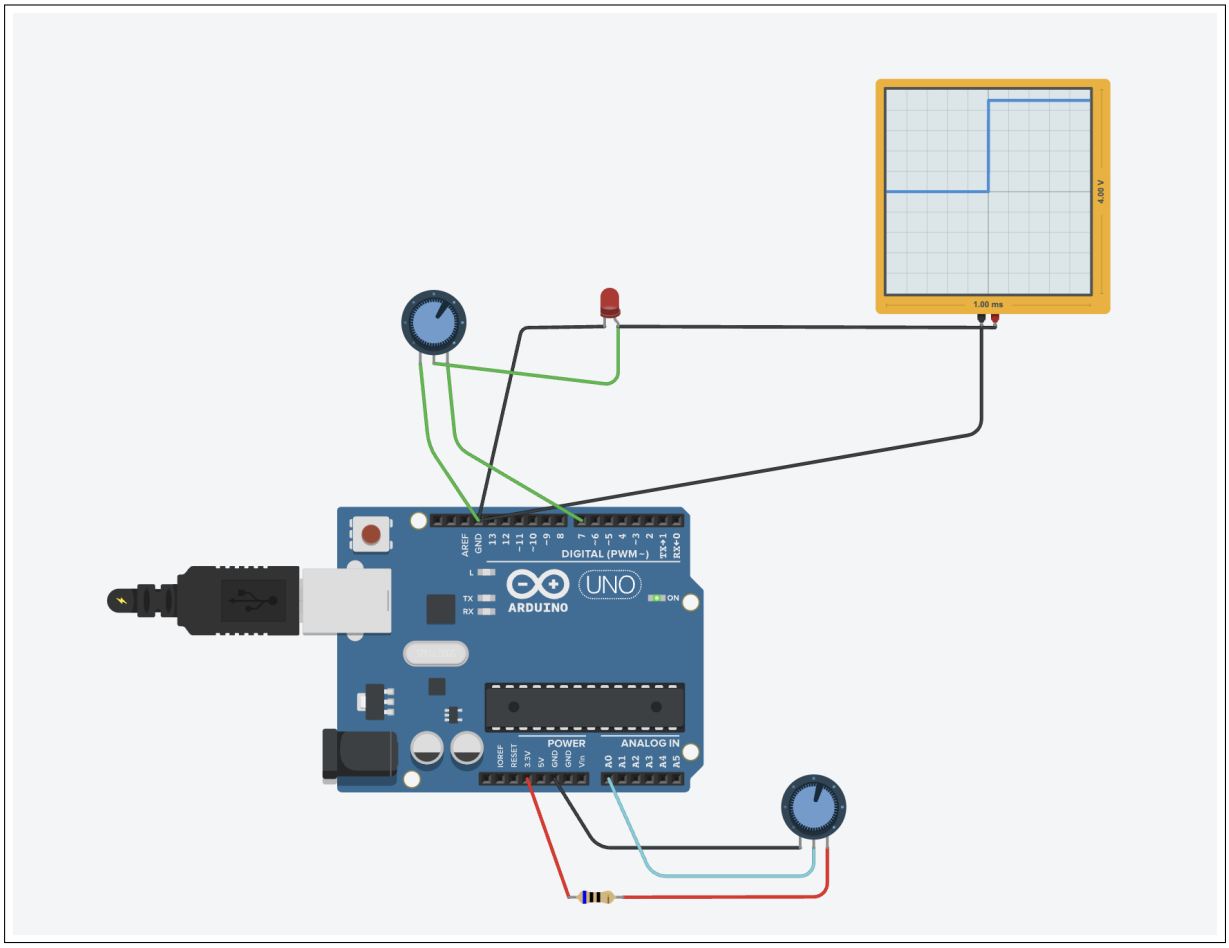

Figure 4.39: Simulation of Square Wave(Produced using TinkerCAD)

4.8.2 Simulation for Ramp Wave

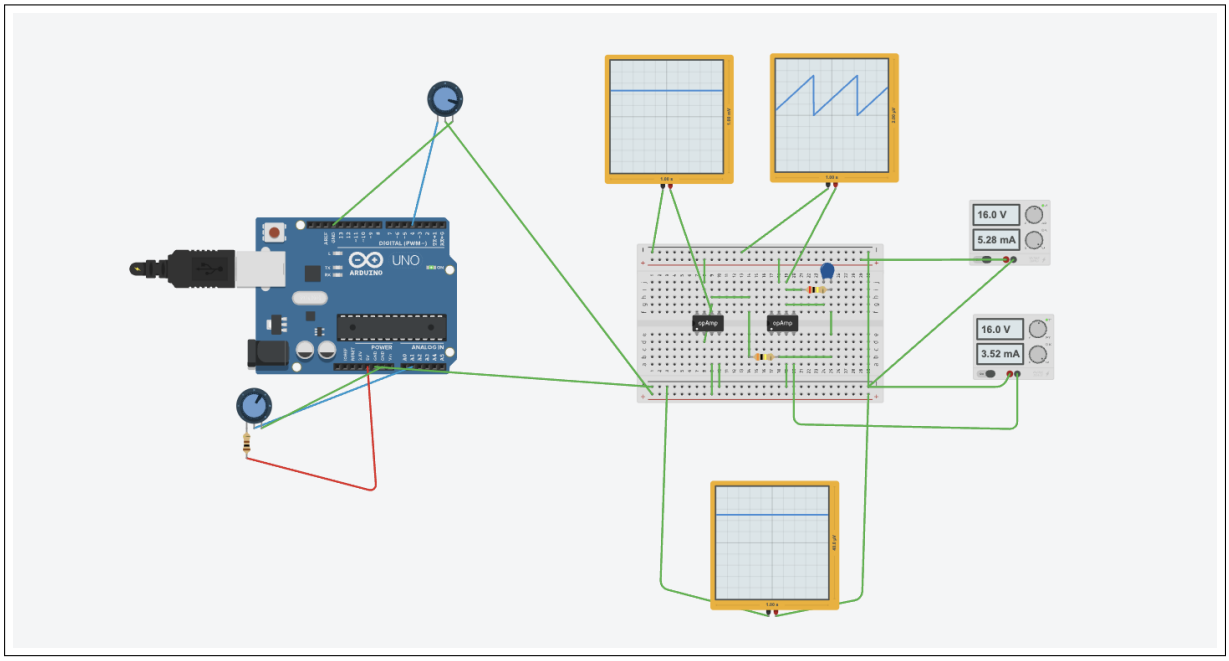

Figure 4.40: Simulation of Ramp Wave(Produced using TinkerCAD)

4.8.3 Simulation for Sine Wave

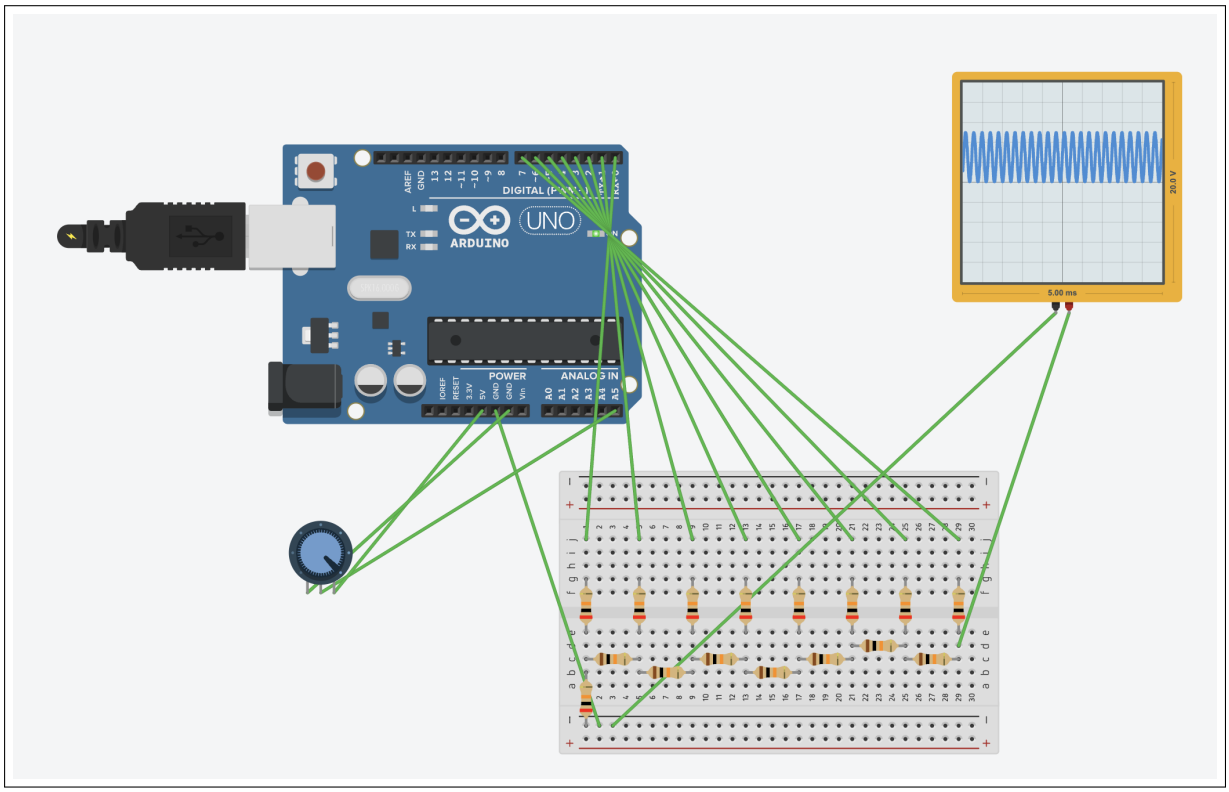

Figure 4.41: Simulation of Sine Wave(Produced using TinkerCAD)

4.8.4 Simulation for Triangular Wave

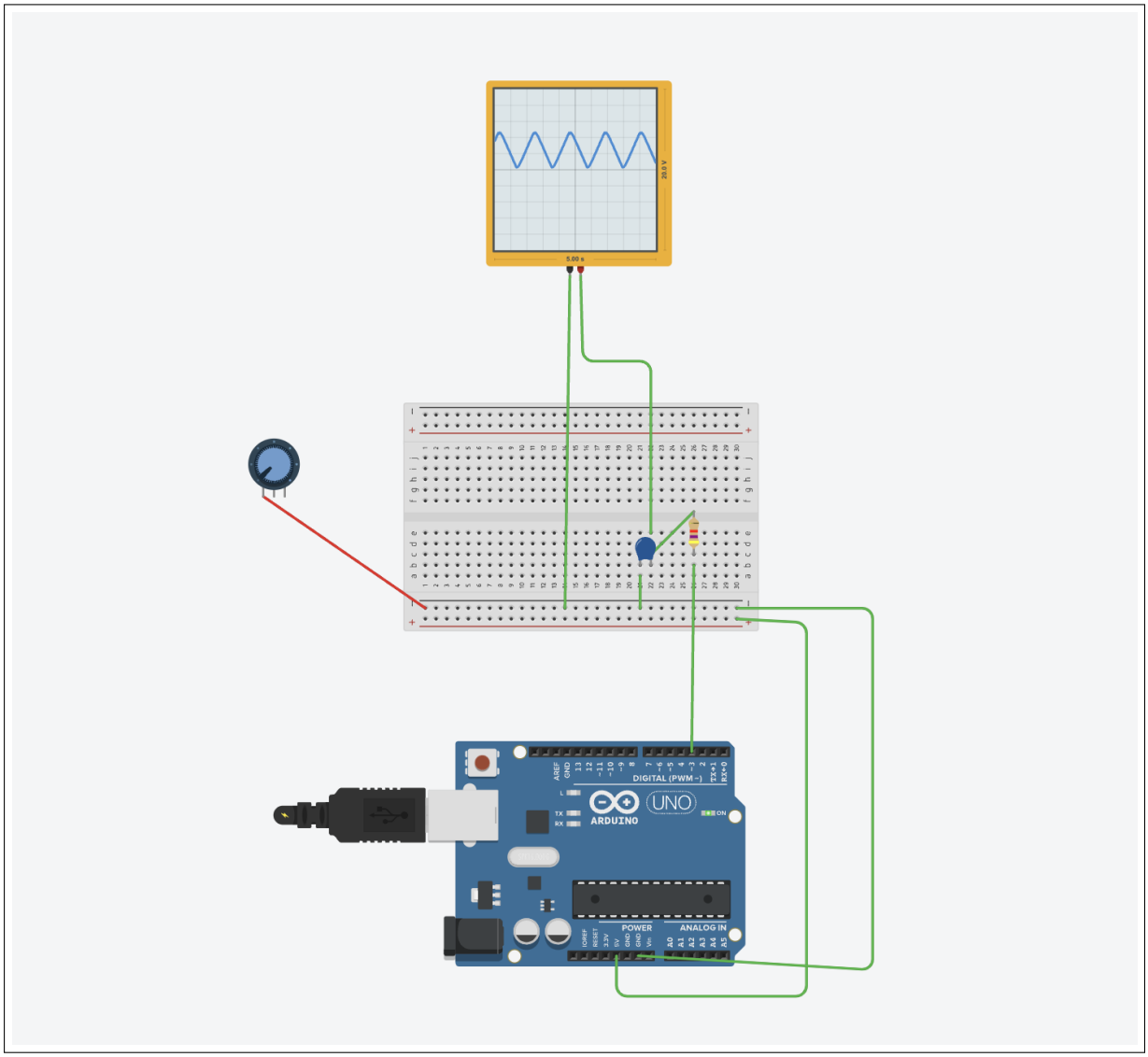

Figure 4.42: Simulation of Triangular Wave(Produced using TinkerCAD)

4.8.5 Simulation for Pulse Wave

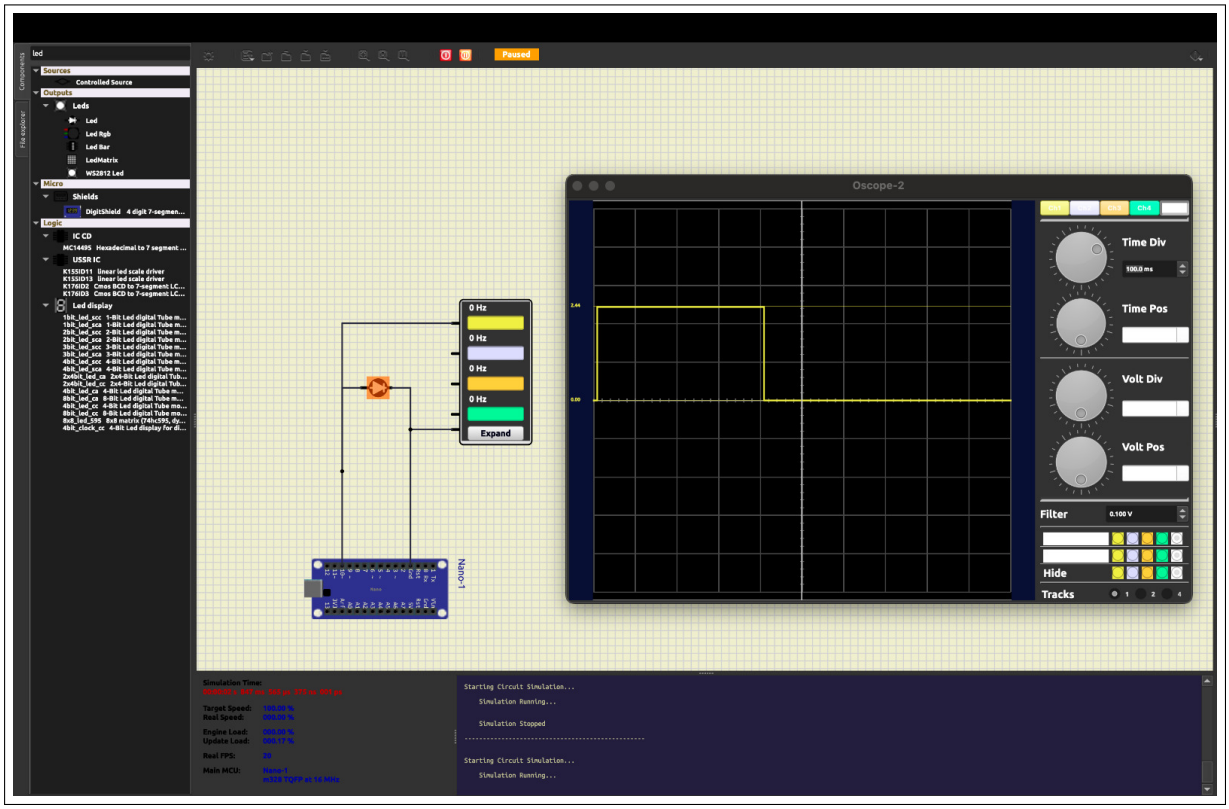

Figure 4.43: Simulation of Pulse Wave(Produced using SimulIDE)

4.9 Design Iterations

4.9.1 Software Iterations

Chip Programming

We chose arduino UNO on the basis of the findings of the research subtribe. Then we divided ourselves into pairs and each pair was tasked with generation, coding and simulation of one type of waveform along with varying frequency and amplitude. We then discussed all these simulations and codes and made improvements as suggested during the discussion. Through simulations we found slight jaggedness in the sine waveform at low frequencies which was likely due to the step function implementation. Further through simulation and lab tryout we also discovered that despite theoretical possibilities, **arduino** UNO or **microcontrollers** in general have a limit on the frequency they can achieve which is capped around **1 kHz**. Based on specifications of the function generator we decided to make, we had to achieve up to at least **1 MHz**. For the same on research and exploration of function generator production we narrowed down on a chip (**IC AD9833**) for waveform generation over a broad frequency range. Next we plan on simulating and testing the same.

Display Programming

There were many options available on which display to use some of the options listed- **OLED, TFT, LCD, LED** We needed a display with some basic features like displaying alphabets and numbers, easy to use, compatible with Arduino Nano(Atmega328p) and preferably low cost. We researched about different displays like **OLED - 128x64 or 128x32** pixels, I2C or SPI interface, High contrast, low power consumption, supports graphics ,Small screen size, but relatively higher cost than the LCD display. TFT - SPI interface, Supports full-color graphics, touchscreen option, High power usage, relatively higher cost than **OLED, LCD. LED** - Medium to high power usage, SPI interface and relatively similar, a little costlier than LCD. LCD - Uses liquid crystals to display characters in rows and columns, low power consumption, Parallel or I2C interface available, easy to use out of these LCD was the one which was most suitable for the Function generator in terms of cost, needed functionality of displaying characters and numbers , compatibility with the Arduino (**Atmega328p**) and easy to use in LCD there were 2 types available for interface/ connection. parallel and I2C - chose I2C as it is easy to use, connect, and reduces the analog pins required for the display 4 pins required for parallel connection(excluding ground and Vcc) , 2 pins required for I2C (excluding ground and Vcc) 20X4 i.e 20 characters X 4 lines was chosen to match and implement the displays as present in the function generator and thus reached the conclusion for LCD display with I2C interface and 20X4 and then tried programming and simulation for the LCd in WOKWI and TinkerCad using the **LiquidCrystalI2C** library and after learning all the required commands in the **LiquidCrystalI2C** library, coded for the display

4.9.2 Hardware Iterations

Laser Cutting

Last week, our focus was on designing the outer body of the function generator using acrylic sheets and a laser cutter. We finalized a structure consisting of five sides, leaving the top part removable for accessibility. To achieve this, we designed a single acrylic piece with a **central quadrilateral** surrounded by four adjacent sections. These sections will then be bent using a blow dryer and joined using chloroform (acrylic solvent) for a seamless finish.

For the front panel, we incorporated cutouts for the button, screen, and knob, along with engraved labels for clarity. To ensure easy removal of the top part when needed, we explored various mechanisms such as sliders and locks. After discussion, we decided on a **slit-and-wedge** friction-fit system, which would allow the top panel to stay securely in place while still being removable when necessary.

To validate our approach, we laser-cut a test piece to check the functionality of the slit mechanism, which worked as expected. Moving forward, we will proceed with cutting and assembling the complete outer body while implementing the finalized design.

Circuit Design

This week, our team improved our waveform generation approach. Initially, we were generating all waveforms directly through code executed on an Arduino. However, we realized that at higher frequencies, this method introduced errors. To address this, we

integrated the **AD9833**, a dedicated waveform generation IC capable of producing sine, triangular, and square waves with precision. By leveraging this IC, we successfully generated all required waveforms while ensuring accuracy across different frequencies. Additionally, we designed and implemented an offset and frequency control circuit, allowing fine-tuned adjustments to the output. This enhancement not only improved reliability but also provided greater flexibility in waveform control.

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- Word count: 19487
- Number of sentences: 5332
- Number of characters: 121512
- Readability Indices:
  - Readability Score(WebFx): 45.1
  - Flesch Reading Ease: 47.2
  - Flesch-Kincaid Grade Level: 8.5
  - Gunning Fog Index: 14.75
  - Coleman Liau Index: 12.97
- A WebFX readability score of **45.1** indicates that the document can easily be understood by **17 to 18 year olds**.
- **Flesch Reading Ease** score of **47.2** and **Flesch-Kincaid Grade level** of **8.5** indicates that the text is **slightly tougher to comprehend** and best understood by individuals with a **college level education**.
- A **Gunning Fog Index** of **14.75** suggests that the text requires a reading level equivalent to a **college student**.
- A **Coleman-Liau Index** score of **12.97** indicates that the text is written at a level appropriate for someone at a college freshman reading level.

B. Softwares Used

The software(s) we used to prepare this report are as follows:

1. **Latex** - which is a high-quality typesetting system, commonly used for producing scientific and technical documents. It can be downloaded from:
    - Project Website: `https://www.latex-project.org/get/`
2. **Zotero** - Which is a reference management software. Used to manage data and related research materials. It can be downloaded from:
    - Zotero Website: `https://www.zotero.org/download/`
3. **ProjectLibre** - Which is project management software system. It helps in planning, scheduling, and tracking projects. It can be downloaded from:
    - ProjectLibre Website: `https://www.projectlibre.com/`
4. **PlantUML** -Which is a open-source tool allowing users to create diagrams and mindmaps. It can be downloaded from:
    - PlantUML Website: `https://plantuml.com`
5. **TinkerCAD** - Which is a free online 3D modeling program. It can be downloaded from:
    - Tinkercad Website: `https://www.tinkercad.com/`
6. **Microsoft 365/Microsoft Office** - Which is a collection of applications like Microsoft World, Excel and more. It is commonly used for document editing.
    - Access Microsoft 365: `https://www.microsoft365.com/`
7. **FreeCADweb** - Which is an open-source parametric 3D modeler made primarily to design real-life objects. It can be downloaded from:
    - FreeCADweb Website: `https://www.FreeCADweb.org/`
8. **Arduino IDE 2.3.4** - Which is an open-source Integrated Development Environment (IDE) that allows users to write and upload code to Arduino boards. It can be downloaded from:
    - Arduino IDE Website: `https://www.arduino.cc/en/software`
9. **Python** - Which is a high-level, general-purpose programming language.It can be downloaded from:
    - Python Website: `https://www.arduino.cc/en/software`

10. **Simulide** - is a simple real time electronic circuit simulator, intended for hobbyist or students to learn and experiment with analog and digital electronic circuits and microcontrollers. It supports PIC, AVR , Arduino and other MCUs and MPUs.It can be downloaded from:

    - Simulide Website: `https://simulide.com/p/`

C. Document ID

- **Document type**: Major
- **Document authorized by**: Saiyam Jain (2022MT11962)
- **Publication date**: 30th January 2025
- **Version Number**: 3.1.1
- **Github Repo details**: `https://github.com/xfppm47/elp305_p1`

D. Minutes of the Meeting

D.1 Week 1 (10/01/25 - 23/01/25)

D.1.1 Market Research Subtribe

i. Meeting 1:

Date: 12th January 2025
Time: 4.00 PM
Location: Offline (Mech Lawn)
Attendees: All members of the team were present.
Agenda: Brainstorming ideas for new features to implement.
Discussion: The meeting started off with an introduction and getting to know each other's relevant work experiences to optimally assign work. After that we have decided to look for inspirations on the features that we can implement in our function generator.
Resolutions: We have identified a few features that make our function generator more attractive to the market.

- Implementation of an interface which runs on PC which can be used to save a few regularly used preset values and also to vary the parameters of the output wave.
- Making the device much more compact and implementing a power backup to make this device portable, handheld and help out in situations like power cut.
- Making the body using recycled plastic instead of acrylic to cut down costs and making this more eco-friendly

These suggestions were passed on to the concerned vertical and we proceeded to look deeper into the financial benefits if we implemented these features.
Work distribution:

- Cost analysis for internal circuit components- Kaneesha Jain and Sanya Sachan
- Cost analysis for external hardware components- Ayush Nayak and Satvik Prasad
- Market analysis to estimate best- and worst-case scenarios- Gauri Agarwal
- Repurposing possibilities to broaden the function generator's market reach- Pratyush Shrivastava and Siya Gupta
- Analysis of the stakeholder ecosystem and product's market potential- Ashmit Nangia and Aahna Jain
- Exploration of feasibility of recycled plastic as an alternative for acrylic- Rahul Athipatla and Tanya Jain

ii. Meeting 2:

Date: 15th January 2025
Time: 6:00 PM
Location: Offline (Mech Lawn)
Attendees: All members of the team were present.
Agenda: Updates on work done and researching the market
Discussion: After discussing with other verticals we have ruled out the first two suggestions but the third one seems viable so we proceeded with this one and we have started to compile the report by researching potential markets and the impact that our USP will create on the markets and the scale and means of production we will need if this thing actually goes into the market

D.1.2 Software Subtribe

i. Meeting 1:

Date: 14th January 2025
Time: 3.00 PM
Location: Offline (Vindhyachal Hostel CR)
Attendees: All members of the Software Team were present.
Agenda: The main agenda of the meeting was division of the subtribe into subgroups based on tasks that the software subtribe needs to undertake.
Discussion: We started off the meeting with gauging skillsets of everyone present in the subtribe and the relevance of those skills to the project at hand. While most of the people are well versed with high level programming, hardware programming is new to them. This then led to the conclusion that we should be spending the first week in skill development through research. We also decided to divide ourselves into subgroups to facilitate specialized research and skill development making it easier for everyone to contribute.

Resolutions:
Divided the team into 3 subgroups: Chip programming, Simulations, and Display programming as follows:

1. Chip programming-
    - Shrenik Sakala
    - Yaswant Galla
    - Suneel Masarapu
    - Yuvraj Singh
    - Arnav Tiwari
    - Lakshaya Jain
    - Siddharth Saini
    - Nobin K. Benny
    - Punit Meena
    - Sumit Sonowal
    - Niraj Agarwal
    - Niranjan Rajeev
    - Dhruv Chaurasiya
    - Praveen Lakhara
2. Simulations
    - Rijul Barot
3. Display programming
    - Abhinav Nimkar

- Priyansh Prakash
- Mukul Sahu
- Sarthak Gangwal
- Chintada Srinivasa Rao

We then decided to work in these subgroups and update about the progress through an online meet the next day.

ii. Meeting 2:

Date: 15th January 2025
Time: 9:00 PM
Location: Online (G-meet)
Attendees: All members of the Software Team were present.
Agenda: Updates on work done.
Discussion:

- Chip programming: Selected an optimum chip in terms of price, requirements and performance. Researched about chip programming and multiple mediums for the same to choose the most efficient method. Settled on Atmega328p chip and arduino programming. Also settled on making an Arduino from scratch using a crystal oscillator and PCB.

- Display programming: Researched on various possible displays and configurations. Selected optimum display based on compatibility, use case and price. Settled on LCD 20X4 display.

- Simulation: Assigned task to create a CAD model. Will simulate circuits once the specifications are ascertained by all verticals. Researched about various simulation software and learned to use the same.

D.1.3 Documentation subtribe

i. Meeting 1:

Date: 10th January 2025
Time: 9:30 PM
Location: Online (G-meet)
Attendees: All members of the Documentation Team were present.
Agenda: The main agenda of the meeting was to discuss and assign tasks for the detailed report for the function generator project. The detailed report should consist of the following sections/ tasks:

- Avoid any type of plagiarism
- Title
- Team Members and Entry Numbers, Email Designation
- Involvement Factor
- Table of Content
- List of Tables
- List of Figures
- List of Abbreviations
- Glossary
- Mind Map
- Project Management Software Outputs
- Abstract
- Motivation Section
- Requirements Section
- References
- Appendix: Document ID
- Appendix: Document Statistics
- Appendix: Readability Indices
- Proofreading
- Project Statement
- Software Used
- SPOC
- Tribe Name
- PDF File Format

Discussion:

The meeting began with a review of the detailed report structure and the identification of the required sections giving specific guidelines for each. .

Resolutions:

1. The team agreed to divide the work between members based on their expertise and availability.
2. The timeline for completing each section was agreed upon, with a follow-up meeting scheduled for 15th January 2025 at 9:50 PM to review the progress.
3. It was decided that everyone will upload their completed sections in a shared folder for review before the next meeting.

Action Items and Responsibilities:

1. **Sachin** - Plagiarism check, Proofreading
2. **Keshav** - Table of Contents, List of Tables, List of Figures
3. **Ojas** - Abstract
4. **Madhav** - Motivation section, Requirements section
5. **Shivaani** - References, Readability Indices
6. **Ishant** - Software used
7. **Kabir** - Mind Map, PDF file format
8. **Utkarsh** - Project Management software outputs (Network Chart / WBS / Gantt Chart / Resource Breakdown)
9. **Shivang** - Document ID and Document Statistics
10. **Om Goel** - Title, Team Members and Entry Numbers, Involvement Factor, List of Abbreviations, Glossary, Project Statement, SPOC, Tribe Name, and work on Minutes
11. **Nilay Sharma** - Overall coordination, compilation

The next meeting was set to be scheduled on 15th Jan, 9:50 PM.

ii. Meeting 2:

Date: 15th January 2025
Time: 9:30 PM
Location: Online(G-meet)
Attendees: All members of the Documentation Team were present
Agenda: The main agenda of the meeting was to review the progress of the various sections of the report for the function generator project, ensuring that tasks were on track and addressing any challenges.
Discussion: The meeting was held to check the progress of the report sections, and only small discussions were conducted regarding the various sections of the report. Each member gave an update on the work completed so far:
Resolutions: All members were asked to continue working on their respective sections and finalize them before the next review.
Action Items and Responsibilities: All team members are expected to complete their assigned sections as per the previous distribution and upload them to the shared folder

D.1.4 Hardware Subtribe

i. Meeting 1:

Date:11th January 2025
Time:9:00 PM
Location: Online G-Meet
Attendees: All Members of the Subtribe
Agenda: Agenda of the meeting was to divide the whole subtribe in smaller groups and distribute the task of gathering information and collecting information for designing the function generator and distribute the work accordingly for the week.
Discussion: First of all everyone shared their ideas on how we can proceed further and what data and information they have collected till now which can help us in designing the circuit.
Resolutions:

- Everyone shared their work load and other commitments in the upcoming week and we all analysed the respective strength and expertise of team members.
- The work was then divided to the members considering point 1 and subtribe was divided accordingly in different groups.
- It was decided that we'll be in touch through Whatsapp groups so that whenever another person requires help then anyone can answer him/her.
- After assigning the tasks to every individual, we decided to be in touch through whatsapp or call still, the strict deadline of 15th January 2025 9:00 PM was set to update on their findings and what is the idea they came up with.

Responsibilities given to every individual:
Understanding the requirements and working of the microchip:

- Adarsh Singh
- Abhishek Singh
- Tirth Punit Golwala
- Saiyam Jain
- Priyanshu Jindal
- Jenit Jain

Understand the power management of the system:

- Nagure Kalyani Paramanand
- Viha Singla
- Khushi Gupta
- Suhani Soni

- Syna Rajvanshi
- Tushar Goyal
- Vatsal Manish Sejpal
- Umang Agarwal

Worked on the outer body of the function generator

- Deevyansh Khadria
- Sushil Kumar
- Saksham Kumar Rohilla
- Ajaypal Kulhari
- Arpit Mourya
- Ambhore Soham Bhaskhar
- Lokendra Singh Gohil

Next meeting scheduled on 15th January 2025

ii. Meeting 2:

Date: 15th January 2025
Time: 9:00 PM
Location: Online G-Meet
Attendees: All Members of the Subtribe

Agenda: Agenda of the meeting was to collectively present our findings and ideas and discuss the final requirements that we'll need for the project and also deal with the problems that we faced.
Discussion: As we were continuously in touch throughout the week through whatsapp groups we had formed, there was not much to discuss. Everyone updated their work and we finalised our requirement list.
Resolutions: As the requirements were more or less finalised, everyone had decided to move ahead to gather further ideas and update the subtribe if they find anything.
Responsibilities given to every individual: Every team member was told to have a look at the design and circuit that we'll be building and read about the different functionalities of the items we are going to use and how we can be better.

D.2 Week 2 (17/01/25 - 23/01/25)

D.2.1 Market Research Subtribe

Date: 17th January 2025
Time: 2.30 PM
Location: Offline (Lab)
Attendees: All members of the team were present either online or offline.
Agenda: Optimising costs and allocating work to everyone.
Discussion:
The meeting started off with an introduction and getting to know each other's relevant work experiences to optimally assign work. We have realised that the costs are expected to reach above the prescribed Rs.1000/- budget so we wanted to find ways to cut our costs.
Resolutions: We have identified a few avenues to cut costs.

- Using ATMEGA328P chip instead of ATMEGA328P board cuts the costs by approx 100 rs
- We have found cheaper alternatives in a few other items like rotary switches etc.

We made a detailed budget plan for this project by including all the updated requirements from the software and the hardware team.
Meanwhile, a section of the team is working on the feasibility of implementing new features like implementing battery operation for the function generator etc.

D.2.2 Software Subtribe

Date: 17th January 2025
Time: 2.30 PM
Location: Embedded lab
Attendees: All members of the software team were present.
Agenda: The main agenda of the meeting was to distribute tasks among the members of the subtribe and then keep track of work done on the WhatsApp group, which will be discussed in the next lab.
Discussion:
We studied the function generator and its functionalities. The display programming subgroup was tasked with choosing an optimum display for our application purposes, and the documentation included their findings and conclusions. The simulation subgroup will have work when fabrication and circuit design begin. This week, they were tasked with deciding and researching the software specifications. The chip programming subgroup members were divided into pairs and tasked with implementing and simulating the five waveforms generated by the model function generator.
Resolutions: Divided the Chip programming subgroup into pairs as follows:

- Square: Punit, Nobin
- Triangle: Sumit, Lakshaya Jain
- Sine: Praveen, Dhruv Ch.
- Ramp: Manas, Yaswant
- Pulse: Chintada Srinivasa Rao, Suneel
- TTL: Shrenik, Arnav

Reshuffled subgroup members based on requirements:

1. Simulations- Rijul Barot, Niranjan Rajeev, Niraj Agarwal, Siddharth Saini
2. Display Programming- Abhinav Nimkar, Priyansh Prakash, Mukul Sahu, Sarthak Gangwal, Chintada Srinivasa Rao, Devansh Upadhyay

D.2.3 Documentation Subtribe

i. Meeting 1:

Date: 17th January 2025
Time: 9:30 PM
Location: Online (G-meet)
Attendees: The following members were present:

- Sachin Hiren Trivedi
- Shivang Goyal
- Shivaani Hari
- Nilay Sharma
- Utkarsh Dubey
- Keshav Rai
- Kabir Uberoi
- Madhav Biyani
- Om Goel
- Pratyush Sharma
- Ojas Sharma
- Ishant Yadav

Agenda: The main agenda of the meeting was to discuss and assign tasks for the detailed report for the function generator project. The detailed report should consist of the following sections/tasks:

- Avoid any type of plagiarism.
- Title.
- Team Members and Entry Numbers, Email Designation.
- Involvement Factor.
- Table of Content.
- List of Tables.
- List of Figures.
- List of Abbreviations.
- Glossary.
- Mind Map.

- Project Management Software Outputs.
- Abstract.
- Motivation Section.
- Requirements Section.
- Specification Section.
- References.
- Appendix: Document ID.
- Appendix: Document Statistics.
- Appendix: Readability Indices.
- Definitions of Readability Indices.
- Proofreading.
- Project Statement.
- Software Used.
- SPOC.
- Tribe Name.
- PDF File Format.
- Review remarks made by Prof. and make sure to incorporate them in upcoming reports.

Discussion: The meeting began with a review of the detailed report structure and the identification of the required sections, giving specific guidelines for each. Roles and responsibilities were discussed, tasks were assigned, and remarks made by the supervisor were reviewed to ensure alignment with expectations.

Resolutions: The team agreed to divide the work among the members based on their expertise and availability. The timeline for completing each section was agreed upon, with a follow-up meeting scheduled for 22th January 2025 at 9:50 PM to review the progress. All members will upload their completed sections to a shared folder for review before the next meeting.

Action Items and Responsibilities:

- Om Goel: MOMs and General Formatting
- Kabir and Utkarsh: General Formatting, Mind Map, ProjectLibre.
- Keshav: Requirements.
- Madhav, Ojas and Sachin: Specifications.

- Ishant: Software Used.
- Shivaani: References and Review
- Nilay: Glossary ,Abbreviations and Review
- Shivang: Document Statistics, Document ID, Readability, Definitions of Readability Indices.
- Sachin: Plagiarism Check, Proofreading.
- Pratyush Sharma-Ensure that all remarks made by the prof were incorporated and general formatting

The next meeting was set to be scheduled on 22th Jan, 9:30PM.

ii. Meeting 2:

Date: 22th January 2025
Time: 9:30 PM
Location: Online (G-meet)
Attendees: The following members were present:

- Sachin Hiren Trivedi
- Shivang Goyal
- Shivaani Hari
- Nilay Sharma
- Utkarsh Dubey
- Keshav Rai
- Kabir Uberoi
- Madhav Biyani
- Om Goel
- Pratyush Sharma
- Ojas Sharma
- Ishant Yadav

Agenda: The main agenda of the meeting was to review the progress of the various sections of the report for the function generator project, ensuring that tasks were on track and addressing any challenges.
Discussion: The meeting was held to check the progress of the report sections, and only small discussions were conducted regarding the various sections of the report. Each member gave an update on the work completed so far.
Resolutions: All members were asked to continue working on their respective sections and finalize them before the next review (if needed).
Action Items and Responsibilities: All team members are expected to complete their assigned sections as per the previous distribution.

D.2.4 Hardware Subtribe

i. Meeting 1:

Date: 18th January 2025
Time: 1:00 PM
Location: Biotech Lawns
Attendees: All Members of the Subtribe
Agenda: To divide the whole subtribe in two groups and distribute the task of gathering information and collecting information for specifications of the product to one group and try to learn laser cutting software to another

Discussion: First of all, everyone shared their ideas on how we can proceed further and what data and information they have collected till now which can help us in designing the circuit.
Resolutions: Everyone shared their work load and other commitments in the upcoming week and we all analysed the respective strength and expertise of team members. The work was then divided to the members considering point 1 and subtribe was divided according to their background. It was decided that we'll be in touch through Whatsapp groups so that whenever another person requires help then anyone can answer him/her. After assigning the tasks to every individual, we decided to be in touch through whatsapp or call still, the strict deadline of 19th January 2025 9:00 PM was set to update on their findings and what is the idea they came up with.

Responsibilities given to every individual:
Understanding the laser cutting software and try to come up with a very rough model for the generator:

- Adarsh Singh
- Abhishek Singh
- Tirth Punit Golwala
- Saiyam Jain
- Vatsal Sejpal
- Kalyani Nagure Paramachand
- Viha Singla

Understand the working on how to implement different waves:

- Sushil Kumar
- Umang Agarwal
- Divyansh Khadria
- Tushar Goyal
- Saksham Kumar Rohilla

- Ajaypal Kulhari
- Arpit Mourya
- Ambhore Soham Bhaskar
- Lokendra Singh Gohil
- Saiyam Jain

Next meeting scheduled for 22nd January 2025

ii. Meeting 2:

Date: 22nd January 2025
Time: 1:00 PM
Location: Biotech Lawns
Attendees: All Members of the Subtribe

Agenda: Agenda of the meeting was to collectively present our findings and ideas and discuss the final requirements that we'll need for the project and also deal with the problems that we faced.

Discussion: As we were continuously in touch throughout the week through whatsapp groups we had formed, there was not much to discuss. Everyone updated their work and we finalised our requirement list.

Resolutions: As the requirements were more or less finalised, everyone had decided to move ahead to gather further ideas and update the subtribe if they find anything.
Responsibilities given to every individual: Every team member was told to have a look at the design and circuit that we'll be building and read about the different functionalities of the items we are going to use that how we can be better.

D.3 Week 3 (24/01/25 - 30/01/25)

D.3.1 Market Research Subtribe

Date: 25th January 2025
Time: 8:30 PM
Location: Online (Gmeet)
Attendees:

- Rahul Athipatla
- Siya Gupta
- Kaneesha Jain
- Aahna Jain
- Tanya Jain
- Pratyush Shrivastava
- Sanya Sachan
- Satvik Prasad
- Ayush Nayak
- Ashmit Nangia
- Gauri Agarwal

Agenda:

- Analysis of jitter and RC filter effects on stakeholders (ELP101 students).
- Strategies for making the device compact and identifying cost-effective materials for hardware design.

Discussion: Since achieving high functionality at a lower cost was a priority, we analyzed how different design choices influenced performance. One key area of focus was the waveform generation, where we explored how small step approximations impact experiments. While high-precision signals are ideal, we found that for ELP101 students, the existing design effectively supports experiments like frequency response analysis, AM signal generation, and oscillator phase shift testing, ensuring clear conceptual understanding.
We also examined the components used in conventional function generators and explored cost-effective alternatives. The analysis showed that with careful selection, performance remains strong while making the device more accessible. Simple optimizations, such as filtering or fine-tuning step resolution, further enhance output quality. This approach successfully balances affordability with functionality, ensuring a reliable and efficient learning tool.

Resolution: Team members were allotted works based on their experience with certain fields. They were divided into Quality Assurance for Stakeholders, Cost Analysis respectively whereas one person would still be on the lookout for any new features that we can implement. These people are again allotted different subtribes to communicate with them and finalise requirements. Communication shall be maintained via WhatsApp groups and team members will be provided assistance as needed.

D.3.2 Software Subtribe

Date: 24th January 2025
Time: 2.30 PM
Location: Embedded Lab
Attendees: All members of the Software Team were present.

Agenda: The main agenda of the meeting was to take updates on the assigned task from the members of the subtribe and discuss possible improvements implementing them during the lab. Decided deadlines for tasks that were required more time.
Discussion: The display programming subgroup produced their findings and first draft of the functions coded for display. A subgroup was formulated for buttons interface programming and simulation. The chip programming sub group produced their codes for the assigned waveforms and we discussed the pros and cons and possible improvements.

Resolutions:
The Chip programming subgroup produced codes for waveforms as follows:

- Square: Punit, Nobin
- Triangle: Sumit, Lakshaya Jain
- Sine: Praveen, Dhruv Chaurasiya
- Ramp: Manas, Yaswant
- Pulse: Chintada Srinivasa Rao, Suneel
- TTL: Shrenik, Arnav

Further task assignment was done as follows-

1. Buttons interface programming- Rijul Barot, Niranjan Rajeev, Niraj Agarwal, Siddharth Saini
2. Display Programming- Abhinav Nimkar, Priyansh Prakash, Mukul Sahu, Sarthak Gangwal, Chintada Srinivasa Rao, Devansh Upadhyay

The display programming team shared their findings so far, and discussed further work allotment and deadlines.

D.3.3 Documentation Subtribe

i. Meeting 1:

Date: 24th January 2025
Time: 9:30 PM
Location: Online(G-meet)
Attendees: The following members were present:

- Sachin Hiren Trivedi
- Shivang Goyal
- Shivaani Hari
- Nilay Sharma
- Utkarsh Dubey
- Keshav Rai
- Kabir Uberoi
- Madhav Biyani
- Om Goel
- Pratyush Sharma
- Ojas Sharma
- Ishant Yadav
- Shashwat Kasliwal
- Yuvraj Singh

Agenda: A detailed report should include the following, ensuring avoidance of any type of plagiarism:

- Title.
- Team Members and Entry Numbers, Email Designation.
- Involvement Factor.
- Table of Content.
- List of Tables.
- List of Figures.
- List of Abbreviations.
- Glossary.
- Mind Map.

- Project Management Software Outputs.
- Abstract.
- Motivation Section.
- Requirements Section.
- Specification Section.
- References.
- Appendix: Document ID.
- Appendix: Document Statistics.
- Appendix: Readability Indices.
- Definitions of Readability Indices.
- Proofreading.
- Project Statement.
- Software Used.
- SPOC.
- Tribe Name.
- PDF File Format.
- Review remarks made by Prof. and make sure to incorporate them in upcoming reports.
- Minutes of Meeting
- Correcting Specifications
- Working Flowchart
- Remove Unwanted Citations
- Arduino Code
- Project Libre
- CAD Models, Frequency and Amplitude
- Working in Model
- Stages of Working (DEMO Design + Industrial Model)
- Role of Parts of Model
- Software Used, Change/Remove Previously Plagiarized Text

- Types of Waves and Their Implementation

Discussion Points: The meeting began with a review of the detailed report structure and the identification of the required sections, giving specific guidelines for each. Roles and responsibilities were discussed, tasks were assigned, and remarks made by the supervisor were reviewed to ensure alignment with expectations.
Resolutions: The team agreed to divide the work among the members based on their expertise and availability. The timeline for completing each section was agreed upon, with a follow-up meeting scheduled for 28 January 2025 at 9:30 PM to review the progress. All members will upload their completed sections to a shared folder for review before the next meeting.
Action Items and Responsibilities:

- Kabir: Responsible for creating the mind map, correcting specifications, and working on the flowchart.
- Nilay Sharma:Responsible for reviewing and coordinating whole work
- Om: Tasked with preparing the Minutes of Meeting (MoM) and General Formatting
- Shivang: Will remove unwanted citations, check document statistics, and improve readability.
- Yuvraj: Responsible for writing and testing the Arduino code.
- Utkarsh: Handling project scheduling using Project Libre.
- Shivaani: In charge of compiling references for the document.
- Pratyush: Will work on the glossary and abbreviations section.
- Sachin: Managing CAD models and ensuring correct frequency and amplitude functioning in the model.
- Madhav and Ojas: Working on different stages of the project, including the DEMO design and industrial model.
- Keshav: Explaining the role of different parts of the model.
- Ishant: Listing and discussing the software used and modifying/removing any previously plagiarized content.
- Shashwat: Researching and documenting the types of waves and their implementation in the project.

Next Steps: Each team member is to complete their assigned tasks by 28 January,2025. Regular follow-ups to ensure smooth progress. Any challenges or roadblocks to be communicated to the team lead for resolution.
The next meeting was set to be scheduled on 28th Jan, 9:30PM.

ii. Meeting 2:

Date: 28th January 2025
Time: 9:30 PM
Location: Online(G-meet)
Attendees: The following members were present:

- Sachin Hiren Trivedi
- Shivang Goyal
- Shivaani Hari
- Nilay Sharma
- Utkarsh Dubey
- Keshav Rai
- Kabir Uberoi
- Madhav Biyani
- Om Goel
- Pratyush Sharma
- Ojas Sharma
- Ishant Yadav
- Shashwat Kasliwal
- Yuvraj Singh

Agenda: The main agenda of the meeting was to review the progress of the various sections of the report for the function generator project, ensuring that tasks were on track and addressing any challenges.
Discussion: The meeting was held to check the progress of the report sections, and discussions were conducted regarding the various sections of the report. Each member gave an update on the work completed so far.
Resolutions: All members were asked to continue working on their respective sections and finalize them before the next review(if needed).
Action Items and Responsibilities: All team members are expected to complete their assigned sections as per the previous distribution.

D.3.4 Hardware Subtribe

Date: 25th January 2025
Time: 1:00 PM
Location: LH313.3
Attendees: All Members of the Subtribe
Agenda: The purpose of the meeting was to divide the subtribe into two groups: one responsible for gathering and compiling product specifications, and the other focused on learning laser cutting software.
Discussion: The meeting began with everyone sharing their ideas on how to move forward and presenting the data and information they had collected so far, which could assist in designing the circuit.
Resolutions: Team members discussed their workload and upcoming commitments, allowing for an assessment of individual strengths and expertise. Based on these considerations, tasks were allocated accordingly, and the subtribe was divided based on relevant backgrounds.It was agreed that communication would be maintained via WhatsApp groups, enabling team members to seek and provide assistance as needed. After assigning tasks, it was reaffirmed that members could stay connected via WhatsApp or calls. A strict deadline of January 5, 2025, at 9:00 PM was set for everyone to update their progress and share their ideas.

Responsibilities given to every individual:
Understanding the laser cutting software and try to come up with a very rough model for the generator

- Adarsh Singh
- Abhishek Singh
- Tirth Punit Golwala
- Saiyam Jain
- Vatsal Sejpal
- Kalyani Nagure Paramachand
- Viha Singla

Understand the working on how to implement different waves

- Sushil Kumar
- Umang Agarwal
- Divyansh Khadria
- Tushar Goyal
- Saksham Kumar Rohilla
- Ajaypal Kulhari
- Arpit Mourya

- Ambhore Soham Bhaskar
- Lokendra Singh Gohil
- Saiyam Jain