An Adjustable Hybrid SC-BP Polar Decoder

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***Abstract*—Polar codes have drawn lots of attentions for the capacity-achieving property and low encoding/decoding complexity. As two promising decoding algorithms, successive cancellation (SC) decoding shows better performance but limited by high latency. Otherwise, belief Propagation (BP) algorithm presents high throughput yet with performance degradation. In this paper, a hybrid decoding architecture combining SC and BP decoding is proposed, which could process both algorithms in unified module within one decoding step. The simulation result reflects a trade-off between decoding latency and performance with different decomposition levels. In terms of hardware implementation, the adjustable architecture is implemented based on systolic BP decoder and look-ahead SC decoder. The hybrid decoder offers the flexibility and generality which could apply on different conditions.**

***Index Terms*—polar codes, successive cancellation (SC) decoding, belief propagation (BP) decoding, hybrid architecture**

I. Introduction

Polar codes, proposed by Arıkan in [1] have drawn attentions of information theory and can reach the symmetric channel capacity of binary-input discrete memoryless channels (B-DMCs). Among varieties of decoding algorithm, successive cancellation (SC) decoding algorithm [1] utilizes the property of polarization and has $\mathcal{O}(N \log N)$ complexity. Another algorithm is belief propagation (BP) decoding algorithm [2], which could be implemented in parallel and achieve high throughput. In term of hardware implementation, SC decoder shows better decoding performance whereas suffering from low throughput and high decoding latency due to the serial decoding strategy. Approaches to tackle the problems are described in [3–6]. [3] improves the throughout and maximize the hardware utilization using overlapping technique. In [4], the latency of SC decoding is decreased by computing the propagating log likelihood ratio (LLR) in advance. However, the optimized SC decoders above are still much slower than pipelined BP decoder proposed in [2], especially when code length is large. For BP decoder, [7, 8] exploit several hardware architectures with transformation techniques and reduces hardware complexities. Besides, a low-latency BP decoder which employs early stopping detection within the maximum iteration number is proposed in [9].

It should be noted that the latency of SC decoder is mainly contributed by serial property. To overcome this issue, a novel hybrid scheme was proposed to decrease the serial stages. [10] replaces a part of stages with parallel maximum likelihood (ML) decoding and decreases the conventional SC decoder latency by 82.25%. Illuminated by this idea, we propose an architecture which combines conventional SC and BP decoder, utilizing the parallelization of BP decoding to decrease decoding latency of polar codes.

Different from another SC-BP hybrid decoding architecture [11], which uses SC decoding to process the failed frames after BP decoding, our architecture is the mixture of two algorithms in single decoding step. In term of hardware implementation, [11] also gives a unified processing unit (PU) which can either acts as SC decoder or BP decoder. However, considering the difference of decoding flow, we present an optimized merged architecture, which is adaptive to any stage classification. This flexibility enables us to achieve different levels of performance by configure the portion of SC/BP part of the hybrid decoder. FPGA implementations results have shown similar hardware cost as the existing design. Additionally, this work mainly focuses on the flexibility of the hybrid algorithm and decoding architecture. Therefore, only original designs of SC and BP decoding scheme are considered as benchmarks in hardware cost.

The remainder of this paper is organized as follows. Section II briefly reviews the preliminaries of polar decoding. In Section III, the proposed hybrid decoding algorithm combining SC and BP is illustrated in detail. Moreover, its corresponding hardware architecture is given in Section IV. Hardware performance of proposed hybrid decoding architecture is compared with conventional SC and BP decoders, respectively. Finally, Section V concludes the entire paper.

II. Polar Codes

A. Decomposition of Polar Encoding and Decoding

According to channel polarization and [10], the recursive pattern of polar encoding could be represented as follows,

$$\begin{cases} x_{1,o}^{N} = (u_1^{N/2}\mathbf{B}_{N/2}\mathbf{F}^{\otimes(n-1)}) \oplus (u_{N/2+1}^{N}\mathbf{B}_{N/2}\mathbf{F}^{\otimes(n-1)}), \\ x_{1,e}^{N} = u_{N/2+1}^{N}\mathbf{B}_{N/2}\mathbf{F}^{\otimes(n-1)}, \end{cases} \tag{1}$$

where $x_{1,o}^{N}$ and $x_{1,e}^{N}$ denote the odd elements and even elements among $\{x_1, x_2, \cdots, x_N\}$, $\mathbf{B}$ represents the bit-permutation matrix and $\mathbf{F}^{\otimes n}$ is the *Kronecker power* of n with $\mathbf{F} = \left[\begin{smallmatrix} 1 & 0 \\ 1 & 1 \end{smallmatrix}\right]$, $n = \log_2 N$. Therefore, a polar encoder with N-length is composed of a pair of $N/2$-length encoders and an attached stage. The attached stage implements XOR and PASS

operation on $v_i^{(1)}$ and $v_i^{(2)}$ to get u_i and $u_{N/2+i}$, respectively. Note that the output set of the two encoders are $\{v_i^{(1)}\}$ and $\{v_i^{(2)}\}$, $i = 1, 2, \cdots, N/2$, whose combination is called the outer codes at the 1st decomposition level according to [10]. Correspondingly, the codes being processed in the attached stage are named as inner codes, which are processed by $N/2$ paralleled 2-bit polar encoders. In a more general case, when the original polar encoder is decomposed at k-th level, the outer polar encoder consists of 2^{n-k} separate polar encoders and produces 2^k blocks of outer codes. The combination of i-th output of 2^k outer code encoders $\{v_i^{(1)}, v_i^{(2)}, \cdots, v_i^{(2^k)}\}$ turns out as the input of i-th inner code encoders.

B. Decomposition of Polar Decoding

Correspondingly, SC decoder can also be viewed by the inner and outer code pattern, which is illustrated in Fig. 1. Different from polar encoding process, decomposed SC decoder starts with channel likelihood ratios (LRs) of 2^{n-k} blocks of inner codes with 2^k-length block and gets LRs of the first block in outer codes. During the decoding process, After the j-th block of estimated results $u_{(j-1)2^{n-k}+1}^{j2^{n-k}}$ is derived, the outer code decoder feeds the i-th inner code decoder with the encoded estimated bits $\hat{v}_i^{(j)}$, and the inner code decoder produces LRs for next block of outer codes. The whole SC decoding process finishes after outer code decoder is invoked by 2^k times.

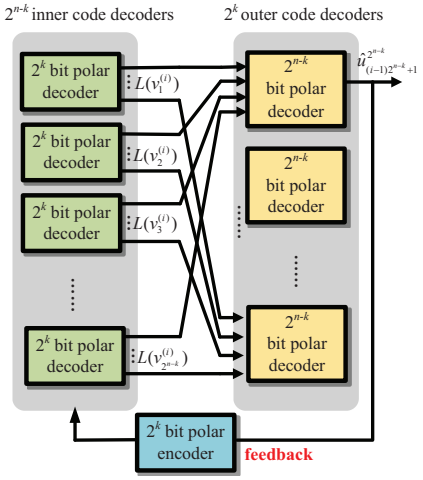

Fig. 1. SC decoder at the k-th decomposition level.

The decomposability of SC decoder allows part of the decoding stages be substituted by other polar decoding schemes. In this paper, we substitute the outer code decoder by 2^{n-k}-length BP decoder to reduce decoding latency and improve throughput. Owing to the similarity between the equations and FFT-like architectures of SC and BP decoder, the two algorithms can be implemented via the same set of hardware architecture [11]. The substitution of BP decoding in hybrid decoding helps increasing the flexibility of hardware architecture, which will be introduced concretely in Section IV.

III. Proposed Hybrid Decoding Approach

In this section, the proposed hybrid decoding algorithm is introduced, and the error-correction performance comparing with traditional SC and BP decoding algorithm is also given. According to Section II, it can be implemented by substitution of outer codes with 2^k BP decoders.

A. SC-BP Hybrid Decoding Algorithm

According to the decomposition technique mentioned in [10], Fig. 2 views the algorithm from a binary tree manner. For each SC-node of the tree that operates as part of inner decoder, it produces LLRs for left child based on input LLRs α_v. Attached on the leaf nodes in the binary tree are BP decoders, which returns the estimated 2^{n-k}-length feedback to inner codes. SC-node is invoked again when the estimated results are passed from left child and calculates α_r for right child. Feedback from both children are combined together as β_v and passed to parent node. At last, the output of the hybrid decoder is obtained by encoding the β_v of the father code.

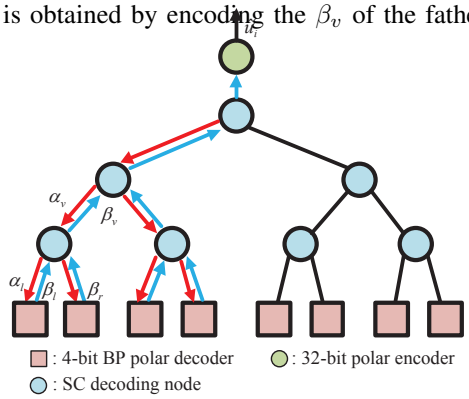

Fig. 2. Decoding process of SC-BP hybrid decoding algorithm for $N = 32$ polar code at decomposition level 2.

The latency of the decoding process is analyzed as follows: Notice that the decoding latency of a 2^{n-k}-bit systolic BP decoder with constant iteration number itr is $2(itr-1)+(n-k)$ clock cycles [7], the total clock cycles that the decoder spends on BP decoding is $2^{k+1}(itr-1)+2^k(n-k)$. Comparing with 2^k sequentially invoked look-ahead SC outer decoder for length 2^{n-k}, which requires at least $N-2^k$ clock cycles by implementing pre-computation scheme launched in [3]. With the help of previous analysis, the hybrid decoding latency should be written in the equation as below,

$$\begin{aligned} T_{hybird} &= T_{\mathrm{SC}} + T_{\mathrm{BP}} \\ &= 2^k - 1 + 2^{k+1}(itr-1) + 2^k(n-k) \\ &(0 < k < n). \end{aligned} \tag{2}$$

The hybrid decoder saves extra clock cycles in outer decoding process comparing to SC decoder at long outer code length. For instance, to decode a polar code with $N = 2048, itr = 15, k = 5$, look-ahead SC decoder requires 2047 clock cycles, while hybrid decoder costs only 988 clock cycles. Hybrid decoding costs less time than half of SC decoding.

Fig. 3 shows the simulation results of the algorithm above, when k is small, the hybrid decoder is mainly composed of SC algorithm, and the simulation performance is more

close to that of SC decoder. On the other hand, increasing k degrades performance that close to BP decoder's. Therefore, the adjustment of k offers trade-off between latency and performance.

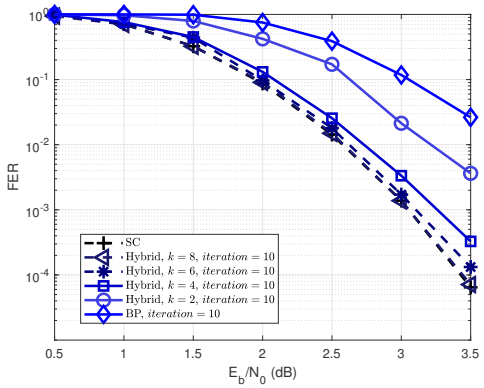

Fig. 3. BER performance of a $(1024, 512)$ polar code.

IV. Hardware Architecture of Hybrid Decoder

In this section, an adjustable architecture of hybrid decoder is proposed. The architecture implements the unified unit introduced in [11] in order to reuse a single architecture for both algorithms, and the pre-computation technique in [4] is also employed to reduce the decoding latency of SC part. The corresponding feedback circuit is also designed for implementing different decomposition level k on a single architecture.

A. Implementation of SC-BP Combined Nodes

According to [2], the computing unit of BP decoder consists of two kinds of operation: $g(\cdot)$ function and addition. Hence, it can be converted to SC decoder by operating few modifications on traditional BP computing unit.

Notice that the two LLR calculation equations in SC decoding each consists of one of the operations mentioned above, we can achieve the function of SC computing unit by disabling one of the operation in BP computing unit. Due to the symmetry of computing $L_{i,j}^t$ and $R_{i,j}^t$, two equations are listed as the examples. Eq. (3) illustrates the transformation from BP computing unit to SC computing unit.

$$\begin{cases} L_{i,j}^t = g(L_{i,j+1}^{t-1}, L_{i+N/2^j,j+1}^{t-1} + 0), \\ L_{i+N/2^j,j}^t = L_{i+N/2^j,j+1}^{t-1} + g(L_{i,j+1}^{t-1}, (1-2\hat{u}) \times (+\inf)). \end{cases} \tag{3}$$

Owing to the property mentioned above, the hardware architecture of corresponding implementation is shown in Fig. 4 and Fig. 5. In hardware implementation of unified computation unit, the modules **ABS** and **CMP** make up circuit to compute function $g(\cdot)$. In Fig. 5, $+\inf$ is denoted by the largest binary number to pass a directly into addition operation when whole circuit acts as SC decoding unit. C is the signal which switches SC and BP computing. When $C = 0$, the unified node converts to computing node in SC decoder. Otherwise, it executes the BP updating function.

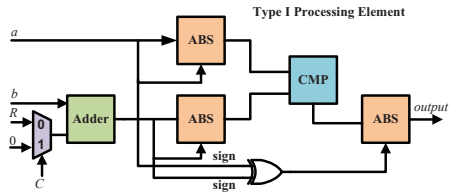

Fig. 4. Type I unified computing unit.

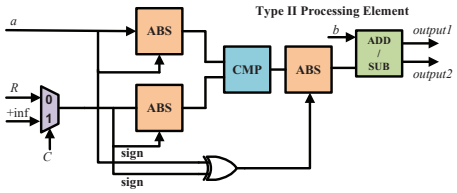

Fig. 5. Type II unified computing unit.

B. Architecture of Mainframe and Feedback Part

In this subsection, a generalized hardware architecture is proposed, this hardware architecture can receive decomposition level k as input to adjust the proportion of BP decoder in hybrid algorithm. Fig. 6. shows the overall architecture and processing pattern for an 8-bit hybrid decoder when $k = 1$.

When implementing BP decoding algorithm under a systolic architecture [7], at least $N \log_2 N/2$ PEs are used in order to satisfy the hardware consumption. In the case, k equals to 0, which is viewed as BP decoder. Notice that both BP and SC decoders have FFT-like architecture [3], so the connection between PEs requires no adjustment when decomposition parameter k switches from SC decoding mode to BP decoding mode. Moreover, for each unified unit, a MUX is required for selecting the $\mathbb{L}_N^{(2i)}(y_1^N, \hat{u}_1^{2i-1})$ that computed in advance, when corresponding stage is processing SC decoding algorithm.

Based on the feedback part of SC decoder proposed in [3], the feedback circuit of hybrid decoder is a pipelined FFT-like

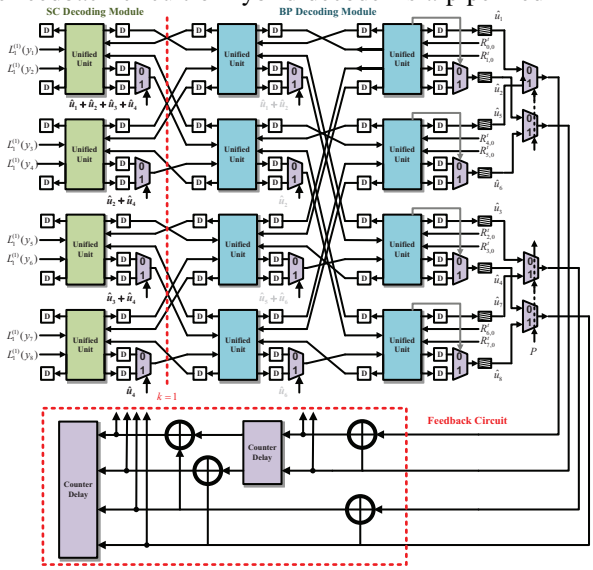

Fig. 6. Architecture of 8-bit hybrid decoder.

TABLE I
COMPARISON FOR DIFFERENT POLAR DECODERS.

Algorithm	**Pre-computation SC** [4]	**Line SC** [12]	**Systolic BP** [9]	**Hybrid Decomposition Level** k
# of PEs	$N-1$	$N/2$	$N\log_2 N/2$	$N\log_2 N/2$
Decoding Latency	$N-1$	$2(N-1)$	$2itr-2+\log_2 N$	$2^{k+1}(itr-1)+2^k(n-k)+2^k-1$
Decoding Throughput (Normalized)	2	1	$\log_2 N$	$\log_2 N-k$
Hardware comparison for $N=32$ polar code*				
# of REGs	770	150	——	2,608
# of GATEs	4,350	2,380	——	80,688
Hardware comparison for $N=1024$ polar code*				
# of REGs	24,640	150	——	83,456
# of GATEs	139,200	76,160	2,892,263	2,581,376

* 8-bit quantization is considered here.

polar encoder with $N/2$-length to meet the requirement of $k=1$. At the m-th stage of feedback circuit, the estimated outer codes with 2^m-block length require $T_{m,k}$ clock cycles of delay to wait the reception of another block of outer codes. We can verify $T_{m,k}$ to control the delay of each register with the help of counter in it. When $m \le k$, which means encoded estimated results have to wait for another block of inner codes to come, $T_{m,k}$ is defined as follows,

$$T_{m,k} = 2^{k-m} - 1 + (k-m+1)T_{\mathrm{BP}}, \quad m \le k. \tag{4}$$

Otherwise, $T_{m,k}$ equals to zero because the block length is enough for continuing encoding operation.

C. Hardware Performance Analysis

Table I compares the proposed hybrid architecture with other polar decoder architectures, including SC and BP architectures. The hybrid decoder is simulated on Xilinx XA3S1500 FPGA by ISE Design Suite. From the table, the following analyses can be derived:

1) The latency of hybrid decoder is far less than SC decoder. However, it suffers high hardware consumption.
2) The hardware utilization is nearly the same as BP decoder, since it should consider the condition of $k=n$. Compared with BP decoder, the performance is improved and latency increases.
3) The hybrid decoder offers more flexibility by adjusting the value of k. It could accommodate various scenarios with different requirements in real-life communication.

V. CONCLUSION

In this paper, a hybrid decoding scheme of polar code is proposed. The simulation results indicates that by combining SC and BP decoding process at different levels, the hybrid decoding algorithm allows us to reach a trade-off between better decoding performance and higher throughput. Additionally, the corresponding architecture of hybrid decoder that works under $0 \le k \le n$ is proposed.

ACKNOWLEDGEMENT

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