MCIMX6UL-BB

Schematics DevBoard

Table of Content

Revision History

Rev. Code	Date	By		Description
A	2015-02-28	Javen	1	Revision A released
B	2015-07-07	Javen	1	DNP R1023 DNP R1435, R1404, Add R1436 DNP R1517,Install R1520 Change Camera J1801 connector Change JTAG J1902 footprint Change SODIMM J2101 footprint Change R2101 from PU to PD Change J1901 PIN sequence
C	2015-07-14	Javen	1	Add R919-R946,L903-L905 DNP R1436,Install R1404,R1435 Change HP_MIC1N to LINPUT1 Add BT_DISABLE,ECSPI4_SS0,ECSPI4_MOSI,ECSPI4_SCLK for BT Add R2107~R2116 to reduce the VSNVS power consumption due to the TAMPER reason Add L903~L930 as FCC/CE backup Change Camera J1801 connector direction on layout Add C905 Change J1701 from TOP contact to BOT contact for BT

1. Unless Otherwise Specified:

   All resistors are in ohms, 10%, 1/8 Watt,0603
   All capacitors are in uF, 20%, 50V,0603
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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Drawn by: DRAWN_BY	Page Title: Title and Rev History		
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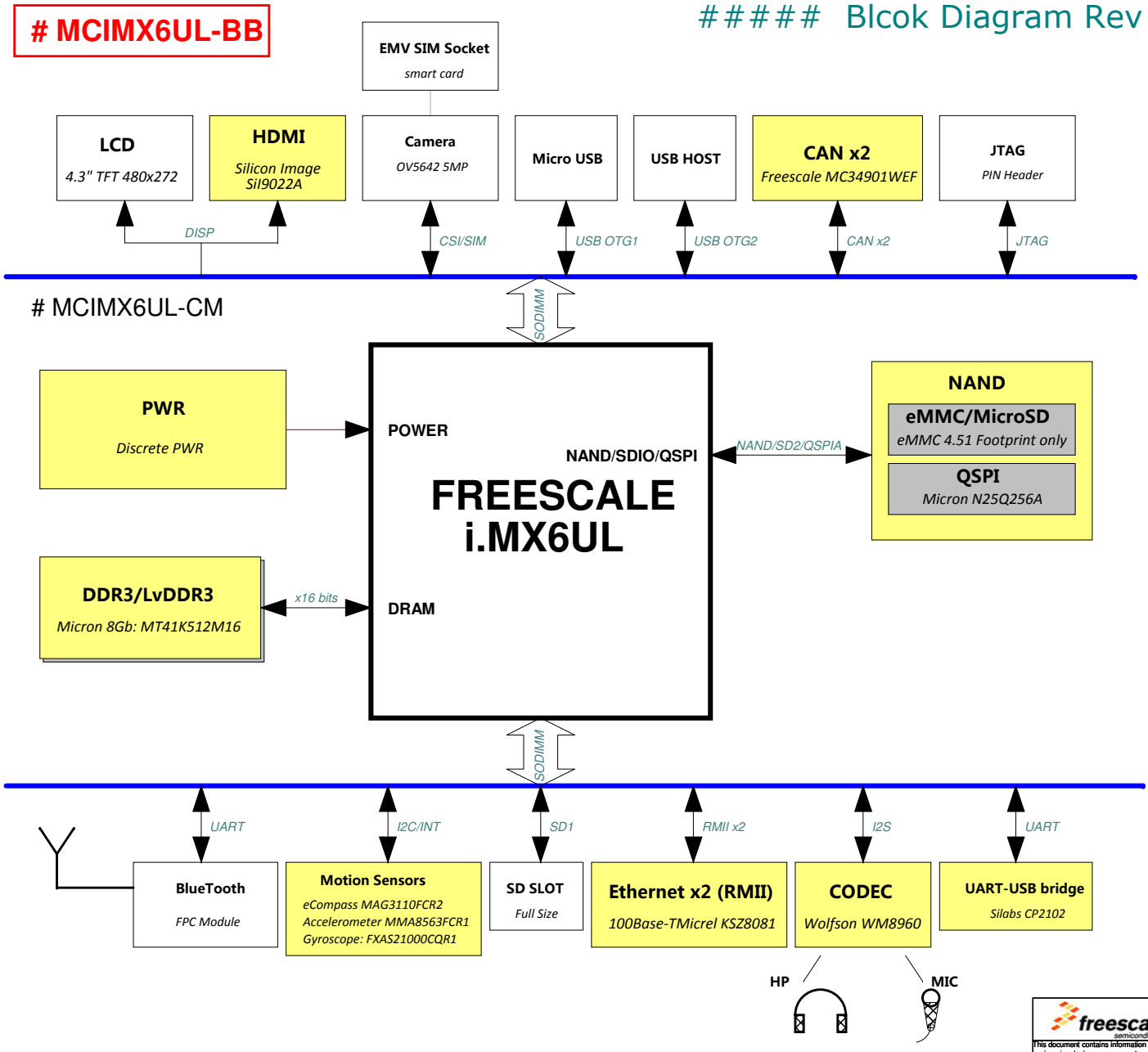
i.MX6UL EVK Block Diagram

Blcok Diagram Rev 1.0

MPN: MCIMX6UL-BB Agile No: 28616
MPN: MCIMX6UL-CM Agile No: 28617



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i.MX6UL EVK PWR TREE

WALL Adapter: 5V/3A

OVP

VSYS
5V/3A

MCIMX6UL-BB

Always ON
LDO
RICHTEK RT9169
3.3V/100mA Iq = 4uA

VDD_SNVS_IN

PMIC_ON_REQ
DC/DC BUCK
MPS MP2144
3.3V/2A Iq=40uA

VDD_HIGH_IN

DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.275V/1A Iq=40uA

VDDARM_IN

DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.35V/1A Iq=40uA

VDD_MEM1V5

1.8V for eMMC HS200 mode
LDO
RICHTEK RT9169
1.8V/100mA Iq = 4uA

DCDC_3V3
HIGH PSRR LDO
RICHTEK RT9193
3.3V/300mA

VLDO_3V3

DCDC_3V3_PG
LDO
RICHTEK RT9065
1.8V/3.3V/500mA

NVCC_SD (3.3V/1.8V)

1.8V for CSI:
1.8V/3.3V for SIM
DCDC_3V3
LDO
RICHTEK RT9065
1.8V/3.3V/500mA

NVCC_CSI (1.8V/3.3V)

USB_OTGx_PWR
LOAD SW

USB_OTG_VBUS
USB_HOST_VBUS

VDD_SNVS_IN
276uA
LDO_ARM_SOC
VDD_SNVS_CAP

LDO_1P1
NVCC_PLL

VDD_HIGH_IN
125mA
LDO_2P5
VDD_HIGH_CAP

NVCC_GPIO/NVCC_ENET/NVCC_LCDIF
NVCC_DRAM_2P5

VDD_SOC_IN
900mA
LDO_ARM_SOC
VDD_ARM_CAP
VDD_SOC_CAP

NVCC_DRAM
50mA
NVCC_NAND

FSL i.MX6UL CPU

VDDA_ADC_3P3

NVCC_SD

NVCC_CSI

50mA
USB_OTG1_VBUS
USB_OTG2_VBUS
LDO_USB
VDD_USB_CAP

LvDDR3
Micron: MT41K512M16

RGB LCD
TianMa TFT
VLCD_3V3
3.3V/23mA
5S2P
16V/25mA
BACKLIGHT
RICHTEK RT9293B
BLT_PWM

HDMI
SILICON IMAGE SiI9022A
VHDMI_3V3
3.3V/10mA
VLDO_1V2
1.2V/69.2mA
LDO
RICHTEK RT9169

Audio Codec
WM8960
VSPK_5V
5V/511mA
VAUD_3V3
3.3V/62.58mA

SENSOR
eCompass/
G-sensor/Gyroscope
VSENSOR_3V3
3.3V/6.9mA

CAN
FSL MC34901WEF
CAN_VIO_3V3
3.3V/1mA
CAN_VDD_5V
5V/65mA

Ethernet x2
Micrel KSZ8081RNB
VENET_3V3
3.3V/48.7mA
LOAD SW

Camera/EMV SIM
CSI B2B CN
AVDD_2V8
LDO
RICHTEK RT9065
2.8V/500mA
DVDD1V5
LDO
RICHTEK RT9065
1.5V/500mA

DCDC_3V3
3.3V/200mA
eMMC 4GB
Micron MTFC8GLCDM

NVCC_NAND
3.3V/1.8V
QSPI
Micron N25Q256

DCDC_3V3
3.3V/20mA

DCDC_3V3
3.3V/50mA
NAND
Micron MT29F32G08

MCIMX6UL-CM

USB_OTG_VBUS
USB OTG

USB_HOST_VBUS
USB HOST

SD1_nRST/POR_B
LOAD SW
SD Socket
BT MOD

ICAP Classification: FCP: FIUO: X PUBI:

Designer: DESIGNER	Drawing Title: MCIMX6UL-BB	
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LCD IF

BLT_PWM
USB_OTG2_OC
USB_OTG1_OC
USB_OTG1_PWR
USB_OTG2_PWR
LCD_DISP
LCD_PCLK
LCD_DE
LCD_HSYNC
LCD_VSYNC
LCD_DATA[23:0]
ECSPI4_SCLK
ECSPI4_MOSI
ECSPI4_MISO
ECSPI4_SS0
I2C2_SDA
I2C2_SCL

BLT_PWM
GPIO_3
GPIO_1
GPIO_4
GPIO_2
LCD_DISP
LCD_PCLK
LCD_DE
LCD_HSYNC
LCD_VSYNC
ENET2_TXD1
ENET2_TXEN
ENET2_TX_CLK
ENET2_RXER
I2C2_SDA
I2C2_SCL

PWR

LCD Standby Mode PWR: 50uW

R901 DNP 0_0603_CC
DCDC_3V3
VLCD_3V3
Q901 IRLML6401
R913 100K
R914 10K
D901 RB521S30T1G
LCD_nPWREN
GND

LCD CN

J901
FPC05050-08100

LCD_DATA[23:0]
LCD_DATA0 R919 0 B0 1
LCD_DATA1 R920 0 B1 2
LCD_DATA2 R921 0 B2 3
LCD_DATA3 R922 0 B3 4
LCD_DATA4 R923 0 B4 5
LCD_DATA5 R924 0 B5 6
LCD_DATA6 R925 0 B6 7
LCD_DATA7 R926 0 B7 8
GND 9
LCD_DATA8 R927 0 G0 10
LCD_DATA9 R928 0 G1 11
LCD_DATA10 R929 0 G2 12
LCD_DATA11 R930 0 G3 13
LCD_DATA12 R931 0 G4 14
LCD_DATA13 R932 0 G5 15
LCD_DATA14 R933 0 G6 16
LCD_DATA15 R934 0 G7 17
GND 18
LCD_DATA16 R935 0 R0 19
LCD_DATA17 R936 0 R1 20
LCD_DATA18 R937 0 R2 21
LCD_DATA19 R938 0 R3 22
LCD_DATA20 R939 0 R4 23
LCD_DATA21 R940 0 R5 24
LCD_DATA22 R941 0 R6 25
LCD_DATA23 R942 0 R7 26
GND 27
LCD_DE R943 0 DE 28
LCD_HSYNC R944 0 HSYNC 29
LCD_VSYNC R945 0 VSYNC 30
GND 31
LCD_PCLK R946 0 DCLK 32
GND 33
USB_OTG1_PWR GPIO_4 R903 0 xpul X_L 34
USB_OTG2_OC GPIO_3 R904 0 xnur X_R 35
USB_OTG2_PWR GPIO_2 R905 0 ypll Y_T 36
USB_OTG1_OC GPIO_1 R906 0 ynlr Y_B 37
ECSPI4_SCLK ENET2_TXD1 R907 0 DNP SPI_CLK 38
ECSPI4_MOSI ENET2_TXEN R908 0 DNP SPI_MOSI 39
ECSPI4_MISO ENET2_TX_CLK R910 0 DNP SPI_MISO 40
ECSPI4_SS0 ENET2_RXER R911 0 DNP SPI_CS 41
I2C2_SCL L904 120 Ohm I2C_CLK 42
I2C2_SDA L905 120 Ohm I2C_SDA 43
GND 44
R912 0 VDD_1.8V 45
VDD_3.3V 46
VDD_5V 47
VDD_5V 48
LCD_DISP R917 0 RESET 49
BLT_PWM L903 120 Ohm PWREN 50
51 52

C905 18PF 0402_CC DNP
GND

VLCD_3V3
L901 470 Ohm
C903 10uF 10V 0603_CC
C902 0.1uF 25V 0402_CC
GND

VSYS
L902 470 Ohm
C901 10uF 10V 0603_CC
C904 0.1uF 25V 0402_CC
GND

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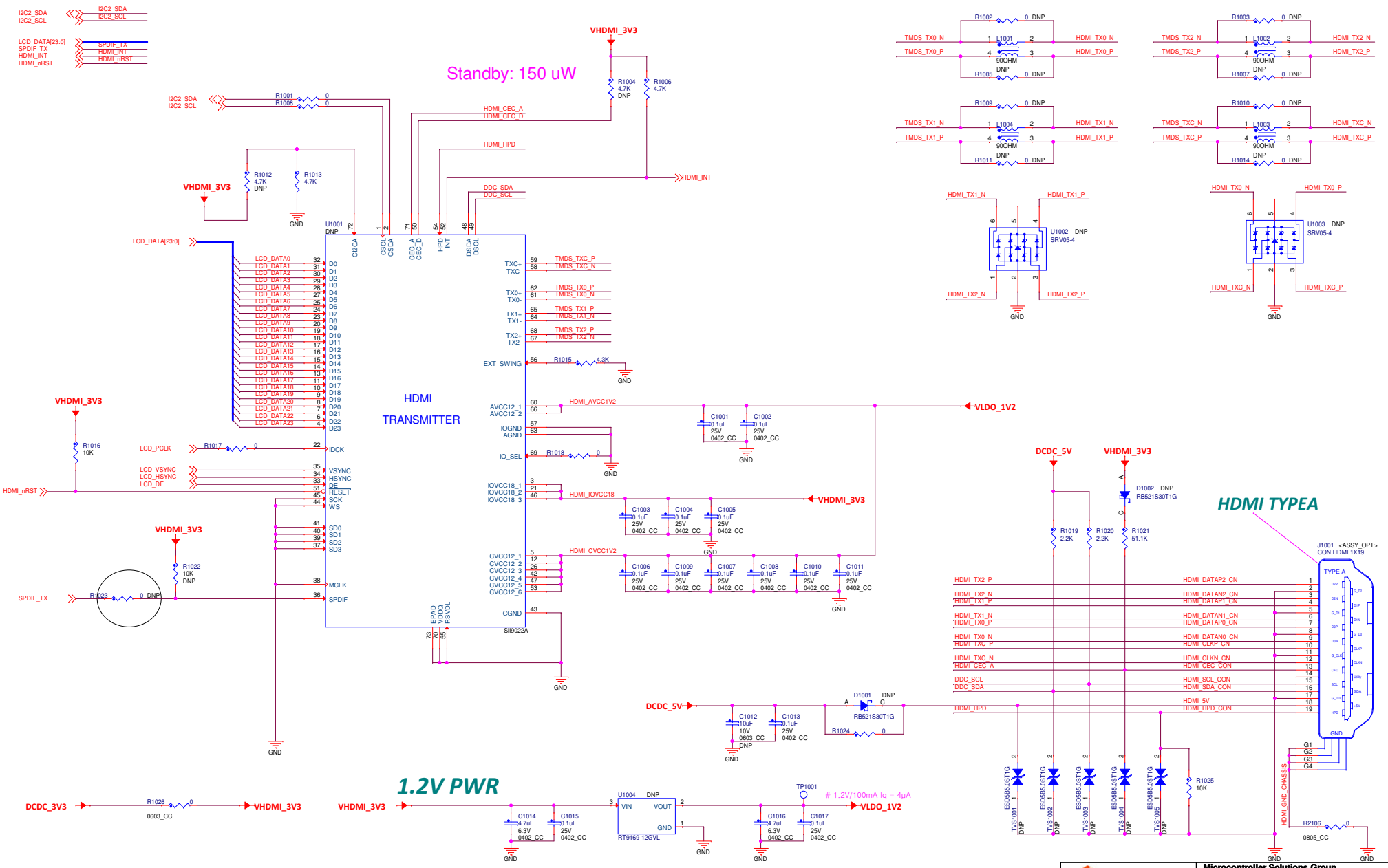
HDMI Transmitter



EMI/ESD

#Res Overlap with EMI Choke

HDMI TYPEA

1.2V PWR

Internal Function	CI2CA = LOW	CI2CA = HIGH
Transmitter Programming Interface (TPI) device address	0x72	0x76
CEC Programming Interface (CPI) device address	0xC0	0xC4
Sil9020-compatible internal registers: first device address	0x72	0x76
Sil9020-compatible internal registers: second device address	0x7A	0x7E

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USB HOST/OTG

USB Client PWR

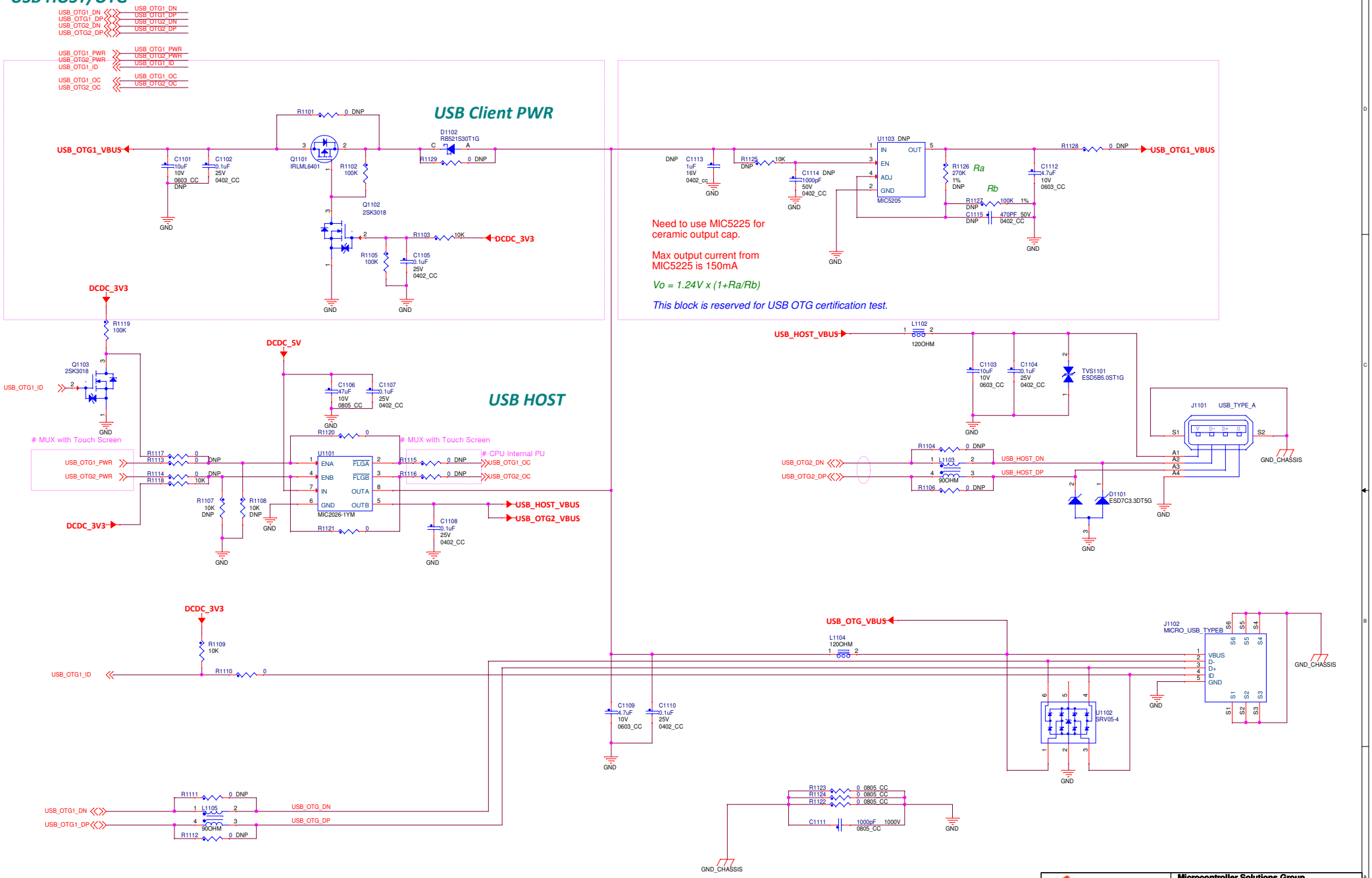
USB HOST

Need to use MIC5225 for ceramic output cap.

Max output current from MIC5225 is 150mA

Vo = 1.24V x (1+Ra/Rb)

This block is reserved for USB OTG certification test.



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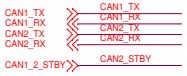
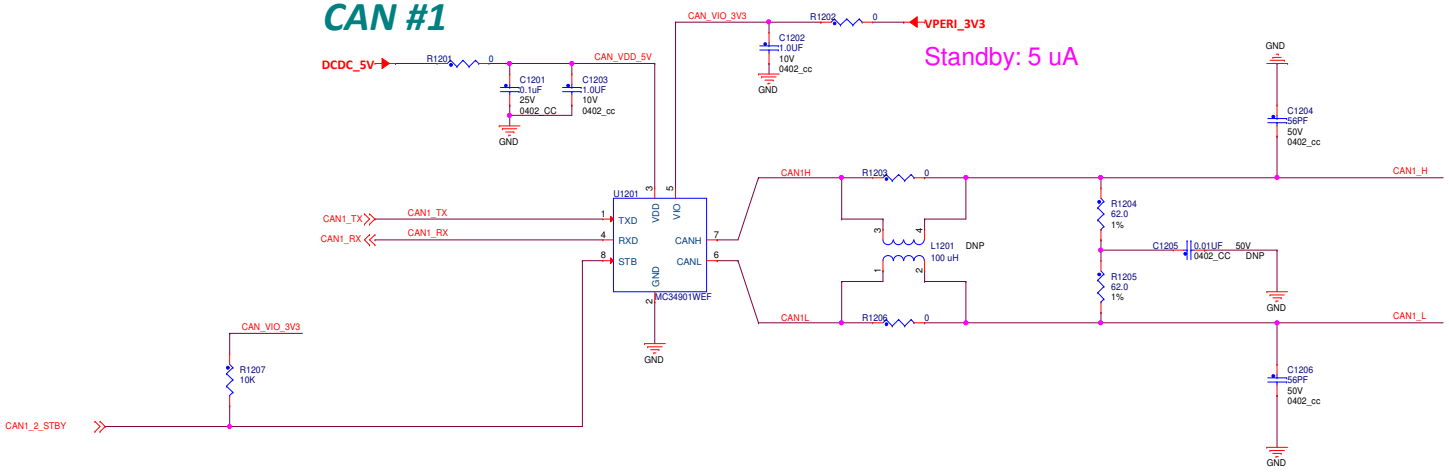
High Speed CAN Transceiver

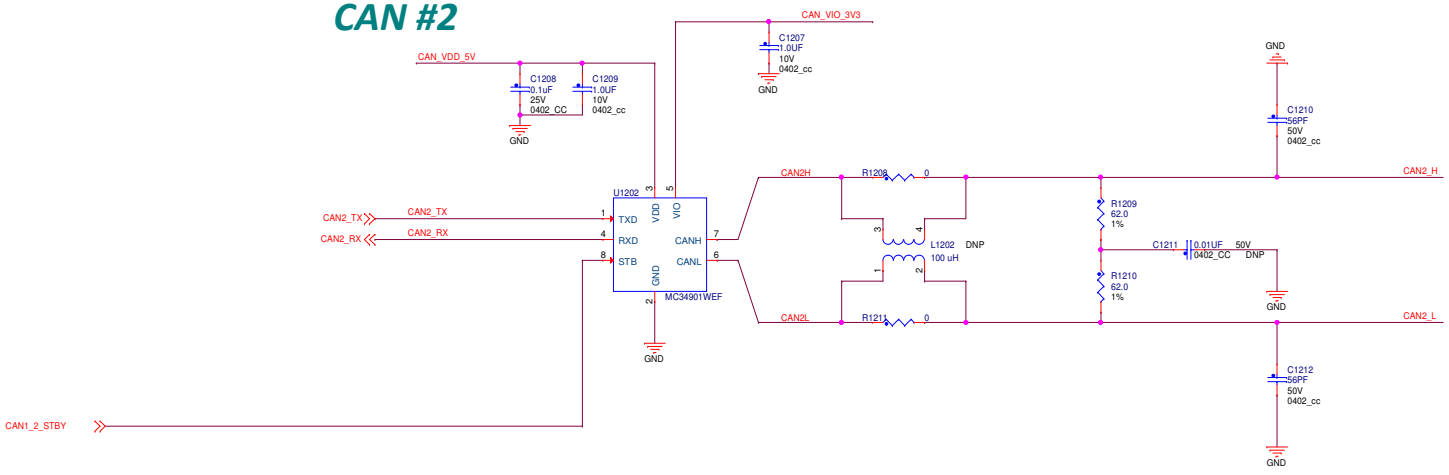
 # FSL High Speed CAN Transceiver



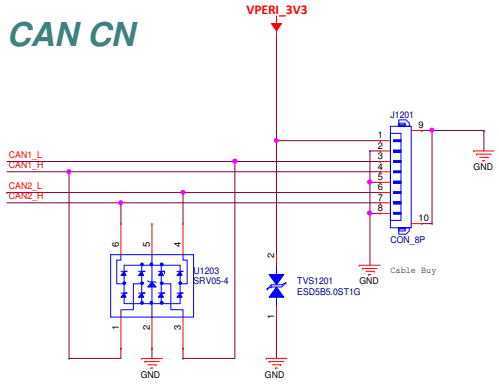
CAN #1



CAN #2



CAN CN



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Approved: APPROVER	Size: C	Document Number: SCH-28616 PDF: SPF-28616	Rev: C
	Date: Tuesday, July 14, 2015	Sheet 7 of 18	

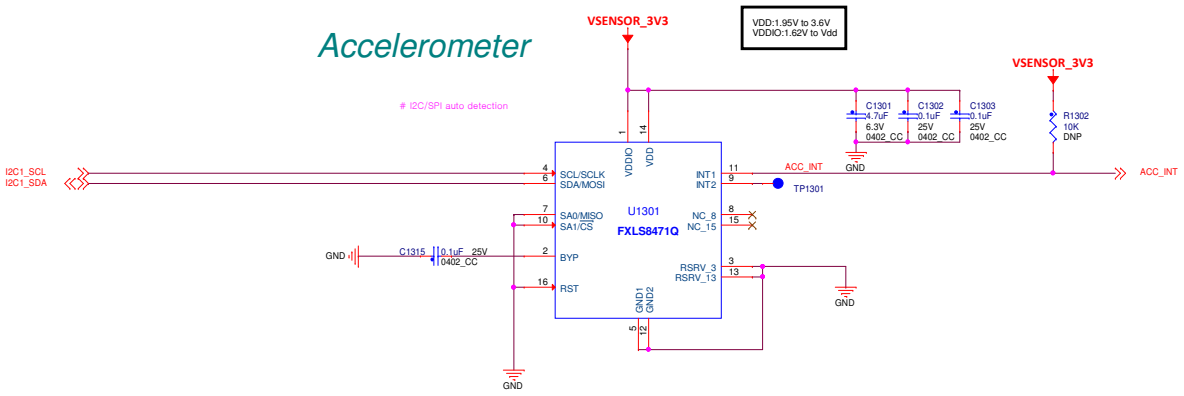
Motion Sensor 9-axis

I2C1_SDA
I2C1_SCL
ACC_INT

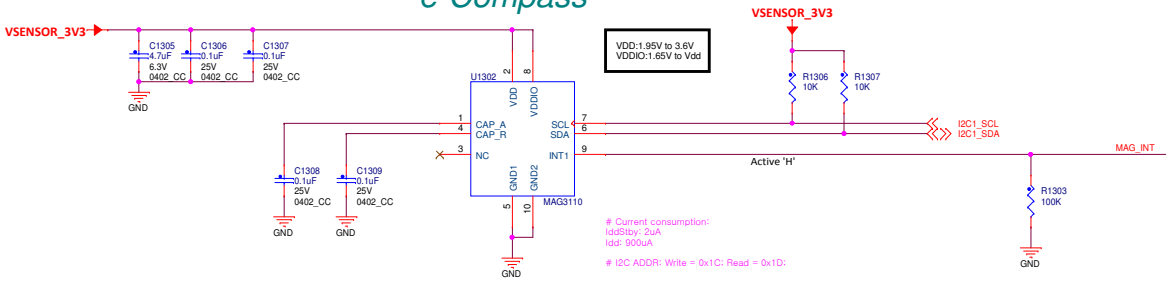
I2C1_SDA
I2C1_SCL
ACC_INT

VPERI_3V3 — R1301 0 — VSENSOR_3V3

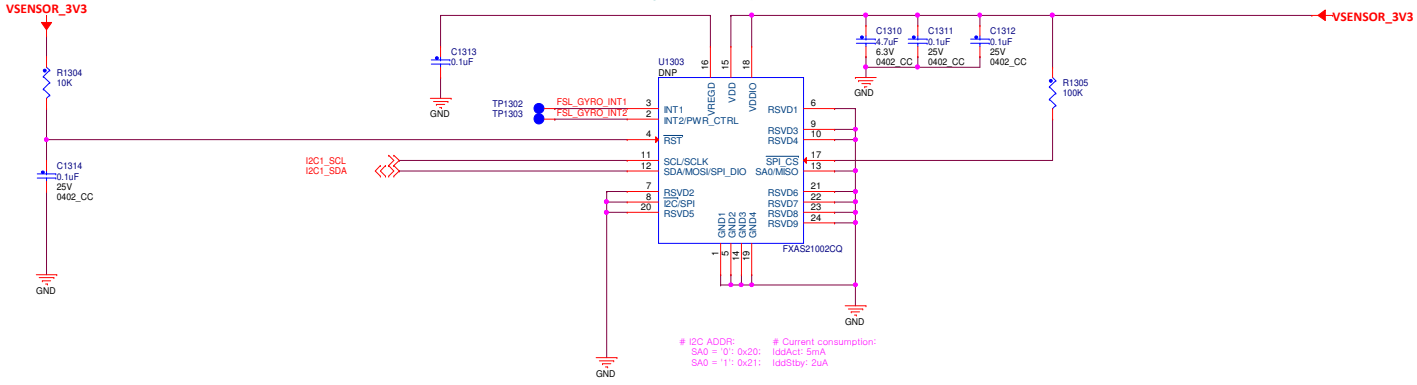
Accelerometer



e-Compass



Gyroscope



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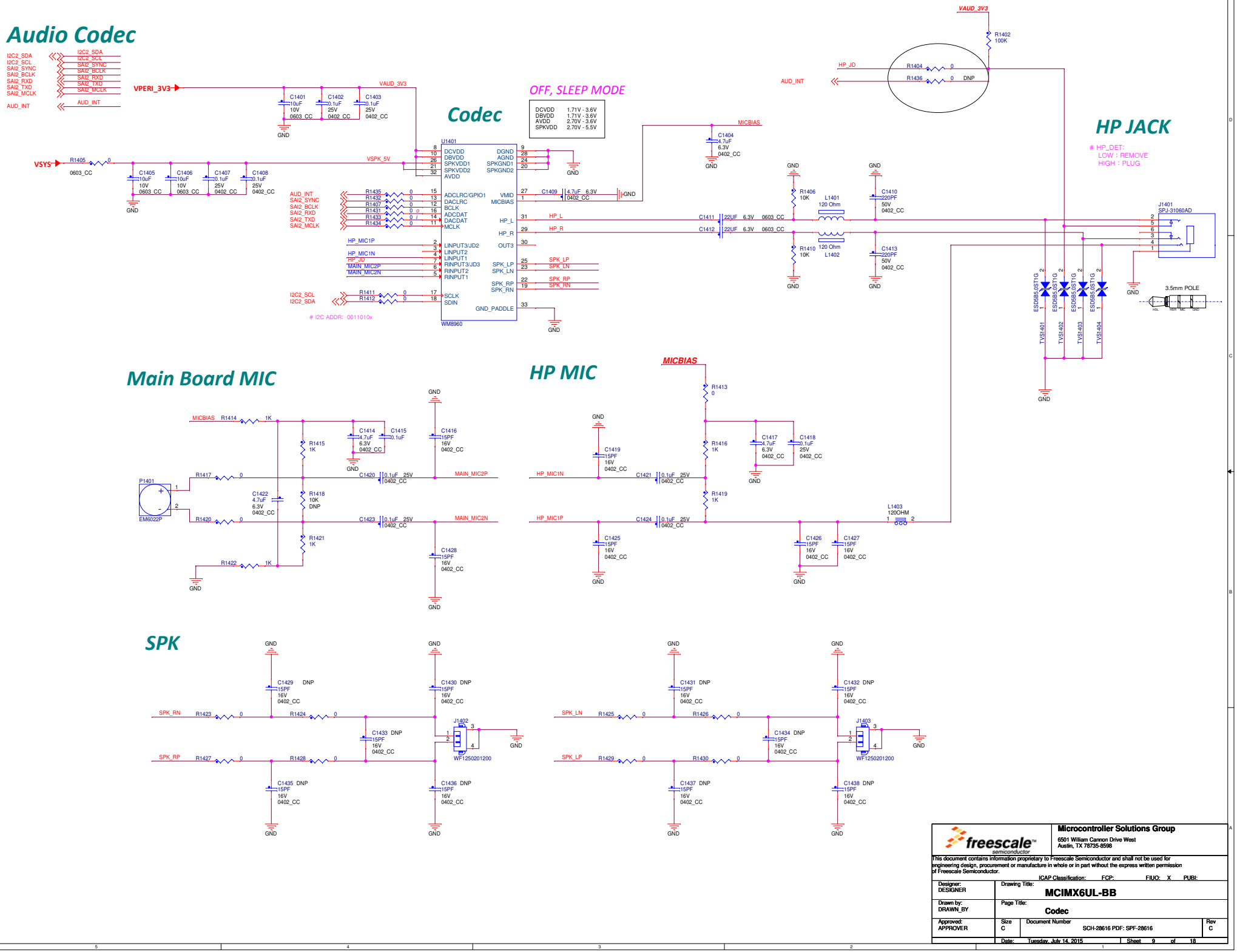
Audio Codec



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100M ETHERNET RMII PHY x1

ENET_MDIO
ENET_MDC
ENET1_TXD0
ENET1_TXD1
ENET1_TXEN
ENET1_TX_CLK
ENET1_RXD0
ENET1_RXD1
ENET1_RXER
ENET1_CRS_DV

ENET1_nINT
ENET1_nRST

Software power-down mode:
VDDA_3.3: 1.36mA
VDDIO: 0.45mA

PHY PWR

VENET_3V3
VPERI_3V3
VDDCO_1_1V8
L1501 470 Ohm
C1501 22UF 6.3V 0603_CC
C1502 0.1uF 25V 0402_CC
C1503 22UF 6.3V 0603_CC
C1504 0.1uF 25V 0402_CC
C1505 0.1uF 25V 0402_CC
VDDIO: 3.3V/2.5V/1.8V
R1501 1K
R1504 1K
R1508 1K
R1509 10K
C1508 0.1uF 25V 0402_CC
TP1501
TP1502
TP1503
R1515 6.49K
C1506 0.1uF 25V 0402_CC
C1507 0.1uF 25V 0402_CC
GND
GND_CHASSIS

U1501
KSZ8081RNB

MDIO
MDC
RXD0/DUPLEX
RXD1/PHYAD2
PHYAD1
PHYAD0
CRS_DV/CONFIG2
RXER/ISO
REF_CLK/B-CAST_OFF
TXD0
TXD1
NC2
NC3
TXEN
NC1
INTRP/NAND_TREE
RST
XI
XO
VDDIO
VDDA_3.3
VDD_1.2
TXP
TXM
RXP
RXM
LED0/NWAYEN
LED1/SPEED
REXT
CONFIG0
CONFIG1
GND
PADDLE

J1501A
RJ45 HY911205C
CON_2XRJ45
1CT:1CT
1000pF 2KV
4X75 ohms
LED1
LED2
R1505 220
R1507 220
SH1
SH2
SH3

RMII CFG

R1516 4.7K DNP
R1517 1K DNP
R1518 1K
R1519 1K
R1520 4.7K
R1521 4.7K DNP
R1522 1K DNP
R1523 1K
R1524 1K
R1525 4.7K
R1526 4.7K DNP
R1527 4.7K DNP
R1528 1K
R1529 4.7K DNP
R1530 1K
R1531 1K
R1532 1K
R1533 4.7K DNP
R1534 1K

# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00001 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (defaule) = Disable
SPEED	SPEED mode Pull-up (defaule) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (defaule) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (defaule) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (defaule) = Disable Pull-down = Enable

ESD PROTECTION

 # 2rd LEVEL ESD

ETH1_TXP
ETH1_TXM
ETH1_RXP
ETH1_RXM
U1502 SRV05-4 DNP

Designer: DESIGNER	Drawing Title: MCIMX6UL-BB
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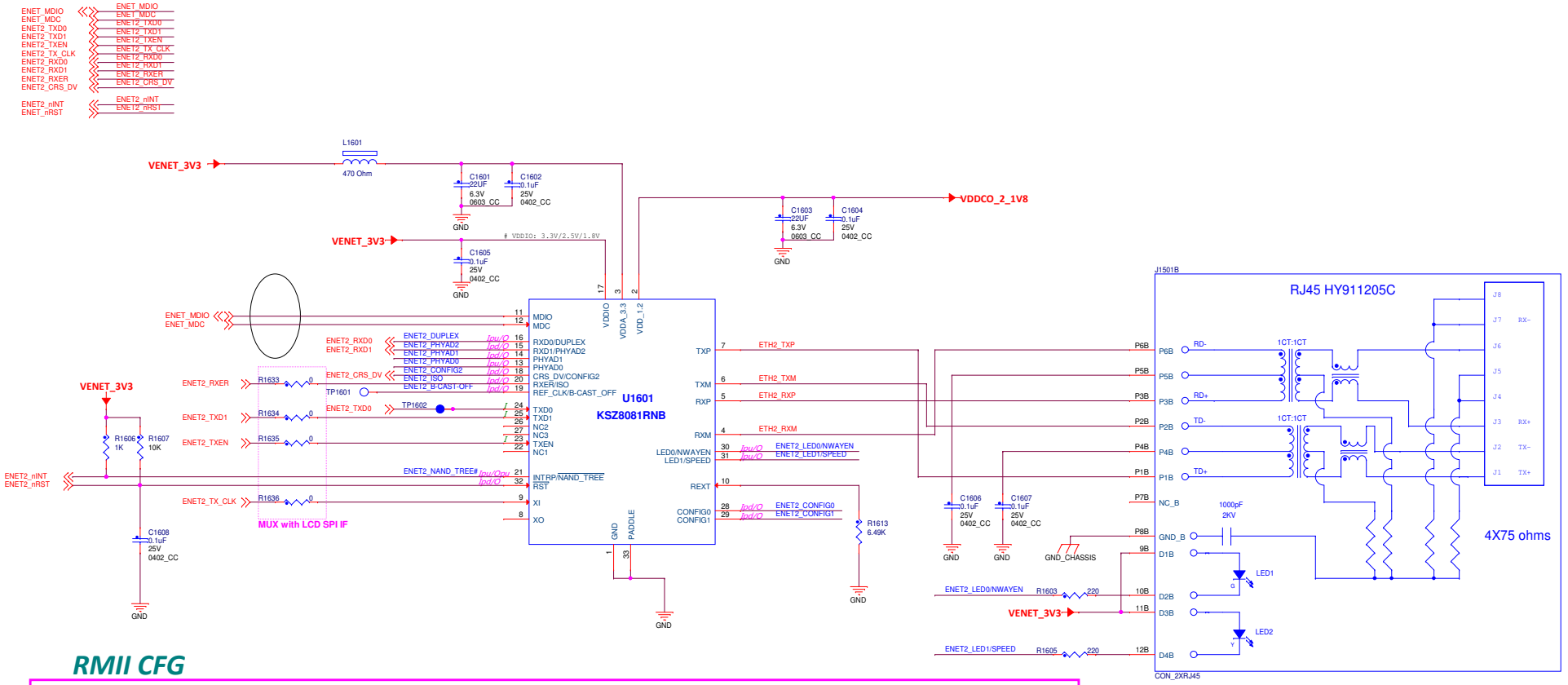
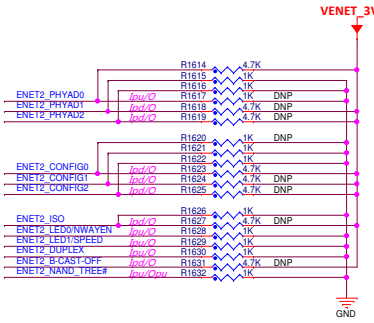
100M ETHERNET RMII PHY x2



RMII CFG

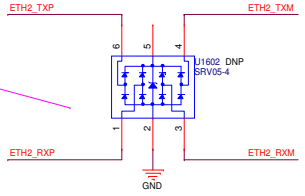


# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00001 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (defeault) = Disable
SPEED	SPEED mode Pull-up (defeault) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (defeault) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (defeault) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (defeault) = Disable Pull-down = Enable

2rd LEVEL ESD

ESD PROTECTION



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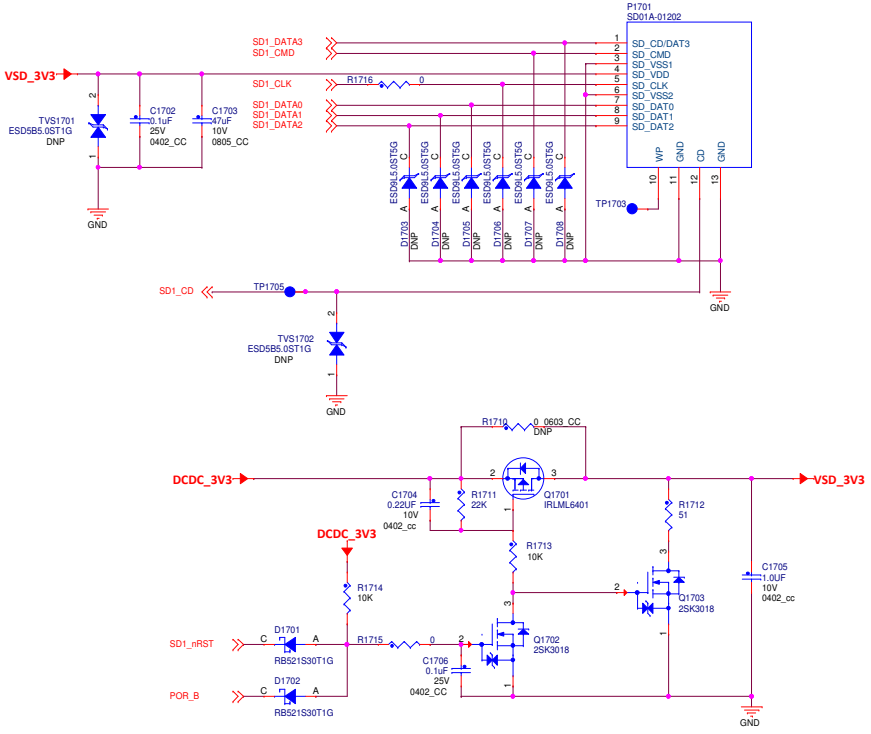
BLUETOOTH / SD FULL SOCKET

SD SLOT

 # for WiFi and SD Accessories

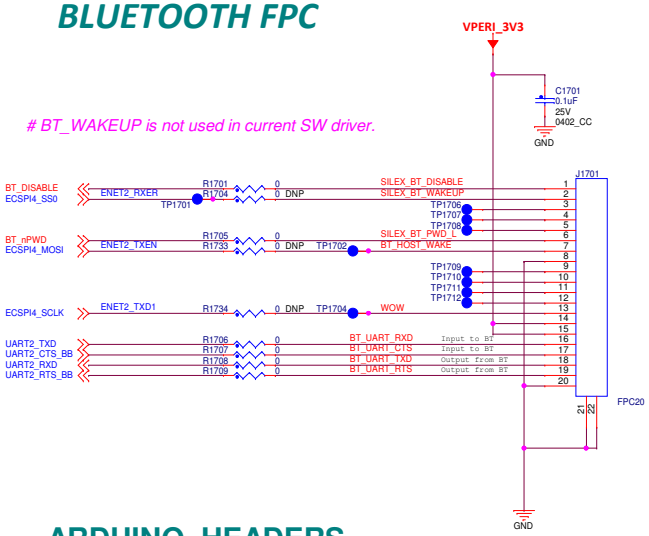


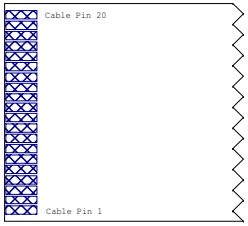
NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

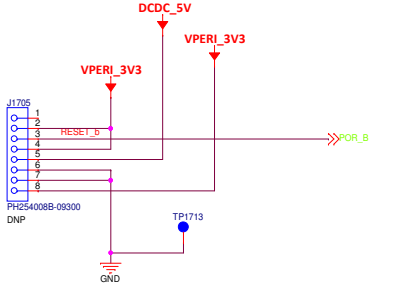
BLUETOOTH FPC

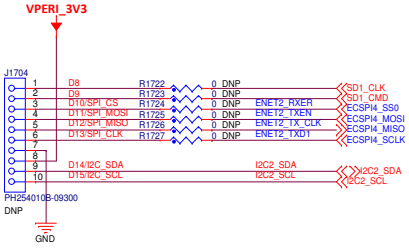
 # BT_WAKEUP is not used in current SW driver.

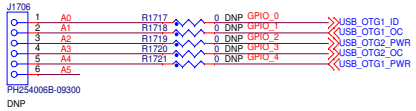


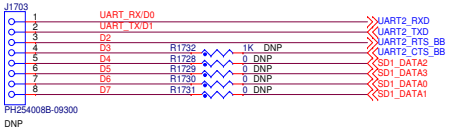


ARDUINO_HEADERS









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Microcontroller Solutions Group
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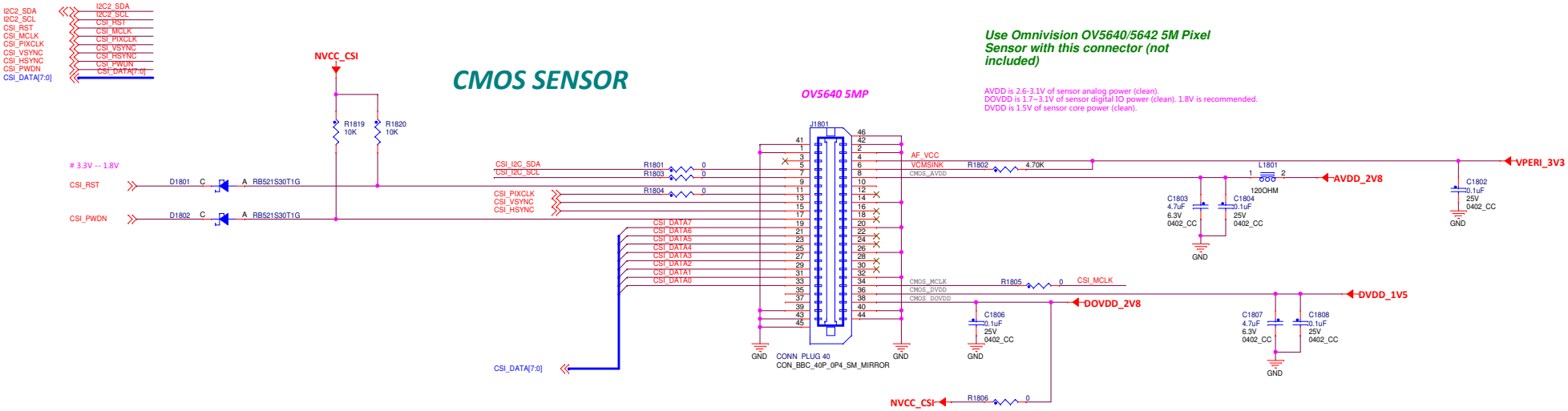
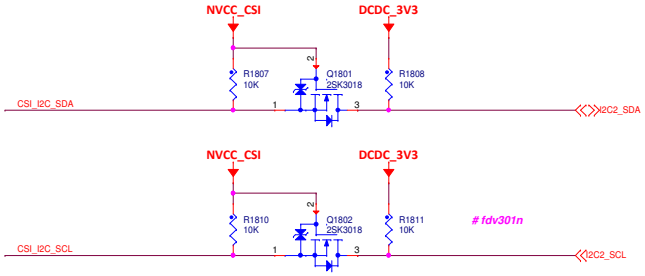
Austin, TX 78735-8598

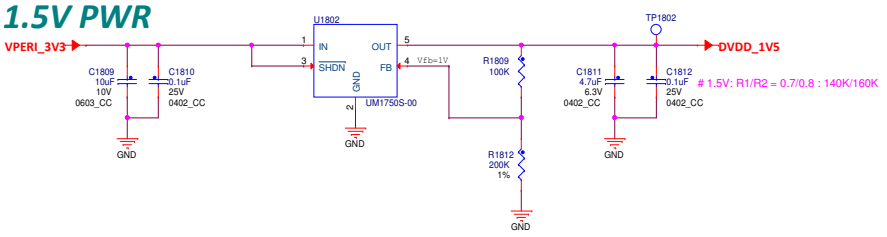
ICAP Classification: FCP: FIUO: X PUBI:

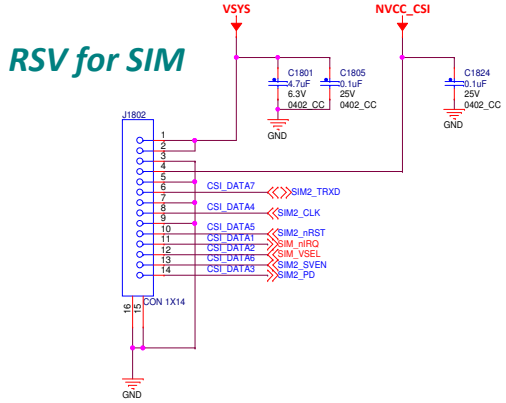
Designer: DESIGNER	Drawing Title: MCIMX6UL-BB		
Drawn by: DRAWN_BY	Page Title: BT/SD		
Approved: APPROVER	Size C	Document Number SCH-28616 PDF: SPF-28616	Rev C
	Date: Thursday, July 16, 2015	Sheet 12 of 18	

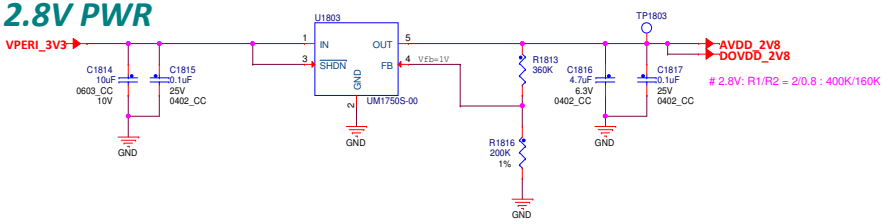
Camera / SIM











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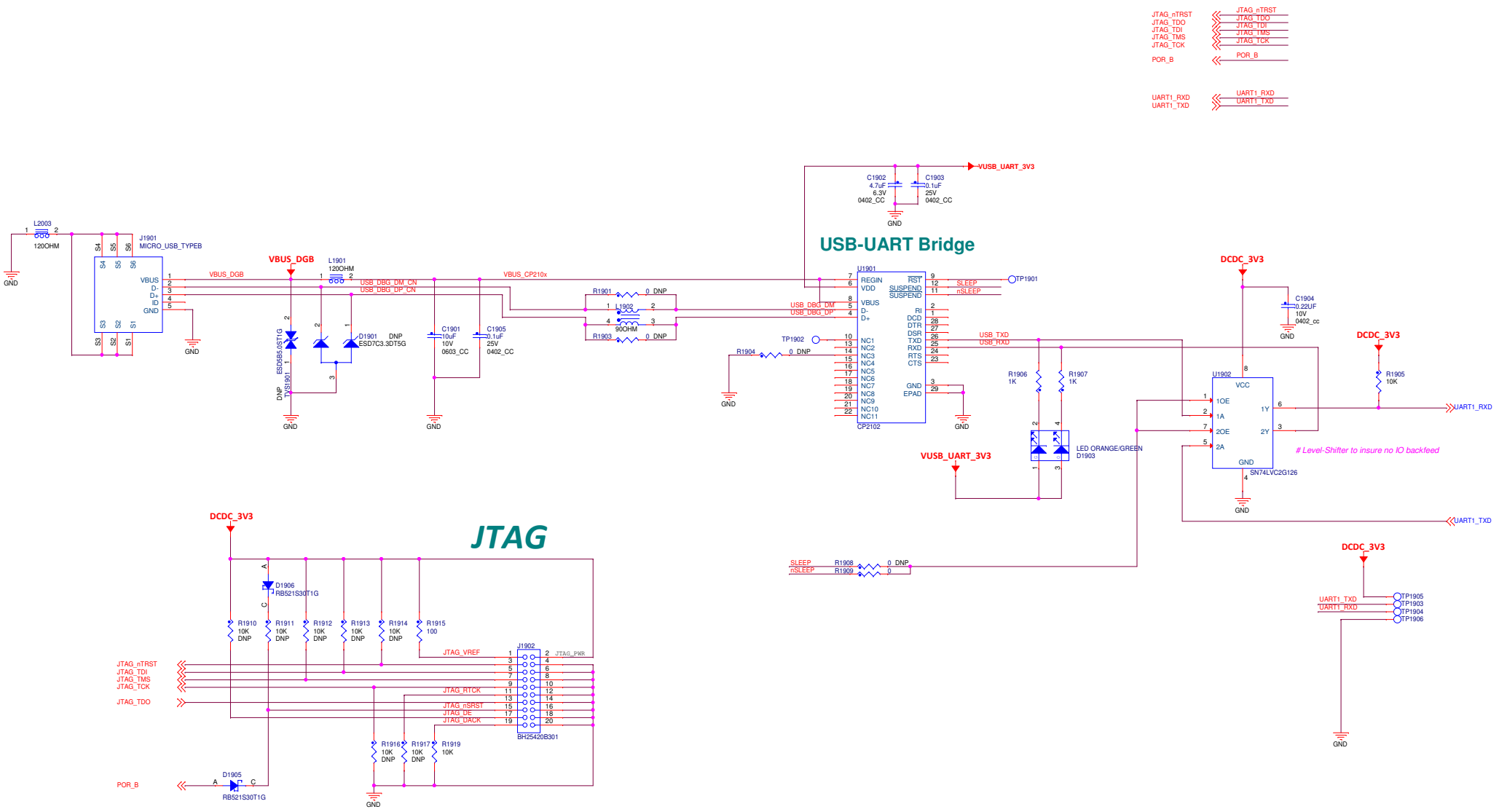
Drawn by: DRAWN_BY	Page Title: CAMERA/EMV SIM	
Approved: APPROVER	Size C	Document Number SCH-28616 PDF: SPF-28616 Rev C
	Date: Tuesday, July 14, 2015	Sheet 13 of 18

UART-USB DBG / JTAG



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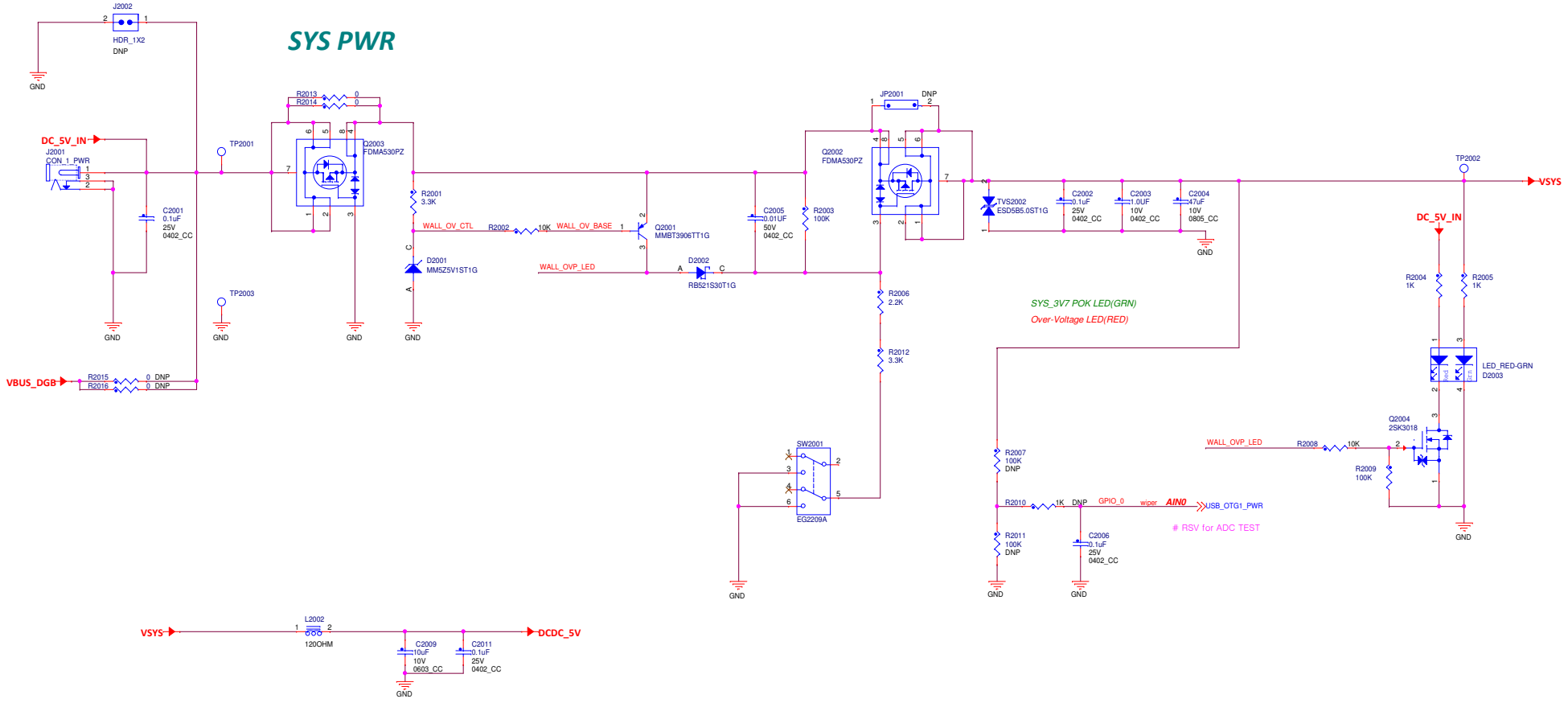
Designer: DESIGNER	Drawing Title: MCIMX6UL-BB	
Drawn by: DRAWN_BY	Page Title: DEBUG/JTAG	
Approved: APPROVER	Size C / Document Number SCH-28616 PDF: SPF-28616	Rev C
	Date: Tuesday, July 14, 2015	Sheet 14 of 18



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Drawn by: DRAWN_BY	Page Title: PWR	
Approved: APPROVER	Size C	Document Number SCH-28616 PDF: SPF-28616 Rev C
	Date: Tuesday, July 14, 2015	Sheet 15 of 18

SODIMM 200

TP for SODIMM MFG

CPU SODIMM TST/DBG

DCDC_3V3

UART1_TXD — TP2101
UART1_RXD — TP2102
TP2103
TP2104
TP2105
USB_OTG1_DN — TP2106
USB_OTG1_DP — TP2107
TP2108
TP2109

USB_OTG1_VBUS

GND

BMOD TP for MFG TOOL

BOOT_MODE0 — TP2110
BOOT_MODE1 — TP2111
VDD_SNVS_IN — TP2112
TP2113
GND
VSYS — TP2114
TP2115
ONOFF — TP2116

J2101
DDR2 SODIMM 200

CSI_HSYNC
CSI_DATA1
CSI_DATA4
SIM_nIRQ
SIM2_CLK
CSI_MCLK
CSI_PIXCLK
SD1_CLK
SD1_DATA2
SD1_CMD
SD1_DATA1
SD1_DATA3
SD1_DATA0
LCD_DE
LCD_PCLK
LCD_RST
TP2128
LCD_RST has been used as WDOG on CPU BOARD

SD CARD

LCD_DATA1
LCD_DATA0
LCD_DATA6
LCD_DATA5
LCD_DATA9
LCD_DATA8
LCD_DATA14
LCD_DATA13
LCD_DATA18
LCD_DATA17
LCD_DATA22
LCD_DATA21

100M RMII PHY

ECSPI4_MOSI
ECSPI4_SCLK
ENET2_TXEN
ENET2_TXD1
ECSPI4_SS0
ENET2_RXER
ECSPI4_MISO
ENET2_TX_CLK
ENET2_TXD0
ENET2_RXD1
ENET2_RXD0
ENET2_RXER
ENET2_CRS_DV
ENET2_TX_CLK
ENET1_CRS_DV
ENET1_RXD1
ENET1_RXD0

DCDC_3V3

C2133 0.1uF 25V 0402_CC
C2134 1.0UF 10V 0402_cc
C2135 22UF 6.3V 0603_CC
GND

Maxim DCDC_3V3 supply current for Base Board: 1.2A

I2C2_SCL
I2C1_SDA
I2C1_SCL
UART2_RTS_BB
UART2_CTS_BB
UART2_RXD
UART2_TXD
UART1_RXD
ENET_MDIO
UART1_TXD
USB_OTG2_OC
ENET_MDC
TP2120
SD1_VSELECT
USB_OTG1_PWR
BLT_PWM
JTAG_TDI
SAI2_BCLK

BT UART

UART5_TXD
UART4_RXD
UART4_TXD
UART3_RXD
UART3_TXD
UART2_RTS
UART2_CTS
UART2_TXD
UART1_RXD
GPIO_6
UART1_TXD
GPIO_3
GPIO_7
GPIO_5
GPIO_4
GPIO_8
JTAG_TDI

Debug UART

CLK1_P
CLK1_N
TP2117
TP2118
JTAG_MOD
nUSB_OTG_CHD
SPDIF_TX
TP2121
USB_OTG1_DN
USB_OTG1_DP
USB_OTG2_DN
USB_OTG2_DP

USB OTG

USB HOST

USB_OTG1_VBUS

C2105 10uF 10V 0603_CC DNP
C2106 0.1uF 25V 0402_CC
GND

USB_OTG2_VBUS

C2108 10uF 10V 0603_CC
C2107 0.1uF 25V 0402_CC
GND

SHIFT_SDI
SHIFT_SHCP
TP2126
TP2127
BOOT_MODE0
BOOT_MODE1
PMIC_ON_REQ
PMIC_STBY_REQ

VPERI_3V3

C2136 0.1uF 25V 0402_CC
C2137 0.1uF 25V 0402_CC
C2138 0.1uF 25V 0402_CC
C2139 0.1uF 25V 0402_CC
C2140 0.1uF 25V 0402_CC
C2152 0.1uF 25V 0402_CC
C2153 0.1uF 25V 0402_CC
C2154 0.1uF 25V 0402_CC
GND
C2147 0.1uF 25V 0402_CC
C2148 0.1uF 25V 0402_CC
C2149 0.1uF 25V 0402_CC
C2150 0.1uF 25V 0402_CC
C2151 0.1uF 25V 0402_CC
GND

CSI_VSYNC
CSI_DATA2
CSI_DATA3
CSI_DATA5
CSI_DATA7
CSI_DATA6
LCD_DATA7
LCD_DATA2
LCD_VSYNC
LCD_HSYNC
LCD_DATA4
LCD_DATA3
LCD_DATA10
LCD_DATA12
LCD_DATA11
LCD_DATA16
LCD_DATA15
LCD_DATA20
LCD_DATA19
LCD_DATA23
ENET1_RXER
ENET1_TXD1
ENET1_TXD0
ENET1_TX_CLK
ENET1_TXEN
UART3_RTS
UART2_RTS
UART3_CTS
UART1_RTS
UART2_CTS
UART5_RXD
UART1_CTS
GPIO_0
GPIO_1
GPIO_2
GPIO_9
JTAG_TCK
JTAG_TDO
JTAG_nTRST
JTAG_TMS
SNVS_TAMPER2
SNVS_TAMPER6
PERI_PWREN
ENET2_nINT
SNVS_TAMPER0
SNVS_TAMPER3
SNVS_TAMPER1
SNVS_TAMPER4
SNVS_TAMPER7
SNVS_TAMPER8
POR_B
ONOFF
SNVS_TAMPER5
SNVS_TAMPER9
LCD_DISP
MX6_POR_B
ACC_INT
BT_DISABLE
AUD_INT
SHIFT_STCP
SHIFT_nOE
GPIO_DVFS
TP2124
CAN1_RX
CAN2_RX
CAN1_TX
CAN2_TX
I2C2_SDA
HDMI_INT
USB_OTG1_ID
USB_OTG1_OC
USB_OTG2_PWR
SD1_nRST
SAI2_RXD
SAI2_SYNC
SAI2_TXD
SAI2_MCLK

Camera/EVMSIM

SIM_VSEL
SIM2_PD
SIM2_nRST
SIM2_TRXD
SIM2_SVEN
C2101 10uF 10V 0603_CC
C2102 0.1uF 25V 0402_CC
NVCC_CSI

LCD/HDMI

SNVS_TAMPER0 — R2107 1M
SNVS_TAMPER1 — R2108 1M
SNVS_TAMPER2 — R2109 1M
SNVS_TAMPER3 — R2110 1M
SNVS_TAMPER4 — R2111 1M
SNVS_TAMPER5 — R2112 1M
SNVS_TAMPER6 — R2113 1M
SNVS_TAMPER7 — R2114 1M
SNVS_TAMPER8 — R2115 1M
SNVS_TAMPER9 — R2116 1M
GND

Reduce the VSNVS Power consumption during power down mode

JTAG/Audio

PHY PWR

R2102 0.02 DNP
DCDC_3V3
Q2101 IRLML6401
VPERI_3V3
PERI_PWREN
R2101 10K
GND

C2127 47uF 10V 0805_CC
C2128 47uF 10V 0805_CC
C2129 0.1uF 25V 0402_CC
C2130 0.1uF 25V 0402_CC
L2101 120OHM
L2102 120OHM
VSYS

VPERI_3V3
C2132 4.7uF 6.3V 0402_CC
C2131 0.1uF 25V 0402_CC
GND

VDD_SNVS_IN PWR Domain

SHIFT_SDI
SHIFT_SHCP
SHIFT_STCP
SHIFT_nOE
R2105 10K
U2101 74LV595PW
HDMI_nRST
ENET1_nRST
ENET2_nRST
CAN1_2_STBY
BT_nPWD
CSI_RST
CSI_PWDN
LCD_nPWREN

SW2101
ONOFF
CPU ONOFF Button
SW2102
MX6_POR_B
System Reset Button
SPST PB
GND

VDD_SNVS_IN
C2103 10uF 10V 0603_CC
C2104 0.1uF 25V 0402_CC
C2109 10uF 10V 0603_CC
C2110 0.1uF 25V 0402_CC
BT2101 2994TR DNP
VDD_COIN_3V

U2102 MOUNTING HOLE
U2103 MOUNTING HOLE
BH2101 MOUNTING HOLE
BH2102 MOUNTING HOLE
BH2103 MOUNTING HOLE
BH2104 MOUNTING HOLE
TP2129
TP2130

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Drawn by: DRAWN_BY	Page Title: BASE-SODIMM200		
Approved: APPROVER	Size: C	Document Number: SCH-28616 PDF: SPF-28616	Rev: C
	Date: Tuesday, July 14, 2015	Sheet 16 of 18	

NOTE: EMV SIM will be placed on the daughter board

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7

All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1'b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)

i.MX6UL IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	PAD DFU
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									100K PD
POR_B	src.POR_B	src.POR_B									100K PU
ONOFF	src.RESET_B	src.RESET_B									100K PU
SNVS_PMIC_ON_REQ	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	snvs_lp_wrapper.PMIC_ON_REQ									100K PU
CCM_PMIC_STBY_REQ	ccm.PMIC_VSTBY_REQ	ccm.PMIC_VSTBY_REQ									100K PD
BOOT_MODE0	src.BOOT_MODE[0]	src.BOOT_MODE[0]					gpio5.IO[10]				100K PD
BOOT_MODE1	src.BOOT_MODE[1]	src.BOOT_MODE[1]					gpio5.IO[11]				100K PD
SNVS_TAMPER0	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[0]					gpio5.IO[0]				Keeper
SNVS_TAMPER1	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[1]					gpio5.IO[1]				Keeper
SNVS_TAMPER2	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[2]					gpio5.IO[2]				Keeper
SNVS_TAMPER3	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[3]					gpio5.IO[3]				Keeper
SNVS_TAMPER4	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[4]					gpio5.IO[4]				Keeper
SNVS_TAMPER5	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[5]					gpio5.IO[5]				Keeper
SNVS_TAMPER6	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[6]					gpio5.IO[6]				Keeper
SNVS_TAMPER7	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[7]					gpio5.IO[7]				Keeper
SNVS_TAMPER8	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[8]					gpio5.IO[8]				Keeper
SNVS_TAMPER9	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[9]					gpio5.IO[9]				Keeper
JTAG_MOD	sjc.MOD	sjc.MOD	gpt2.CLK	spdif.OUT	anatop.ENET_REF_CLK_25M	ccm.PMIC_RDY	gpio1.IO[10]	sdma.EXT_EVENT[0]			100K PU
JTAG_TMS	sjc.TMS	sjc.TMS	gpt2.CAPTURE1	sai2.MCLK	ccm.CLKO1	ccm.WAIT	gpio1.IO[11]	sdma.EXT_EVENT[1]		epit1.OUT	47K PU
JTAG_TDO	sjc.TDO	sjc.TDO	gpt2.CAPTURE2	sai2.TX_SYNC	ccm.CLKO2	ccm.STOP	gpio1.IO[12]	mqs.RIGHT		epit2.OUT	100K PU
JTAG_TDI	sjc.TDI	sjc.TDI	gpt2.COMPARE1	sai2.TX_BCLK	ccm.OUT0	pwm6.OUT	gpio1.IO[13]	mqs.LEFT		sim1.POWER_FAIL	47K PU
JTAG_TCK	sjc.TCK	sjc.TCK	gpt2.COMPARE2	sai2.RX_DATA	ccm.OUT1	pwm7.OUT	gpio1.IO[14]	osc32k.32K_OUT		sim2.POWER_FAIL	47K PU
JTAG_TRST_B	sjc.TRSTB	sjc.TRSTB	gpt2.COMPARE3	sai2.TX_DATA	ccm.OUT2	pwm8.OUT	gpio1.IO[15]	anatop.24M_OUT		caam_wrapper.RNG_OSC_OBS	47K PU
GPIO1_IO00	gpio1.IO[0]	i2c2.SCL	gpt1.CAPTURE1	anatop.OTG1_ID	anatop.ENET_REF_CLK1	mqs.RIGHT	gpio1.IO[0]	enet1.1588_EVENT0_IN	src.SYSTEM_RESET	wdog3.WDOG_B	Keeper
GPIO1_IO01	gpio1.IO[1]	i2c2.SDA	gpt1.COMPARE1	usb.OTG1_OC	anatop.ENET_REF_CLK2	mqs.LEFT	gpio1.IO[1]	enet1.1588_EVENT0_OUT	src.EARLY_RESET	wdog1.WDOG_B	Keeper
GPIO1_IO02	gpio1.IO[2]	i2c1.SCL	gpt1.COMPARE2	usb.OTG2_PWR	anatop.ENET_REF_CLK_25M	usdhc1.WP	gpio1.IO[2]	sdma.EXT_EVENT[0]	src.ANY_PU_RESET	uart1.TX	Keeper
GPIO1_IO03	gpio1.IO[3]	i2c1.SDA	gpt1.COMPARE3	usb.OTG2_OC	osc32k.32K_OUT	usdhc1.CD_B	gpio1.IO[3]	ccm.DI0_EXT_CLK	src.TESTER_ACK	uart1.RX	Keeper
GPIO1_IO04	gpio1.IO[4]	anatop.ENET_REF_CLK1	pwm3.OUT	usb.OTG1_PWR	anatop.24M_OUT	usdhc1.RESET_B	gpio1.IO[4]	enet2.1588_EVENT0_IN	ccm.PLL2_BYP	uart5.TX	Keeper
GPIO1_IO05	gpio1.IO[5]	anatop.ENET_REF_CLK2	pwm4.OUT	anatop.OTG2_ID	csi.FIELD	usdhc1.VSELECT	gpio1.IO[5]	enet2.1588_EVENT0_OUT	ccm.PLL3_BYP	uart5.RX	Keeper
GPIO1_IO06	gpio1.IO[6]	enet1.MDIO	enet2.MDIO	usb.OTG_PWR_WAKE	csi.MCLK	usdhc2.WP	gpio1.IO[6]	ccm.WAIT	ccm.REF_EN_B	uart1.CTS_B	Keeper
GPIO1_IO07	gpio1.IO[7]	enet1.MDC	enet2.MDC	usb.OTG_HOST_MODE	csi.PIXCLK	usdhc2.CD_B	gpio1.IO[7]	ccm.STOP	ecspi1.TESTER_TRIGGER	uart1.RTS_B	Keeper
GPIO1_IO08	gpio1.IO[8]	pwm1.OUT	wdog1.WDOG_B	spdif.OUT	csi.VSYNC	usdhc2.VSELECT	gpio1.IO[8]	ccm.PMIC_RDY	ecspi2.TESTER_TRIGGER	uart5.RTS_B	Keeper
GPIO1_IO09	gpio1.IO[9]	pwm2.OUT	global wdog	spdif.IN	csi.HSYNC	usdhc2.RESET_B	gpio1.IO[9]	usdhc1.RESET_B	ecspi3.TESTER_TRIGGER	uart5.CTS_B	Keeper
UART1_TXD	gpio1.IO[16]	uart1.TX	enet1.RDATA[2]	i2c3.SCL	csi.DATA[2]	gpt1.COMPARE1	gpio1.IO[16]	anatop.USBPHY1_TSTI_TX_LS_MODE	ecspi4.TESTER_TRIGGER	spdif.OUT	Keeper
UART1_RXD	gpio1.IO[17]	uart1.RX	enet1.RDATA[3]	i2c3.SDA	csi.DATA[3]	gpt1.CLK	gpio1.IO[17]	anatop.USBPHY1_TSTI_TX_HS_MODE	usdhc1.TESTER_TRIGGER	spdif.IN	Keeper
UART1_CTS	gpio1.IO[18]	uart1.CTS_B	enet1.RX_CLK	usdhc1.WP	csi.DATA[4]	enet2.1588_EVENT1_IN	gpio1.IO[18]	anatop.USBPHY1_TSTI_TX_DN	usdhc2.TESTER_TRIGGER	usdhc2.WP	Keeper
UART1_RTS	gpio1.IO[19]	uart1.RTS_B	enet1.TX_ER	usdhc1.CD_B	csi.DATA[5]	enet2.1588_EVENT1_OUT	gpio1.IO[19]	anatop.USBPHY1_TSTO_RX_SQUELCH	qspi.TESTER_TRIGGER	usdhc2.CD_B	Keeper
UART2_TXD	gpio1.IO[20]	uart2.TX	enet1.TDATA[2]	i2c4.SCL	csi.DATA[6]	gpt1.CAPTURE1	gpio1.IO[20]	anatop.USBPHY1_TSTO_RX_DISCON_DET	rawnand.TESTER_TRIGGER	ecspi3.SS0	Keeper
UART2_RXD	gpio1.IO[21]	uart2.RX	enet1.TDATA[3]	i2c4.SDA	csi.DATA[7]	gpt1.CAPTURE2	gpio1.IO[21]	anatop.USBPHY1_TSTO_RX_HS_RXD	sjc.DONE	ecspi3.SCLK	Keeper
UART2_CTS	gpio1.IO[22]	uart2.CTS_B	enet1.CRS	can2.TX	csi.DATA[8]	gpt1.COMPARE2	gpio1.IO[22]	anatop.USBPHY2_TSTO_RX_FS_RXD	sjc.DE_B	ecspi3.MOSI	Keeper
UART2_RTS	gpio1.IO[23]	uart2.RTS_B	enet1.COL	can2.RX	csi.DATA[9]	gpt1.COMPARE3	gpio1.IO[23]	anatop.USBPHY1_TSTO_RX_FS_RXD	sjc.FAIL	ecspi3.MISO	Keeper
UART3_TXD	gpio1.IO[24]	uart3.TX	enet2.RDATA[2]	sim1.PORT0_PD	csi.DATA[1]	uart2.CTS_B	gpio1.IO[24]	anatop.USBPHY1_TSTI_TX_DP	sjc.JTAG_ACT	anatop.OTG1_ID	Keeper
UART3_RXD	gpio1.IO[25]	uart3.RX	enet2.RDATA[3]	sim2.PORT0_PD	csi.DATA[0]	uart2.RTS_B	gpio1.IO[25]	anatop.USBPHY1_TSTI_TX_EN	sim_m.HADDR[0]	epit1.OUT	Keeper
UART3_CTS	gpio1.IO[26]	uart3.CTS_B	enet2.RX_CLK	can1.TX	csi.DATA[10]	enet1.1588_EVENT1_IN	gpio1.IO[26]	anatop.USBPHY1_TSTI_TX_HIZ	sim_m.HADDR[1]	epit2.OUT	Keeper
UART3_RTS	gpio1.IO[27]	uart3.RTS_B	enet2.TX_ER	can1.RX	csi.DATA[11]	enet1.1588_EVENT1_OUT	gpio1.IO[27]	anatop.USBPHY2_TSTO_RX_HS_RXD	sim_m.HADDR[2]	wdog1.WDOG_B	Keeper
UART4_TXD	gpio1.IO[28]	uart4.TX	enet2.TDATA[2]	i2c1.SCL	csi.DATA[12]	csu.CSU_ALARM_AUT[2]	gpio1.IO[28]	anatop.USBPHY1_TSTO_PLL_CLK20DIV	sim_m.HADDR[3]	ecspi2.SCLK	Keeper
UART4_RXD	gpio1.IO[29]	uart4.RX	enet2.TDATA[3]	i2c1.SDA	csi.DATA[13]	csu.CSU_ALARM_AUT[1]	gpio1.IO[29]	anatop.USBPHY2_TSTO_PLL_CLK20DIV	sim_m.HADDR[4]	ecspi2.SS0	Keeper
UART5_TXD	gpio1.IO[30]	uart5.TX	enet2.CRS	i2c2.SCL	csi.DATA[14]	csu.CSU_ALARM_AUT[0]	gpio1.IO[30]	anatop.USBPHY2_TSTO_RX_SQUELCH	sim_m.HADDR[5]	ecspi2.MOSI	Keeper
UART5_RXD	gpio1.IO[31]	uart5.RX	enet2.COL	i2c2.SDA	csi.DATA[15]	csu.CSU_INT_DEB	gpio1.IO[31]	anatop.USBPHY2_TSTO_RX_DISCON_DET	sim_m.HADDR[6]	ecspi2.MISO	Keeper
ENET1_RXD0	gpio2.IO[0]	enet1.RDATA[0]	uart4.RTS_B	pwm1.OUT	csi.DATA[16]	can1.TX	gpio2.IO[0]	kpp.ROW[0]	sim_m.HADDR[7]	usdhc1.LCTL	Keeper
ENET1_RXD1	gpio2.IO[1]	enet1.RDATA[1]	uart4.CTS_B	pwm2.OUT	csi.DATA[17]	can1.RX	gpio2.IO[1]	kpp.COL[0]	sim_m.HADDR[8]	usdhc2.LCTL	Keeper
ENET1_CRS_DV	gpio2.IO[2]	enet1.RX_EN	uart5.RTS_B	osc32k.32K_OUT	csi.DATA[18]	can2.TX	gpio2.IO[2]	kpp.ROW[1]	sim_m.HADDR[9]	usdhc1.VSELECT	Keeper
ENET1_TXD0	gpio2.IO[3]	enet1.TDATA[0]	uart5.CTS_B	anatop.24M_OUT	csi.DATA[19]	can2.RX	gpio2.IO[3]	kpp.COL[1]	sim_m.HADDR[10]	usdhc2.VSELECT	Keeper
ENET1_TXD1	gpio2.IO[4]	enet1.TDATA[1]	uart6.CTS_B	pwm5.OUT	csi.DATA[20]	enet2.MDIO	gpio2.IO[4]	kpp.ROW[2]	sim_m.HADDR[11]	wdog1.WDOG_RST_B_DEB	Keeper
ENET1_TXEN	gpio2.IO[5]	enet1.TX_EN	uart6.RTS_B	pwm6.OUT	csi.DATA[21]	enet2.MDC	gpio2.IO[5]	kpp.COL[2]	sim_m.HADDR[12]	wdog2.WDOG_RST_B_DEB	Keeper
ENET1_TXCLK	gpio2.IO[6]	enet1.TX_CLK	uart7.CTS_B	pwm7.OUT	csi.DATA[22]	anatop.ENET_REF_CLK1	gpio2.IO[6]	kpp.ROW[3]	sim_m.HADDR[13]	gpt1.CLK	Keeper
ENET1_RXER	gpio2.IO[7]	enet1.RX_ER	uart7.RTS_B	pwm8.OUT	csi.DATA[23]	weim.CRE	gpio2.IO[7]	kpp.COL[3]	sim_m.HADDR[14]	gpt1.CAPTURE2	Keeper
ENET2_RXD0	gpio2.IO[8]	enet2.RDATA[0]	uart6.TX	sim1.PORT0_TRXD	i2c3.SCL	enet1.MDIO	gpio2.IO[8]	kpp.ROW[4]	sim_m.HADDR[15]	usb.OTG1_PWR	Keeper
ENET2_RXD1	gpio2.IO[9]	enet2.RDATA[1]	uart6.RX	sim1.PORT0_CLK	i2c3.SDA	enet1.MDC	gpio2.IO[9]	kpp.COL[4]	sim_m.HADDR[16]	usb.OTG1_OC	Keeper
ENET2_CRS_DV	gpio2.IO[10]	enet2.RX_EN	uart7.TX	sim1.PORT0_RST_B	i2c4.SCL	weim.ADDR[26]	gpio2.IO[10]	kpp.ROW[5]	sim_m.HADDR[17]	anatop.ENET_REF_CLK_25M	Keeper
ENET2_TXD0	gpio2.IO[11]	enet2.TDATA[0]	uart7.RX	sim1.PORT0_SVEN	i2c4.SDA	weim.EB_B[2]	gpio2.IO[11]	kpp.COL[5]	sim_m.HADDR[18]	anatop.24M_OUT	Keeper
ENET2_TXD1	gpio2.IO[12]	enet2.TDATA[1]	uart8.TX	sim2.PORT0_TRXD	ecspi4.SCLK	weim.EB_B[3]	gpio2.IO[12]	kpp.ROW[6]	sim_m.HADDR[19]	usb.OTG2_PWR	Keeper
ENET2_TXEN	gpio2.IO[13]	enet2.TX_EN	uart8.RX	sim2.PORT0_CLK	ecspi4.MOSI	weim.ACLK_FREERUN	gpio2.IO[13]	kpp.COL[6]	sim_m.HADDR[20]	usb.OTG2_OC	Keeper
ENET2_TXCLK	gpio2.IO[14]	enet2.TX_CLK	uart8.CTS_B	sim2.PORT0_RST_B	ecspi4.MISO	anatop.ENET_REF_CLK2	gpio2.IO[14]	kpp.ROW[7]	sim_m.HADDR[21]	anatop.OTG2_ID	Keeper
ENET2_RXER	gpio2.IO[15]	enet2.RX_ER	uart8.RTS_B	sim2.PORT0_SVEN	ecspi4.SS0	weim.ADDR[25]	gpio2.IO[15]	kpp.COL[7]	sim_m.HADDR[22]	global wdog	Keeper
LCD_CLK	gpio3.IO[0]	lcdif.CLK	lcdif.WR_RWN	uart4.TX	sai3.MCLK	weim.CS2_B	gpio3.IO[0]	ocotp_ctrl_wrapper.FUSE_LATCHED	sim_m.HADDR[23]	wdog1.WDOG_RST_B_DEB	Keeper
LCD_ENABLE	gpio3.IO[1]	lcdif.ENABLE	lcdif.RD_E	uart4.RX	sai3.TX_SYNC	weim.CS3_B	gpio3.IO[1]	anatop.TESTI[0]	sim_m.HADDR[24]	ecspi2.RDY	Keeper
LCD_HSYNC	gpio3.IO[2]	lcdif.HSYNC	lcdif.RS	uart4.CTS_B	sai3.TX_BCLK	wdog3.WDOG_RST_B_DEB	gpio3.IO[2]	anatop.TESTI[1]	sim_m.HADDR[25]	ecspi2.SS1	Keeper
LCD_VSYNC	gpio3.IO[3]	lcdif.VSYNC	lcdif.BUSY	uart4.RTS_B	sai3.RX_DATA	wdog2.WDOG_B	gpio3.IO[3]	anatop.TESTI[2]	sim_m.HADDR[26]	ecspi2.SS2	Keeper
LCD_RESET	gpio3.IO[4]	lcdif.RESET	lcdif.CS	ca7_platform.EVENTI	sai3.TX_DATA	global wdog	gpio3.IO[4]	anatop.TESTI[3]	sim_m.HADDR[27]	ecspi2.SS3	Keeper
LCD_DATA00	gpio3.IO[5]	lcdif.DATA[0]	pwm1.OUT	ca7_platform.TRACE[0]	enet1.1588_EVENT2_IN	i2c3.SDA	gpio3.IO[5]	src.BT_CFG[0]	sim_m.HADDR[28]	sai1.MCLK	Keeper
LCD_DATA01	gpio3.IO[6]	lcdif.DATA[1]	pwm2.OUT	ca7_platform.TRACE[1]	enet1.1588_EVENT2_OUT	i2c3.SCL	gpio3.IO[6]	src.BT_CFG[1]	sim_m.HADDR[29]	sai1.TX_SYNC	Keeper
LCD_DATA02	gpio3.IO[7]	lcdif.DATA[2]	pwm3.OUT	ca7_platform.TRACE[2]	enet1.1588_EVENT3_IN	i2c4.SDA	gpio3.IO[7]	src.BT_CFG[2]	sim_m.HADDR[30]	sai1.TX_BCLK	Keeper
LCD_DATA03	gpio3.IO[8]	lcdif.DATA[3]	pwm4.OUT	ca7_platform.TRACE[3]	enet1.1588_EVENT3_OUT	i2c4.SCL	gpio3.IO[8]	src.BT_CFG[3]	sim_m.HADDR[31]	sai1.RX_DATA	Keeper
LCD_DATA04	gpio3.IO[9]	lcdif.DATA[4]	uart8.CTS_B	ca7_platform.TRACE[4]	enet2.1588_EVENT2_IN	spdif.SR_CLK	gpio3.IO[9]	src.BT_CFG[4]	sim_m.HBURST[0]	sai1.TX_DATA	Keeper
LCD_DATA05	gpio3.IO[10]	lcdif.DATA[5]	uart8.RTS_B	ca7_platform.TRACE[5]	enet2.1588_EVENT2_OUT	spdif.OUT	gpio3.IO[10]	src.BT_CFG[5]	sim_m.HBURST[1]	ecspi1.SS1	Keeper
LCD_DATA06	gpio3.IO[11]	lcdif.DATA[6]	uart7.CTS_B	ca7_platform.TRACE[6]	enet2.1588_EVENT3_IN	spdif.LOCK	gpio3.IO[11]	src.BT_CFG[6]	sim_m.HBURST[2]	ecspi1.SS2	Keeper
LCD_DATA07	gpio3.IO[12]	lcdif.DATA[7]	uart7.RTS_B	ca7_platform.TRACE[7]	enet2.1588_EVENT3_OUT	spdif.EXT_CLK	gpio3.IO[12]	src.BT_CFG[7]	sim_m.HMASTLOCK	ecspi1.SS3	Keeper
LCD_DATA08	gpio3.IO[13]	lcdif.DATA[8]	spdif.IN	ca7_platform.TRACE[8]	csi.DATA[16]	weim.DATA[0]	gpio3.IO[13]	src.BT_CFG[8]	sim_m.HPROT[0]	can1.TX	Keeper
LCD_DATA09	gpio3.IO[14]	lcdif.DATA[9]	sai3.MCLK	ca7_platform.TRACE[9]	csi.DATA[17]	weim.DATA[1]	gpio3.IO[14]	src.BT_CFG[9]	sim_m.HPROT[1]	can1.RX	Keeper
LCD_DATA10	gpio3.IO[15]	lcdif.DATA[10]	sai3.RX_SYNC	ca7_platform.TRACE[10]	csi.DATA[18]	weim.DATA[2]	gpio3.IO[15]	src.BT_CFG[10]	sim_m.HPROT[2]	can2.TX	Keeper
LCD_DATA11	gpio3.IO[16]	lcdif.DATA[11]	sai3.RX_BCLK	ca7_platform.TRACE[11]	csi.DATA[19]	weim.DATA[3]	gpio3.IO[16]	src.BT_CFG[11]	sim_m.HPROT[3]	can2.RX	Keeper
LCD_DATA12	gpio3.IO[17]	lcdif.DATA[12]	sai3.TX_SYNC	ca7_platform.TRACE[12]	csi.DATA[20]	weim.DATA[4]	gpio3.IO[17]	src.BT_CFG[12]	sim_m.HREADYOUT	ecspi1.RDY	Keeper
LCD_DATA13	gpio3.IO[18]	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[18]	src.BT_CFG[13]	sim_m.HRESP	usdhc2.RESET_B	Keeper
LCD_DATA14	gpio3.IO[19]	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[19]	src.BT_CFG[14]	sim_m.HSIZE[0]	usdhc2.DATA4	Keeper
LCD_DATA15	gpio3.IO[20]	lcdif.DATA[15]	sai3.TX_DATA	ca7_platform.TRACE[15]	csi.DATA[23]	weim.DATA[7]	gpio3.IO[20]	src.BT_CFG[15]	sim_m.HSIZE[1]	usdhc2.DATA5	Keeper
LCD_DATA16	gpio3.IO[21]	lcdif.DATA[16]	uart7.TX	ca7_platform.TRACE_CLK	csi.DATA[1]	weim.DATA[8]	gpio3.IO[21]	src.BT_CFG[24]	sim_m.HSIZE[2]	usdhc2.DATA6	Keeper
LCD_DATA17	gpio3.IO[22]	lcdif.DATA[17]	uart7.RX	ca7_platform.TRACE_CTL	csi.DATA[0]	weim.DATA[9]	gpio3.IO[22]	src.BT_CFG[25]	sim_m.HWRITE	usdhc2.DATA7	Keeper
LCD_DATA18	gpio3.IO[23]	lcdif.DATA[18]	pwm5.OUT	ca7_platform.EVENTO	csi.DATA[10]	weim.DATA[10]	gpio3.IO[23]	src.BT_CFG[26]	tpsmp.CLK	usdhc2.CMD	Keeper
LCD_DATA19	gpio3.IO[24]	lcdif.DATA[19]	pwm6.OUT	global wdog	csi.DATA[11]	weim.DATA[11]	gpio3.IO[24]	src.BT_CFG[27]	tpsmp.HDATA_DIR	usdhc2.CLK	Keeper
LCD_DATA20	gpio3.IO[25]	lcdif.DATA[20]	uart8.TX	ecspi1.SCLK	csi.DATA[12]	weim.DATA[12]	gpio3.IO[25]	src.BT_CFG[28]	tpsmp.HTRANS[0]	usdhc2.DATA0	Keeper
LCD_DATA21	gpio3.IO[26]	lcdif.DATA[21]	uart8.RX	ecspi1.SS0	csi.DATA[13]	weim.DATA[13]	gpio3.IO[26]	src.BT_CFG[29]	tpsmp.HTRANS[1]	usdhc2.DATA1	Keeper
LCD_DATA22	gpio3.IO[27]	lcdif.DATA[22]	mqs.RIGHT	ecspi1.MOSI	csi.DATA[14]	weim.DATA[14]	gpio3.IO[27]	src.BT_CFG[30]	tpsmp.HDATA[0]	usdhc2.DATA2	Keeper
LCD_DATA23	gpio3.IO[28]	lcdif.DATA[23]	mqs.LEFT	ecspi1.MISO	csi.DATA[15]	weim.DATA[15]	gpio3.IO[28]	src.BT_CFG[31]	tpsmp.HDATA[1]	usdhc2.DATA3	Keeper
NAND_RE_B	gpio4.IO[0]	rawnand.RE_B	usdhc2.CLK	qspiB_SCLK	kpp.ROW[0]	weim.EB_B[0]	gpio4.IO[0]	anatop.TESTO[0]	tpsmp.HDATA[2]	ecspi3.SS2	Keeper
NAND_WE_B	gpio4.IO[1]	rawnand.WE_B	usdhc2.CMD	qspiB_SS0_B	kpp.COL[0]	weim.EB_B[1]	gpio4.IO[1]	anatop.TESTO[1]	tpsmp.HDATA[3]	ecspi3.SS3	Keeper
NAND_DATA00	gpio4.IO[2]	rawnand.DATA00	usdhc2.DATA0	qspiB_SS1_B	kpp.ROW[1]	weim.AD[8]	gpio4.IO[2]	anatop.TESTO[2]	tpsmp.HDATA[4]	ecspi4.RDY	Keeper
NAND_DATA01	gpio4.IO[3]	rawnand.DATA01	usdhc2.DATA1	qspiB_DQS	kpp.COL[1]	weim.AD[9]	gpio4.IO[3]	anatop.TESTO[3]	tpsmp.HDATA[5]	ecspi4.SS1	Keeper
NAND_DATA02	gpio4.IO[4]	rawnand.DATA02	usdhc2.DATA2	qspiB_DATA[0]	kpp.ROW[2]	weim.AD[10]	gpio4.IO[4]	anatop.TESTO[4]	tpsmp.HDATA[6]	ecspi4.SS2	Keeper
NAND_DATA03	gpio4.IO[5]	rawnand.DATA03	usdhc2.DATA3	qspiB_DATA[1]	kpp.COL[2]	weim.AD[11]	gpio4.IO[5]	anatop.TESTO[5]	tpsmp.HDATA[7]	ecspi4.SS3	Keeper
NAND_DATA04	gpio4.IO[6]	rawnand.DATA04	usdhc2.DATA4	qspiB_DATA[2]	ecspi4.SCLK	weim.AD[12]	gpio4.IO[6]	anatop.TESTO[6]	tpsmp.HDATA[8]	uart2.TX	Keeper
NAND_DATA05	gpio4.IO[7]	rawnand.DATA05	usdhc2.DATA5	qspiB_DATA[3]	ecspi4.MOSI	weim.AD[13]	gpio4.IO[7]	anatop.TESTO[7]	tpsmp.HDATA[9]	uart2.RX	Keeper
NAND_DATA06	gpio4.IO[8]	rawnand.DATA06	usdhc2.DATA6	sai2.RX_BCLK	ecspi4.MISO	weim.AD[14]	gpio4.IO[8]	anatop.TESTO[8]	tpsmp.HDATA[10]	uart2.CTS_B	Keeper
NAND_DATA07	gpio4.IO[9]	rawnand.DATA07	usdhc2.DATA7	qspiA_SS1_B	ecspi4.SS0	weim.AD[15]	gpio4.IO[9]	anatop.TESTO[9]	tpsmp.HDATA[11]	uart2.RTS_B	Keeper
NAND_ALE	gpio4.IO[10]	rawnand.ALE	usdhc2.RESET_B	qspiA_DQS	pwm3.OUT	weim.ADDR[17]	gpio4.IO[10]	anatop.TESTO[10]	tpsmp.HDATA[12]	ecspi3.SS1	Keeper
NAND_WP_B	gpio4.IO[11]	rawnand.WP_B	usdhc1.RESET_B	qspiA_SCLK	pwm4.OUT	weim.BCLK	gpio4.IO[11]	anatop.TESTO[11]	tpsmp.HDATA[13]	ecspi3.RDY	Keeper
NAND_READY_B	gpio4.IO[12]	rawnand.READY_B	usdhc1.DATA4	qspiA_DATA[0]	ecspi3.SS0	weim.CS1_B	gpio4.IO[12]	anatop.TESTO[12]	tpsmp.HDATA[14]	uart3.TX	Keeper
NAND_CE0_B	gpio4.IO[13]	rawnand.CE0_B	usdhc1.DATA5	qspiA_DATA[1]	ecspi3.SCLK	weim.DTACK_B	gpio4.IO[13]	anatop.TESTO[13]	tpsmp.HDATA[15]	uart3.RX	Keeper
NAND_CE1_B	gpio4.IO[14]	rawnand.CE1_B	usdhc1.DATA6	qspiA_DATA[2]	ecspi3.MOSI	weim.ADDR[18]	gpio4.IO[14]	anatop.TESTO[14]	tpsmp.HDATA[16]	uart3.CTS_B	Keeper
NAND_CLE	gpio4.IO[15]	rawnand.CLE	usdhc1.DATA7	qspiA_DATA[3]	ecspi3.MISO	weim.ADDR[16]	gpio4.IO[15]	anatop.TESTO[15]	tpsmp.HDATA[19]	uart3.RTS_B	Keeper
NAND_DQS	gpio4.IO[16]	rawnand.DQS	csi.FIELD	qspiA_SS0_B	pwm5.OUT	weim.WAIT	gpio4.IO[16]	sdma.EXT_EVENT[1]	tpsmp.HDATA[17]	spdif.EXT_CLK	Keeper
SD1_CMD	gpio2.IO[16]	usdhc1.CMD	gpt2.COMPARE1	sai2.RX_SYNC	spdif.OUT	weim.ADDR[19]	gpio2.IO[16]	sdma.EXT_EVENT[0]	tpsmp.HDATA[18]	usb.OTG1_PWR	Keeper
SD1_CLK	gpio2.IO[17]	usdhc1.CLK	gpt2.COMPARE2	sai2.MCLK	spdif.IN	weim.ADDR[20]	gpio2.IO[17]	ccm.OUT0	observe_mux.OUT[0]	usb.OTG1_OC	Keeper
SD1_DATA0	gpio2.IO[18]	usdhc1.DATA0	gpt2.COMPARE3	sai2.TX_SYNC	can1.TX	weim.ADDR[21]	gpio2.IO[18]	ccm.OUT1	observe_mux.OUT[1]	anatop.OTG1_ID	Keeper
SD1_DATA1	gpio2.IO[19]	usdhc1.DATA1	gpt2.CLK	sai2.TX_BCLK	can1.RX	weim.ADDR[22]	gpio2.IO[19]	ccm.OUT2	observe_mux.OUT[2]	usb.OTG2_PWR	Keeper
SD1_DATA2	gpio2.IO[20]	usdhc1.DATA2	gpt2.CAPTURE1	sai2.RX_DATA	can2.TX	weim.ADDR[23]	gpio2.IO[20]	ccm.CLKO1	observe_mux.OUT[3]	usb.OTG2_OC	Keeper
SD1_DATA3	gpio2.IO[21]	usdhc1.DATA3	gpt2.CAPTURE2	sai2.TX_DATA	can2.RX	weim.ADDR[24]	gpio2.IO[21]	ccm.CLKO2	observe_mux.OUT[4]	anatop.OTG2_ID	Keeper
CSI_MCLK	gpio4.IO[17]	csi.MCLK	usdhc2.CD_B	rawnand.CE2_B	i2c1.SDA	weim.CS0_B	gpio4.IO[17]	snvs_hp_wrapper.VIO_5_CTL	tpsmp.HDATA[20]	uart6.TX	Keeper
CSI_PIXCLK	gpio4.IO[18]	csi.PIXCLK	usdhc2.WP	rawnand.CE3_B	i2c1.SCL	weim.OE	gpio4.IO[18]	snvs_hp_wrapper.VIO_5	tpsmp.HDATA[21]	uart6.RX	Keeper
CSI_VSYNC	gpio4.IO[19]	csi.VSYNC	usdhc2.CLK	sim1.PORT1_CLK	i2c2.SDA	weim.RW	gpio4.IO[19]	pwm7.OUT	tpsmp.HDATA[22]	uart6.RTS_B	Keeper
CSI_HSYNC	gpio4.IO[20]	csi.HSYNC	usdhc2.CMD	sim1.PORT1_PD	i2c2.SCL	weim.LBA_B	gpio4.IO[20]	pwm8.OUT	tpsmp.HDATA[23]	uart6.CTS_B	Keeper
CSI_DATA00	gpio4.IO[21]	csi.DATA[2]	usdhc2.DATA0	sim1.PORT1_RST_B	ecspi2.SCLK	weim.AD[0]	gpio4.IO[21]	src.INT_BOOT	tpsmp.HDATA[24]	uart5.TX	Keeper
CSI_DATA01	gpio4.IO[22]	csi.DATA[3]	usdhc2.DATA1	sim1.PORT1_SVEN	ecspi2.SS0	weim.AD[1]	gpio4.IO[22]	sai1.MCLK	tpsmp.HDATA[25]	uart5.RX	Keeper
CSI_DATA02	gpio4.IO[23]	csi.DATA[4]	usdhc2.DATA2	sim1.PORT1_TRXD	ecspi2.MOSI	weim.AD[2]	gpio4.IO[23]	sai1.RX_SYNC	tpsmp.HDATA[26]	uart5.RTS_B	Keeper
CSI_DATA03	gpio4.IO[24]	csi.DATA[5]	usdhc2.DATA3	sim2.PORT1_PD	ecspi2.MISO	weim.AD[3]	gpio4.IO[24]	sai1.RX_BCLK	tpsmp.HDATA[27]	uart5.CTS_B	Keeper
CSI_DATA04	gpio4.IO[25]	csi.DATA[6]	usdhc2.DATA4	sim2.PORT1_CLK	ecspi1.SCLK	weim.AD[4]	gpio4.IO[25]	sai1.TX_SYNC	tpsmp.HDATA[28]	usdhc1.WP	Keeper
CSI_DATA05	gpio4.IO[26]	csi.DATA[7]	usdhc2.DATA5	sim2.PORT1_RST_B	ecspi1.SS0	weim.AD[5]	gpio4.IO[26]	sai1.TX_BCLK	tpsmp.HDATA[29]	usdhc1.CD_B	Keeper
CSI_DATA06	gpio4.IO[27]	csi.DATA[8]	usdhc2.DATA6	sim2.PORT1_SVEN	ecspi1.MOSI	weim.AD[6]	gpio4.IO[27]	sai1.RX_DATA	tpsmp.HDATA[30]	usdhc1.RESET_B	Keeper
CSI_DATA07	gpio4.IO[28]	csi.DATA[9]	usdhc2.DATA7	sim2.PORT1_TRXD	ecspi1.MISO	weim.AD[7]	gpio4.IO[28]	sai1.TX_DATA	tpsmp.HDATA[31]	usdhc1.VSELECT	Keeper

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