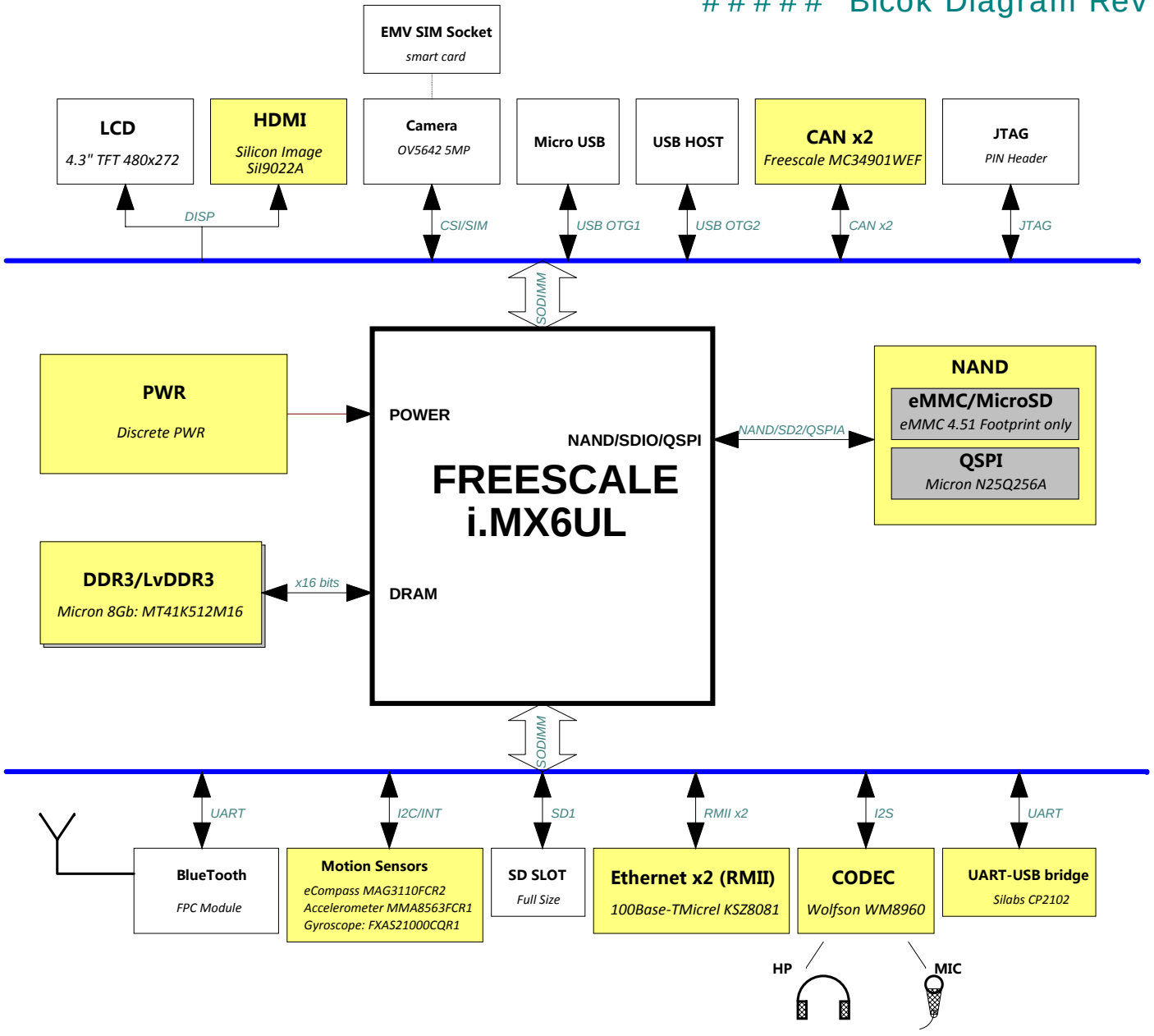
CM-i.MX6UL

Blcok Diagram Rev 1.0



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Title: Block Diagram		
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i.MX6UL EVK PWR TREE

WALL Adapter: 5V/3A

OVP

VSYS
5V/3A

MCIMX6UL-BB

Always ON
LDO
RICHTEK RT9169
3.3V/100mA Iq = 4uA
VDD_SNVS_IN

PMIC_ON_REQ
DC/DC BUCK
MPS MP2144
3.3V/2A Iq=40uA
VDD_HIGH_IN
DCDC_3V3

DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.275V/1A Iq=40uA
VDDARM_IN

DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.35V/1A Iq=40uA
VDD_MEM1V5

1.8V for eMMC HS200 mode
LDO
RICHTEK RT9169
1.8V/100mA Iq = 4uA

DCDC_3V3
HIGH PSRR LDO
RICHTEK RT9193
3.3V/300mA
VLDO_3V3

DCDC_3V3_PG
LDO
UNION UM1750S
1.8V/3.3V/300mA
NVCC_SD (3.3V/1.8V)

1.8V for CSI:
1.8V/3.3V for SIM
DCDC_3V3
LDO
UNION UM1750S
2.8V/300mA
NVCC_CSI (1.8V/3.3V)

USB_OTGx_PWR
LOAD SW
USB_OTG_VBUS
USB_HOST_VBUS

VDD_SNVS_IN
276uA
LDO_ARM_SOC
VDD_SNVS_CAP

LDO_1P1
NVCC_PLL

VDD_HIGH_IN
125mA
LDO_2P5
VDD_HIGH_CAP

NVCC_GPIO/NVCC_ENET/NVCC_LCDIF
NVCC_DRAM_2P5

VDD_SOC_IN
900mA
LDO_ARM_SOC
VDD_ARM_CAP
VDD_SOC_CAP

NVCC_DRAM
50mA
NVCC_NAND

FSL i.MX6UL CPU

VDDA_ADC_3P3
NVCC_SD
NVCC_CSI

50mA
USB_OTG1_VBUS
USB_OTG2_VBUS
LDO_USB
VDD_USB_CAP

LvDDR3
Micron: MT41K512M16

RGB LCD
TianMa TFT
VLCD_3V3
3.3V/23mA
5S2P
16V/25mA
BACKLIGHT
RICHTEK RT9293B
BLT_PWM

HDMI
SILICON IMAGE Sil9022A
VHDMI_3V3
3.3V/10mA
VLDO_1V2
1.2V/69.2mA
LDO
RICHTEK RT9169

Audio Codec
WM8960
VSPK_5V
5V/511mA
VAUD_3V3
3.3V/62.58mA

SENSOR
eCompass/
G-sensor/Gyroscope
VSENSOR_3V3
3.3V/6.9mA

CAN
FSL MC34901WEF
CAN_VIO_3V3
3.3V/1mA
CAN_VDD_5V
5V/65mA

Ethernet x2
Micrel KSZ8081RNB
VENET_3V3
3.3V/48.7mA
LOAD SW

Camera/EMV SIM
CSI B2B CN
DVDD1V5
AVDD_2V8
LDO
UNION UM1750S
1.5V/300mA

DCDC_3V3
3.3V/200mA
eMMC 4GB
Micron MTFC8GLCDM

NVCC_NAND
3.3V/1.8V
QSPI
Micron N25Q256

DCDC_3V3
3.3V/20mA

DCDC_3V3
3.3V/50mA
NAND
Micron MT29F32G08

MCIMX6UL-CM

USB_OTG_VBUS
USB OTG

USB_HOST_VBUS
USB HOST

SD1_nRST/POR_B
LOAD SW
SD Socket
BT MOD

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Title	PWR TREE	
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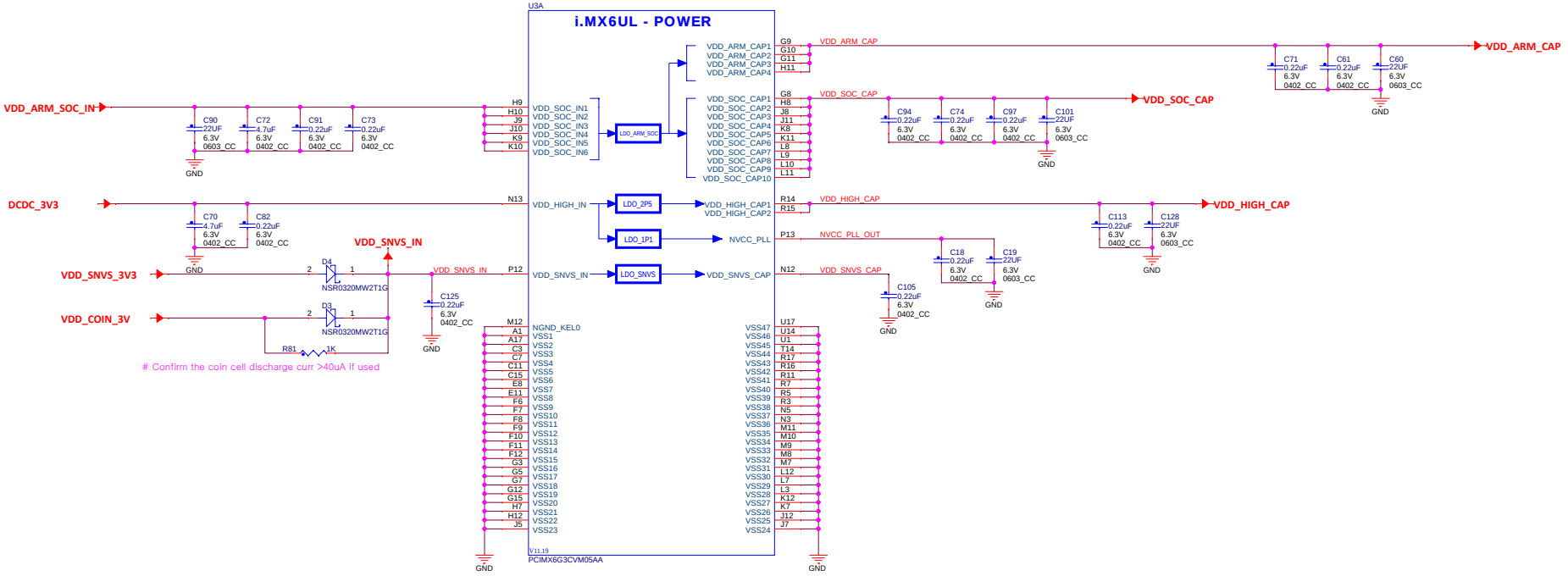
i.MX6UL PWR



Title	CPU PWR
Size	C
Document Number	CM-I.MX6ul
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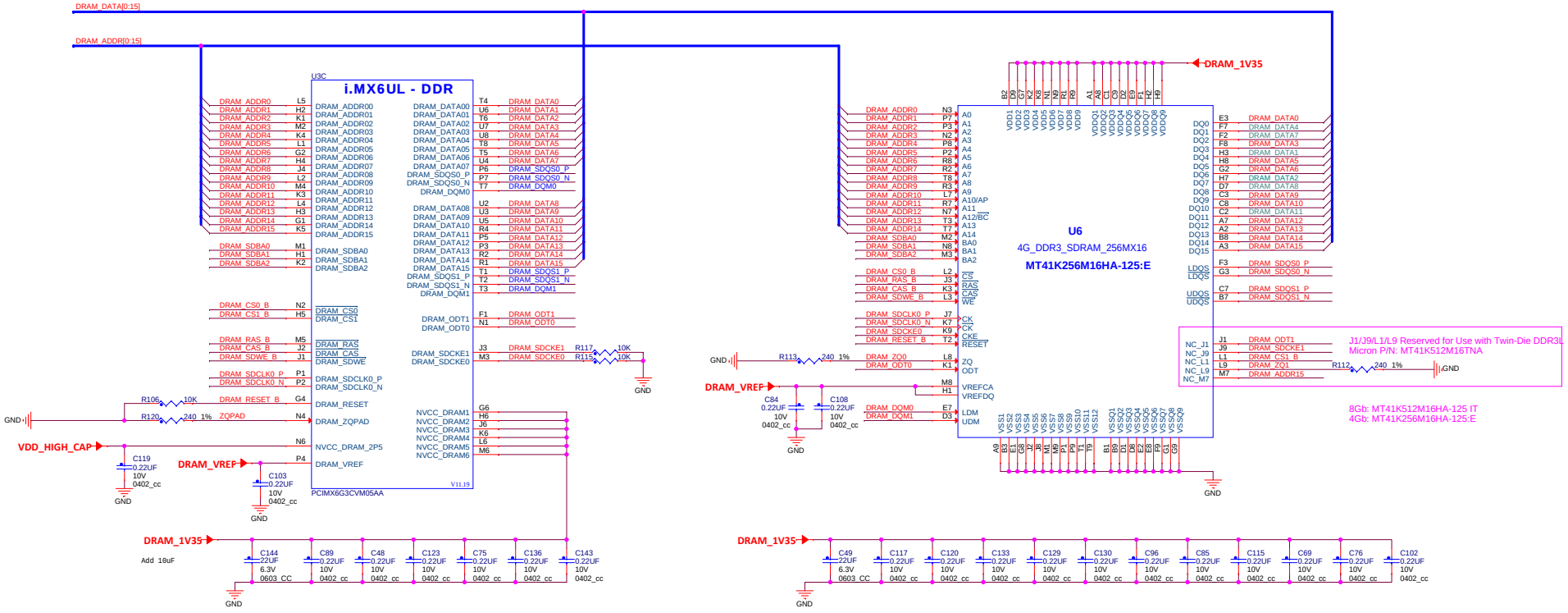
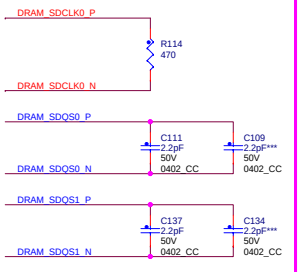
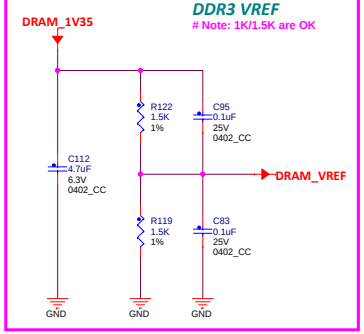
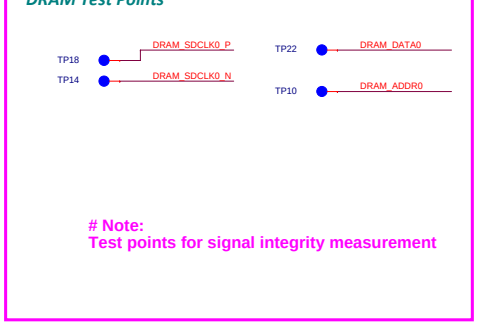
DDR3/LvDDR3



Note:
CLK termination: Place R54 close to U2.







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Title	DDR3	
Size C	Document Number CM-I.MX6ul	Rev V1.0
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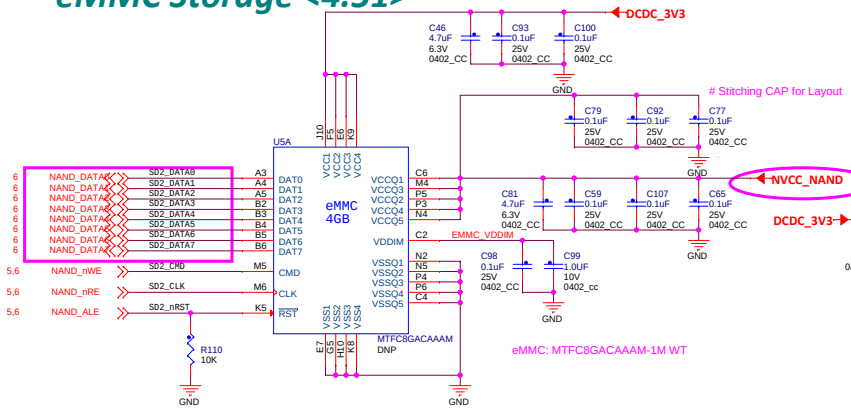
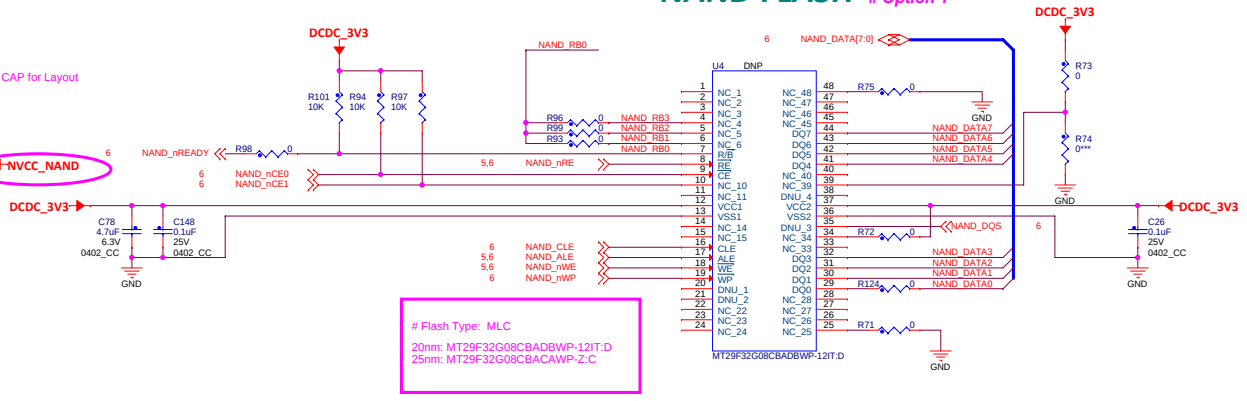
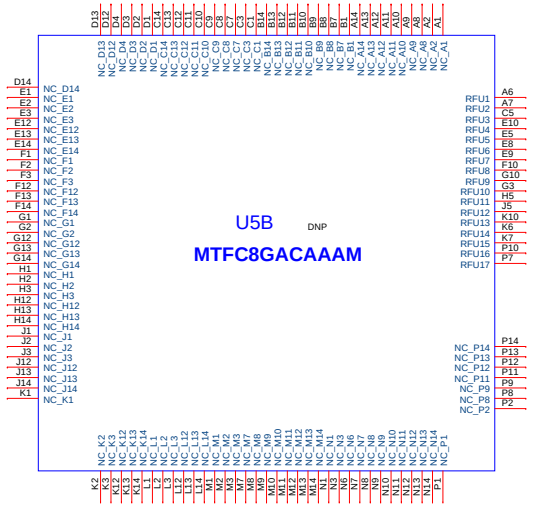
eMMC Storage <4.51>



NAND FLASH # Option 1





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Title: FLASH		
Size: C	Document Number: CM-I.MX6ul	Rev: V1.0
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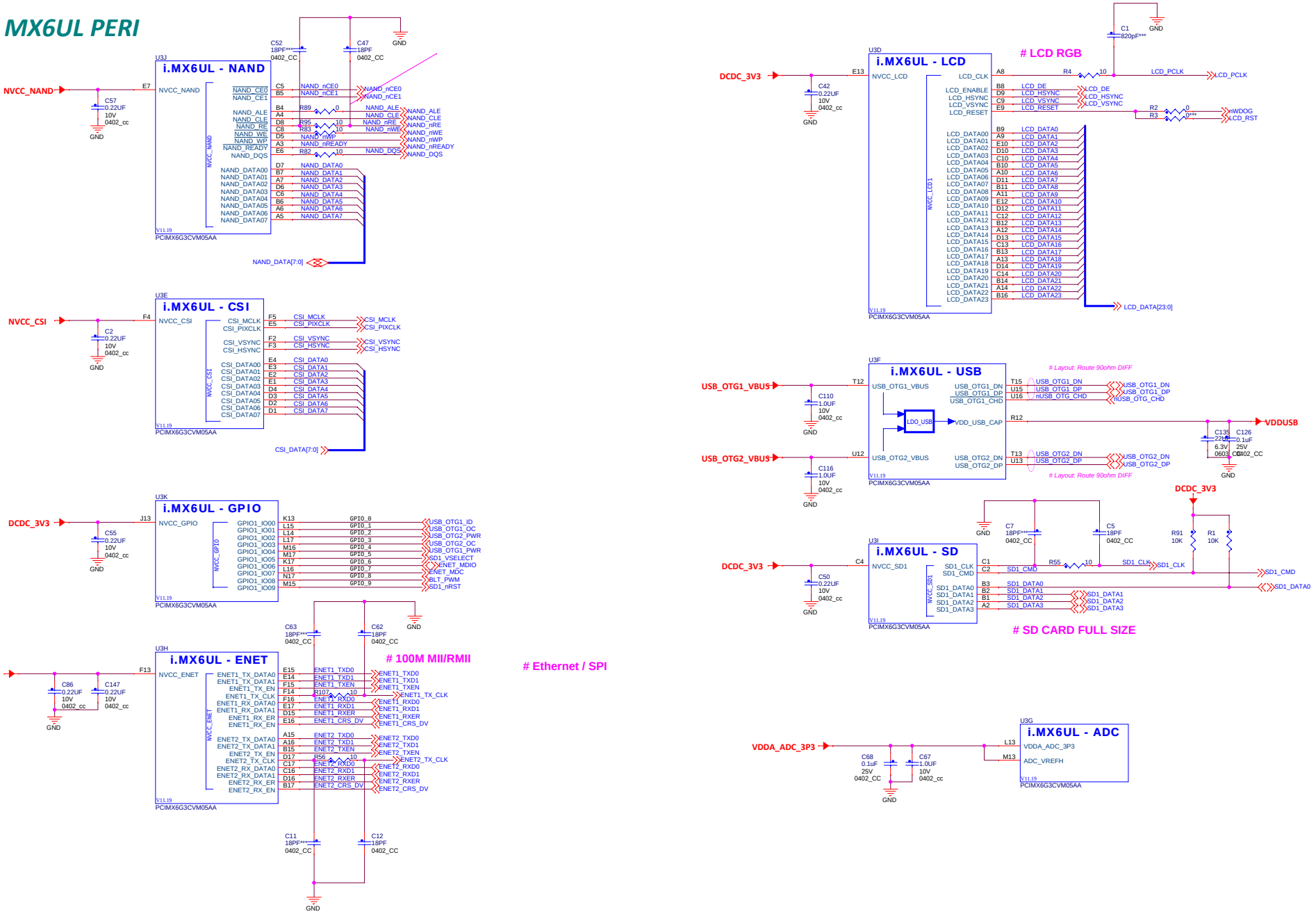
MX6UL PERI



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Title: CPU PREIX1		
Size: C	Document Number: CM-I.MX6ul	Rev: V1.0
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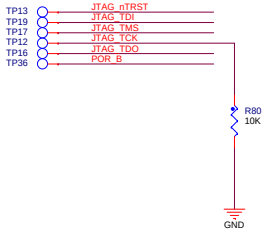
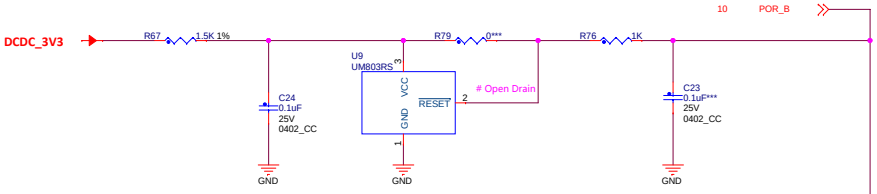
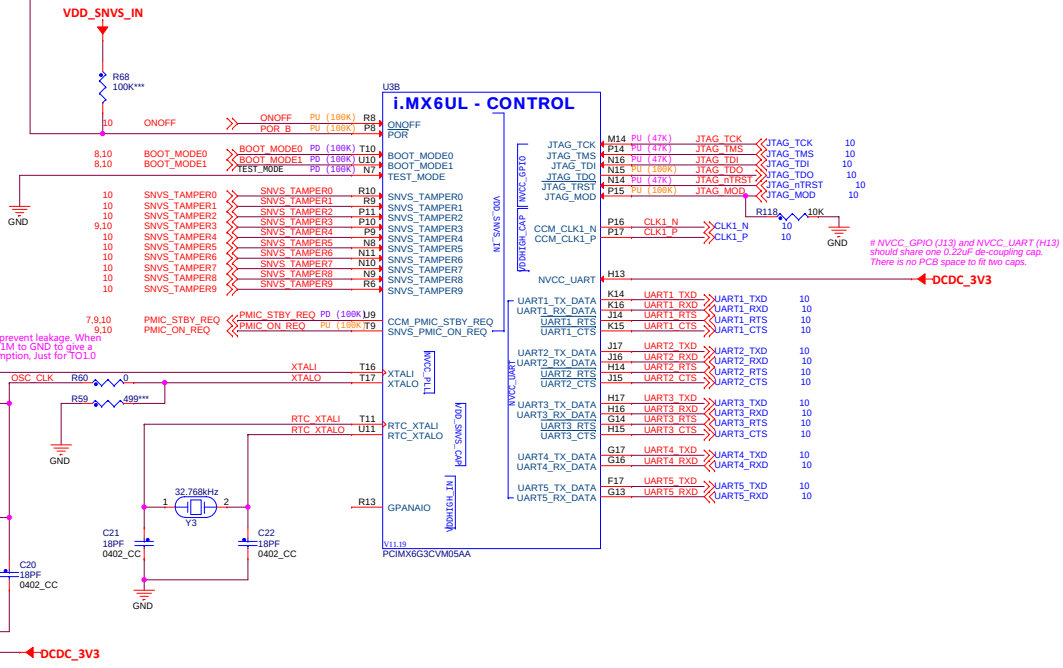
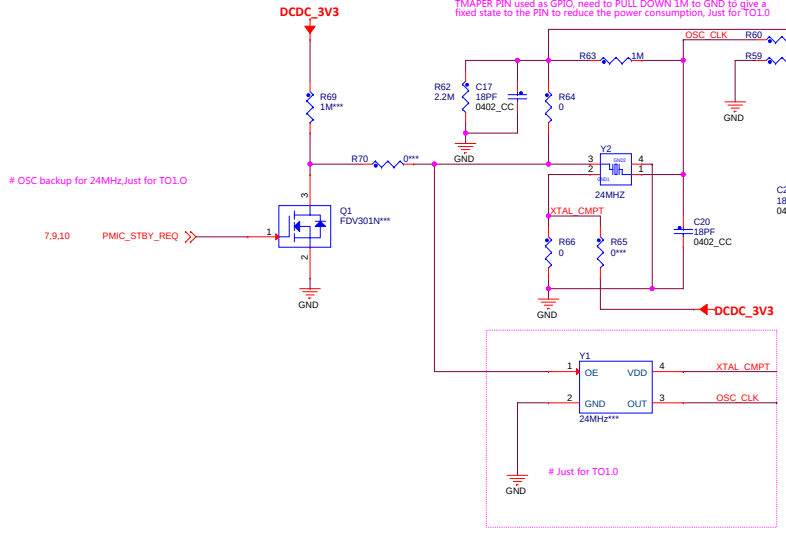
JTAG Debug



i.MX6UL RESET







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Title: CPU PERIX2			
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FUSE MAP

<Default: QSPI BOOT>

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
	0/1	0/1	0/1	1	0	0	0	0
QSPI	0	0	0	1	Reserved		DDRSMP: "000" : Default "001-111"	
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - Highl 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable "0" - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: (0) - 2 01 - 3 10 - 4 11 - 5	

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
	0	0	0	0	1	0	0	0
QSPI	Reserved	HSPHS: Half Speed Phase Selection '0': select sampling at non-inverted clock '1': select sampling at inverted clock	HSDLY: Half Speed Delay selection '0': one clock delay '1': two clock delay	FSPHS: Full Speed Phase Selection '0': select sampling at non-inverted clock '1': select sampling at inverted clock	FSDLY: Full Speed Delay selection '0': one clock delay '1': two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

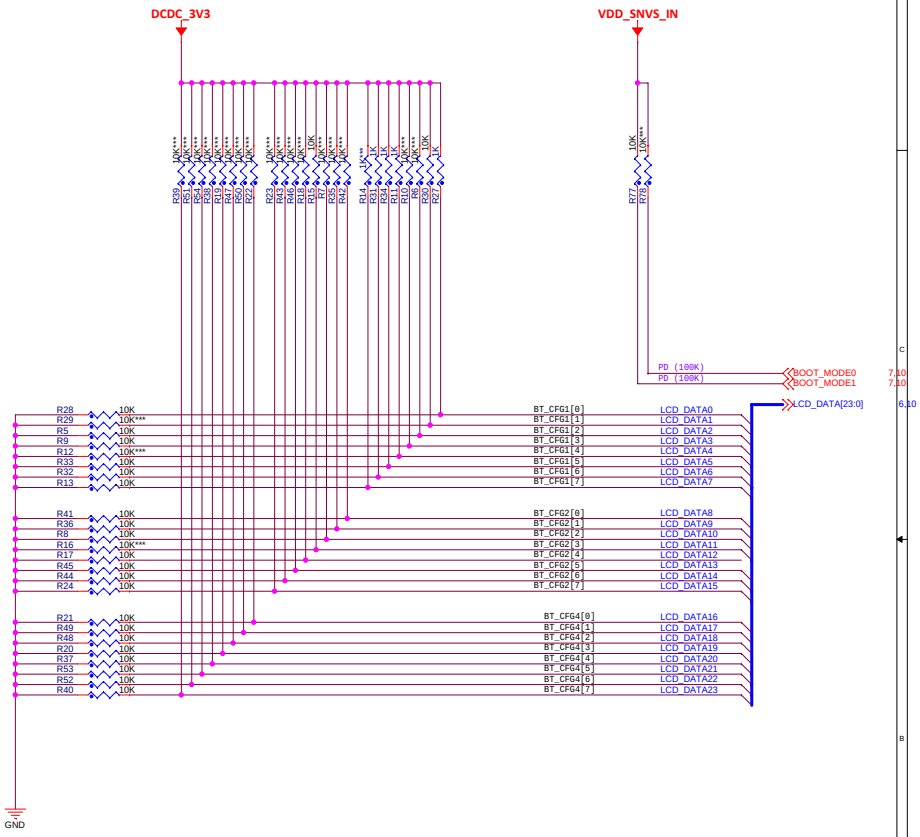
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
	0	0	0	0	0	0	0	0
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

NAND MT29F32G08CBACA

1 page = (4K + 224 bytes)
1 block = (4K + 224) bytes x 256 pages
= (1024K + 56K) bytes
1 plane = (1024K + 56K) bytes x 2048 blocks
= 17,280Mb
1 LUN = 17,280Mb x 2 planes
= 34,560Mb

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

Boot Configuration



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Title	BOOT CFG
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i.MX6UL PWR

Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				

DCDC_3V3 / VLDO_1V8 → R103 0 / R102 0*** → NVCC_NAND # 1.8V for eMMC HS200 mode

DCDC_3V3 / VLDO_1V8 → R25 0*** / R26 0*** → NVCC_CSI # CSI default 2.8V from the base board

DCDC_3V3 / VLDO_3V3 → R109 0*** / R111 0 → VDDA_ADC_3P3

SNVS

二这只焊其一

VSYS → C141 22UF 6.3V 0603_CC / C142 0.1uF 25V 0402_CC → U12 RT9169-33GVL (VIN, VOUT, GND) → DCDC_3V3 → R130 0*** → TP24 → C146 4.7uF 6.3V 0402_CC / C145 0.1uF 25V 0402_CC → VDD_SNVS_3V3 # 3.3V/100mA Iq = 4μA

RT9166-33GVL 静态电流大一些

ARM/SOC

Current 1A
I_Quiescent : 17μA

VSYS # 2.5V to 6V → C80 22UF 6.3V 0603_CC / C66 0.1uF 25V 0402_CC → U2 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) → L1 1uH → # 1.35V/1.05V/1.225V → TP1 → VDD_ARM_SOC_IN

DCDC_3V3_PG → R58 10K → EN

C64 0.1uF 25V 0402_CC

或者MP2144GJ

Vfb=0.6V / +-3%

Vo=Vfb*(R1+R2)/R2 = Vfb(1+R1/R2)

R1/R2 = (Vo-Vfb)/Vfb

1.4V: R1/R2 = 213K/160K
1.3V: R1/R2 = 186.7K/160K
0.925V: R1/R2 = 86.7K/160K

R57 215K / R85 147K / R86 1.5M → Q4 FDV301N / Q5 FDV301N → C6 22UF 6.3V 0603_CC / C8 0.1uF 25V 0402_CC → R84 51

DISCHG_EN → Q3 FDV301N → C58 1000pF 50V 0402_CC

1.035M OHM GPIO_DVFS → SNVS_TAMPER3
225K OHM PD (100K) → PMIC_STBY_REQ

TP9 → ARM_SOC_PG

R105 160K 1% / R104 100K*** / R100 100K

PMIC_STBY_REQ = 0, GPIO_DVFS = 0, output is 1.4V (1.375V + 25mV)
PMIC_STBY_REQ = 0, GPIO_DVFS = 1, output is 1.3V (1.275V + 25mV)
PMIC_STBY_REQ = 1, GPIO_DVFS = 0, output is 0.925V (0.9V + 25mV)

Important: GPIO_DVFS / PMIC_STBY_REQ should be PULL DN when system reboot to ensure the VDD_ARM_SOC_IN voltage is not effected by DVFS

VDDHIGH / NVCC_xxx

Current 2A
I_Quiescent : 40μA 或者MP2144GJ
DCDC_3V3

VSYS # 2.5V-to-5.5V → C121 22UF 6.3V 0603_CC / C114 0.1uF 25V 0402_CC / R125 100K*** → U7 MP2144GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) → L3 1uH → TP15 → VDD_SNVS_3V3

PMIC_ON_REQ → R61 10K → EN

C124 0.22UF 10V 0402_cc

PG pin is pulled up to VIN by the internal resistor 500K OHM

R1/R2 = 9/2

R121 180K 1% / R123 40.2K 1% → C13 22UF 6.3V 0603_CC / C16 0.1uF 25V 0402_CC

R108 51

R128 100K / R116 10K → Q6 FDV301N / Q7 FDV301N → C104 0.1uF 25V 0402_CC

DISCHG_EN

R127 0 / R131 0** → DCDC_3V3_PG → TP23 → C138 1000pF*** 50V 0402_CC / C139 1000pF*** 50V 0402_CC

R126 0***

Reset Button
MX6_POR_B → R132 100 → D2 NSR0320MW2T1G

GPIO/WDOG PWR OFF->ON
nWDOG → C132 1.0UF 10V 0402_cc → D1 NSR0320MW2T1G

U8 UM805RE (GND, RESET, MR, VCC) → VDD_SNVS_3V3

C140 1000pF 0402_CC / C131 0.1uF 25V 0402_CC

R129 1M

DCDC_3V3 → # Stitching CAP for Layout → C14 0.1uF 25V 0402_CC / C15 0.1uF 25V 0402_CC

ADC High PSRR

VSYS → U11 RT9193-33GB (VIN, VOUT, EN, GND, BP) → TP11 → VLDO_3V3

C127 22UF 6.3V 0603_CC / C118 0.1uF 25V 0402_CC

DCDC_3V3_PG → C122 1000pF*** 50V 0402_CC

C106 0.022UF 16V 0402_CC

C88 4.7uF 6.3V 0402_CC / C87 0.1uF 25V 0402_CC

1.8V PWR

DCDC_3V3 # RSV for eMMC HS200 → U10 RT9169-18GVL*** (VIN, VOUT, GND) → TP4 → VLDO_1V8 # 1.8V/200mA Iq = 1.2μA

C56 4.7uF*** 6.3V 0402_CC / C51 0.1uF*** 25V 0402_CC

C41 4.7uF*** 6.3V 0402_CC / C43 0.1uF*** 25V 0402_CC

LvDDR3

Current 1A
I_Quiescent : 17μA
DRAM_1V35

VSYS # 2.5V to 6V → C53 22UF 6.3V 0603_CC / C54 0.1uF 25V 0402_CC → U1 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) → L2 1uH → TP3

DCDC_3V3_PG → R88 10K → EN

C44 0.1uF 25V 0402_CC

或者MP2144GJ

Update to MP2159

R92 200K 1% / R87 160K 1% → C9 22UF 6.3V 0603_CC / C10 0.1uF 25V 0402_CC

R90 51

R1/R2 = 0.75/0.6

DISCHG_EN → Q2 FDV301N → C45 1000pF*** 50V 0402_CC

PG pin is pulled up to VIN by the internal resistor 550K OHM

TP8 → DRAM_PG

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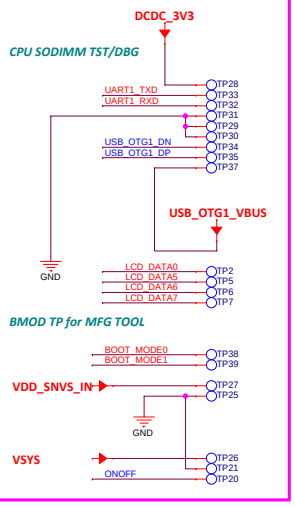
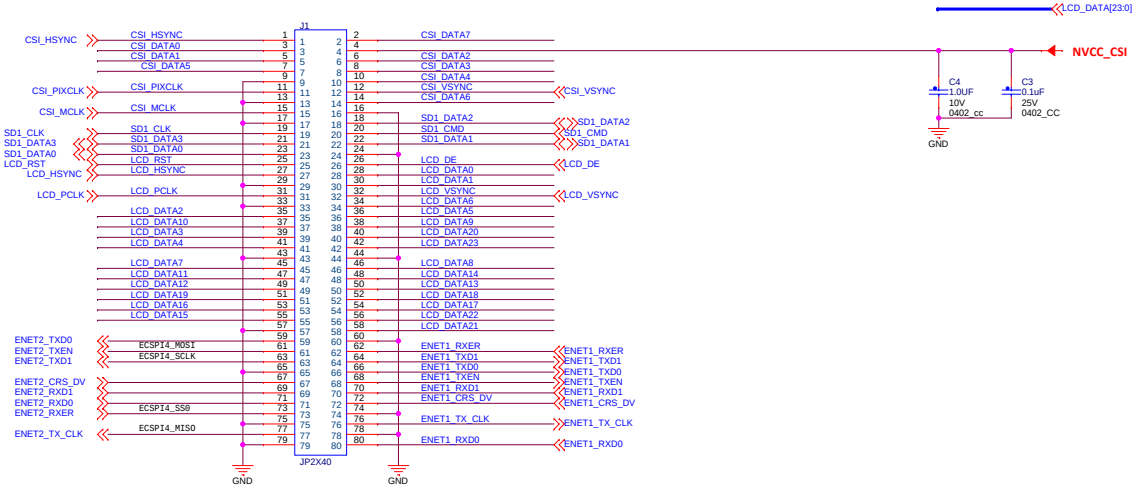
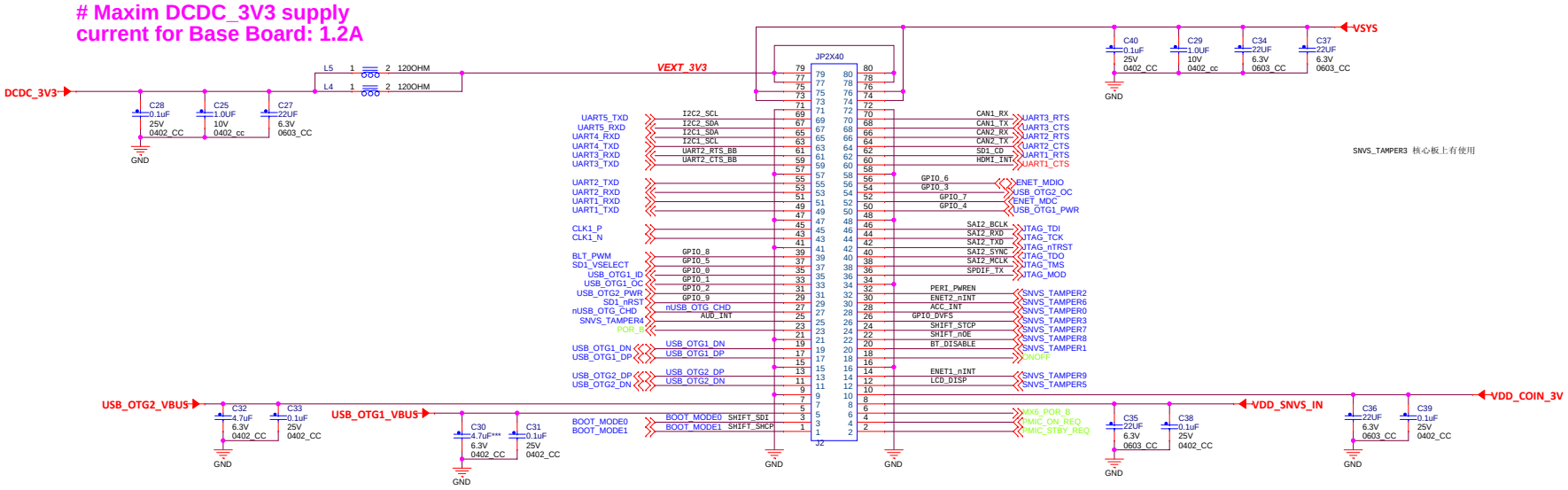
TP for SODIMM MFG



LCD_RST has been used as WDOG on CPU BOARD



Maxim DCDC_3V3 supply current for Base Board: 1.2A



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