B. We need a forwarding path MEM->MEM

ld r1 ... (r?) IF ID MEM EX WB

add r5, r4, r1 IF ID MEM EX WB

one path from the EXE to the EXE

add r2 r1 r3 IF ID MEM EXE WB

add r4, r2, r5 IF ID MEM EXE WB

one path from the Exe stage to the MEM one

[illegible] r2 r1 (r3) IF ID MEM EXE WB

and [illegible] r2 (r2) IF ID stall MEM EXE WB

[illegible] r1, r2, (r?) IF ID MEM EXE WB

add r2, r1, r6 IF ID MEM EXE WB

[illegible] r2, 0 (r?) IF ID MEM EXE WB

add r2, r1, r2 IF ID MEM EXE WB

[illegible] r1 r1 r2 IF ID stall MEM EXE WB

[illegible] r1, 0 (r2) IF stall ID stall MEM EXE WB

Q2 A · ASICs are hard to design but very power efficient

· Designing an application for a processor is [illegible] easier but less efficient

· ELM finds the middle ground

B 1. The largest portion (42%) of the required energy goes to the instruction supply, so by Amdahl's law it makes sense to optimize this

2. Dennard scaling does not help with energy usage [illegible] the energy remains fixed, while in the worst case (post-Dennard) it goes up by S^2

So the motivation is that it makes sense to improve the energy efficiency by using other ways

Q3 1. The general formula for the overall speedup is the following

$$\text{speedup} = \frac{\text{Execution time}_{old}}{\text{Execution time}_{new}} = \frac{1}{(1 - \text{Fraction}_{enhanced}) + \frac{\text{Fraction}_{enhanced}}{\text{Speedup}_{enhanced}}}$$

where the Fraction enhanced is the percentage of the process that gets improved and the Speedup enhanced is the individual speedup we have for this portion. [illegible] when there is a combination of more than one enhancements we end up having speedup =

$$\frac{1}{(1 - \text{fraction}_1 - \text{fraction}_2 - \ldots) + \frac{\text{fraction}_1}{\text{speedup}_1} + \frac{\text{fraction}_2}{\text{speedup}_2} + \ldots}$$

So: Speedup =

$$\frac{1}{(1 - 0.2 - 0.3) + \frac{0.2}{10} + \frac{0.3}{15}} = \frac{1}{0.5 + 0.02 + 0.02} = \frac{1}{0.54} \simeq 1.85$$

Since there is an upper [illegible] for speedup [illegible] that affects the [illegible] [illegible] [illegible] [illegible] enhancements

speedup [illegible]

[illegible]

B. Speedup $= \frac{1}{[illegible]} = \frac{1}{[illegible]} = \frac{1}{[illegible]} \simeq$ [illegible]

[illegible]

Q1 $S = {}^{45}/_{32} \cong 1.4$

1.1 $C_{final} = {}^{1}/_{S}\, C_{initial} = 0.71\, C_{init}$

1.2 $\frac{E_{final}}{E_{init}} = \frac{\frac{I_{final}}{C_{final} V_{dd}}}{\frac{I_{init}}{C_{init} V_{dd}}} = \frac{I_{final}\, C_{init}}{I_{init}\, C_{final}} = \frac{I_{final}\, C_{init}}{C_{init}\, \frac{1}{S}\, I_{init}} = \frac{\frac{W_{final}\, V_{dd}}{L_{final}}}{\frac{W_{init}\, V_{dd}}{L_{init}}}$ [illegible]

$= \frac{S \frac{1}{S} W_{init}\, L_{init}}{W_{init}\, \frac{1}{S} L_{init}} = S \cong 1.4$

1.3 $\frac{E_{final}}{E_{init}} = \frac{C V^2_{dd}}{C V^2_{dd}} = \frac{1}{S} \Rightarrow E_{final} = {}^{1}/_{S}\, E_{init} \cong 0.71\, E_{init}$

2.1. $E = \frac{L\sigma}{Lw}$ (1) $\frac{E_{final}}{E_{init}}$ (1) [illegible] $= S \cong 1.4$

2.2. $C = S \frac{Lw}{d}$ (2) $\frac{C_{final}}{C_{init}}$ (2) [illegible] $= {}^{1}/_{S} \cong 0.71$

2.3 [illegible] remains fixed [illegible] is proportional to [illegible] and C [illegible]

$E = CV^2$ (3) $\frac{E_{final}}{E_{init}} = \frac{E_{final}\, V^2}{C_{init}\, V^2} = {}^{1}/_{S} = 0.71$

According to (3) $E_{final} = S\, E_{init} = 1.4\, E_{init}$

So from (3) we had $E_{final} = E_{init}\, {}^{1}/_{S}$, the energy [illegible] of the frequency though, so it will remain: $E_{final} = {}^{1}/_{S}\, E_{init}$

$Area = W \cdot L$ (4) $\frac{Area_{final}}{Area_{init}} = \frac{W_{f}\, L_{f}}{W_{init}\, L_{init}} = \frac{1}{S} \cdot \frac{1}{S} = \frac{1}{S^2} \cong 0.5$

3.1. S^2 [illegible] $= 1.96 \cong 2$ [illegible] 7.84 So 7 cores will fit in total that is... 3 additional cores

$P = \frac{CV^2}{T} = CV^2 f$ By having $\frac{7}{4}$ more cores the power will get increased by $7/4$ as well

4.1. we assume that the [illegible] cores [illegible] were distributed like this: [illegible] and the [illegible] was passing through the [illegible] Bus [illegible] the [illegible] will [illegible] through central edge of each [illegible] we had the following [illegible] [illegible] area. The [illegible] [illegible] while the [illegible] area [illegible] as long

[illegible] $\frac{E_{f}}{E_{i}} = \frac{\frac{d}{d}}{C_{w}}$ [illegible] $= 2$ [illegible] $E = CV$ [illegible] $\frac{1}{S}\, E_{init}$

[illegible] $\frac{E_{d}\, delay}{B_{i}\, delay} = 1.4$ [illegible] $= 4$ [illegible] delay is [illegible] times as [illegible]