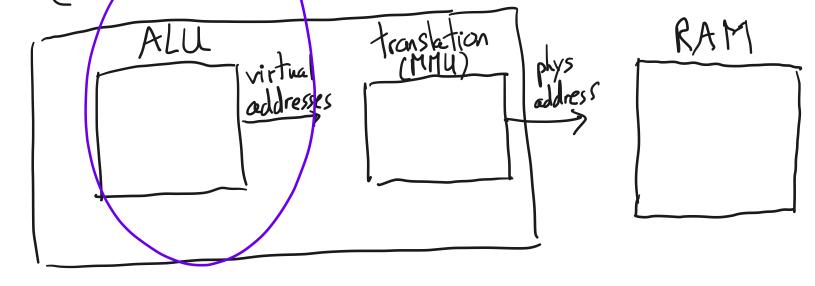
12 I. Last time 12 2. Intro to virtual memory 13 3. Paging 15 Intro 15 Key data structure: page table 15 Multilevel page table 17 Alternatives/Trade offs

2. Intro to virtual memory process sees program excerpt: instruction code address morg 0,200000, /rax 0,500 incq 1, 1/rax 0×508 movg /- rax, 0x 360 000 (1) x 5 \ D y = x+(

CPU



Benefits of virtual memory:

- programmability
  (a) program thinks it has lots of memory
  - (5) programs can use easy addresses: compiler and linker dan't have to worry about where program lives in physical memory
  - (c) multiple instances of a program can be loaded and not collide

- processes cannot read/write each others memory - processes cannot read/write each others memory - enables isolation (which is essential)
- effective use of resources  Shinget()  mmap()
How is translation implemented? - hardware does it, in MMU
OS sets up data structures that the hardware 'Sees.
These data structures are per-process.

## 3. Paging

A. Intro

· Divide memory (virtual + physical) into fixed-size chunks

- These chinks are called PAGES

- PAGE SIZE

- x86-64: 4096 B=4KB=22 bytes

8 bits= ( byte Aside: 1024

210: kilo, ~1000 portxlott

220: mega, ~1 million

230: giga, ~1 billion

240: fera, ~1 trillion

· note a laughtillion

L. Pela, 1900sinilist How many pages are there on a 32-bit architecture? 2 lytes/Qr lytes What if 48 bits are used to address memory? 2 bytes (212 htes/pages) = 2 pages 36 = 30 +6 YPY Page 0: [0,4095] Page 1: [4096,8191]

Page 
$$2^{-1}$$
:

[...,  $2^{3^2}$ -1]

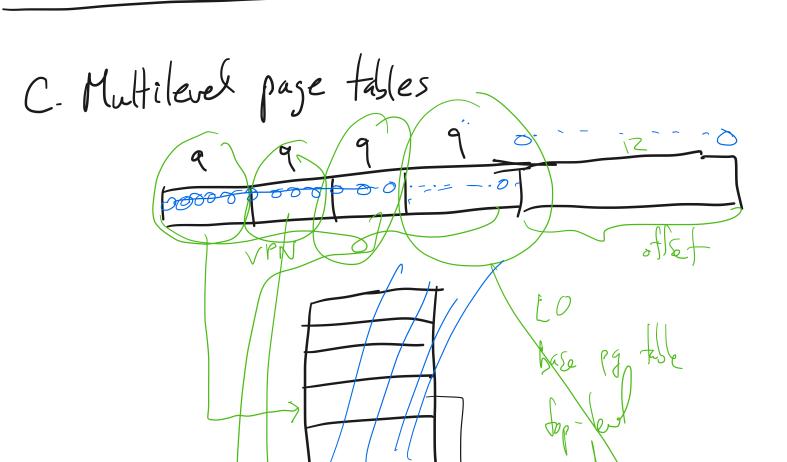
B. Key data structure: page table (per-process) conceptuelly: a map from VPN -> PPN address V9N Page table, cretely

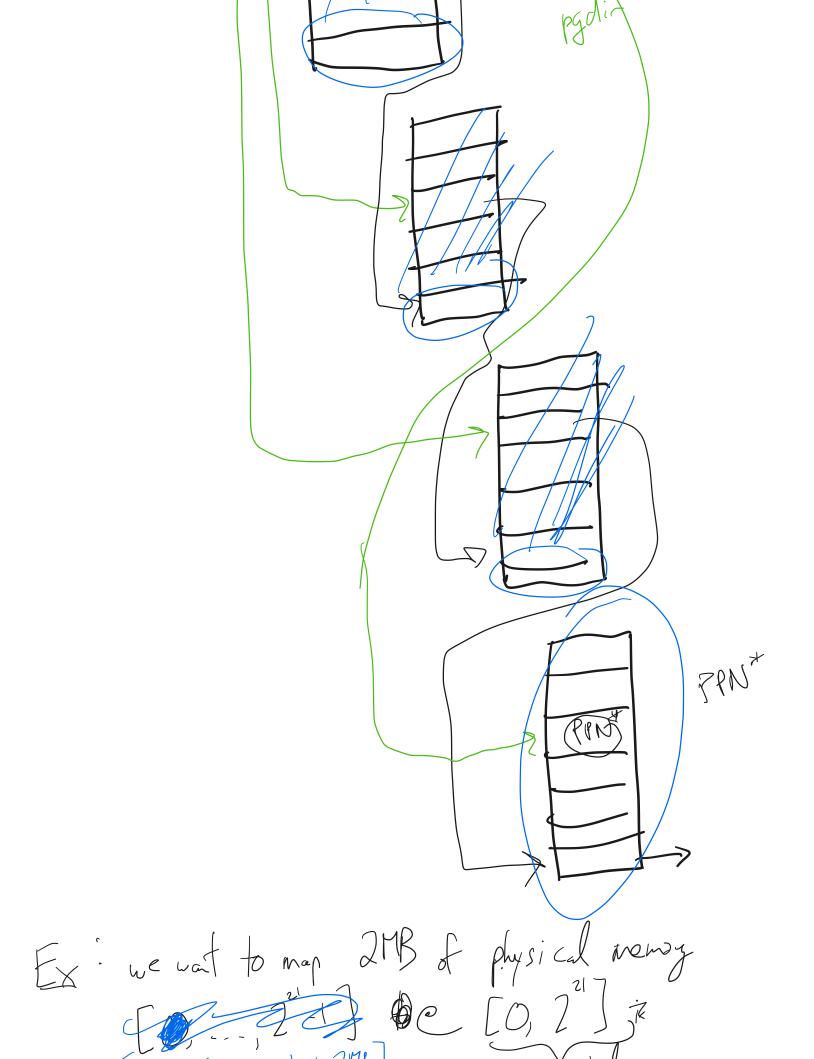
1

O PPN

assume: 48-bit addresses, and 4KB pages (2" bytes) 236 entries 2 entries x 2 htes 8 bytes Ex: OS wants' a process to use address VA: 0200402000 to refer to PA: 0x 00003 5000

table [0x00402] = 0x00003 What's the issue?





(10045MB) - --, (0142MB)

in virtul space