CAO HW5

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1.1

2-way set associative
4 blocks
1 word / block

We have two sets containing two blocks each. Hence we need one bit to select the set. The tag bit is the address size bits(8) - byte offset bits(2) - set bits(1). Therefore, the tag is 5 bits wide.

Stripping the tag bits from the address leaves us three bits, one for the index, and the last two for the byte offset.

It is unclear whether the set or index bits should be different, because they both mean the same thing, or in other words, one can be derived from the other. I assume the set is being derived from the index % 2, hence these bits should be equal.

That the set and index bits are equal is only true in this particular instance, because the number of sets equals the number of blocks in the set.

Time	Access	TAG	SET	INDEX	Byte offset
0	10001101	10001	1	1	01
1	10110010	10110	0	0	10
2	10111111	10111	1	1	11
3	10001100	10010	1	1	00
4	10011100	10011	1	1	00
5	11101001	11101	0	0	01
6	11111110	11111	1	1	10
7	11101001	11101	0	0	01

1.2

See table 1

Table 1: Access sequence ex. 1.2

Access 0		
	Block 0	Block 1
Set 0	X	X
Set 1	10001 0 0	XXXXX 1 X
Access 1		
	Block 0	Block 1
Set 0	10110 0 0	XXXXX 1 X
Set 1	10001 0 0	XXXXX 1 X
Access 2		
	Block 0	Block 1
Set 0	10110 0 0	XXXXX 1 X
Set 1	10001 1 0	10111 0 0
Access 3		
	Block 0	Block 1
Set 0	10110 0 0	XXXXX 1 X
Set 1	10001 0 1	10111 1 0
Access 4		
	Block 0	Block 1
Set 0	10110 0 0	XXXXX 1 X
Set 1	10001 1 0	10011 0 0
Access 5		
	Block 0	Block 1
Set 0	10110 1 0	11101 0 0
Set 1	10001 1 0	10011 0 0
Access 6		
	Block 0	Block 1
Set 0	10110 1 0	11101 0 0
Set 1	11111 0 0	10011 1 0
Access 7		
	Block 0	Block 1
Set 0	10110 1 0	11101 0 1
Set 1	11111 0 0	10011 1 0

1.3

We have 2 hits out of 8 access, so 2/8 = 25%

2

See tables 2, 3, 4 and 5.

Table 2: LRU

Address	hit/miss	set 0	set 0	set 1	set 1
1	miss			1	X
3	miss			1	3
5	miss			5	3
1	miss			5	1
3	miss			3	1
1	hit			3	1
3	hit			3	1
5	miss			3	5
3	hit			3	5

Table 3: MRU

Address	hit/miss	set 0	set 0	set 1	set 1
1	miss			1	X
3	miss			1	3
5	miss			1	5
1	hit			1	5
3	miss			3	5
1	miss			1	5
3	miss			3	5
5	hit			3	5
3	hit			3	5

2.5

This depends too much on how to data is accessed and the size of the data, among other factors. For large datasets, MRU might be more useful if we want to retain older data longer, but then other algorithms might be more feasible depending on the needs of the user.

3.1

Offset is 14 bits (page size is 2^{14} bits). Virtual address space is 2^{38} large dividing these numbers yields 38 - 14 = 24 or 2^{24} PTE's. Physical address space is 2^{33} byets hence we need 33 - 14 = 19 bits to address the physical memory.

3.2

We have 2^{24} entries which are each 2^2 bytes wide, hence 2^{26} = 67 megabytes (or 64 mibibytes)

Table 4: random

Address	hit/miss	set 0	set 0	set 1	set 1
1	miss			1	X
3	miss			1	3
5	miss			5	3
1	miss			5	1
3	miss			3	1
1	hit			3	1
3	hit			3	1
5	miss			5	1
3	miss			3	1

Table 5: optimal

Address	hit/miss	set 0	set 0	set 1	set 1
1	miss			1	X
3	miss			1	3
5	miss			1	5
1	hit			1	5
3	miss			1	3
1	hit			1	3
3	hit			1	3
5	miss			5	3
3	hit			5	3

3.3

32 bits from the PTE, take off the 10 reserved bits leaves 22 bits. The page offset is 14 bits, so in total we have 22+14 = 36 or 2^{36} = 68 gigabytes (64 gibibytes).