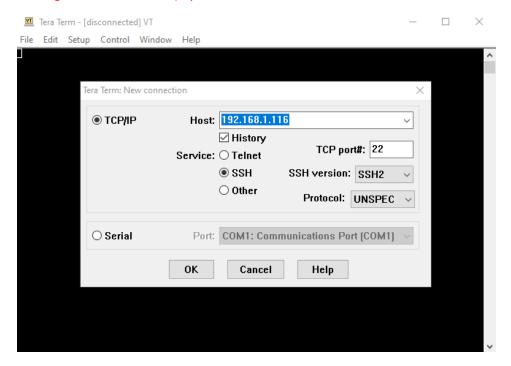
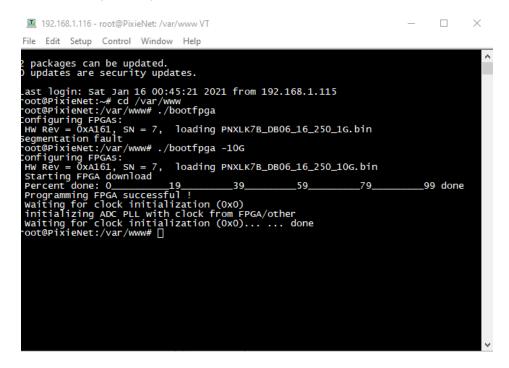
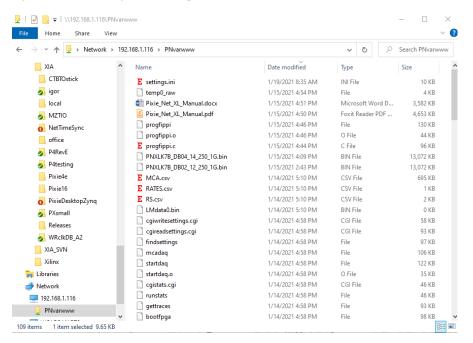
SSH log in to Pixie-Net XL. (If you don't know the IP address, use the USB-UART "serial" option)



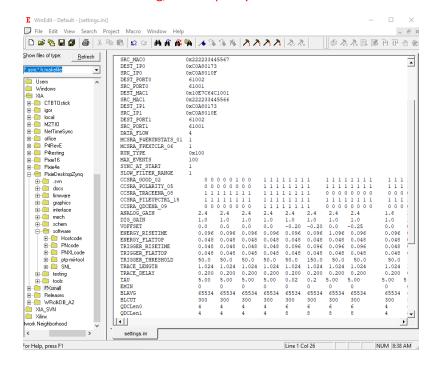
Pixie-Net XL runs Ubuntu 18. Go to shared folder and boot FPGAs by typing "bootfpga" (usually automatic at power up and reboot)



Open Windows Explorer and go to shared folder (Pixie-Net XL IP)

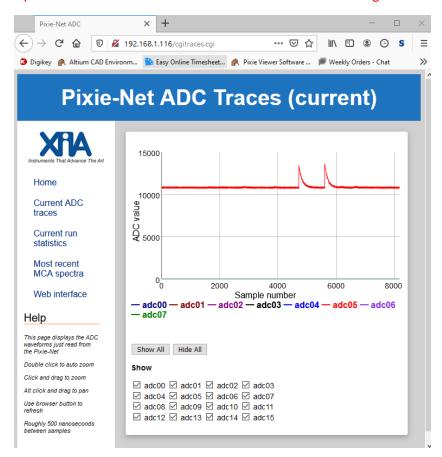


Edit settings.ini, for example analog gain, offset, run type ...
Parameters [mostly] match the Pixie-16 in meaning and value range. See manual for details!
For 10G data streaming, MUST specify correct destination IP and MAC of receiver PC



Apply settings from file by running "progfippi" in terminal

Open web browser to Pixie-Net XL's IP and check detector signal



Open cmd window on PC and start the udp receiver program "udp-receive.exe"

```
Command Prompt - udp_receive.exe
                                               Media disconnected
   Media State . .
   Connection-specific DNS Suffix .
lireless LAN adapter Local Area Connection* 1:
  Media State . . . . . . . . . . . . . Media disconnected Connection-specific DNS Suffix . :
lireless LAN adapter Local Area Connection* 3:
  Media State . . . . . . . . . : Media disconnected Connection-specific DNS Suffix . :
 :\XIA\PixieDesktopZynq\interface\Igor>
:\XIA\PixieDesktopZynq\interface\Igor>
 :\XIA\PixieDesktopZynq\interface\Igor>
 \XIA\PixieDesktopZynq\interface\Igor>
:\XIA\PixieDesktopZynq\interface\Igor>udp_receive.exe
Initialising Winsock...Initialised.
ocket created.
ind done
O_RCVBUF Value: 65536
O_RCVBUF Value: 10000000
Waiting for data...press CTRL-C to quit
Received packet 1 from 192.168.1.14:61001
Received packet 10001 from 192.168.1.14:61001
```

Window may ask for Firewall permission: allow

Start DAQ by typing "startdaq" in terminal ...

PC will now receive packets and Pixie-Net XL will count the run time

```
### 192.168.1.116 - root@PixieNet: /var/www VT

File Edit Setup Control Window Help

Programming FPGA successful!

Waiting for clock initialization (0x0)
initializing ADC PLL with clock from FPGA/other

Waiting for clock initialization (0x0)..... done
'oot@PixieNet:/var/www#./progfippi

DEST_MAC1 equal to 10:F7:66:4c:10:01

SRC_MAC1 equal to 22:22:33:44:55:66

DEST_IP1 0xc0A8010F equal to 192.168.1.115

SRC_IP1 0xc0A8010F equal to 192.168.1.15

UDP_PAUSE, WR Ethernet minimum packet separation: 10 (x 64ns cycles)
PXdesk board temperature: 41 C

DBO board temperature: 511 C

DB1 board temperature: 51 C

DB1 board temperature: 52 C

MZ Zynq temperature: 54 C

Main board Revision 0xA161, Serial Number 7

DB0 Revision 0xFFFF

DB1 Revision 0x0060

oot@PixieNet:/var/www# ./startdaq

ootal_Time 0 43588

ootal_Time 0.87359

ootal_Time 1.3133

ootal_Time 2.2152

ootal_Time 3.095

ootal_Time 3.095

ootal_Time 3.9356

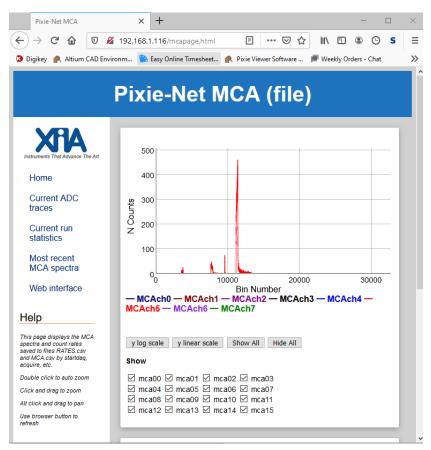
ootal_Time 4.4163

ootal_Time 4.4163

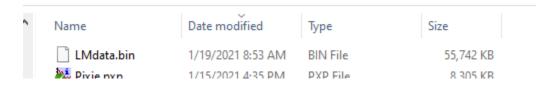
ootal_Time 4.4163

ootal_Time 4.4163
```

Can see MCA on webpage

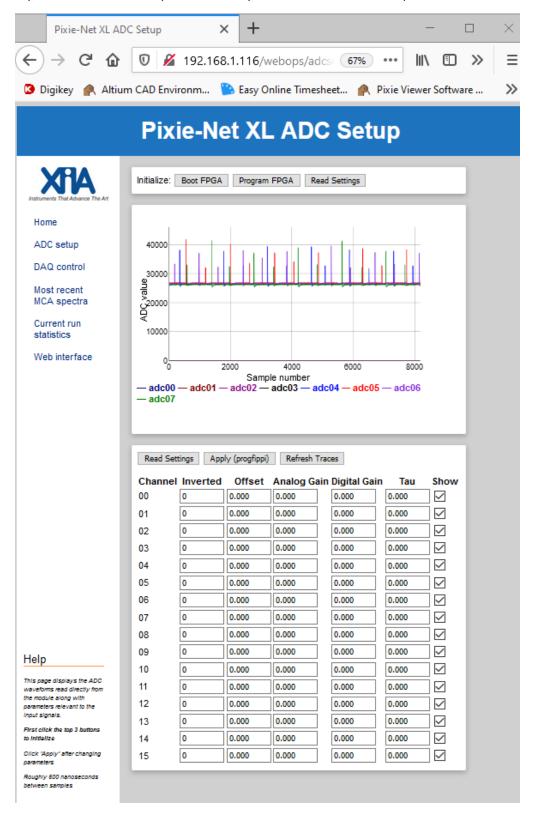


And LM file in Windows Explorer



The UDP receive program exists for Windows and Linux. It's basically copied from a socket programming tutorial, 1-2 pages of code.

If you feel adventurous, you can also try the web interface to set parameters and start runs.



Network setup: The "Receiver PC" can be the same as the "Control PC". However control is 1G Ethernet, data is 10G Ethernet.

