# 叁议电子 OLED 说明书（IIC 接口）

完整版请查看 SSD1306 说明书

## 1. Device Address

**Table 1** OLED Device Address

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | R/W |

## 2. IIC bus data format

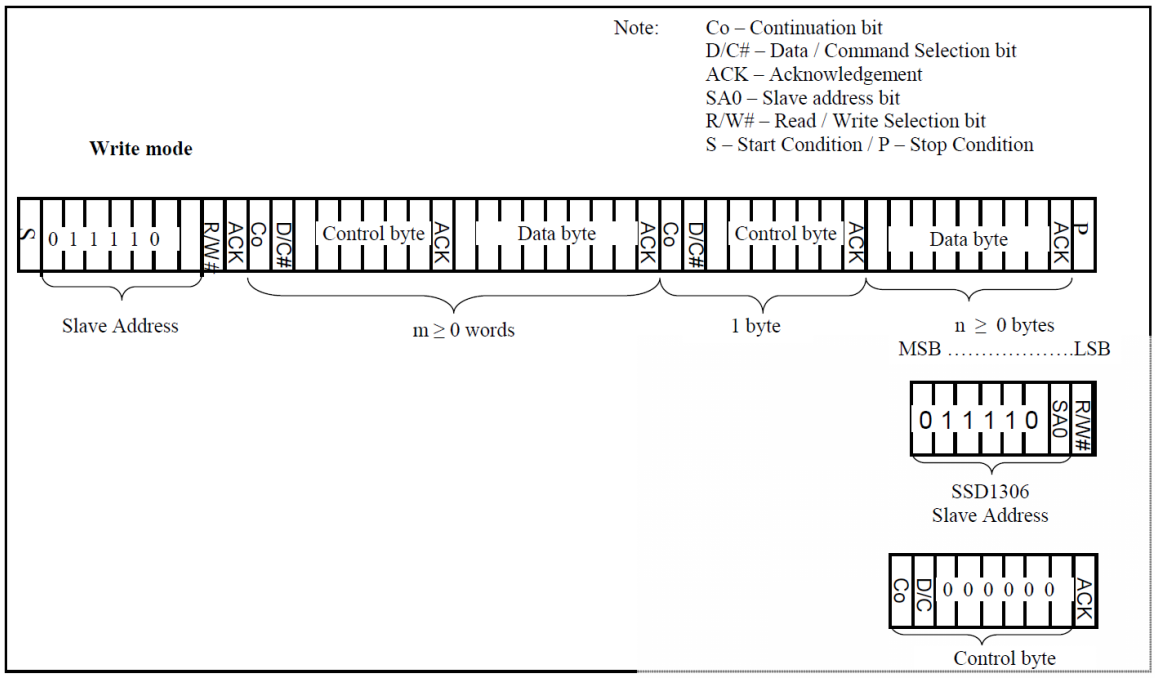


**Figure 1** IIC bus data format

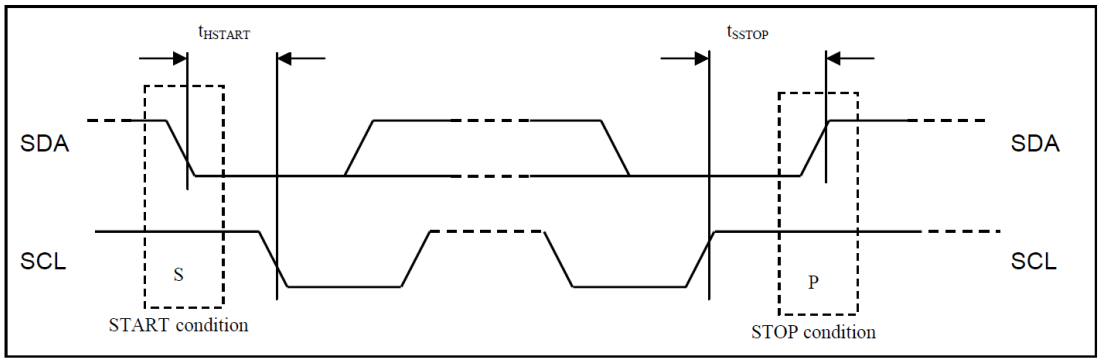


**Figure 2** Definition of the Start and Stop Condition

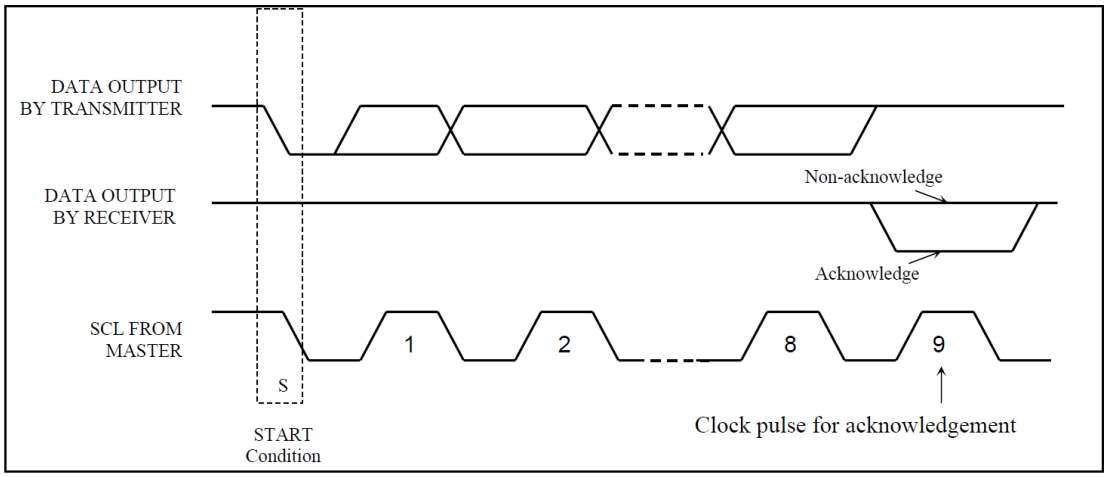


**Figure 3** Definition of the acknowledgement condition

(1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in **Figure 2**. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.

(2) The slave address is following the start condition for recognition use. The slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).

(3) The write mode is established by setting the R/W# bit to logic "0".

(4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the **Figure 3** for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.

(5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0”.

**a.** If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.

**b.** The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

(6) Acknowledge bit will be generated after receiving each control byte or data byte.

(7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in **Figure 2**. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

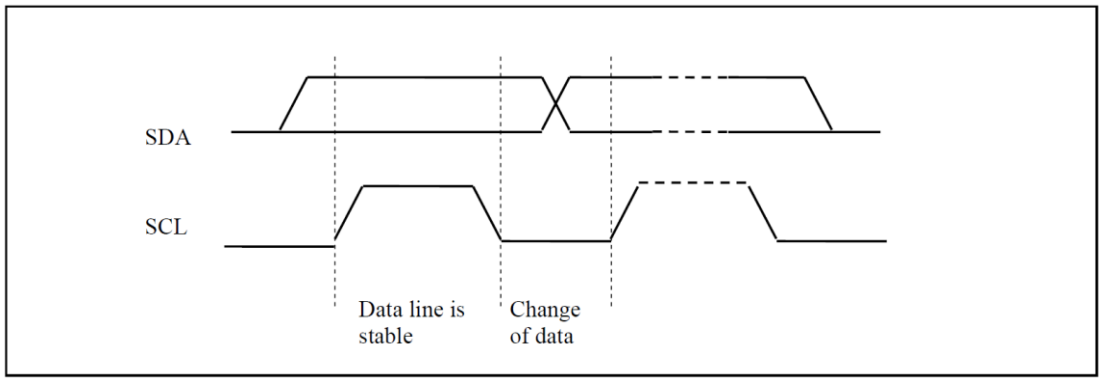


**Figure 4** Definition of the data transfer condition

# 3. Command Table

| 1. Fundamental Command Table | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **D/C#** | **Hex** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Command** | **Description** |
| 0<br>0 | 81<br>A[7:0] | 1<br>$A_7$ | 0<br>$A_6$ | 0<br>$A_5$ | 0<br>$A_4$ | 0<br>$A_3$ | 0<br>$A_2$ | 0<br>$A_1$ | 1<br>$A_0$ | Set Contrast Control | Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.<br>(RESET = 7Fh ) |
| 0 | A4/A5 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $X_0$ | Entire Display ON | A4h, $X_0$=0b: Resume to RAM content display (RESET)<br>Output follows RAM content<br>A5h, $X_0$=1b: Entire display ON<br>Output ignores RAM content |
| 0 | A6/A7 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | $X_0$ | Set Normal/Inverse Display | A6h, X[0]=0b: Normal display (RESET)<br>0 in RAM: OFF in display panel<br>1 in RAM: ON in display panel<br>A7h, X[0]=1b: Inverse display<br>0 in RAM: ON in display panel<br>1 in RAM: OFF in display panel |
| 0 | AE<br>AF | 1 | 0 | 1 | 0 | 1 | 1 | 1 | $X_0$ | Set Display ON/OFF | AEh, X[0]=0b:Display OFF (sleep mode) (RESET)<br>AFh X[0]=1b:Display ON in normal mode |

| 2. Scrolling Command Table | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **D/C#** | **Hex** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Command** | **Description** |
| 0 | 26/27 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | $X_0$ | Continuous Horizontal Scroll Setup | 26h, X[0]=0, Right Horizontal Scroll<br>27h, X[0]=1, Left Horizontal Scroll<br>(Horizontal scroll by 1 column)<br>A[7:0] : Dummy byte (Set as 00h)<br>B[2:0] : Define start page address<br>000b – PAGE0 \| 011b – PAGE3 \| 110b – PAGE6<br>001b – PAGE1 \| 100b – PAGE4 \| 111b – PAGE7<br>010b – PAGE2 \| 101b – PAGE5<br>C[2:0] : Set time interval between each scroll step in terms of frame frequency<br>000b – 5 frames \| 100b – 3 frames<br>001b – 64 frames \| 101b – 4 frames<br>010b – 128 frames \| 110b – 25 frame<br>011b – 256 frames \| 111b – 2 frame<br>D[2:0] : Define end page address<br>000b – PAGE0 \| 011b – PAGE3 \| 110b – PAGE6<br>001b – PAGE1 \| 100b – PAGE4 \| 111b – PAGE7<br>010b – PAGE2 \| 101b – PAGE5<br>The value of D[2:0] must be larger or equal to B[2:0]<br>E[7:0] : Dummy byte (Set as 00h)<br>F[7:0] : Dummy byte (Set as FFh) |
| 0 | A[7:0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 0 | B[2:0] | * | * | * | * | * | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | C[2:0] | * | * | * | * | * | $C_2$ | $C_1$ | $C_0$ | | |
| 0 | D[2:0] | * | * | * | * | * | $D_2$ | $D_1$ | $D_0$ | | |
| 0 | E[7:0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 0 | F[7:0] | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | |

**2. Scrolling Command Table**

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 29/2A | 0 | 0 | 1 | 0 | 1 | 0 | $X_1$ | $X_0$ | Continuous Vertical and Horizontal Scroll Setup | 29h, $X_1X_0$=01b : Vertical and Right Horizontal Scroll<br>2Ah, $X_1X_0$=10b : Vertical and Left Horizontal Scroll<br>(Horizontal scroll by 1 column)<br>A[7:0] : Dummy byte<br><br>B[2:0] : Define start page address<br>000b – PAGE0 \| 011b – PAGE3 \| 110b – PAGE6<br>001b – PAGE1 \| 100b – PAGE4 \| 111b – PAGE7<br>010b – PAGE2 \| 101b – PAGE5 \|<br><br>C[2:0] : Set time interval between each scroll step in terms of frame frequency<br>000b – 5 frames \| 100b – 3 frames<br>001b – 64 frames \| 101b – 4 frames<br>010b – 128 frames \| 110b – 25 frame<br>011b – 256 frames \| 111b – 2 frame<br><br>D[2:0] : Define end page address<br>000b – PAGE0 \| 011b – PAGE3 \| 110b – PAGE6<br>001b – PAGE1 \| 100b – PAGE4 \| 111b – PAGE7<br>010b – PAGE2 \| 101b – PAGE5 \|<br>The value of D[2:0] must be larger or equal to B[2:0]<br><br>E[5:0] : Vertical scrolling offset<br>e.g. E[5:0]= 01h refer to offset =1 row<br>E[5:0] =3Fh refer to offset =63 rows<br>**Note**<br>(1) No continuous vertical scrolling is available. |
| 0 | 2E | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Deactivate scroll | Stop scrolling that is configured by command 26h/27h/29h/2Ah.<br><br>**Note**<br>(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten. |
| 0 | 2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Activate scroll | Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:<br><br>Valid command sequence 1: 26h ;2Fh.<br>Valid command sequence 2: 27h ;2Fh.<br>Valid command sequence 3: 29h ;2Fh.<br>Valid command sequence 4: 2Ah ;2Fh.<br><br>For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands. |

**2. Scrolling Command Table**

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | A3 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Set Vertical Scroll Area | A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0]<br><br>B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]<br>**Note**<br>(1) A[5:0]+B[6:0] <= MUX ratio<br>(2) B[6:0] <= MUX ratio<br>(3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0]<br>(3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0]<br>(4) The last row of the scroll area shifts to the first row of the scroll area.<br>(5) For 64d MUX display<br>A[5:0] = 0, B[6:0]=64 : whole area scrolls<br>A[5:0]= 0, B[6:0] < 64 : top area scrolls<br>A[5:0] + B[6:0] < 64 : central area scrolls<br>A[5:0] + B[6:0] = 64 : bottom area scrolls |
| 0 | A[5:0] | * | * | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | B[6:0] | * | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |

**3. Addressing Setting Command Table**

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00~0F | 0 | 0 | 0 | 0 | $X_3$ | $X_2$ | $X_1$ | $X_0$ | Set Lower Column Start Address for Page Addressing Mode | Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.<br><br>**Note**<br>(1) This command is only for page addressing mode |
| 0 | 10~1F | 0 | 0 | 0 | 1 | $X_3$ | $X_2$ | $X_1$ | $X_0$ | Set Higher Column Start Address for Page Addressing Mode | Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.<br><br>**Note**<br>(1) This command is only for page addressing mode |
| 0 | 20 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Set Memory Addressing Mode | A[1:0] = 00b, Horizontal Addressing Mode<br>A[1:0] = 01b, Vertical Addressing Mode<br>A[1:0] = 10b, Page Addressing Mode (RESET)<br>A[1:0] = 11b, Invalid |
| 0 | A[1:0] | * | * | * | * | * | * | $A_1$ | $A_0$ | | |
| 0 | 21 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Set Column Address | Setup column start and end address<br>A[6:0] : Column start address, range : 0-127d, (RESET=0d)<br><br>B[6:0]: Column end address, range : 0-127d, (RESET =127d)<br>**Note**<br>(1) This command is only for horizontal or vertical addressing mode. |
| 0 | A[6:0] | * | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | B[6:0] | * | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |

| 3. **Addressing Setting Command Table** | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **D/C#** | **Hex** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Command** | **Description** |
| 0<br>0<br>0 | 22<br>A[2:0]<br>B[2:0] | 0<br>*<br>* | 0<br>*<br>* | 1<br>*<br>* | 0<br>*<br>* | 0<br>*<br>* | 0<br>$A_2$<br>$B_2$ | 1<br>$A_1$<br>$B_1$ | 0<br>$A_0$<br>$B_0$ | Set Page Address | Setup page start and end address<br>A[2:0] : Page start Address, range : 0-7d, (RESET = 0d)<br>B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)<br>**Note**<br>(1) This command is only for horizontal or vertical addressing mode. |
| 0 | B0~B7 | 1 | 0 | 1 | 1 | 0 | $X_2$ | $X_1$ | $X_0$ | Set Page Start Address for Page Addressing Mode | Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].<br>**Note**<br>(1) This command is only for page addressing mode |

| 4. **Hardware Configuration (Panel resolution & layout related) Command Table** | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **D/C#** | **Hex** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Command** | **Description** |
| 0 | 40~7F | 0 | 1 | $X_5$ | $X_4$ | $X_3$ | $X_2$ | $X_1$ | $X_0$ | Set Display Start Line | Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$.<br>Display start line register is reset to 000000b during RESET. |
| 0 | A0/A1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $X_0$ | Set Segment Re-map | A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET)<br>A1h, X[0]=1b: column address 127 is mapped to SEG0 |
| 0<br>0 | A8<br>A[5:0] | 1<br>* | 0<br>* | 1<br>$A_5$ | 0<br>$A_4$ | 1<br>$A_3$ | 0<br>$A_2$ | 0<br>$A_1$ | 0<br>$A_0$ | Set Multiplex Ratio | Set MUX ratio to N+1 MUX<br>N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX)<br>A[5:0] from 0 to 14 are invalid entry. |
| 0 | C0/C8 | 1 | 1 | 0 | 0 | $X_3$ | 0 | 0 | 0 | Set COM Output Scan Direction | C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1]<br>C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0<br>Where N is the Multiplex ratio. |
| 0<br>0 | D3<br>A[5:0] | 1<br>* | 1<br>* | 0<br>$A_5$ | 1<br>$A_4$ | 0<br>$A_3$ | 0<br>$A_2$ | 1<br>$A_1$ | 1<br>$A_0$ | Set Display Offset | Set vertical shift by COM from 0d~63d<br>The value is reset to 00h after RESET. |
| 0<br>0 | DA<br>A[5:4] | 1<br>0 | 1<br>0 | 0<br>$A_5$ | 1<br>$A_4$ | 1<br>0 | 0<br>0 | 1<br>1 | 0<br>0 | Set COM Pins Hardware Configuration | A[4]=0b, Sequential COM pin configuration<br>A[4]=1b(RESET), Alternative COM pin configuration<br>A[5]=0b(RESET), Disable COM Left/Right remap<br>A[5]=1b, Enable COM Left/Right remap |

<table>
<tr><th colspan="12">5. Timing & Driving Scheme Setting Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0<br>0</td><td>D5<br>A[7:0]</td><td>1<br>$A_7$</td><td>1<br>$A_6$</td><td>0<br>$A_5$</td><td>1<br>$A_4$</td><td>0<br>$A_3$</td><td>1<br>$A_2$</td><td>0<br>$A_1$</td><td>1<br>$A_0$</td><td>Set Display Clock Divide Ratio/Oscillator Frequency</td><td>A[3:0] : Define the divide ratio (D) of the display clocks (DCLK):<br>Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1)<br><br>A[7:4] : Set the Oscillator Frequency, $F_{OSC}$.<br>Oscillator Frequency increases with the value of A[7:4] and vice versa.<br>RESET is 1000b<br>Range:0000b~1111b<br>Frequency increases as setting value increases.</td></tr>
<tr><td>0<br>0</td><td>D9<br>A[7:0]</td><td>1<br>$A_7$</td><td>1<br>$A_6$</td><td>0<br>$A_5$</td><td>1<br>$A_4$</td><td>1<br>$A_3$</td><td>0<br>$A_2$</td><td>0<br>$A_1$</td><td>1<br>$A_0$</td><td>Set Pre-charge Period</td><td>A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)<br><br>A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h )</td></tr>
<tr><td>0<br>0</td><td>DB<br>A[6:4]</td><td>1<br>0</td><td>1<br>$A_6$</td><td>0<br>$A_5$</td><td>1<br>$A_4$</td><td>1<br>0</td><td>0<br>0</td><td>1<br>0</td><td>1<br>0</td><td>Set $V_{COMH}$ Deselect Level</td><td><table><tr><th>A[6:4]</th><th>Hex code</th><th>$V_{COMH}$ deselect level</th></tr><tr><td>000b</td><td>00h</td><td>~ 0.65 x $V_{CC}$</td></tr><tr><td>010b</td><td>20h</td><td>~ 0.77 x $V_{CC}$ (RESET)</td></tr><tr><td>011b</td><td>30h</td><td>~ 0.83 x $V_{CC}$</td></tr></table></td></tr>
<tr><td>0</td><td>E3</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>NOP</td><td>Command for no operation</td></tr>
</table>

# 4. COMMAND DESCRIPTIONS

## 4.1 Fundamental Command

### 4.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access.

### 4.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access.

### 4.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1306: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, “COL” means the graphic display data RAM column.

**Page addressing mode (A[1:0]=10xb)**

In page addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in **Figure 5**.

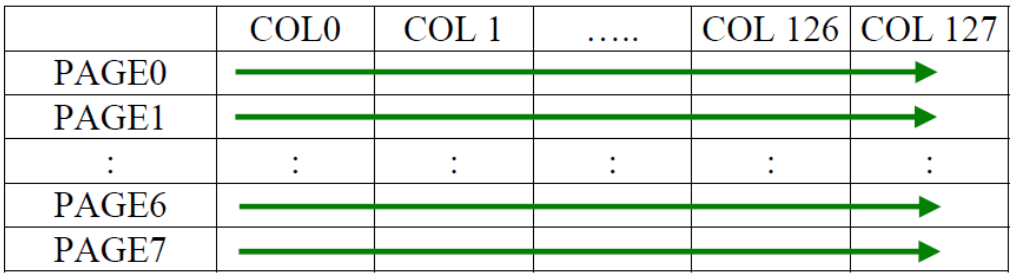


**Figure 5** Address Pointer Movement of Page addressing mode

**Horizontal addressing mode (A[1:0]=00b)**

In horizontal addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in **Figure 6**. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in **Figure 6**.)

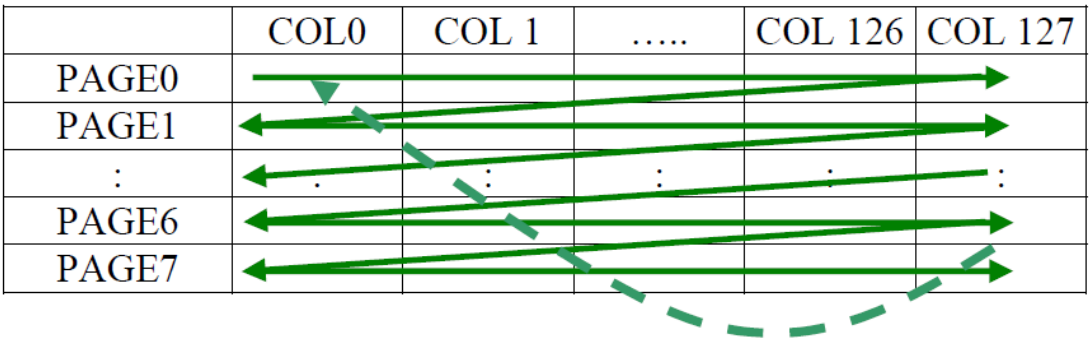


**Figure 6** Address Pointer Movement of Horizontal addressing mode

**Vertical addressing mode: (A[1:0]=01b)**

In vertical addressing mode, after the display RAM is read/written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in **Figure 7**. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (*Dotted line in Figure 7*.)

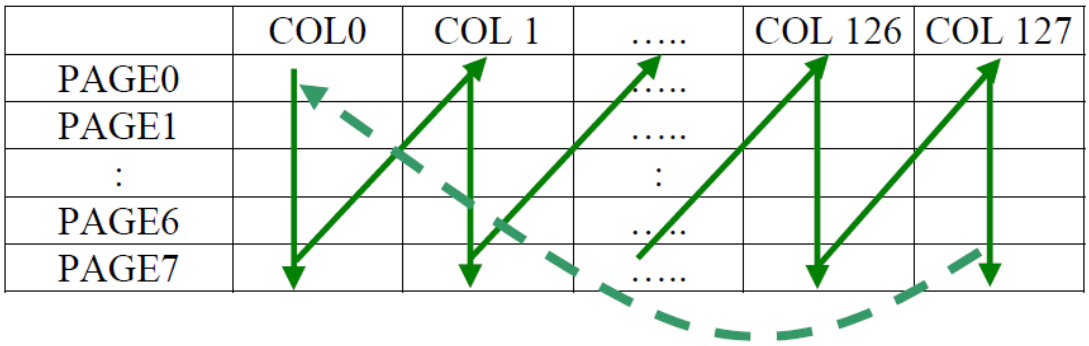


**Figure 7** Address Pointer Movement of Vertical addressing mode

In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

• Set the column start and end address of the target display location by command 21h.

• Set the page start and end address of the target display location by command 22h.

### 4.1.4 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

### 4.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 125, page start address is set to 1 and page end address is set to 6; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from page 1 to page 6 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in* ***Figure 8***). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and page address is automatically increased by 1 (*solid line in* ***Figure 8***). While the end page 6 and end

column 125 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line in* ***Figure 8***).

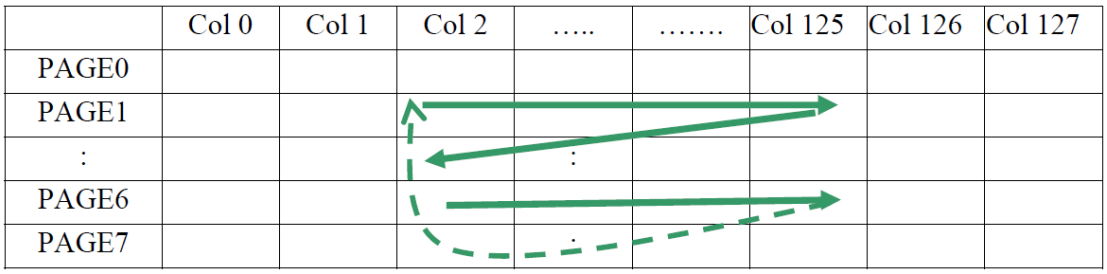


**Figure 8** Example of Column and Row Address Pointer Movement

### 4.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM1 and so on.

### 4.1.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

### 4.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

### 4.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents. If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents. In other words, A4h command resumes the display from entire

display “ON” stage. A5h command forces the entire display to be “ON”, regardless of the contents of the display data RAM.

### 4.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

### 4.1.11 Set Multiplex Ratio (A8h)

This command switches the default 63 multiplex mode to any multiplex ratio, ranging from 16 to 63. The output pads COM0~COM63 will be switched to the corresponding COM signal.

### 4.1.12 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF. When the display is ON, the selected circuits by Set Master Configuration command will be turned ON. When the display is OFF, those circuits will be turned OFF and the segment and common output are in VSS state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

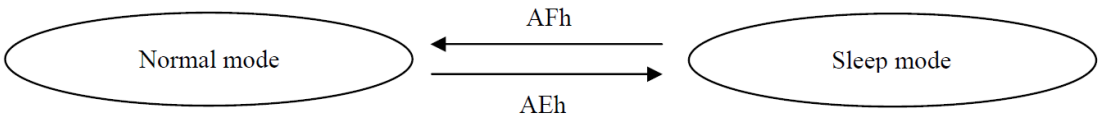


**Figure 9** Transition between different modes

### 4.1.13 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 7 in GDDRAM under Page

Addressing Mode.

### 4.1.14 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately.

### 4.1.15 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0). For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 - 16, so the second byte would be 100000b.

### 4.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D)(A[3:0])

Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 8.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])

Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

#### 4.1.17 Set Pre-charge Period (D9h)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals 2 DCLKs.

#### 4.1.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. The table below shows the COM pin configuration under different conditions (for MUX ratio =64):

#### 4.1.19 Set VCOMH Deselect Level (DBh)

#### 4.1.20 NOP (E3h)

No Operation Command

#### 4.1.21 Status register Read

This command is issued by setting D/C# ON LOW during a data read. It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

### 4.2 Graphic Acceleration Command

#### 4.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed. Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The SSD1306 horizontal scroll is designed for 128 columns scrolling.

### 4.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 6 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, scrolling speed and vertical scrolling offset. The bytes B[2:0], C[2:0] and D[2:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h). Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

### 4.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

### 4.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setupcommands: 26h/27h/29h/2Ah. The setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands. The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

### 4.2.5 Set Vertical Scroll Area(A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29/2Ah), the number of rows that in vertical scrolling can be set smaller or equal to the MUX ratio.

## 5. IIC bus timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 2.5 | - | - | us |
| $t_{HSTART}$ | Start condition Hold Time | 0.6 | - | - | us |
| $t_{HD}$ | Data Hold Time (for "$SDA_{OUT}$" pin) | 0 | - | - | ns |
| | Data Hold Time (for "$SDA_{IN}$" pin) | 300 | - | - | ns |
| $t_{SD}$ | Data Setup Time | 100 | - | - | ns |
| $t_{SSTART}$ | Start condition Setup Time (Only relevant for a repeated Start condition) | 0.6 | - | - | us |
| $t_{SSTOP}$ | Stop condition Setup Time | 0.6 | - | - | us |
| $t_R$ | Rise Time for data and clock pin | - | - | 300 | ns |
| $t_F$ | Fall Time for data and clock pin | - | - | 300 | ns |
| $t_{IDLE}$ | Idle Time before a new transmission can start | 1.3 | - | - | us |

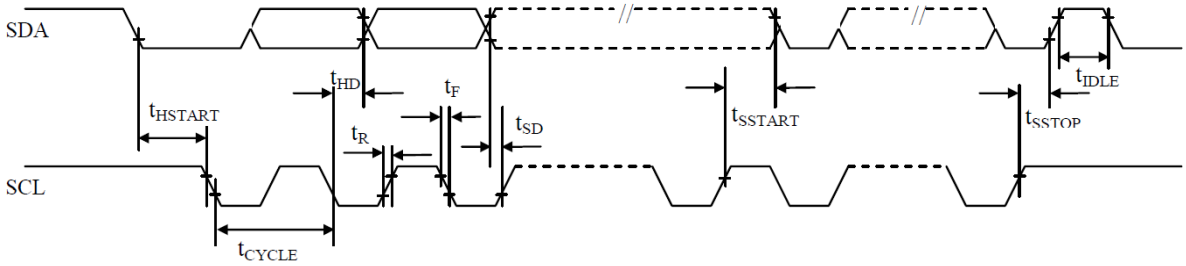


**Figure 10** I2C Interface Timing characteristics

## 6. OLED Initial

（01）display off (0xae)

（02）set low column address (0x00)

（03）set high column address (0x10)

（04）set start line address (0x40)

（05）set page address (0xb0)

（06）contract control (0x81)

（07）send 0xff (多字节指令)

（08）set segment remap (0xa1)

（09）set normal/reverse (0xa6)

（10）set multiplex ratio (1 to 64) (0xa8 )

（11）set duty 1/32 (0x3f)

（12）com scan direction (0xc8)

（13）set display offset (0xd3)

（14）send 0x00

（15）set osc division (0xd5)

（16）send 0x80

（17）set area color mode off (0xd8)

（18）send 0x05

（19）set pre-charge period (0xd9)

（20）send 0xf1

（21）set com pin configuration (0xda)

（22）send 0x12

（23）set Vcomh (0xdb)

（24）send 0x30

（25）set charge pump enable (0x8d)

（26）send 0x14

（27）turn on oled panel(0xaf)