B4 SC3900 Cache Coherency

Michael Liu

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L1 cache
L2 cache
DDR
CoreNet
Coherency Domain
Coherency mechanism
Inter-core communication
Read-modify-write

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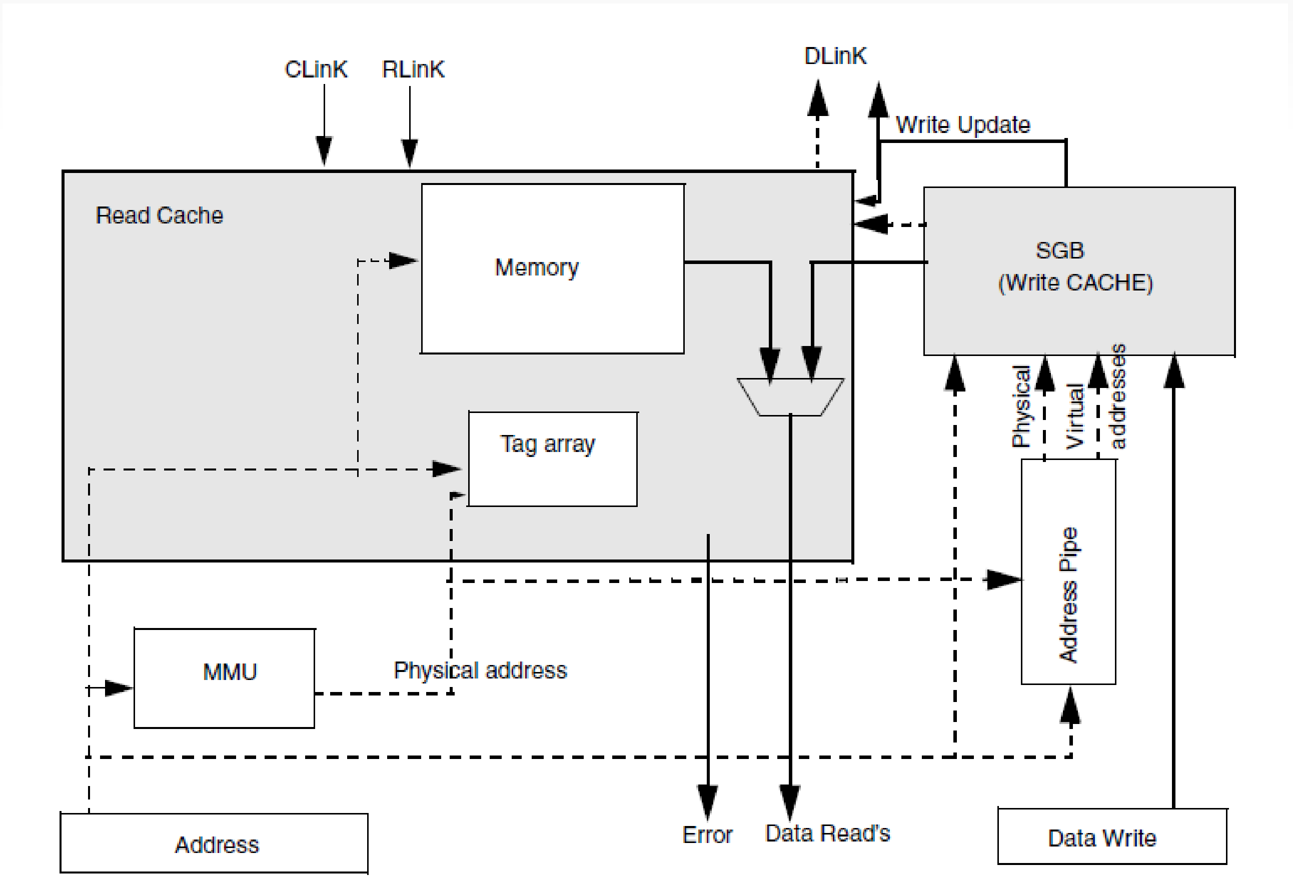
L1 cache



Legend:

Data--> ————————

Address--> - - - - - - - - - -

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L1 cache allocation policy

- Read cache
  - Cacheable read
    - Allocated in I/D cache, trigger next line prefetch if configured
  - Non-cacheable read
    - Not allocated in I/D cache
- Write cache (SGB)
  - Memory Cacheable/non-cacheable write
    - kept in SGB as long as possible
    - Each entry 64B,
    - Separate writes can be merged into 1 64B write if they belong to same cache line.
  - Peripheral Non-cacheable write
    - Send to high level cache(L2) in order, no merging.

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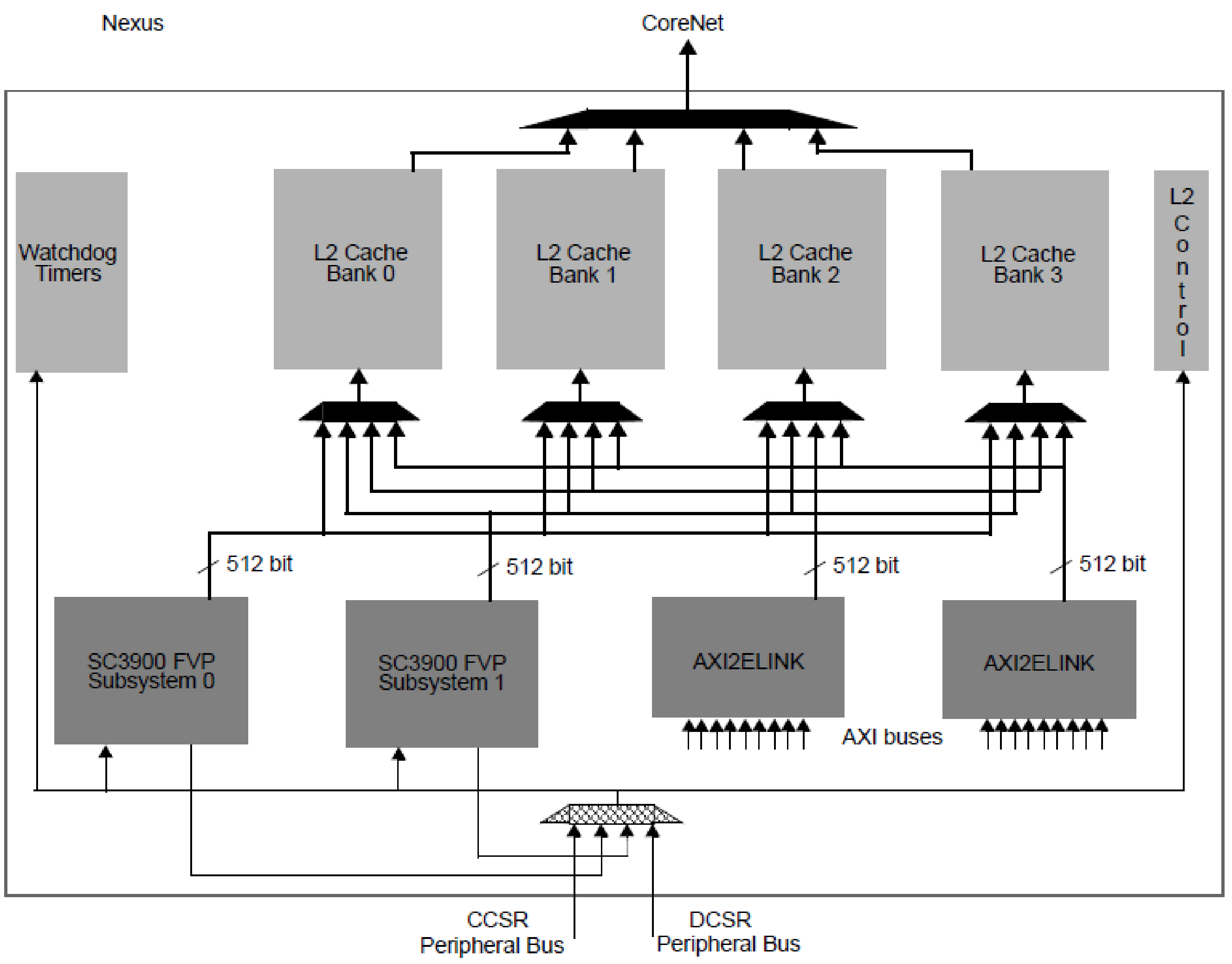
L2 cache



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L2 cache policy

- Noncacheable: on read and write (NC)
- Cacheable write back: cacheable on read and write
- Cacheable write through: cacheable on read and on write hit, and noncacheable on write miss (WT).

- Cache policy is configured in MMU entry and valid for both L1 and L2.

- Out of order
  - The 4 banks are out of order.
  - If order is important, must use barriers, such as DBARM.EIEIO

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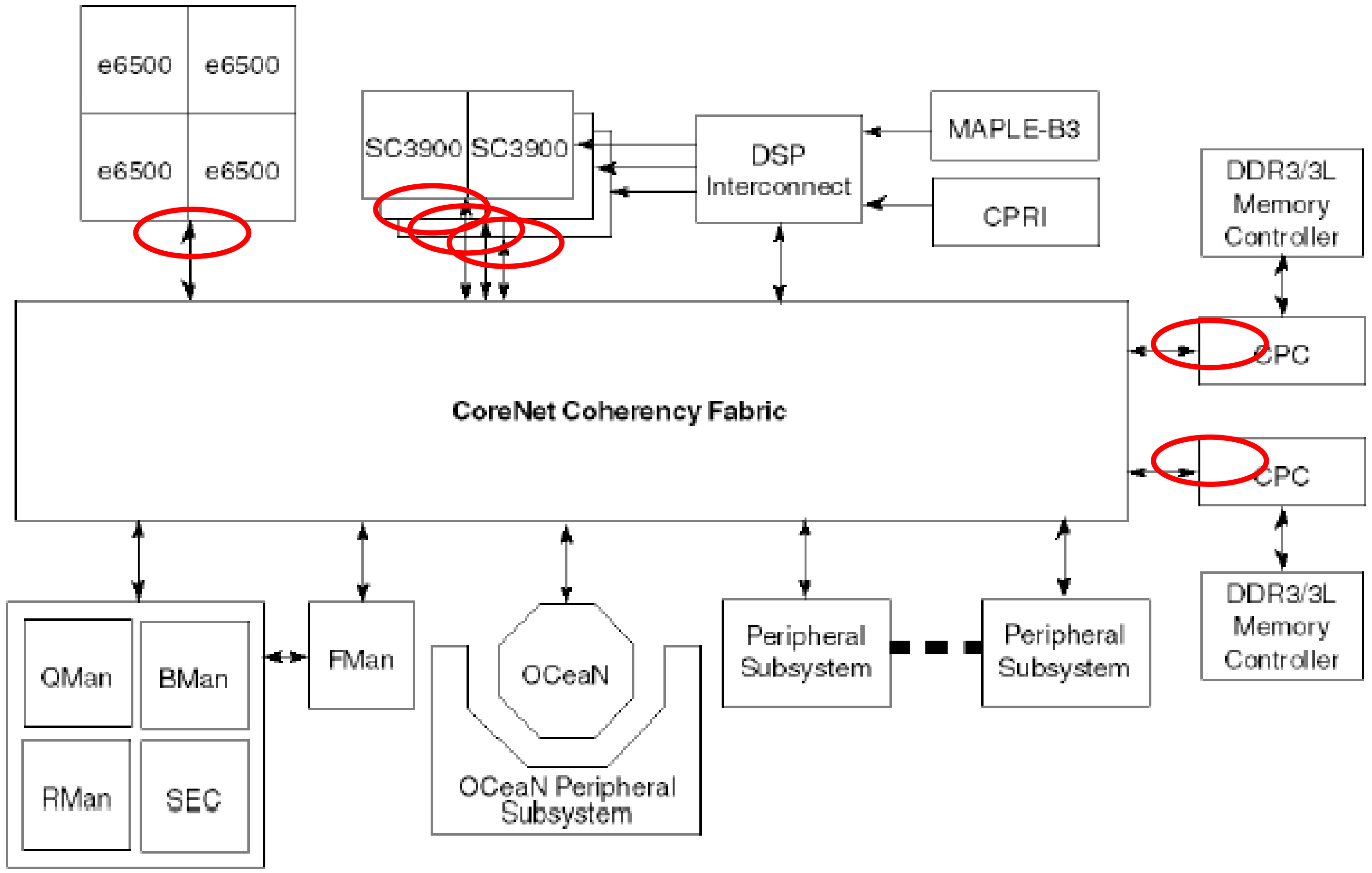
Coherency Domain

- L2 caches
- PAMU caches
- CPC (DDR)



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- L2 cache line status
  - Invalid
  - Exclusive: data only in current cache, clean
  - Shared: data in more than 1 cache, clean
  - Modified: data is modified (written), dirty

- Possible status
  - All invalid
  - One exclusive, others invalid
  - More than 1 shared, others invalid
  - All shared
  - One modified, others invalid

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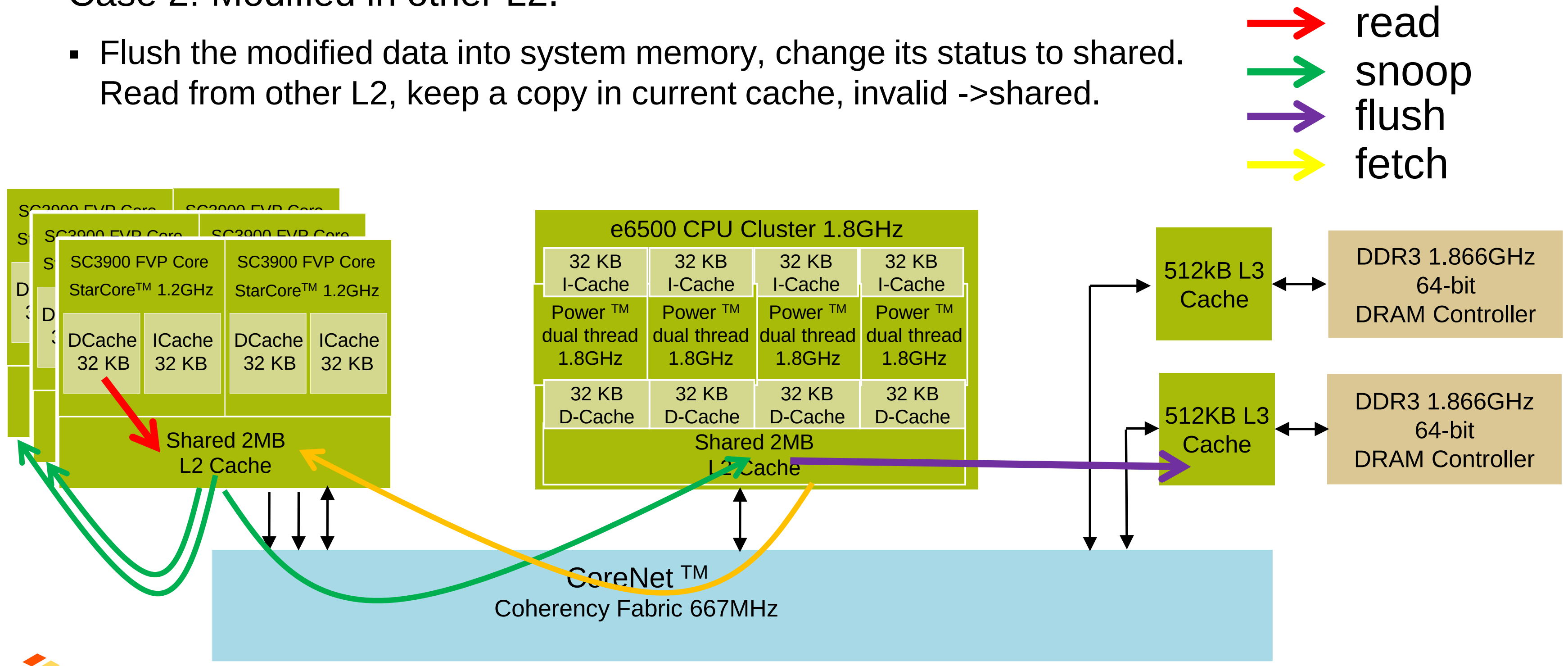
Coherency: read miss

- No copy in any L2
  - Read from system memory, invalid -> exclusive.
- Valid in other L2
  - Case 1: Not modified in other L2
    - read from other L2 and keep a copy in current L2, invalid -> shared
  - Case 2: Modified in other L2.
    - Flush the modified data into system memory, change its status to shared. Read from other L2, keep a copy in current cache, invalid ->shared.



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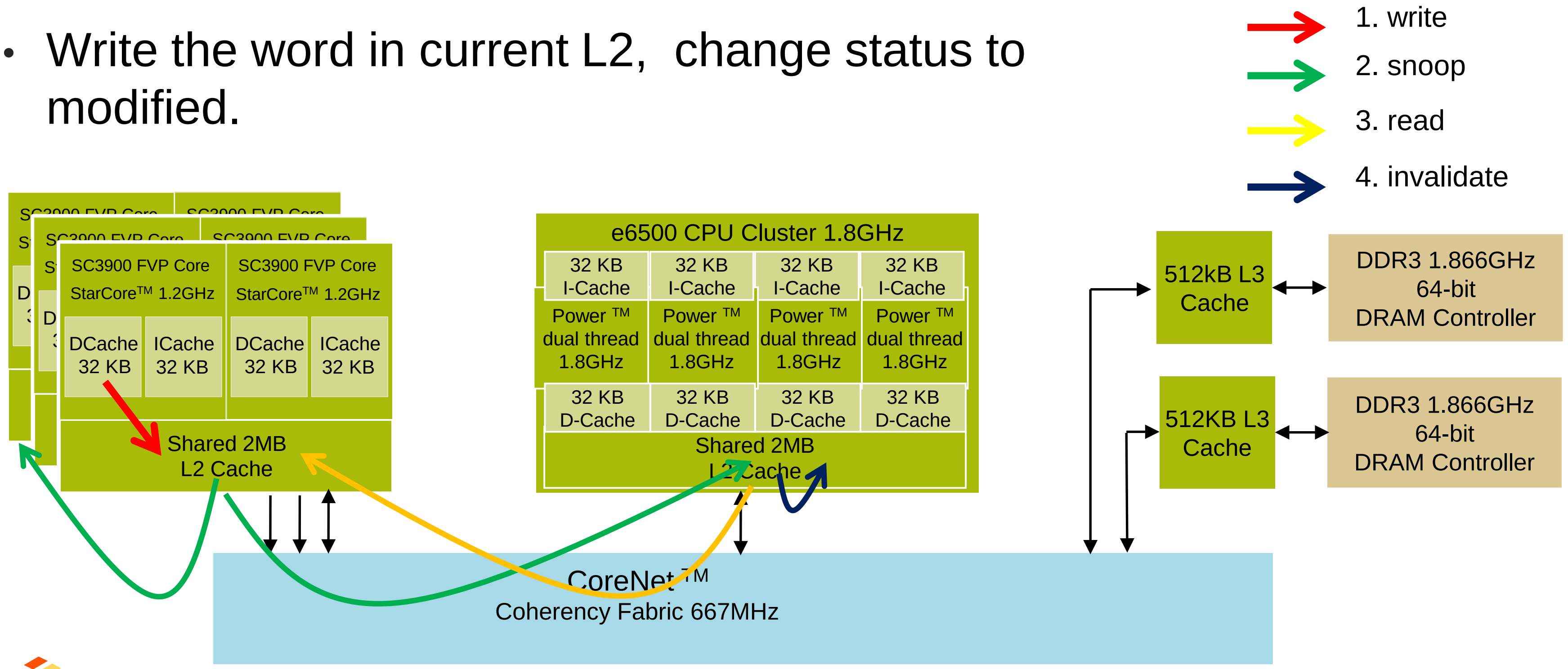
Coherency: write miss

- Read from other L2 if data is valid in other L2 or Read from system memory if data is not valid in any L2
- Update the word (overwrite part of or whole line)
- Invalidate the data in all other L2, change status to invalid
- Write the word in current L2, change status to modified.



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Coherency of L1

- Read cache
  - Back-invalidate by L2 (if L2 is invalidated, L1 is invalidated), done by hardware. So L1 read cache is hardware coherency.
- Write cache – SGB.
  - No hardware coherency.
  - For cacheable data, data will be kept in SGB as long as possible, software should use special instructions to flush SGB into L2 for coherency in case the data are shared with other cores or peripherals.
  - For non-cacheable data, data will not be kept in SGB.

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Coherency of L1

- The only coherency issue that needs software involvement is in the following case:
  - Core A writes data into a buffer for Core B or peripheral to read.
    - Typical cases:
      - DSP core shares data to other DSP cores
      - DSP core shares data to CPU cores
      - DSP core writes to Maple BD or DMA BD which is cacheable
      - DSP core writes to Maple input buffers or DMA source buffers
- Software solution:
  - Step1: Core A writes data
  - Step2: Core A executes a barrier, such as DBAR.IBSS.L12
  - Step3: Core A notifies other cores or peripherals to read the data (optional)
  - Step4: Core A executes a barrier, such as DBAR.IBSS.L12 (optional, when step 3 is through a shared cacheable flag)

- If data is used only by the same core, no coherency issue.

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Inter-core communication example

- Core 0 send, core 2 receive, through cacheable or non-cacheable buffer
  - Core 0 write data into a buffer
  - Core 0 issue a barrier instruction, such as DBAR.IBSS.L12
  - Core 0 send an interrupt to core 2
  - Core 2 read the buffer after getting the interrupt

- Hardware behavior in this case:
  - Core 0 write data into a buffer
    - Read from other L2
    - Invalidate other L2
    - Write into the buffer, only core0’s L2 keep the modified data (note that these 3 steps repeat for each cache line)
  - Core 0 send an interrupt to core 2
    - To make sure all data already in L2, add a barrier after the last write before sending interrupt.
  - Core 2 read the buffer after getting the interrupt
    - At this time core 2 L2 is invalid for the buffer data, it will snoop other L2
    - Flush core 0’s buffer into system memory
    - Read from core 0’s buffer
    - Core 0 and 2 L2 both keep the buffer

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Read-modify-write

- Read-and-reserve instruction
  - Reservation is done in 64 bytes resolution, the actual instruction size can be smaller
- Write conditional instruction
- Memory must be set coherent
  - Cacheable coherent, or
  - Noncacheable coherent.

```
_retry:
  [
   ldrstc ld.b (r0),d7
   sync.b
  ]
  [
   cmp.ne.l #0,d7,p0
   or.l #1,d7,d7
  ]
  if.p0 bra.nobtb _retry
  ldrstc st.b d7,(r0)

  jmprf _retry
```

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Coherent vs non-coherent

- Cacheable Coherent:
  - when read, hardware will check other L2 for most updated data
  - When write, hardware will invalidate other L2

- Cacheable Non-coherent:
  - When read, will not check other L2.
  - When write,
    - if access width is 64B, write directly to L2 without reading from other L2 or DDR.. Non-coherent writing is much higher performance than coherent writing
    - if access width is less than 64B, will read 64B from DDR then overwrite part of the data.

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