B4860 SoC Architecture

Overview

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Agenda

- Architecture Overview
- e6500 core presentation
- Interconnect Fabrics (CoreNet)
- Memory hierarchy
- Interrupt Scheme & Intercore Communication
- Boot & Trust Architecture
- SC3900 core presentation
- MAPLE-B3 overview
- CPRI complex
- Data path Architecture (DPAA)

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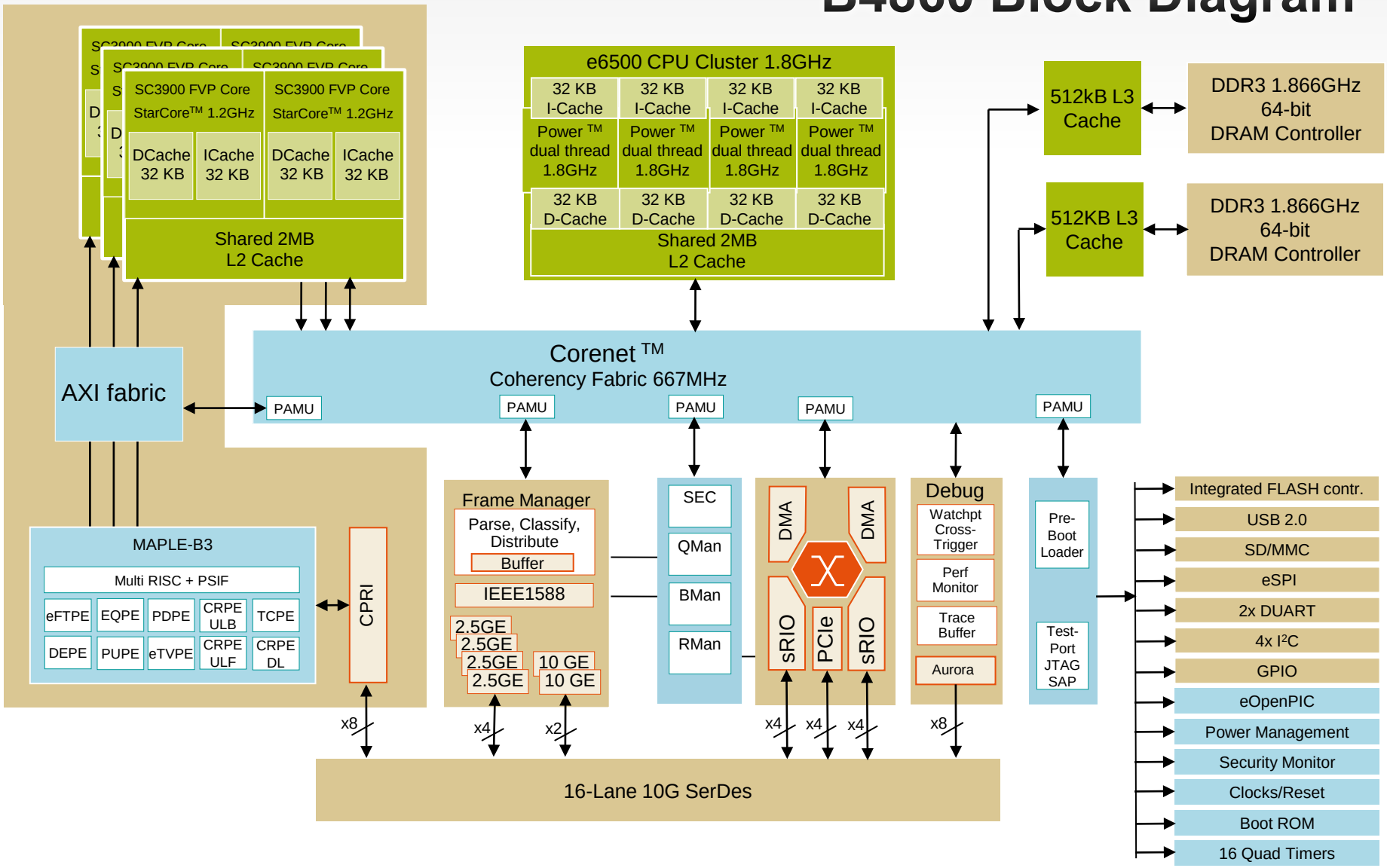
B4860 Block Diagram



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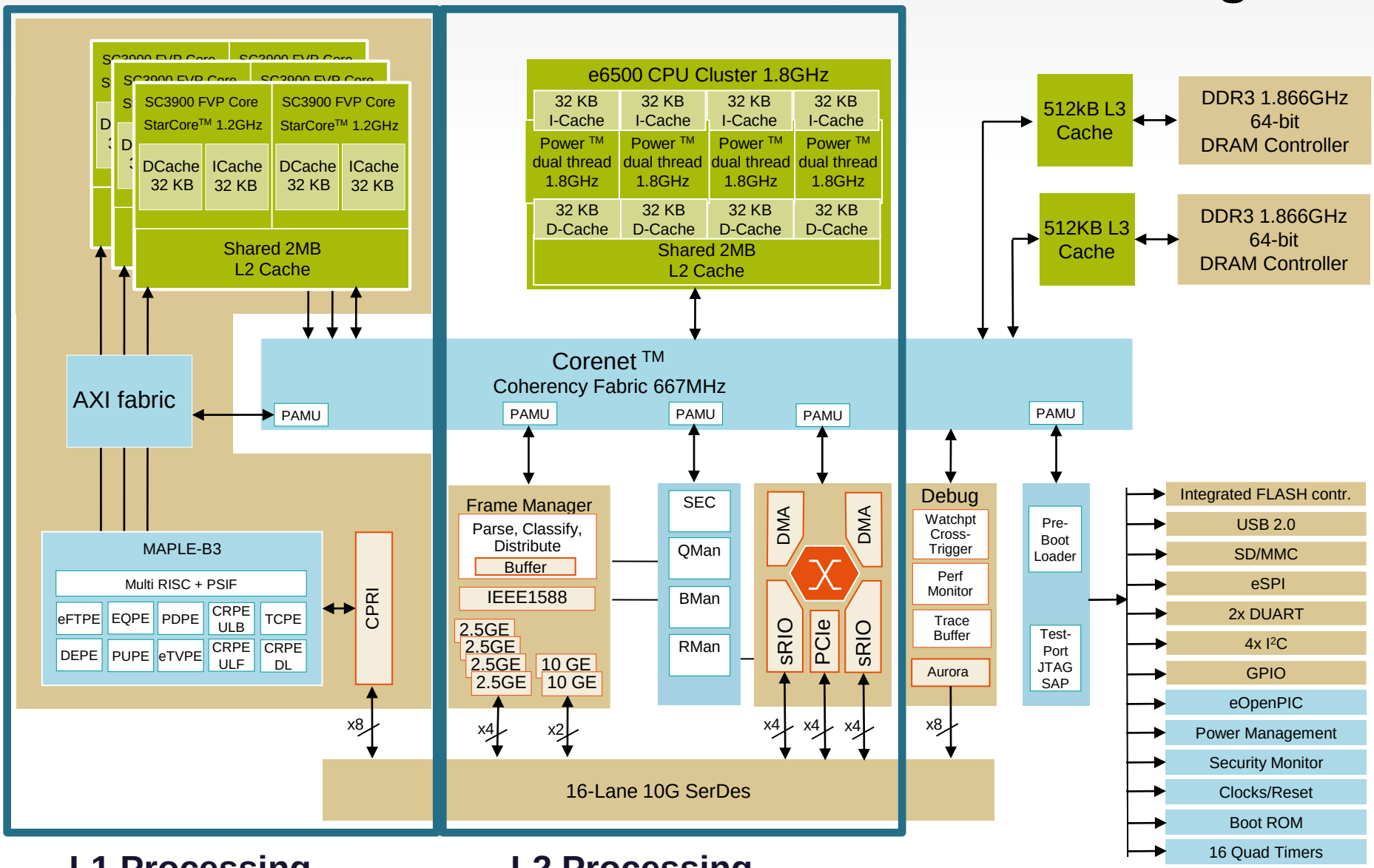

L1 Processing

L2 Processing

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e6500 Cluster

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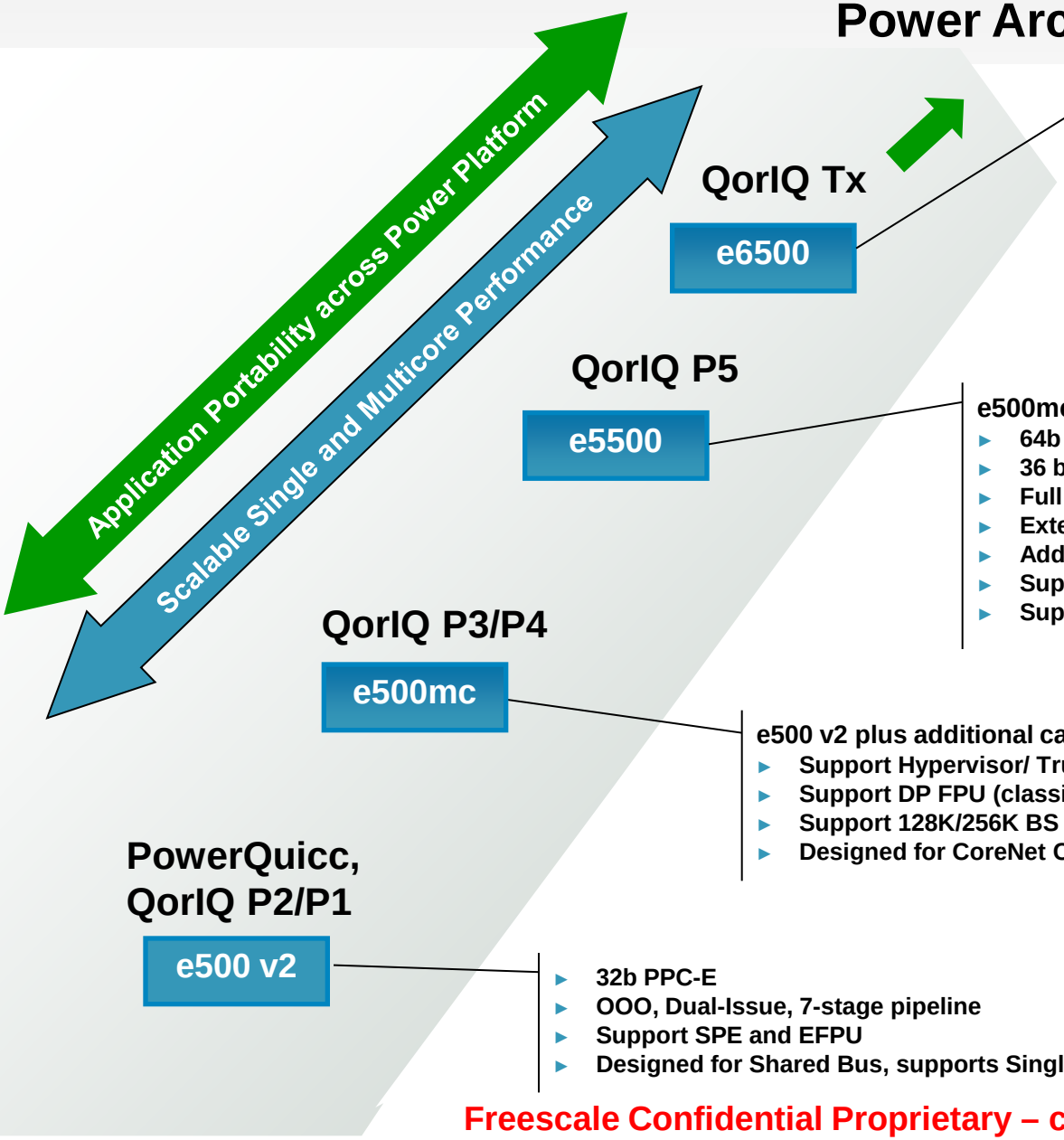
Power Architecture® Core Roadmap



e5500 plus additional capabilities:

- Dual-Threaded core (2 virtual cores per e6500core)
- 256-512KB L2 per core cluster
- Altivec SIMD 128b vector instruction Unit
- 40-bit real address
- Optimized power Mgmt
- HW PTW + LRAT for improved HV performance

e500mc plus additional capabilities:

- 64b ISA2.06
- 36 bit addressing (64GB) per process
- Full speed FPU
- Extended Branch Predictor for 64b mode
- Additional Integer/FP instructions
- Support 512KB BS L2
- Supports 32-bit mode for software legacy

e500 v2 plus additional capabilities:

- Support Hypervisor/ Trust Architecture (secure Boot, anti-Tamper/Detection
- Support DP FPU (classic), decorated L/S instructions
- Support 128K/256K BS L2, 64 entries MMU TLB variable size, 64B CL
- Designed for CoreNet Coherency Fabric, double snoop BW

- 32b PPC-E
- OOO, Dual-Issue, 7-stage pipeline
- Support SPE and EFPU
- Designed for Shared Bus, supports Single & Dual-core

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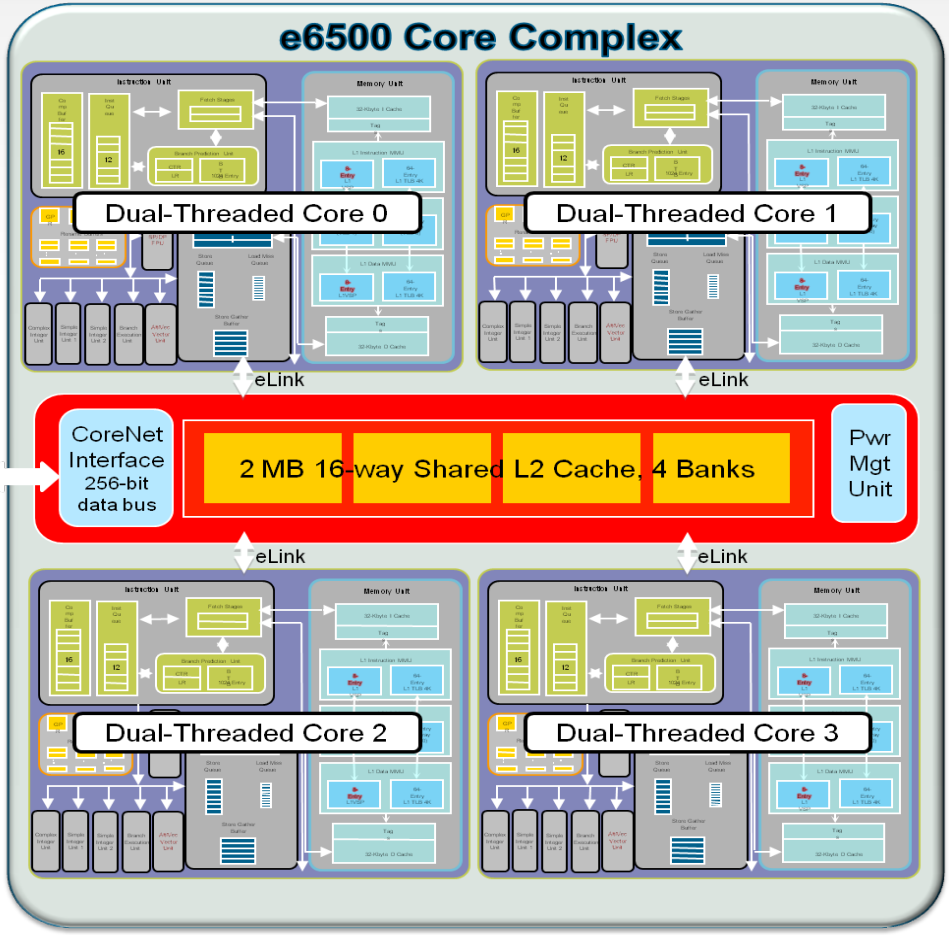
e6500 Core Complex



- 64-bit Power Architecture
- 28nm Technology
- e5500 core features plus:
- Two threads per core (SMT)
- Dual load/store units, one per thread
- Shared L2 in cluster of 4 cores (8 threads per cluster)
  - 2048KB 16-way, 4 Banks
  - High-performance eLink bus between coreLd/St and instruction fetch units
- Enhanced MP Performance
  - Accelerated Atomic Operations
  - Optimized Barrier Instructions
  - Fast intra-cluster sharing
- AltiVec SIMD Unit
- CoreNet BIU
  - 256-bit Din and Dout data busses
- 40-bit Real Address
  - 1 Terabyte physical addr. space
- Hardware Table Walk

- Each thread: Superscalar , seven-issue, out-of-order execution/in-order completion, Branch units with a 512-entry, 4-way set associative Branch Target/History
- Execution units: 1 Load/Store Unit per thread, 2 Simple integer per thread, 1 Complex for integer Multiply & Divide, 1 Floating-point Unit, Altivec
- 64 TLB SuperPages, 1024-entry 4K Pages, 40-bit Physical Address

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Feature Improvements from e500mc to e6500 – 1 of 2

Architecture:

- 64-bit architecture
  - 64b extensions: GPRs, Effective Address, Instruction set capability
  - Supports both 64b native and 32b compatible modes
- Multi-threading
- New Power ISA v.2.06 Instructions
  - instructions for byte- and bit-level acceleration: Parity, population count, bit permute, compare bytes , FPU convert to/from 64-bit integer
- AltiVec
  - Legacy Altivec ISA + addition of new features

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Feature Improvements from e500mc to e6500 – 2 of 2

Core Memory subsystem:

- Re-architected the memory subsystem with shared and larger L2 cache

MMU enhancements

- 4k TLB0 entries from 512 entry, 4-way set associative in e500mc/e5500 to 1024 entry, 8-way set associative
- 4KB to 1TB page sizes in TLB1 (variable pages TLB)
- Added HW-based page tablewalk
- Added hardware LRAT (Logical to Real Address Translation)

MP performance enhancements

- Faster atomic operations, elemental barriers, intra-cluster sharing

Debug architecture enhancements

- Guest-level Performance Monitor support, more counters

Power management features

- New power states and power reduction techniques

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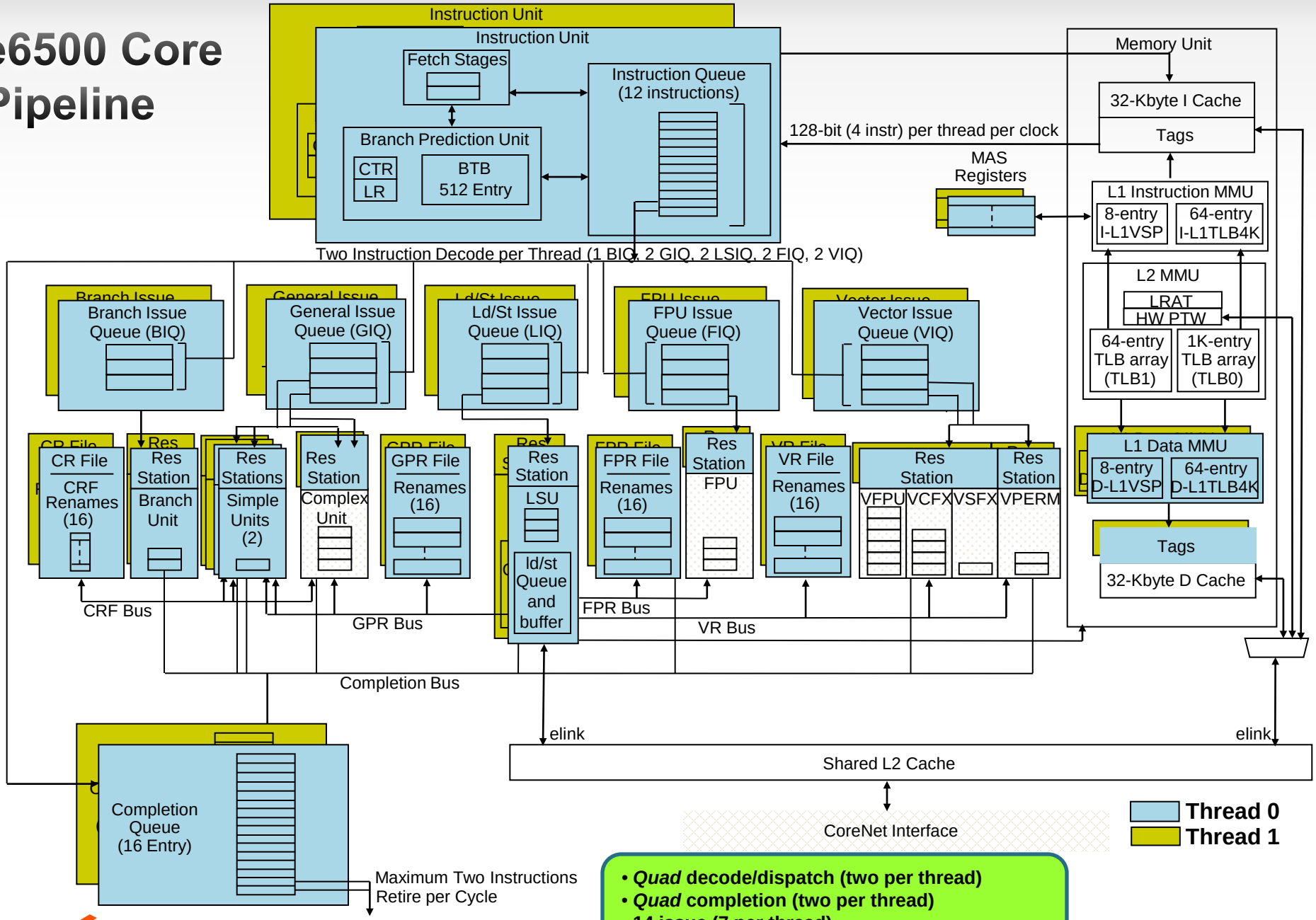
e6500 Core Pipeline



- ***Quad* decode/dispatch (two per thread)**
- ***Quad* completion (two per thread)**
- **14 issue (7 per thread)**
- **14 execution units**

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Multithreading: Software Perspective

- The thread model is an SMP model
  - Exception being some shared resources owned by the hypervisor
- From software's perspective, running on a thread is no different than running on another processor core
- Things that are shared among threads are *shared*, things that are replicated per thread are *private*

Private State

- GPRs, FPRs, VRs
- Most SPRs
- Interrupts, GIVPR, GIVOR
- Processor Identification Register (PIR)
- Timers, Timer Control Register (TCR) and Timer Status Register (TSR)
- Watchdogs: A final timeout from either thread may result in the entire core being reset

Shared State

- L1 Instruction and Data Caches
- IVPR, IVOR
- Memory mapped register
- MMU control and configuration registers: But both threads can translate simultaneously

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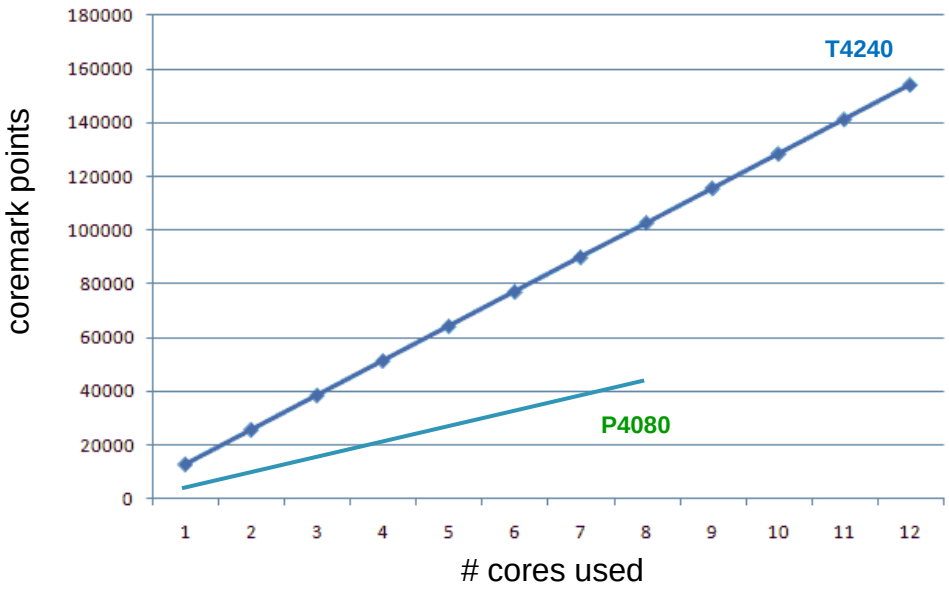
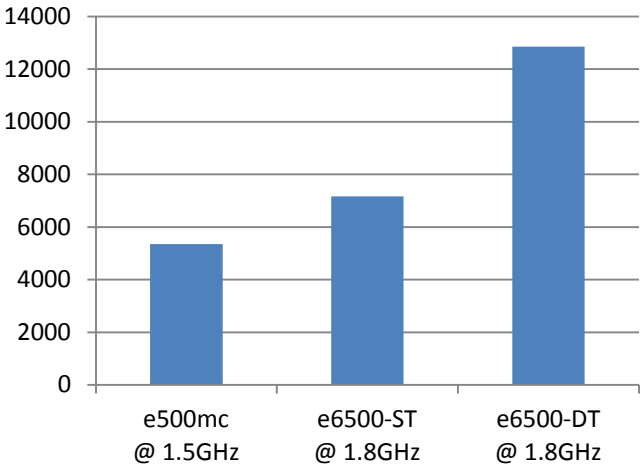
Optimized CoreMark results: T4240 @ 1.8GHz

- CoreMark has a ~ 16k footprint and fits in L1 for all high-end devices, hence it does not test memory subsystem. It is best used to show pipeline and execution unit performance.
- e6500 @ 1.8 GHz in ST mode gives **7197** coremarks
- e6500 @ 1.8 GHz in DT mode gives **12852** coremarks
- Scaling on T4240 indicates to be perfect, see below
- Aggregated score is **154224** coremarks for 1.8GHz T4240





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AltiVec in QorIQ-AMP

- **Classic AltiVec Basics:**
- 32 registers, each 128-bit wide
- Vector packs:
  - 16 8-bit
  - 8 16-bit
  - 4 32-bit integers
  - 4 32-bit single-precision floating-point data
- 156 Instructions
- Number of SIMD operations dependent upon data type
- Powerful permute unit
- Reference: AltiVec Technology Programming Environments Manual

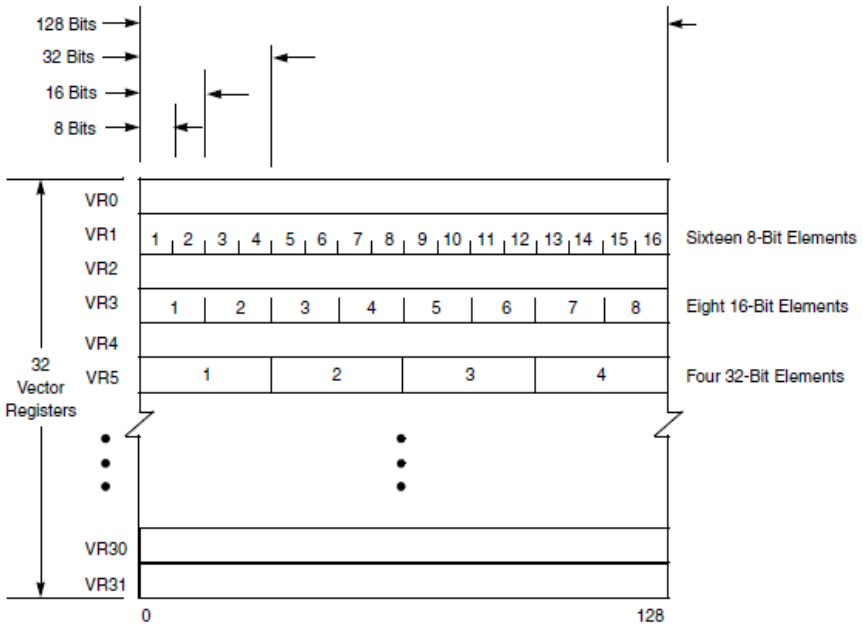

Figure 2-3. Vector Registers (VRs)

- **e6500 Enhancements:**
- Move from GPR to VR
- Absolute differences operation
- Extended support for misaligned vectors, handling head and tail of vectors

Each e6500 core can deliver up to 14.4 GFLOPS with AltiVec FPU

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Interconnect

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SoC Fabrics

- B4860 has two main fabrics
  - Corenet fabric
  - AXI fabric
- Corenet fabric is the major fabric
  - Connect between PPC cluster, DSP clusters, OCeaN world, FM and other to CPC/DDR memories.
- AXI fabric
  - Connect between Maple units, CPRI to SC3900 clusters and to corenet fabric

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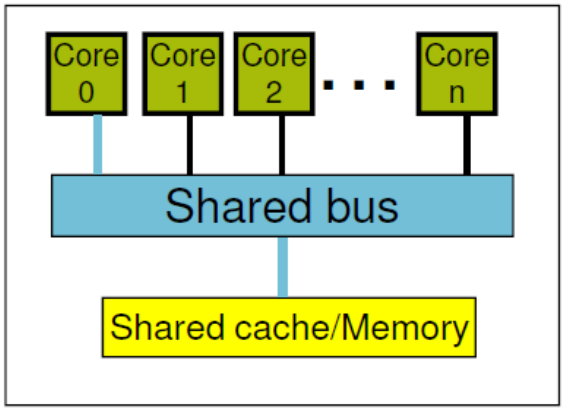
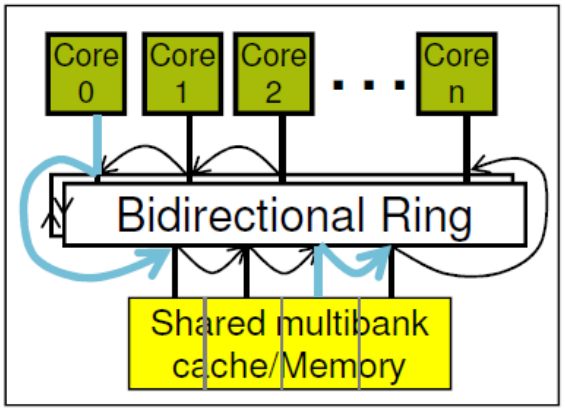
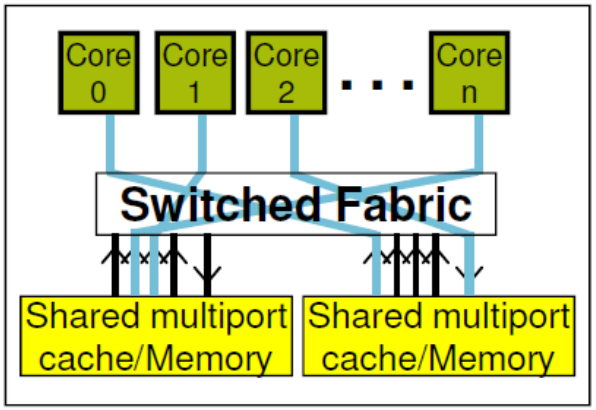
16

Interconnect Topology is Key for Scalability







As just seen:
- Simple & low latency, but one transaction/cycle.
- Frequency & bandwidth decrease with more cores, as latency increases.

- Sustains two transactions per cycle
- But high latency (one hop per cycle – at best).
- R/W Bandwidth does not scale with ring size.
- Cost scales well (O(N)).

- Sustains multiple transactions/cycle yielding highest BW and shortest average latency.
- Bandwidth scales with fabric size.
- Cost does not scale well ($O(N^2)$).

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CoreNet Feature

- **Architecture**
  - Multiple implementations (Cost/Performance Trade-off)
- **Coherent multi-core interconnect**
  - MESI
  - Event driven protocol
- **Scalability**
  - Connectivity scalability: Single core, Multi-core, Multi-cluster, Multi-chip; Topologies
  - Bandwidth scalability: Address, Coherency, Data (Width, Number)
  - Frequency scalability
- **Other differentiating features**
  - Retry-free protocol
  - Stashing
  - Fast Inter-processor communication
  - Selective snooping
  - System Partitioning
  - Multi-clock design
    - Better power control

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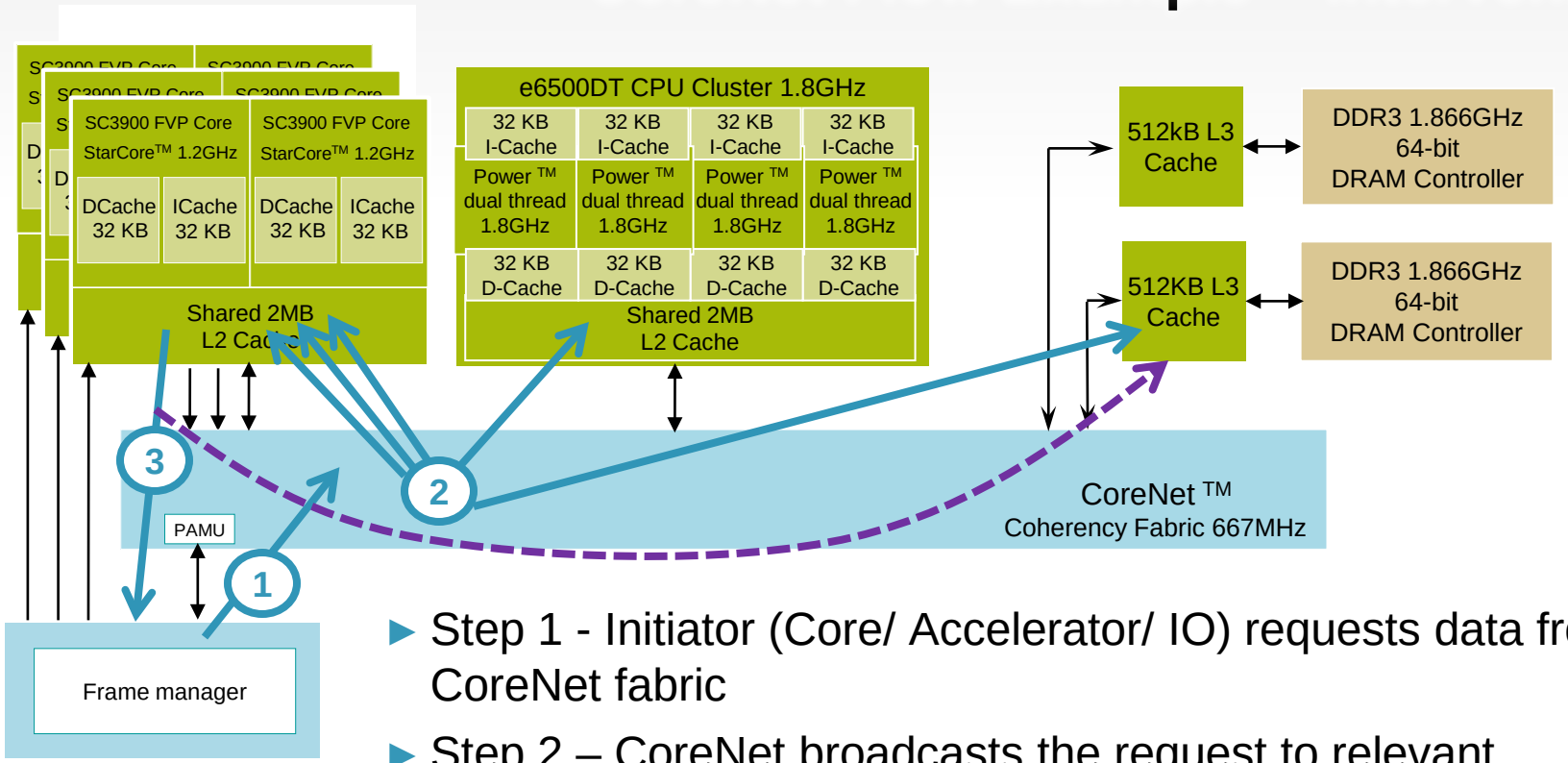
CoreNet Flow Example - Intervention



- Step 1 - Initiator (Core/ Accelerator/ IO) requests data from CoreNet fabric
- Step 2 – CoreNet broadcasts the request to relevant initiators/target that might have the data
- Step 3 – An initiator/Target which has the latest data responds and the data reaches the requestor (and optionally to memory) without a need for SW intervention

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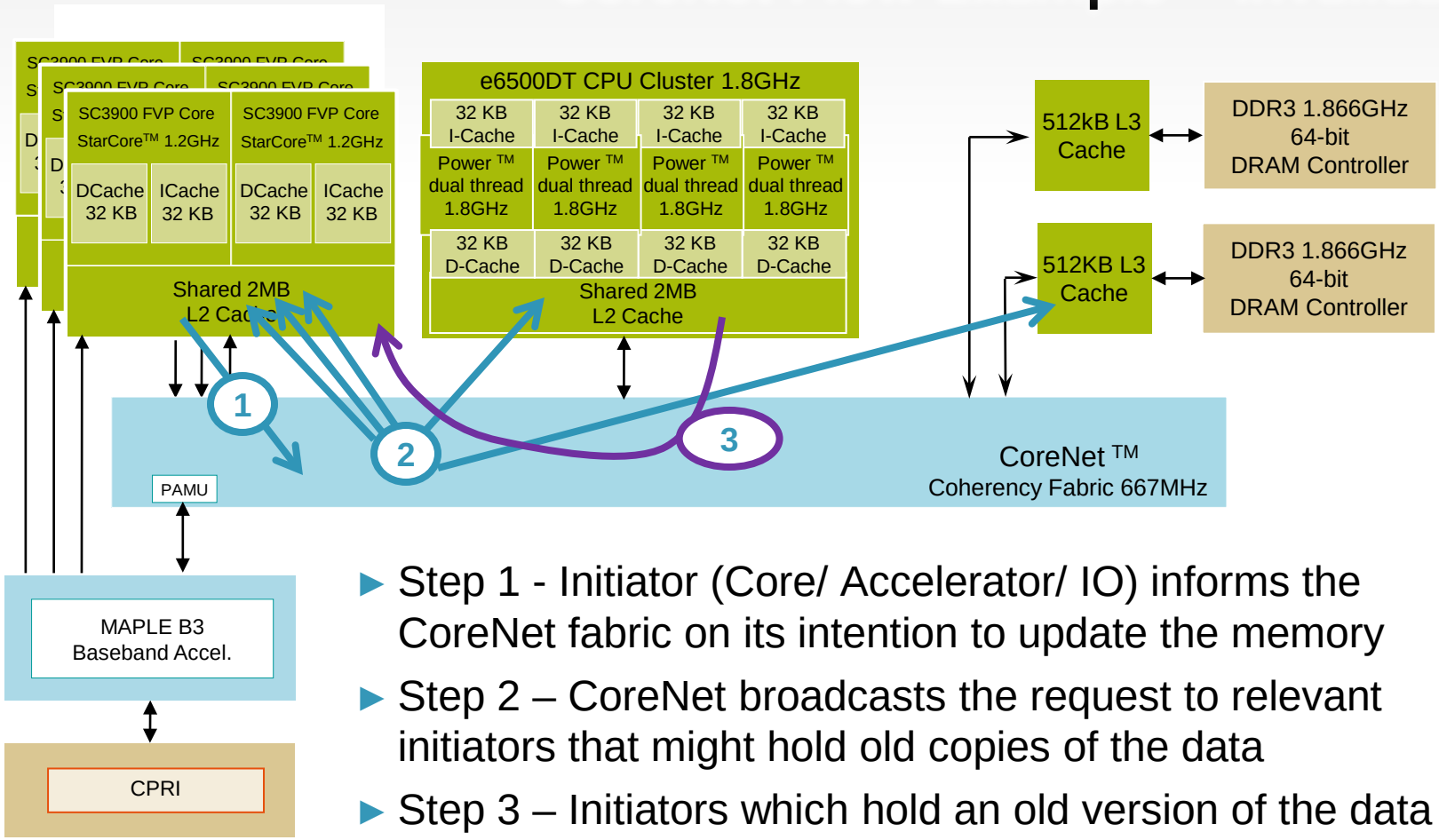
CoreNet Flow Example - Invalidation



- Step 1 - Initiator (Core/ Accelerator/ IO) informs the CoreNet fabric on its intention to update the memory
- Step 2 – CoreNet broadcasts the request to relevant initiators that might hold old copies of the data
- Step 3 – Initiators which hold an old version of the data invalidate it and the write data is returned to the requestor

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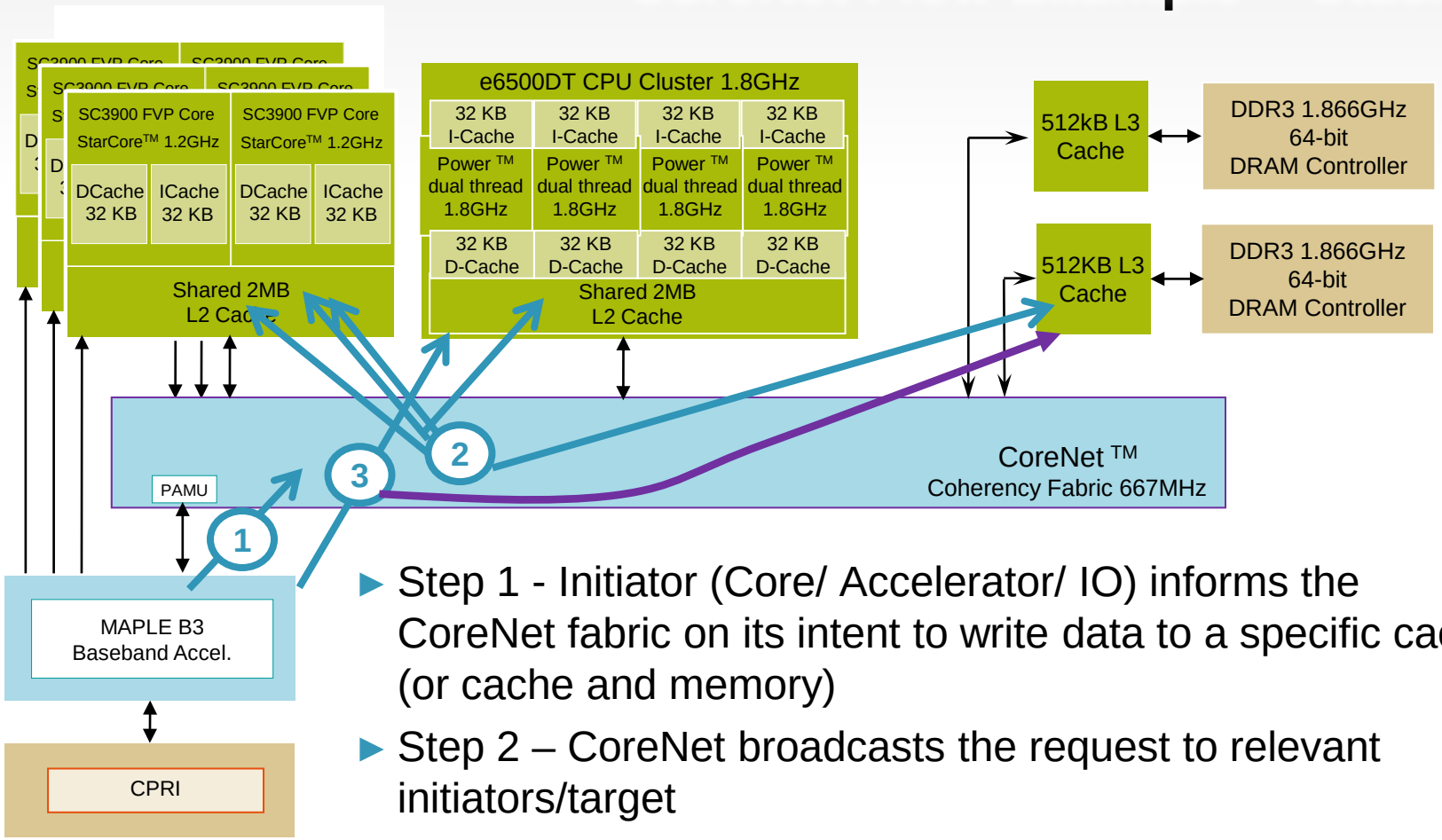
CoreNet Flow Example - Stashing



- Step 1 - Initiator (Core/ Accelerator/ IO) informs the CoreNet fabric on its intent to write data to a specific cache (or cache and memory)
- Step 2 – CoreNet broadcasts the request to relevant initiators/target
- Step 3 – The data is written only to the designated target(s)

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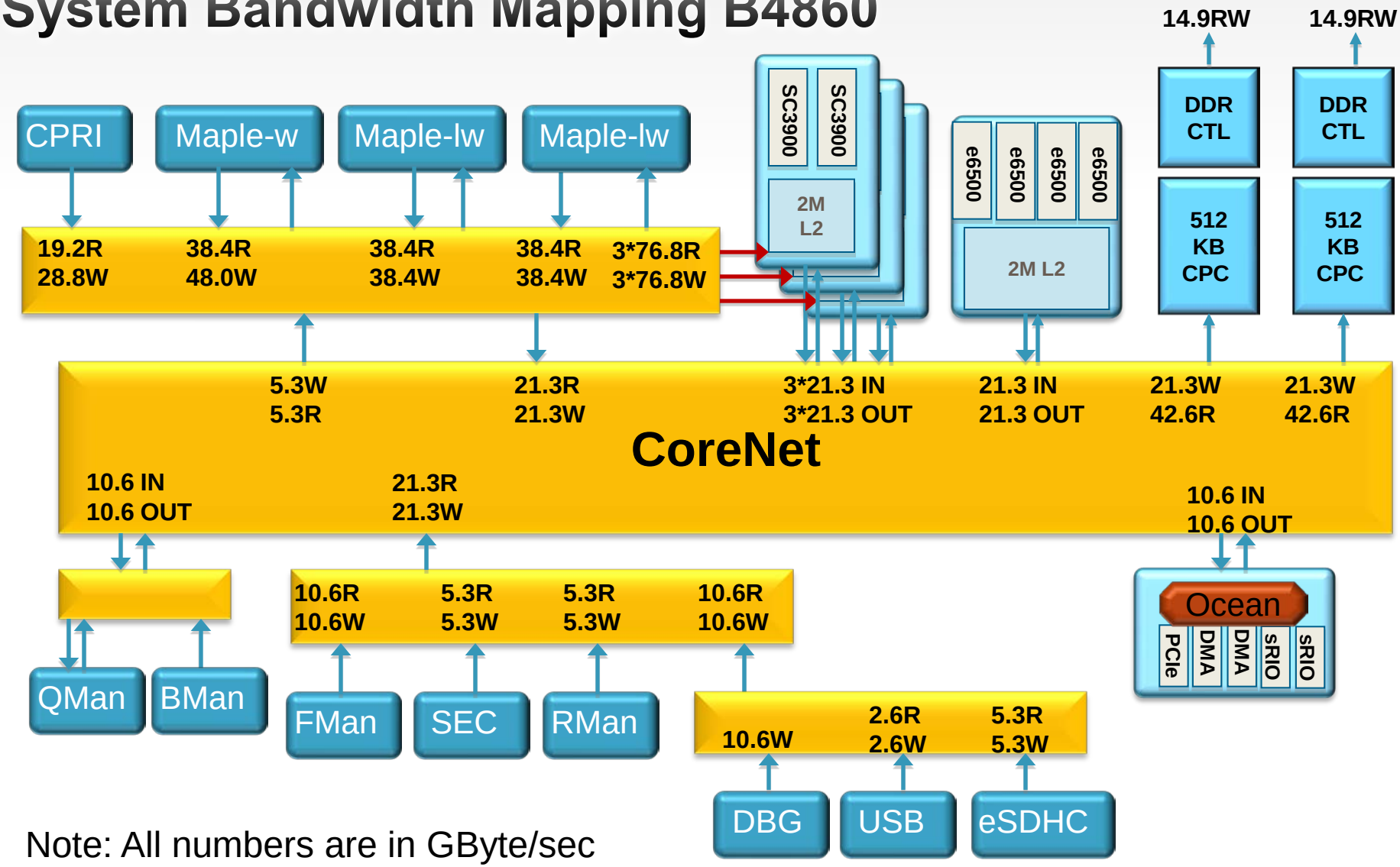
21

System Bandwidth Mapping B4860



Note: All numbers are in GByte/sec

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Software view of CoreNet

- CoreNet is not visible to software
  - FSL Internal-only functionality
  - Software-independent operation
  - Implementations can vary widely
- Some other functions are visible:
  - **Address map:** "Local Access Control" Architecture
  - **Error capture and interrupt enablement**
    - Hardware: ECC, HW data corruption
    - Software: Address map errors, Coherency mistakes
  - **Performance Monitoring**
    - Hot spots; Inefficient software
  - **Debug**
    - MP performance debugging

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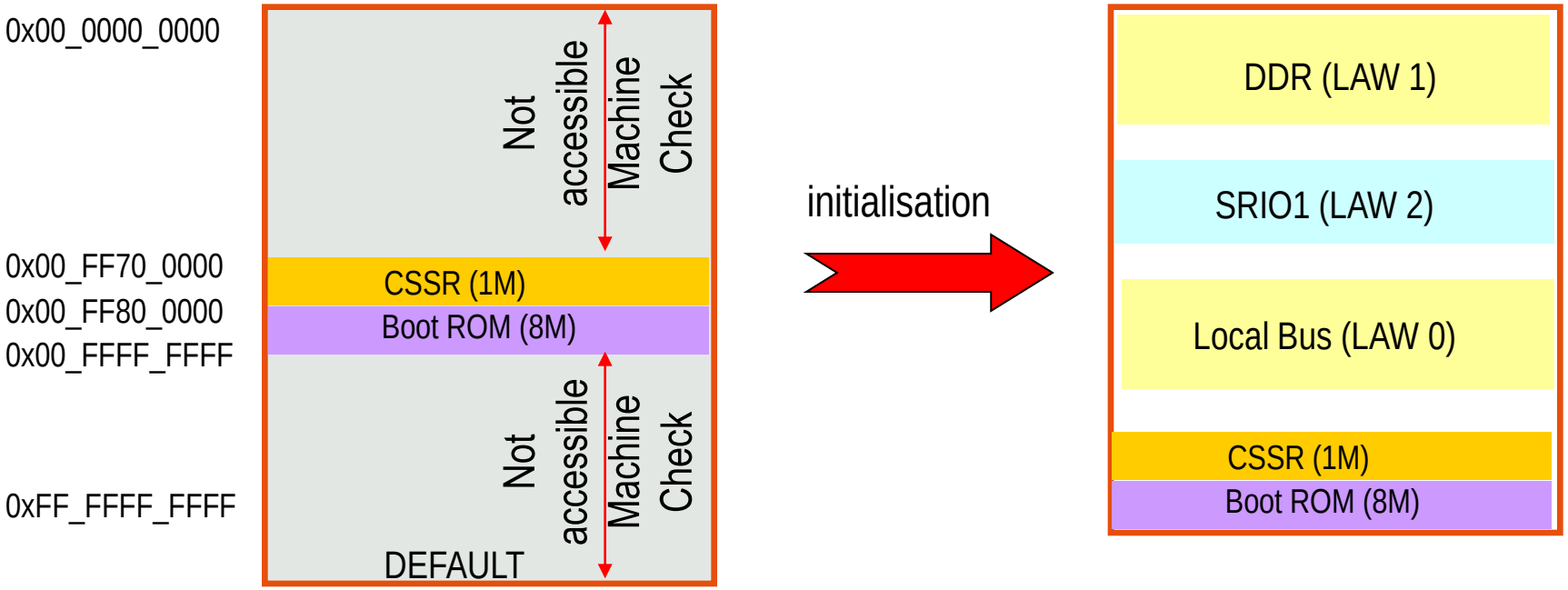
Local Addess Windows (LAW)

- Local memory map is defined by a set of 32 LAWs
- Associate 40-bit address space with a target interface (srio,ddr,lbiu….)
- No Address translation, size 4K to 1Tera bytes
- other local windows CCSRBAR, DCSRBAR, boot ROM, CPCSRCRs…



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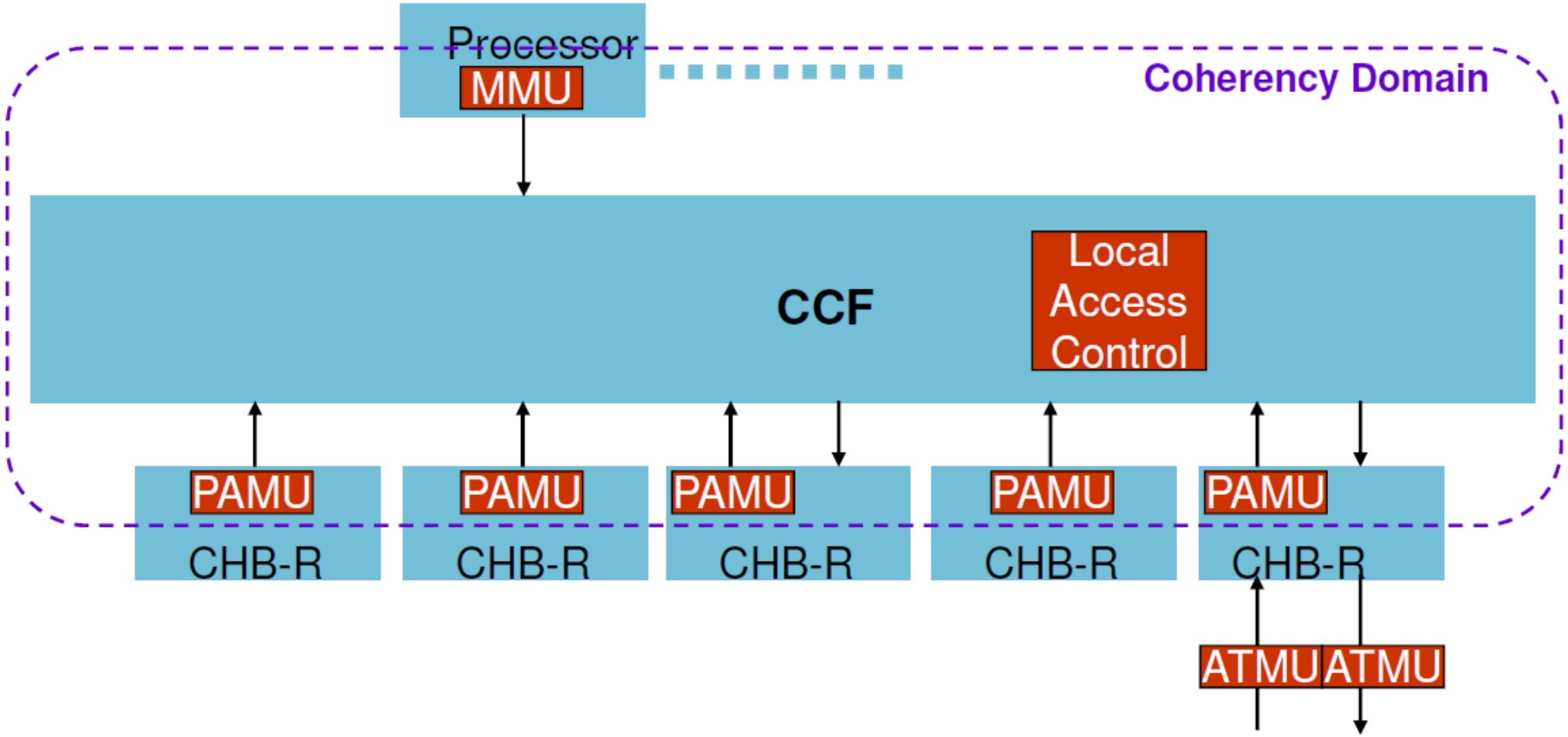
Address Translation in B4860



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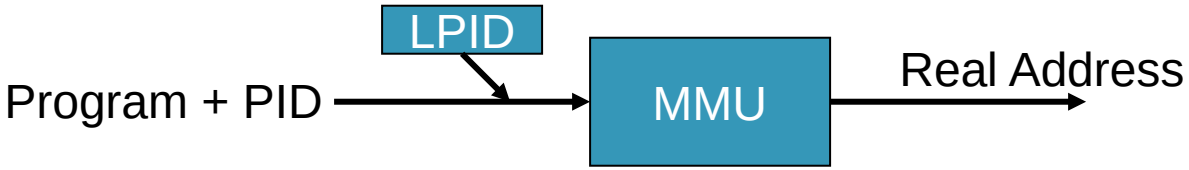
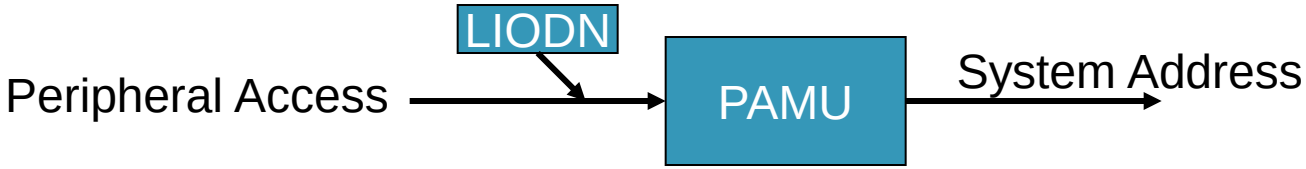
Address Translations and Access Protections

- Programs access address space of the client OS
- OS address space is virtualized via LPID
  - LPID assigned by Hypervisor
- Virtual address authorized and translated to real address via MMU
  - MMU and translation owned and set up by Hypervisor



- IO accesses address space of the client OS
- IO accesses carry an “LIODN” field
  - LIODN assigned by Hypervisor
- I/O accesses are authorized and translated to real address via PAMU (IOMMU)
  - PAMU and translation owned and set up by Hypervisor
- Also enables self-virtualized peripheral devices



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Memories

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DDR Controllers

- B4860 has Two DDRs Controllers which run at 1.866GHz DDR
- Support for a 64-bit and 32-bit data interface
- Four chip selects
  - 8 GByte support per chip-select
- Programmable voltage supporting
  - both DDR3 and DDR3L (but not simultaneously)
- Special hashing mechanism to increase performance
- Accesses towards DDR are re-ordered to increase performance while keeping logical accuracy.
- Full ECC support
  - single-bit error correction
  - Multi-bit error detection
- On-die termination support
- Support for DIMMs/Discrete components

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L3 cache

- B4860 instantiates two L3 caches
  - Located between the corenet fabric and each DDR controller

- Each Cache has the following features
  - 512 KB cache
  - 16-way cache array configurable to any of several modes on a per-way basis
  - Unified cache, I-only, D-only
  - Configurable as Write-Back or Write-Through
  - Pseudo LRU replacement algorithm
  - Stashing of all transactions and sizes supported
  - Explicit (CoreNet signaled) and implicit (address range based) stash allocation
  - Addressable M3 SRAM
  - ECC protection

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Interrupt Scheme

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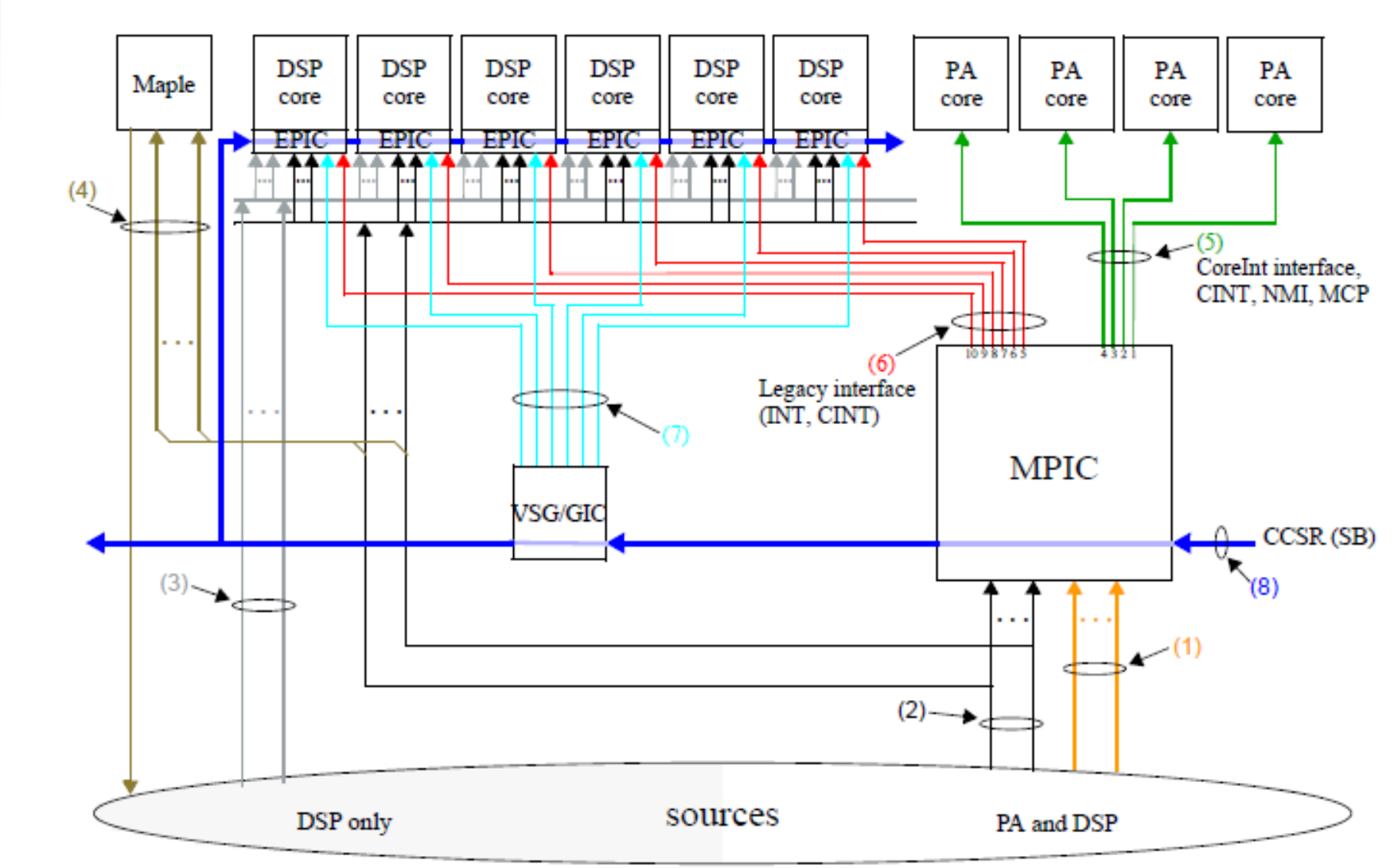
B4860 Interrupt Scheme



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B4860 Interrupt Handling

- MPIC
  - Concentrates and dispatches interrupts to e6500 cores and SC3900 cores
  - 194 - Internal Interrupt sources
  - 12- External Interrupts
  - 20 – error interrupts
  - MPIC-Defined Interrupts
    - Message Interrupts
    - Shared Message Interrupts
    - Inter-processor Interrupts
    - Timer Interrupts

- EPIC
    - Each EPIC handles 32 internal interrupts + 444 SOC interrupts
    - Dispatches the highest priority interrupt to SC3900

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B4860 inter core communication

- The e6500 cores and SC3900 cores can communicate in several ways:
  - Queue Manager can be used to transfer messages/tasks between cores.
  - The MPIC includes a variety of inter-core communication flows and generates interrupts towards the e6500 cores. The e6500 cores and SC3900 cores can activate these interrupts.
  - B4860 instantiates virtual interrupt controllers
    - These interrupts are connected to the SC3900 cores
  - e6500 cores and SC3900 cores share the same software semaphore mechanism, and can use it for semaphoring
  - The e6500 cores and SC3900 cores can send doorbells to each other via the Corenet fabric.
  - Eight hardware semaphores are instantiated.
    - They may be used by internal and external masters.
  - Interrupt mesh network between the SC3900 FVP cores.

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Boot sequence

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Overall Boot sequence – 1/2

(simplified … see Ref.Manual)

PO_Reset (PORESET asserted, min 32x Sysclk)

→ HRESET asserted

Sample POR Config Pins
(upon deassert of PORESET)

Incl. Cfg_RCW_SRC[0-4], selecting the source of further RCW step
(select hard-coded options or I2C, SPI, eSDHC, eLBC)
plus config related to DDR3, Serdes PLL, eLBC/ECC,

Pre-Boot loader loads RCW data
512bits from selected source
(→ to RCWSR regs)

Including:
. All PLL parameters
. Serdes config
. Pre-BootLoader source I/F
(I2C, SPI, eLBC, eSDHC)
. Cores hold-on/off (all cores hold-off / core_0 hold-on, others hold-off)
. Boot location
. Secure Boot enable
. DDR param.
. Pin Muxing config.

hard-coded RCW option

PLL's locked
HRESET released

PBL (part-2)
Pre-Boot initialization

Pre-Boot Loader: internal sequencer supporting various low-speed interfaces (I2C, SPI, eLBC, SD/MMC) for pre-configuration of memory & peripherals+ pre-loading of data to fast-memory (DDR). PBL can release Core0 from reset for booting from DDR.
Before local windows are later initialized by Boot/OS, PBL can reach any address in the local space by configuring ALTCBAR.

Secure Boot
enable ?

Run ISBC (Internal Secure Boot Code)
. Does validation check of further external boot image
(pointed by CCSR register)

→ If fails, HALT

Pass-OK or
fails (then no access to secret keys)

Note: activating HRESET will not sample POR Config Pins again

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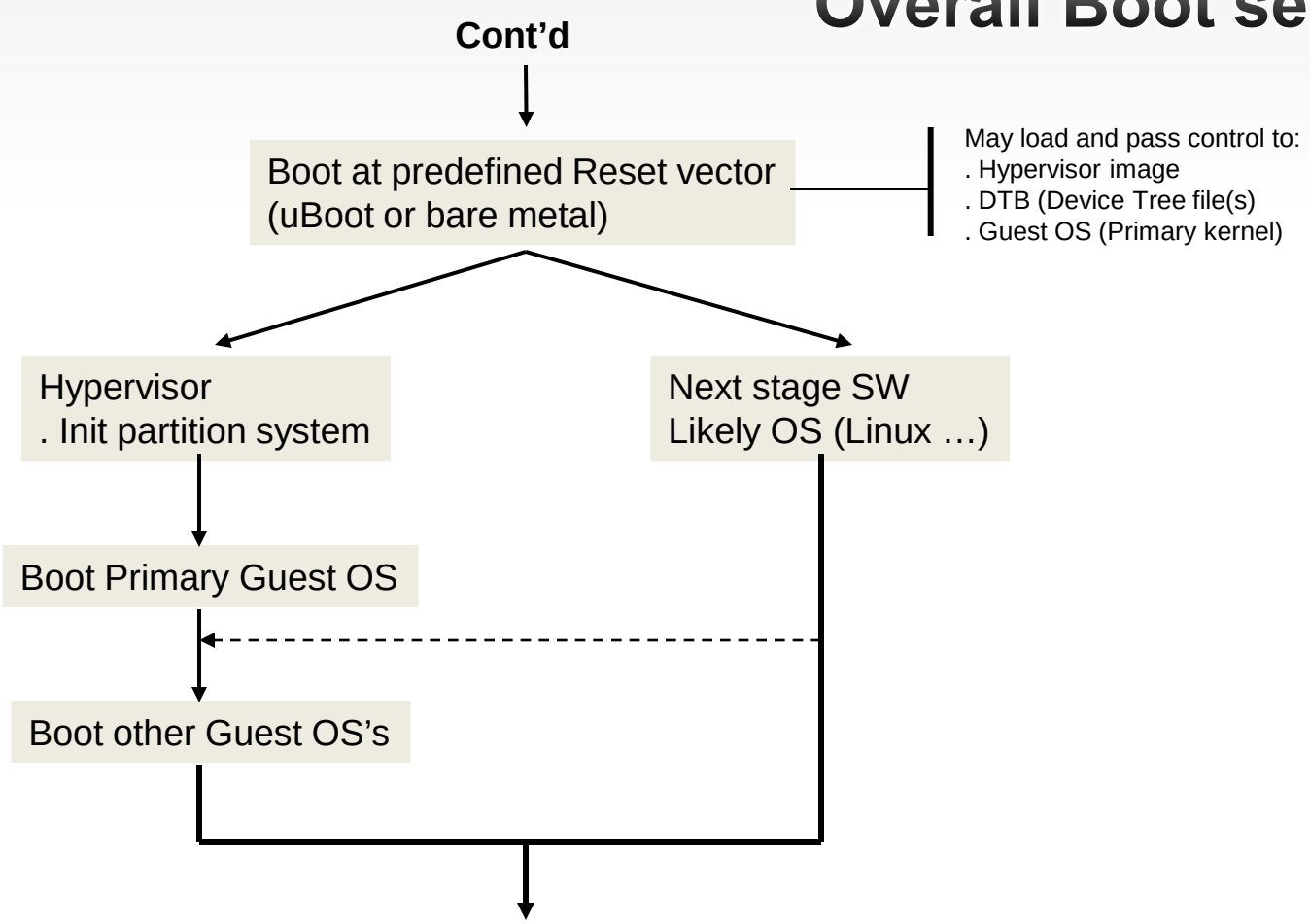
Overall Boot sequence – 2/2



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SC3900 FVP Core

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SC3900 Flexible Vector Processor

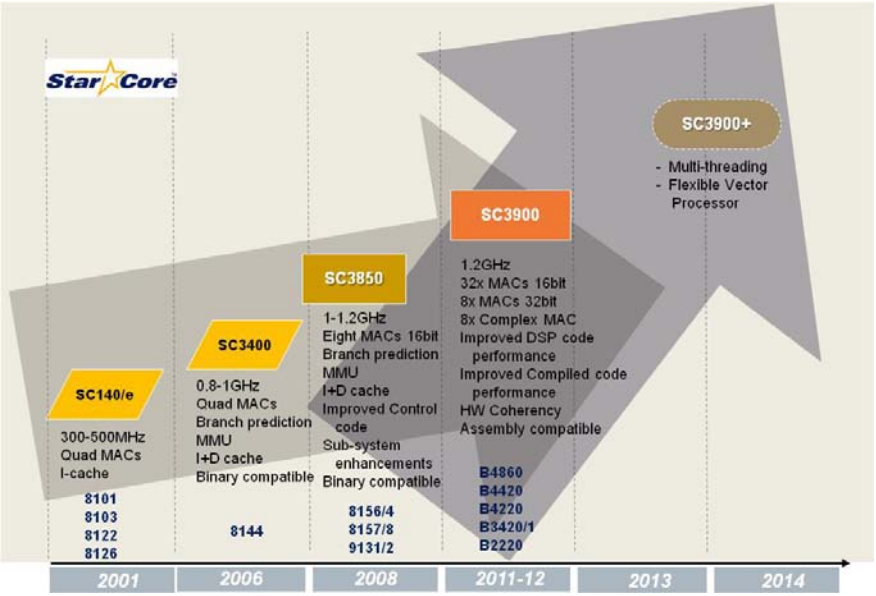
- **Leap in computational performance**
  - High performance for Matrix/Vector and Complex number algebra
  - Architecture tailored for Baseband applications processing
  - High floating point performance (up to 16 FLOPs per cycle)

- **High level programmability**
  - Excellent Out Of the Box compiled code performance for both DSP and Control code

- **Cutting edge memory system**
  - Data streaming capabilities

- **State-of-the-Art Multi-Core**
  - HW coherency support
  - Out of order bus fabric
  - Multi-core tracing capabilities

- **Good power efficiency**
  - High utilization
  - State of the art high frequency low power design methodologies



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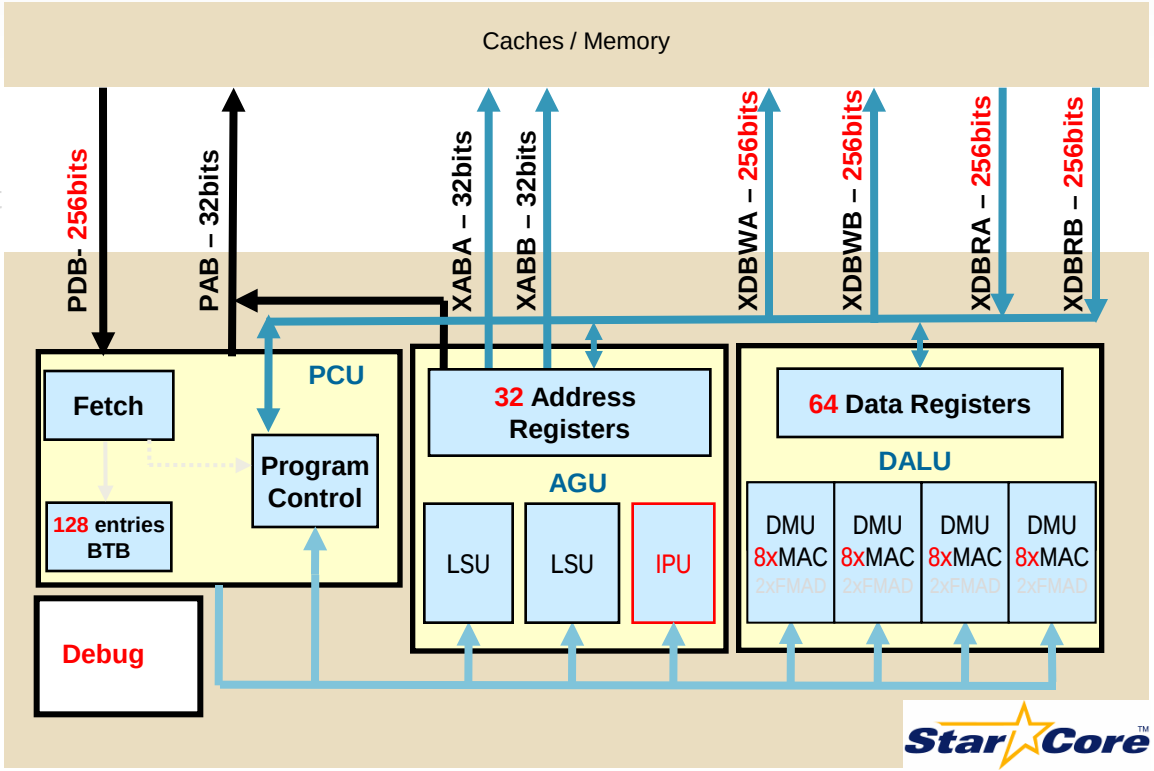
SC3900 FVP Core Block Diagram

SC3900 Main Features:

- ►4 symmetric DMUs in the DALU
  - **32xMACs** per cycle
  - **4xSIMD8/vector** support
  - Single Precision Floating Point support (up to 16 Flops)
- ►**High memory bandwidth**
  - Program bus – 256 bit/cycle
  - Data bus – up to 1024 bit/cycle
- ►Address & integer unit
  - 2 Load/Store units
  - General Integer Processing Unit (IPU)
  - Support multiply and shift
- ►**Large register files**
  - For both AGU and DALU
- ►Enhanced compiler support
  - Improved predication
  - Enhanced prediction mechanisms
- ►**Enriched Instruction Set**
  - New binary & syntax
- ►Improved Multi-core Debug and trace features



Main difference vs. SC3850 are marked in red

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SC3900 Optimized for Baseband L1 Processing

- SC3900 is optimized to efficiently handle Baseband Layer 1 processing

- L1 processing can be divided into three categories:
  - Computation intensive DSP code (mainly MAC intensive)
  - Data manipulation and less intensive DSP code
  - Control code

- Each one of the categories is non-negligible in processing requirements
  - Although dependent on the use-case
- There is no clear boundary separation

- SC3900 accelerates all types of Baseband L1 processing

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Computation Intensive DSP Code Acceleration

- SC3900 provides Vector processor capability by increasing the execution units and the **whole datapath** accordingly
  - Up to 32 MACs per cycles (**4x** versus SC3850)
  - 64 dedicated data registers of 40bit each (**4x** vs. SC3850)
  - Up to 1024bit (128B) core-to-L1 Data Cache throughput per cycle (**8x** versus SC3850)
    - Strong and flexible cache based data streaming abilities

- SC3900 optimized datapath lead to high MAC utilization

- Performance:
  - SC3900 is **3.5x-4x** better than SC3850 in intensive DSP code

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L1 Processing - Data Manipulation Acceleration

- "Data manipulation" stands for many different functions existing in Baseband Layer 1 - For examples:
  - Data preparation before/after intensive kernels
    - Ex: data re-ordering, matrix transpose, pack/unpack
  - Less regular kernels or serial/cyclic kernels with low parallelism
    - Ex: QR Decomposition, IIR, Interleaver, encoder.

- SC3900 architecture addresses "Data manipulation" by different means:
  - Datapath flexibility: This is the "Flexible Vector Processor" essence
    - Register file flexibility: Each unit can read/write any registers
    - Execution unit flexibility: Each unit can run different and independent instructions
  - Rich and flexible Instructions set
    - Efficient instruction set which large support of different data type and size
    - New powerful data manipulation specific instructions

- Performance:
  - SC3900 is **2x-3x** better than SC3850 in "Data Manipulation"

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L1 Processing - Control Code Efficiency

- One of the SC3900 goals is to improve in control code efficiency
  - L1 control functions are tightly integrated with the Arithmetic intensive SW
  - Useful for running scheduling functions that are control intensive

- Control code performance is affected by two main aspects:
  - Core and Compiler efficiency in typical control code constructs
  - Memory system efficiency

- Both have been addressed on the SC3900 – few examples:
  - Ability to flatten decision trees using multiple predicates
  - Third AGU unit with multiply and shift for address calculation and boost control code performance
  - Full support for non-aligned memory access without penalty
  - Larger, clustered 2MB L2 cache to keep the program close to the core

- Performance:
  - SC3900 is up to **1.5x** better than SC3850 in control processing

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SC3900 Instruction Set

- Robust and flexible Instruction set
  - Significant improvement over previous generations
  - Instructions are highly flexible and fit wide range of DSP operations
  - For example, MAC instruction is defined to support:
    - Single precision 16bx16b, mixed-precision 16bx32b and double precision 32bx32b
    - Saturated and non-saturated arithmetic
    - SIMD and dot-product
    - Real x Real, Real x Complex, Complex x Complex, Complex x Conjugate

- Uniform and consistent Instruction set
  - All instructions can use every register, support all data type, and all addressing modes
  - Remove grouping restrictions
    - All instructions can be grouped together (no more grouping “type” like in SC3850)

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Baseband Optimized Instruction Set

- The Instruction set definition is based on deep analysis of baseband requirements and MAPLE™ offloaded functionality
- Powerful application specific instructions are introduced in SC3900 (patents pending) – few examples:
  - Maximum/Peak search
    - Find maximum value and index between 4 words and previous results
    - Up to 4 Maxsearch (total of 20 elements) per cycle
  - Filter and correlation dedicated instructions
    - Support for both complex and real filters
  - FFT/DFT highly optimized kernel and instructions
  - Specialized load/store instructions
    - Support matrix transposed & manipulation (2x2, 2x4, 4x4, 2x8, 4x8, 8x8)
  - Bit manipulation
    - Dedicated instruction for scrambling, puncturing, interleaver
  - Reciprocal (1/x), 1/Square Root and Log approximation instructions

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SC3900 vs. TI-C66 in Numbers – High Level

Kernels	SC3850 cycles	TI-C66x cycles	SC3900 cycles	Improvement factor C66/SC3900
Complex vector multiplication	3N/4	3N/4 [1]	N/8	6x
Complex Correlation	N/2	N/2 [1]	N/8	4x
Complex FFT = 256	820	535 [1]	194	2.8x
Complex FFT = 2048	8770	5568 [2]	1845	3x
Complex FIR	NT/2	NT/4 [2]	NT/8	2x
Matrix mult 32x32	16400	7700 [2]	4100	1.9x
4x4 complex matrix mult	32	12 [2]	8	1.5x
Real Dot Product 16x16	N/4	N/4 [1]	N/16	4x
Division (16 bits)	5	4 [1]	0.5	8x
Maximum and Index search (N=512)	155	142 [1]	35	4x
LTE Descrambler (Cycle/bit)	1.1	1.1 [1]	0.09	12x
LTE L1 Code Block Segmentation (memcopy based)	Z	Z [1]	Z/8	8x
LTE L1 PRB mapping (memcopy based)	Z	Z [1]	Z/4	4x

N: samples, **T**: coefficients
(1) Estimated number based on TI-C66x architecture and instruction set analysis
(2) Numbers reported in TI's Product bulletin: "TMS320C6670 Breakthrough performance for process-intensive applications "

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SC3900 Core – Feature Set vs. SC3850

	SC3850→MSC815x	SC3900→B4860	Comments
DALU	8 MACs 16bx16b	32 MACs 16bx16b	4x
	2 Complex MACs (16b,16b)x(16b,16b)	8 Complex MACs (16b,16b)x(16b,16b)	4x Native support in SC3900 (single inst.)
	Some 16b/20b SIMD2 isa	Many 16b/20b SIMD4 isa Many 32b/40b SIMD2 isa	
	Some application specific isa	Many application specific isa	Mostly Baseband oriented
	16 Data Register of 40bit	64 Data Register of 40bit	4x
AGU	2 Load/Store Units	2 Load/Store Units + 1 IPU	Higher ILP
	2x64bit load/store per cycle	2x256bit load/store per cycle 512bit load + 512bit store per cycle	Very high mem throughput 4x to 8x
	2 cycles address pre-calculation	1 cycles address pre-calculation	Better control code performance
	No multiply/shift (need DALU support)	32bx32b Multiply and 32bit shifter in IPU	
	No Unaligned access support	Unaligned access support	Seamless support with no penalty
PCU	6 instructions per VLES 4xDALU + 1xLSU + 1x(LSU or PCU)	8 instructions per VLES 4xDALU + 2xLSU + 1xIPU + 1xPCU	
	16bit instruction set	32bit instruction set	Non-Binary Compatible
	1 predicate bit (T-bit)	6 predicate bits	
	48 entries BTB	128 entries BTB	Better control code performance

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SC3900 Cluster Overview

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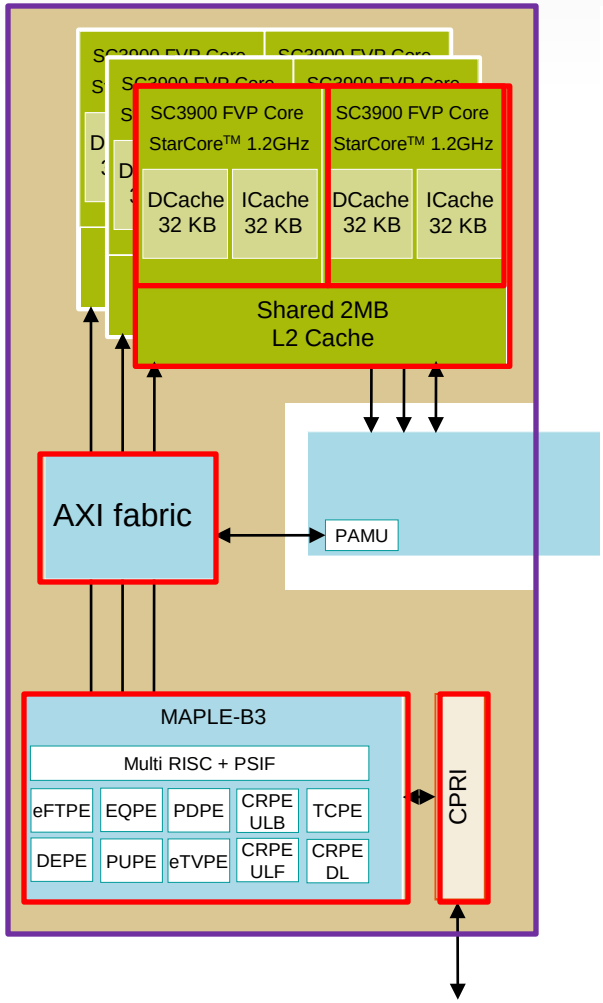
B4860 DSP Platform



DSP Platform includes:

- CPRI: Antenna I/F
- MAPLE - B3: Baseband Accelerator
- AXI fabric
- 3x DSP Clusters
  - Each cluster includes
    - 2x SC3900 Core and L1 Subsystem
    - Shared L2 Cache

- Baseband L1 processing
- Direct CPRI/MAPLE access to DSP L2 Cache
- Direct Connection to Corenet fabric

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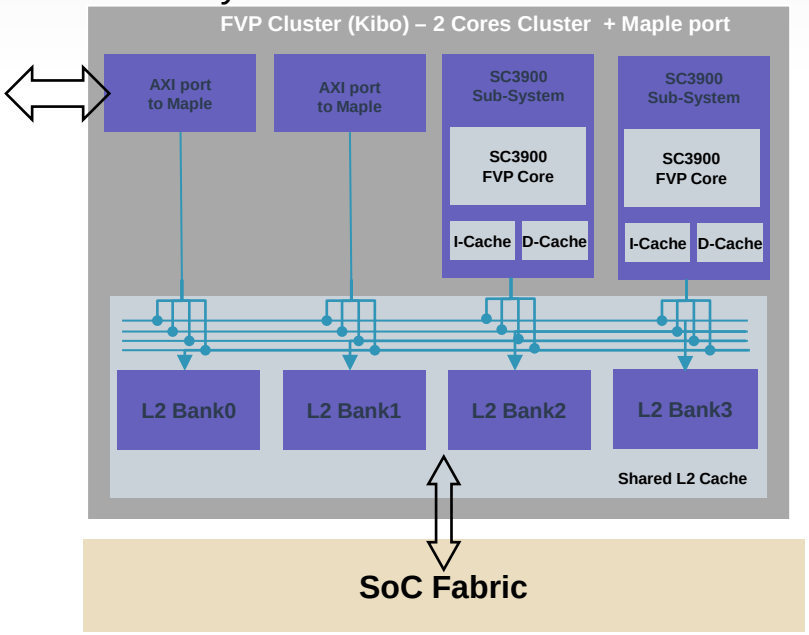
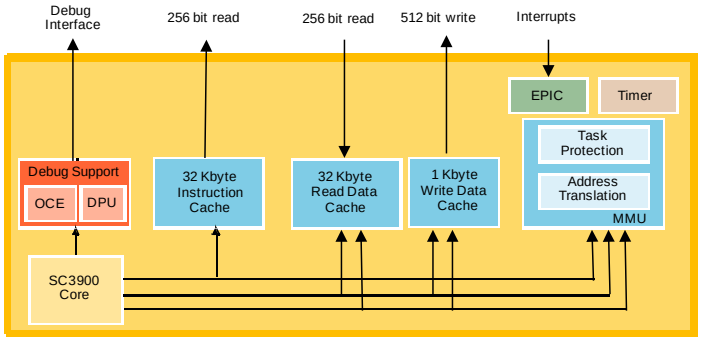
SC3900 DSP Cluster

- Cluster consists of 2x SC3900 under large and fast shared memory
  - Multibank Cache of 2MB
  - AXI based accelerators coupling port (45-90GBps)
- Advanced bus architecture
  - Out of order transaction completion
  - Deep pipeline
  - **Full MESI+L HW Coherency**
- Advanced L1 memory subsystem architecture
  - 36bit address towards memory (64GB space)
  - 32 Kbyte L1 Instruction cache
  - Streaming data paths for read and write
    - 32 Kbyte read only Data Cache
      - 8 way, 128B line, streaming PLRU
    - 1 Kbyte Store/Gather Buffer
- Advanced debug and profiling support
  - Rich event monitoring
  - Multi-core tracing
- Improved core peripherals
  - All core peripherals are SoC accessible
  - Low latency interrupt support





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SC3900 Memory Allocation Options

- SC3900 has a fully cache based memory:
  - No constraints due to internal memory sizes and rigid allocations
  - No DMA management and scheduling overheads
  - Smaller internal memories required as only used code/data is allocated

- In addition, the SC3900 supports:
  - Lock/Unlock of DDR space on the L2 Cache – M2 behavior
  - Partition of the L2 Cache to several orthogonal L2 caches
  - Cache equivalent, DMA operations
    - Tightly coupled accelerator port - Ultra High bandwidth and low latency
    - I/O Stashing and Intervention support
    - Cache Management Engine per core

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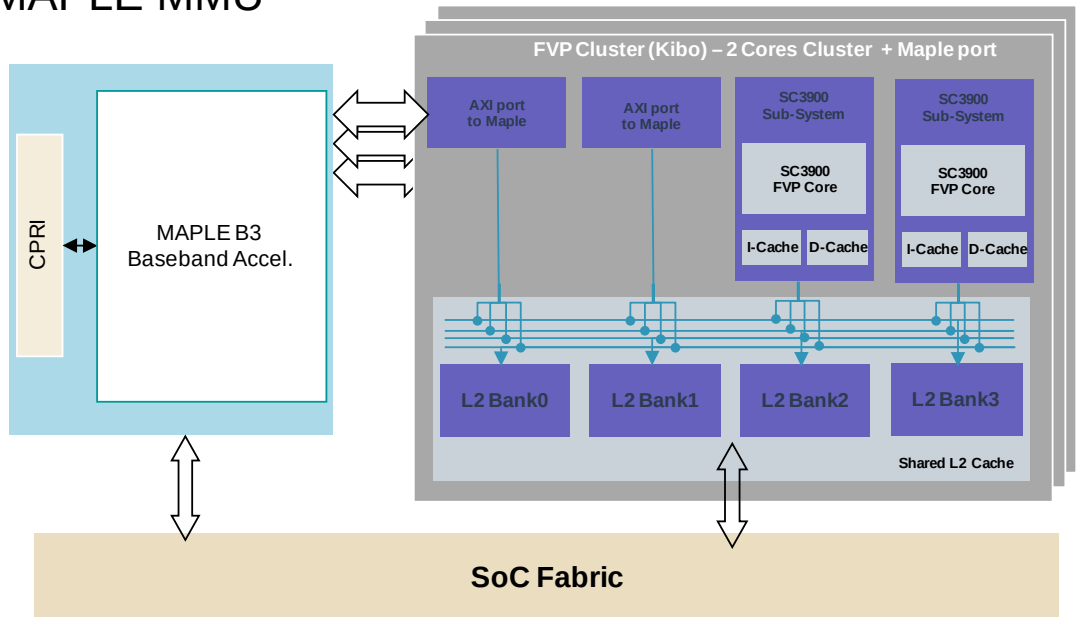
Direct MAPLE/CPRI Access to SC3900 Clusters L2 Caches

- MAPLE/CPRI read/write coherent accesses to L2 via AXI buses
  - Provides tight coupling of MAPLE/CPRI to the DSP cores
  - Provides high BW (>76GBps per cluster) and low latency
  - Significantly reduces DDR bus load and coherency traffic
  - Parallel access to multiple SC3900 clusters
- MAPLE/CPRI accesses to DDRs directly via CoreNet fabric
- Target selection is based on MAPLE MMU



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SC3900 Cluster – Feature Set vs. SC3850

		SC3850→MSC815x	SC3900→B4860	Comments
L1	Size	32 KB	32KB Read + 1KB Write	Support Streaming
	Associativity	8 Ways	8 Ways	
	Line size	256 Byte	128 Byte	Increased flexibility
	HW Pre-fetch	end-of-line	next line	Increased performance
	SW Pre-fetch	Cache ISA	Cache ISA + Background allocation	Allocate data before/during use
	Coherency	SW	HW	Reduce Multi-core complexity
	Core/L1 buses	Instruction - 1x128 bit Data - 2x64 bit	Instruction - 1x256 bit Data – up to 2x512 bit	8x data throughput
	Unaligned access	Not supported	No penalty up to 4K resolution	Increased flexibility
	L1/L2 throughput	128 bit/cycle In of order	Read - 256 bit/cycle + Write - 512 bit/cycle Out of order	>2x data throughput
L2	Organization	Private	Shared - Multi banked	Effective size is larger due to sharing
	Size	512 KB	1MB per core	
	Associativity	8 Ways	16 Ways	
	Line size	64 Byte	64 Byte	
	Data allocation	SW PF	Stashing + Background SW PF	Higher efficiency in data allocation
	Coherency	SW	HW	Reduce Multi-core complexity
	L2/SoC buses	128 bit/cycle In of order	Read - 256 bit/cycle Write – 256 bit/cycle Out of order	

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MAPLE-B3

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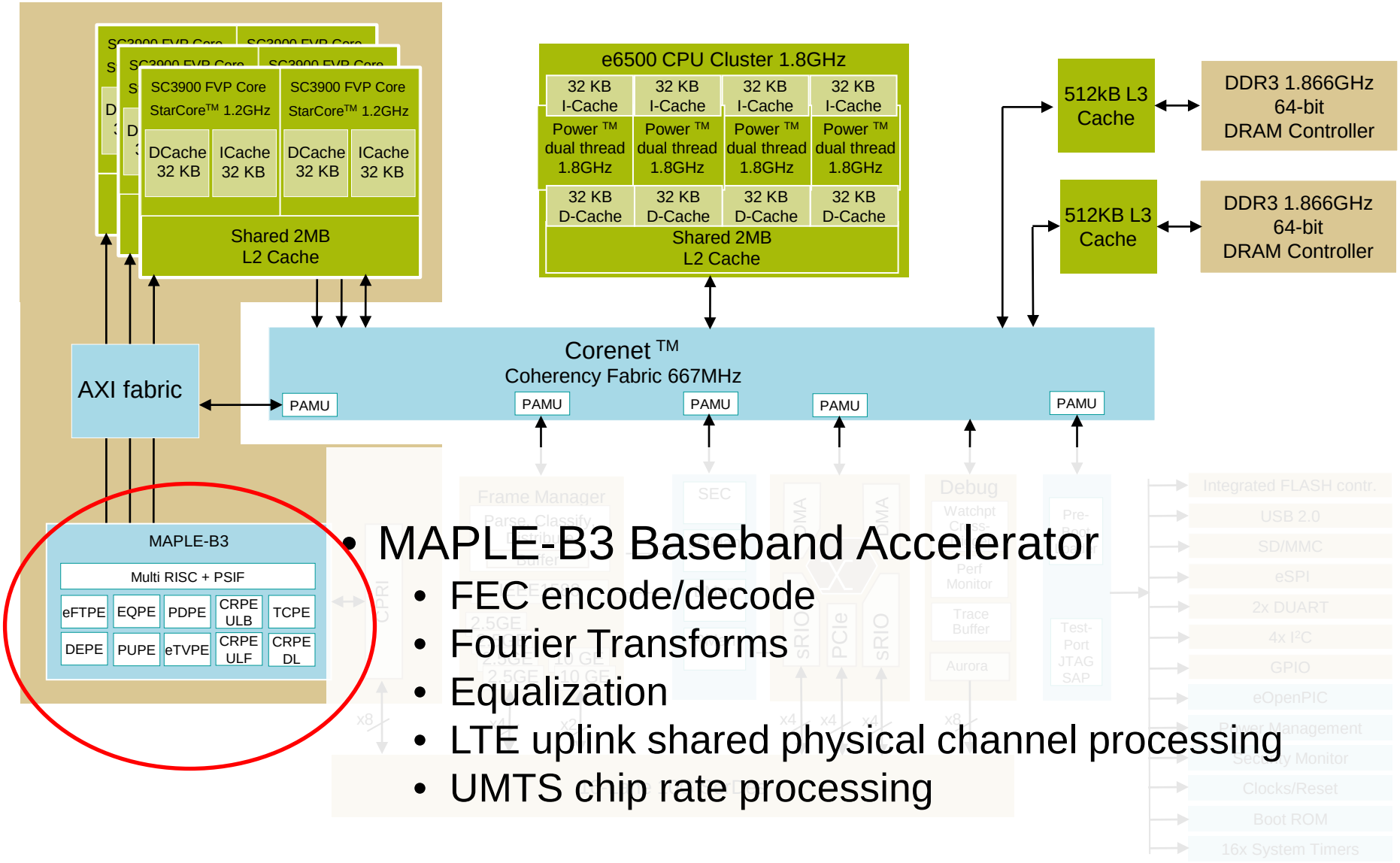
B4860 – MAPLE-B3



- MAPLE-B3 Baseband Accelerator
  - FEC encode/decode
  - Fourier Transforms
  - Equalization
  - LTE uplink shared physical channel processing
  - UMTS chip rate processing

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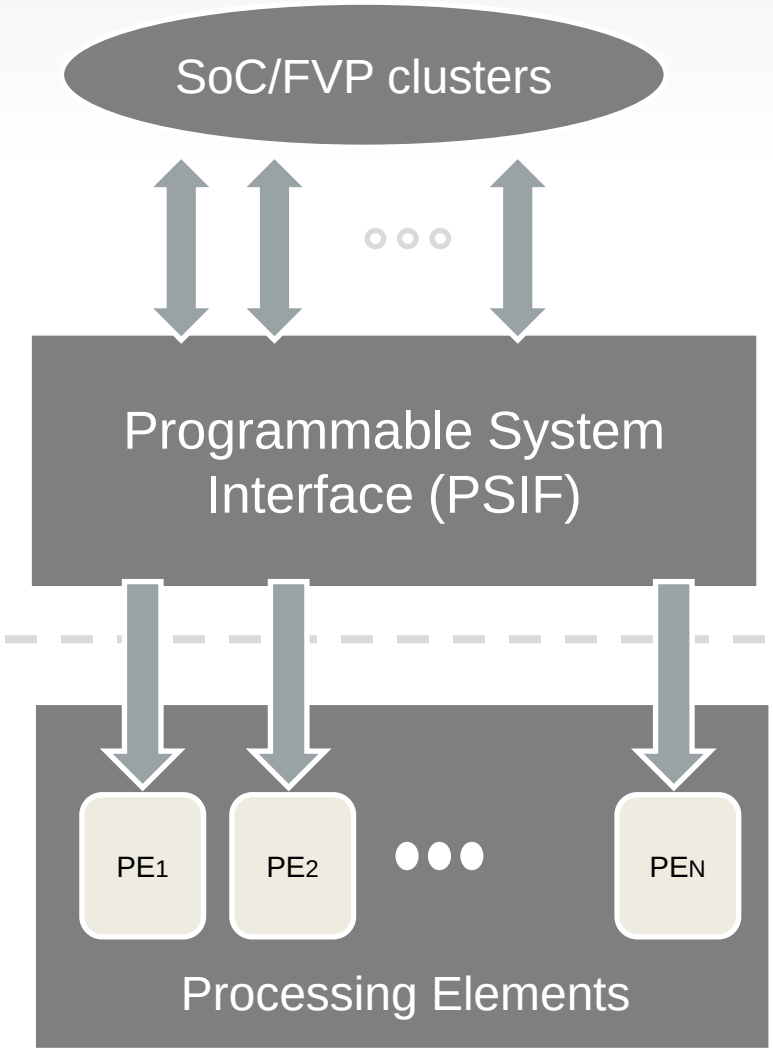
MAPLE Modular Concept



PSIF

Central programmable control for:

- Tasks Scheduling
- Efficient DMAing from/to SoC and internally
- Flexible processing flow allow multiple standards support
- BD parsing and job configurations
- Interrupts handling
- Internal Embedded Data Flows

PE's

- Highly efficient HW implementation of baseband computational extensive algorithms
- Lego like concept allowing:
  - Fast solution derivation (Macro to Femto)
  - Use of algorithms commonality between technologies (LTE, WCDMA, CDMA, WiMAX)

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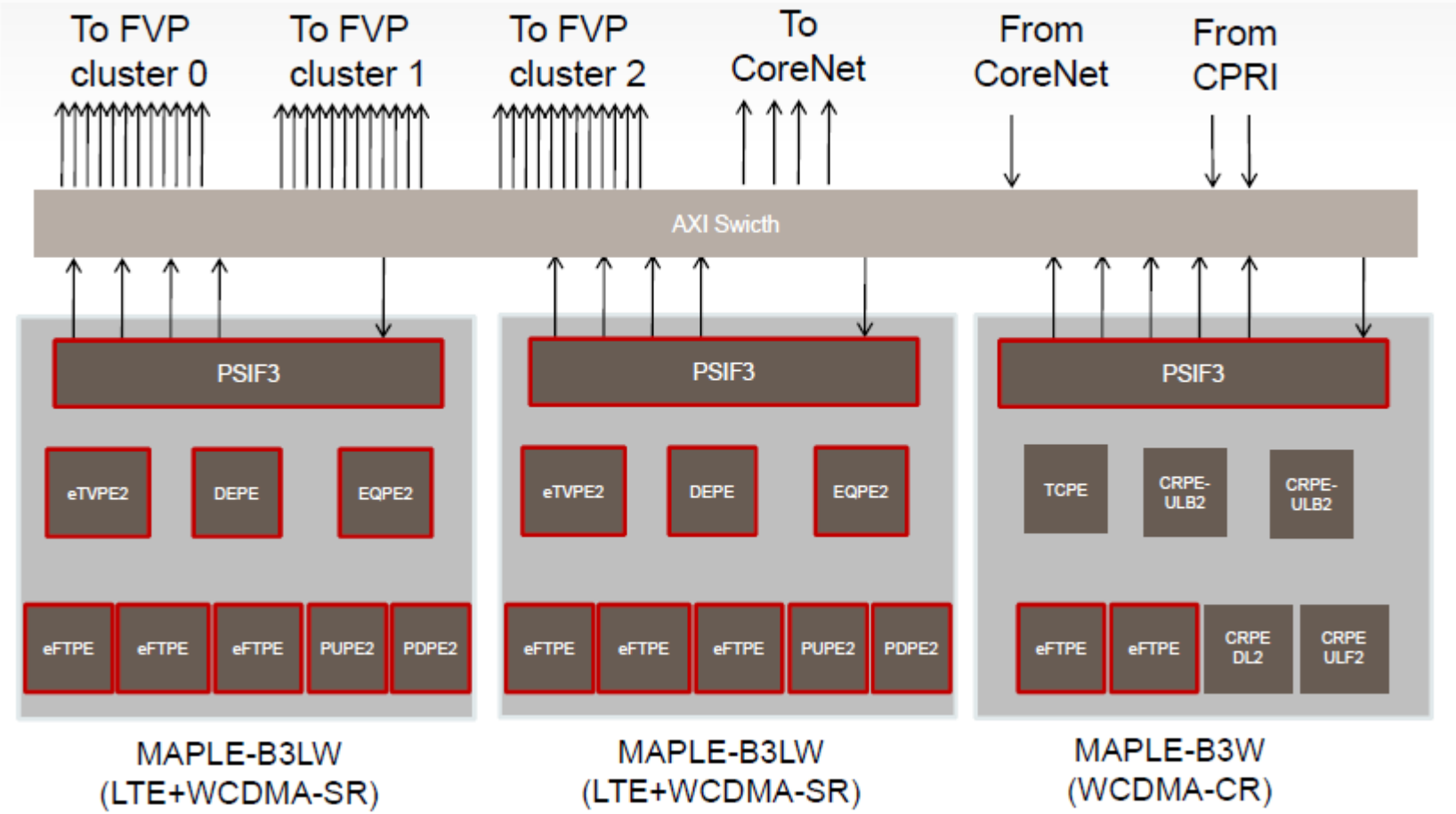
MAPLE-B3 Highlights



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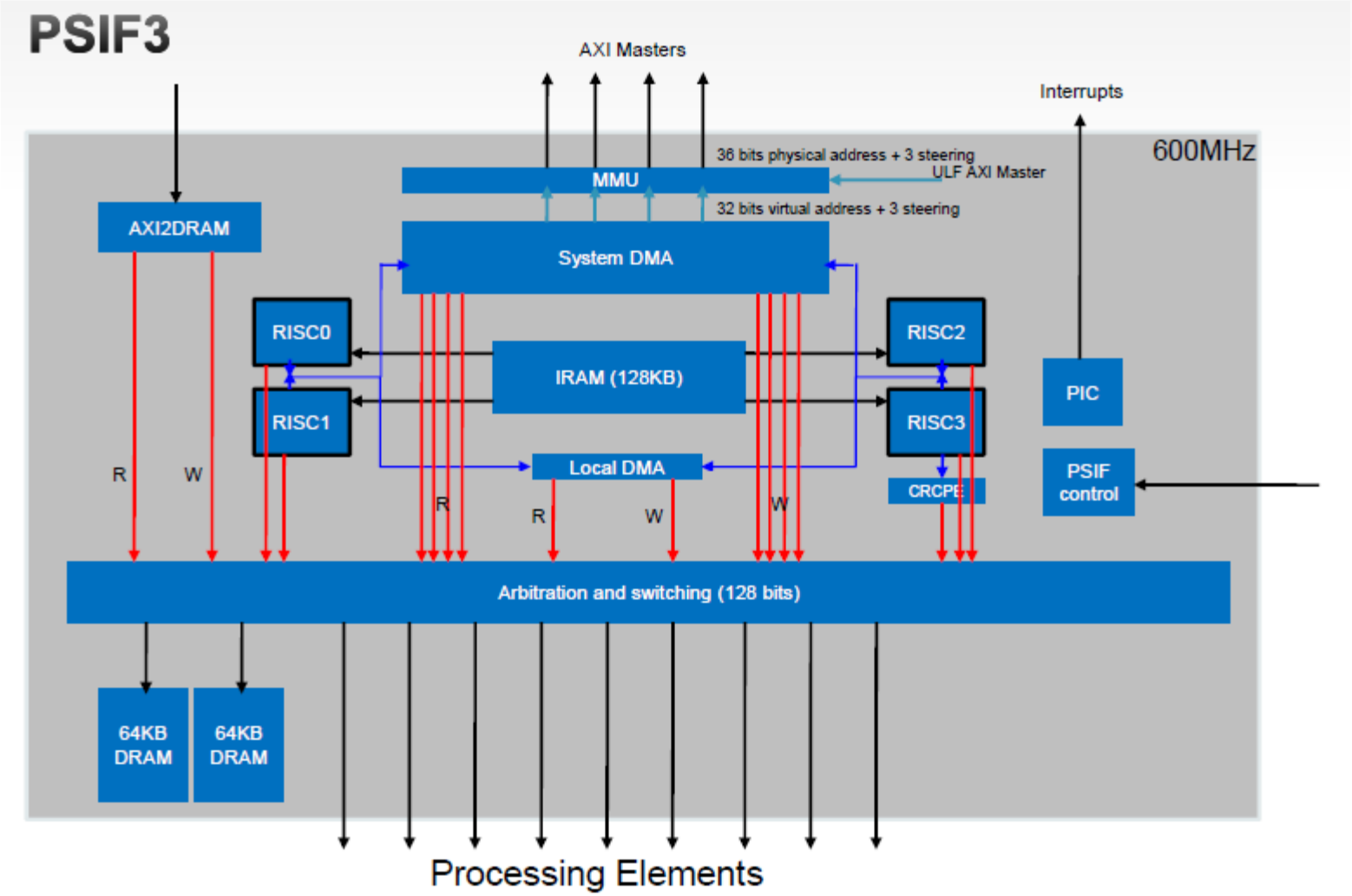
PSIF3 Block Diagram



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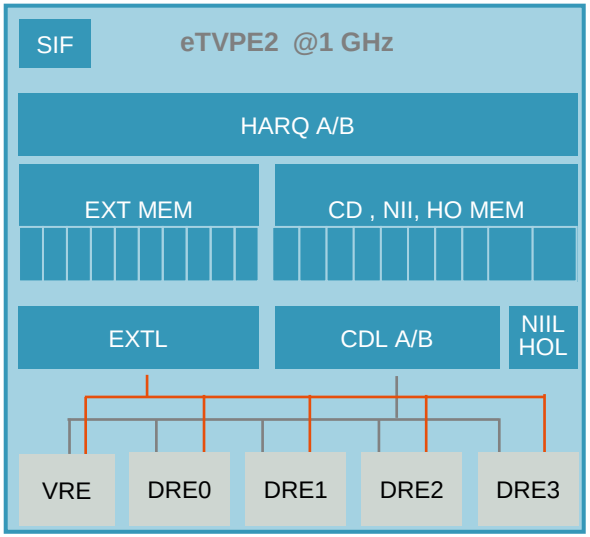
eTVPE2 – FEC decoding highlights

Features:

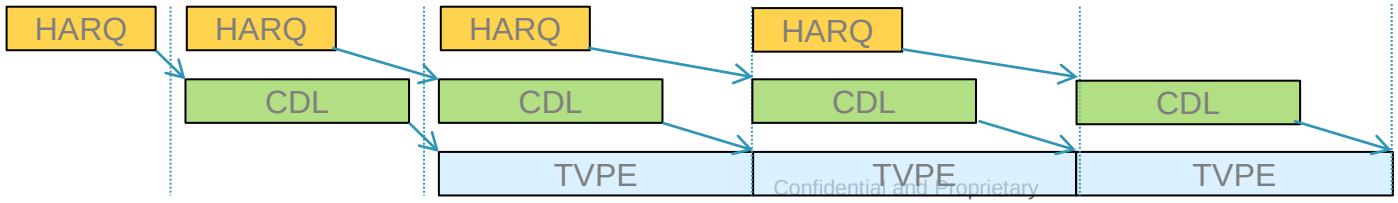
- ✓ Simultaneous Multi-Mode FEC decoding
- ✓ Pre-processing options:
  - ✓ Optional flexible HARQ combining
  - ✓ Optional Rate-De-Matching, Sub-Block Deinterleaving
- ✓ Soft Receivers enabled:
  - ✓ Soft LLRs (either 16 bits LLR of systematic bits only or 8 bits LLR of systematic, parities and tail)
  - ✓ Hard bits order in either ascending or descending order
- ✓ Max Log Map/Linear Log Map
- ✓ Multiple early stopping criteria's (CRC pass, steady, APQ)
- ✓ Programmable number of maximum/minimum iterations.



Performance:

- ✓ ~ 6500 Mbps/ full iteration @ 1 GHz (1100 Mbps @6 full iterations)
- ✓ Pipelined architecture to enable tolerance for system memory latencies
- ✓ Dynamic Power Gating (DPG) utilizing RISC based control.

eTVPE Pipeline implementation:



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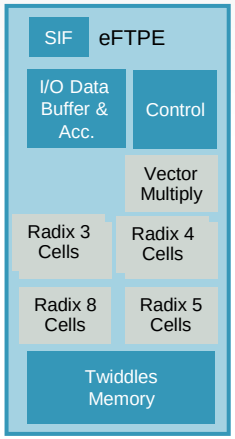
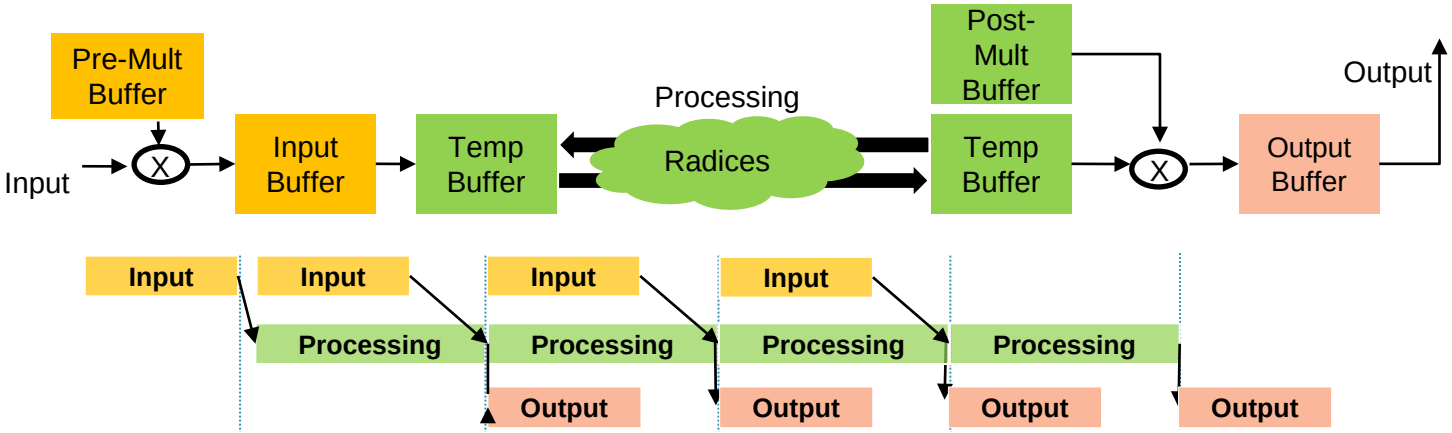
eFTPE2 highlights

- **Features:**
  - High throughput, low power FFT/iFFT, DFT/iDFT Processing Elements
  - Build from multi Radix elements (2xR3, 2xR4, R5, R8)
  - Advanced scaling methods including block floating point
  - Pre/Post-Multiplication ("vector multiplication") support by programmable complex values vector.
  - Post-Multiplication support of all samples by single programmable complex value.
  - Phase rotation of input or output samples, Zero padding of input data
  - Guard bands and DC carrier insertion/removal for iFFT/FFT optimization.
  - CP removal/insertion for minimum data transfers.
  - Jobs repeat
- **Performance:**
  - 740 FFT2048 per cycle, 600+ MHz full yield at 28nm
  - Pipelined architecture to enable tolerance for system memory latencies
  - Dynamic Power Gating (DPG) utilizing RISC based control.





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DEPE – FEC Encoding Highlights

Features:

✓ LTE: DL-SCH and UL-SCH Turbo Encoding and Rate-matching.

✓ HSPA: HS-DSCH and E-DCH (TDD/FDD) Turbo Encoding and Rate Matching.

✓Optional CRC attachments

✓Filler bits insertion, TB segmentation using bit granularity

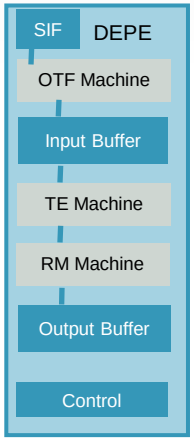
✓ Multi-job in single descriptor

Performance:

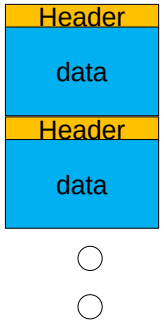
✓2 input bits/cycle HSPA, 4 input bits/cycle LTE, 600+ MHz full yield at 28nm

✓Deeply pipelined architecture to enable tolerance for system memory latencies

✓ Ultra small area and very low power with >2Gbps of encoding capacity



Single Header + Single Data



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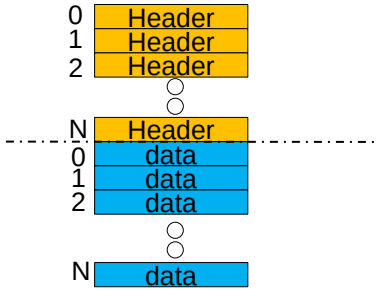

Technology	Header Size	Max Num of Headers in BD
3GLTE	16 Bytes	32
UMTS	32 Bytes	20

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EQPE2 - MMSE/ZF/IRC equalization for LTE

Features:

•Accelerates Equalization DataPath

• Flexibility for customers algorithms adoption and IP preservation

  • flexible programming model

  • various antenna-layer combinations, various MMSE like algorithms

• Floating point implementation for high precision

• High throughput for low latency advanced receivers implementation

•Supporting various Rx Antenna (1,2,4,8) and MIMO layers (1,2,3,4) configurations

•Optional Channel Estimation interpolation with user defined weights

• Embedded support for advanced receivers with iterative interference cancellation schemes with internal layers cancellation, rank reduction, layer discarding and MIMO layers covariance matrix

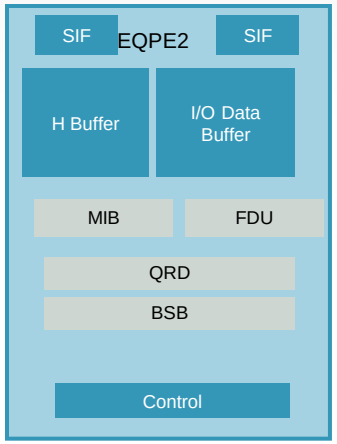
• Statistics computation for modulation de-mapping

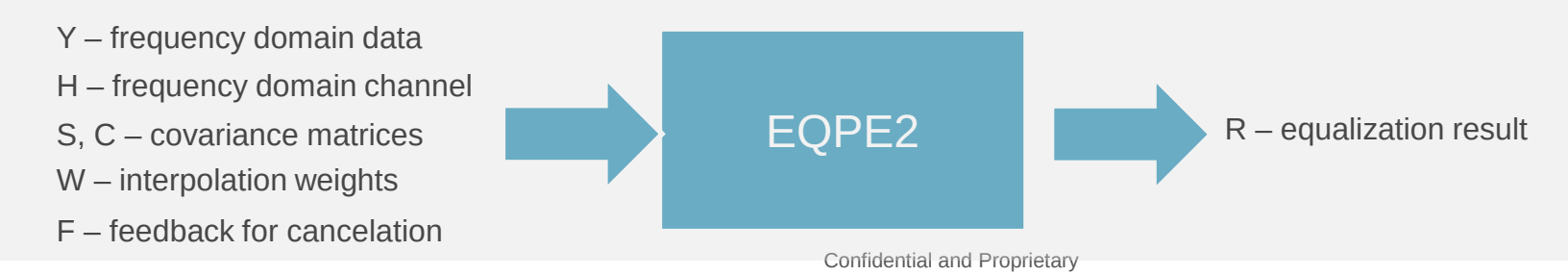
•**Performance:**

• >200 MREps with 600 MHz clock, full yield at 28nm

•Pipelined architecture to enable tolerance for system memory latencies

•Dynamic Power Gating (DPG) utilizing RISC based control





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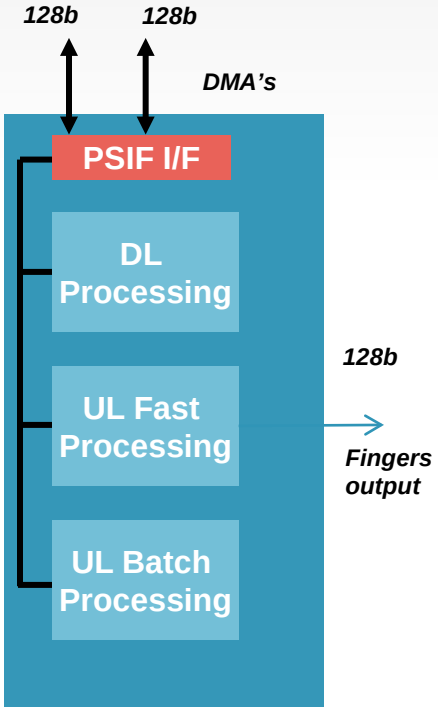
CRPE2 Highlights



Channels/Users control
Using DSP cores and PSIF
- **Add/Remove/Update channel**
- **Add/Remove/Update Finger**
- **Add/Remove User**
- **…..**

DL Processing:
- Optional STTD pre-coding
- Channelization & code generation
- Scrambling & code generation
- Gain, Phase Shift and Combining
- Optional Beam Forming
- Direct CPRI accesses for data streaming & low latency

UL Fast Processing:
- Optional Interpolation
- DPCCH De-Spreading (EOL), E-DPCCH, HS-DPCCH (SF256,128), RACH message control, GP for SNR
- Optional Pilots Correlation
- Direct CPRI interface for data streaming & low latency

UL Batch Processing:
- Optional Interpolation
- DPDCH, E-DPDCH, RACH data de-spreading
- Optional fingers combining and frequency correction

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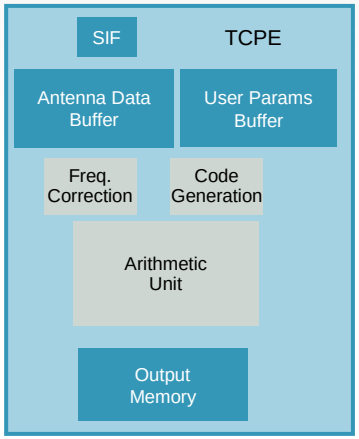
TCPE - highlights

Features:

- Support for RACH preamble detection and DPCCH Path-Search – flexible loading
- Frequency correction
- Coherent and non-coherent correlations
- Internal generation of RACH preamble signatures and DPCCH pilots
- Weighting for non-coherent combining
- Configurable parameters:
    - Correlation length: any length by partitioning into several jobs
    - Search Window: 32 - 2048
    - Combining length: any length by partitioning into several jobs
    - Combining strategies over control symbols
    - No. of antennas/oversampling
- **Performance:**
- Optional, simultaneous Path Search and RACH on same antenna data.
- 1K complex correlations/cycle, 128 MAC's/ cycle for frequency correction
- Extremely low power and area implementation
- 600 MHz @28nm with full yield
- Dynamic Power Gating (DPG) utilizing RISC based control.



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CPRI

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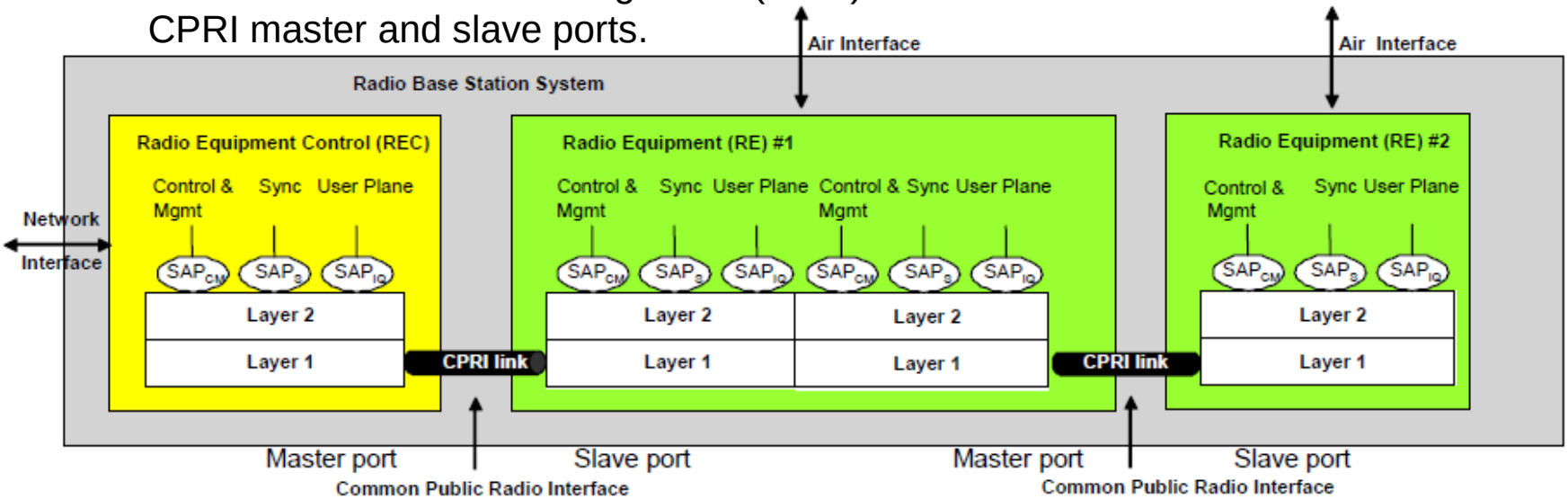
CPRI in B4860

- The CPRI complex enables communication among radio devices over a CPRI bus.
- The CPRI complex is designed to support the CPRI V4.2 specification and can be configured to support several air interface standards, including WiMAX, LTE, and WCDMA.
- The complex supports up to 8 CPRI links (4 pairs) with each link configurable as a master or slave port.
- Each CPRI link supports three types of service access points (SAPs):
  - IQ samples for antenna transferred through the SAP IQ Interface
  - CPRI frames synchronized by the SAP synchronization interface
  - CPRI link control and management (C&M) data transferred between SAPs in both CPRI master and slave ports.



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CPRI – Features (1/5) (new in B4860 vs. 8157/9132)

- Supports the following CPRI link rates:
  - 1228.8 Mbps
  - 2457.6 Mbps
  - 3072.0 Mbps
  - 4915.2 Mbps
  - 6144.0 Mbps
  - 9830.4 Mbps
- Supports up to 8 lanes
- Supports the following mapping methods:
  - LTE mapping method 1 (IQ sample based) and method 3 (Backward compatible)
  - WiMAX mapping method 3 (Backward compatible).
  - WCDMA mapping method 3 (Backward compatible)
- Supports packed position and flexible position of each AxC container

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CPRI – Features (2/5) (new in B4860 vs. 8157/9132)

- Each port supports up to 24 antenna carriers.
- Daisy-chain capability between CPRI lanes pairs that allows cascading devices according to pre-determined user configuration. Chaining can be done for each lane using the CPRI controller. Chaining lanes does not require core intervention or internal device bandwidth overhead.

- Maintain daisy-chain (pass through) link and eliminate inbound/outbound transactions, while DSP sub system (SC3900 clusters and MAPLE) is in reset.

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CPRI – Features (3/5) (new in B4860 vs. 8157/9132)

- 8- (with oversampling), 15- and 16-bit sample width.
- All the following LTE sampling rates:
  - 1.92 MHz (channel BW 1.25 MHz).
  - 3.84 MHz (channel BW 2.5 MHz).
  - 7.68 MHz (channel BW 5 MHz).
  - 15.36 MHz (channel BW 10 MHz).
  - 23.04 MHz (channel BW 15 MHz).
  - 30.72 MHz (channel BW 20 MHz).
- The following WiMAX sampling rates:
  - 4 MHz.
  - 5.6 MHz.
  - 8 MHz.
  - 10 MHz.
  - 11.2 MHz.

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CPRI – Features (4/5) (new in B4860 vs. 8157/9132)

- Transparent mode (all the CPRI frames are transferred to a single buffer in the main memory)
- Fast Control and Management MAC (Ethernet)
- Slow Control and Management MAC (HDLC)
- Vendor Specific Data (VSS)
- L1 Inband.
- Link start-up and speed negotiation by software.
- Accurate delay measurement and calibration integrated in AxC granularity:
  - Round trip delay measurement value updated automatically (polled by the core via the register interface)
  - TX extra delay can be calibrated (if needed) via the register interface

- AXI Bus master interface.
- 32b Bus interface for register and memory configuration.

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CPRI – Features (5/5) (new in B4860 vs. 8157/9132)

- Interrupts: Edge and level.
- Auxiliary logic between pair of lanes to facilitate aggregation and combining functionality. Combining performed in WCDMA DL between the locally generated IQ and single external IQ stream coming from a daisy-chained device. Transmitted AxCs are either Forwarded, local or summed.
- Reflection of a constant 122.88MHz reconstructed clock on an output pin (one per PLL).
- 10ms sync can be either external (also in REC slave), self-generated, extracted from RX data, shared between lanes (group based) or asserted by the extracted signal from the RX pair.
- Reset request indication on an external pin.
- Scrambling (optional)
- Multi-unicast transfer mode (optional)

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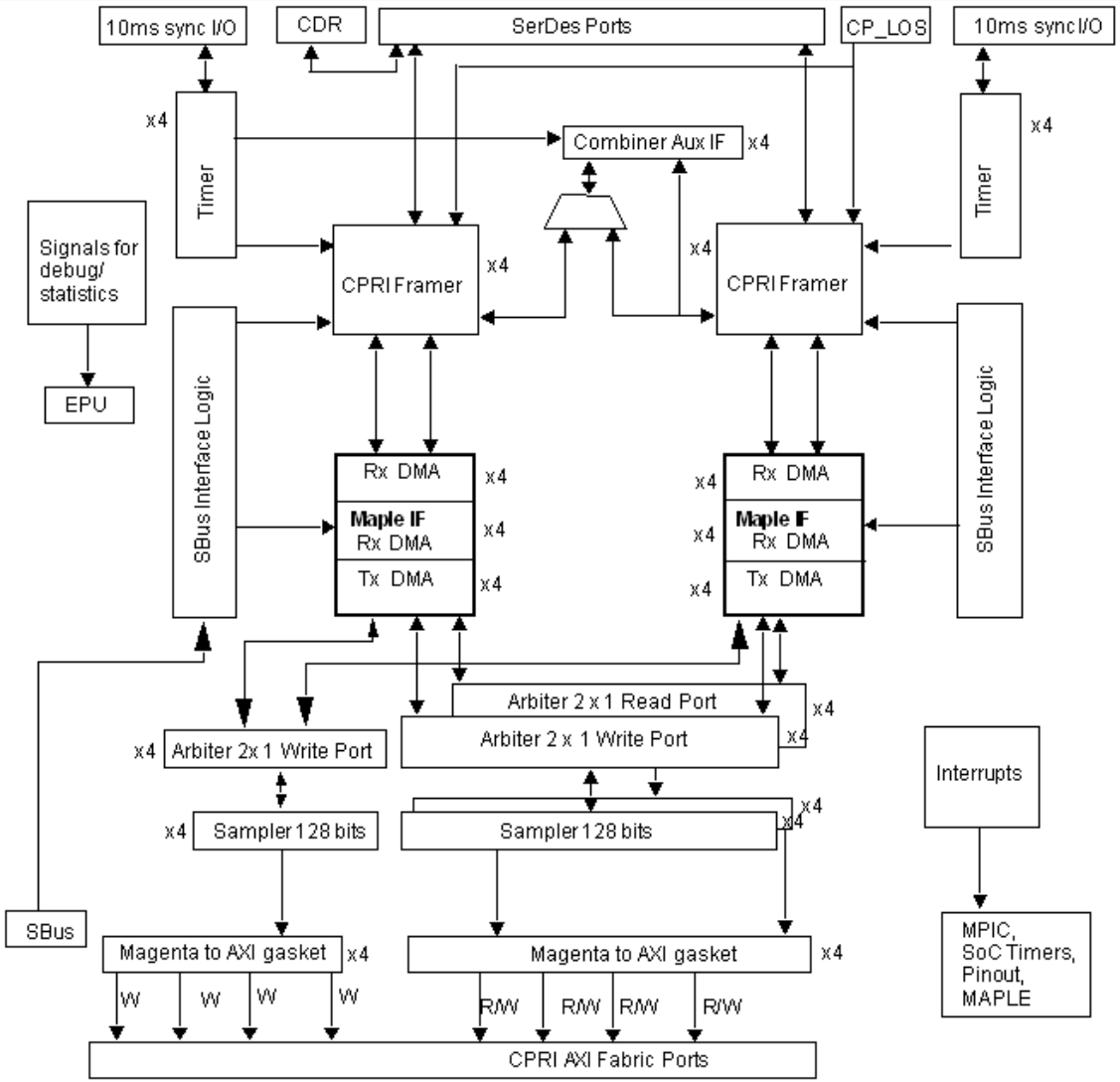
CPRI – Detailed Block Diagram



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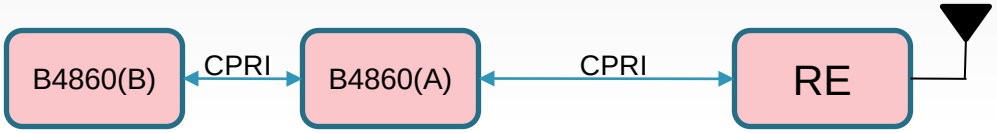
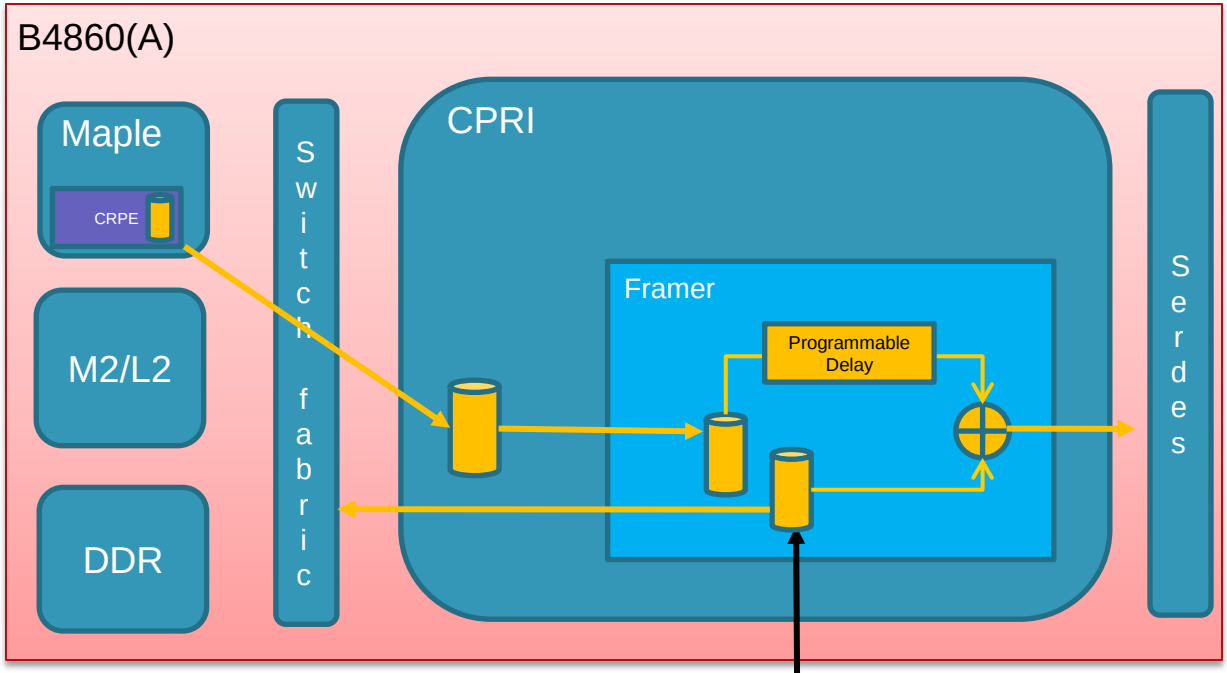
Inter-SoC Combining in DL (in WCDMA)

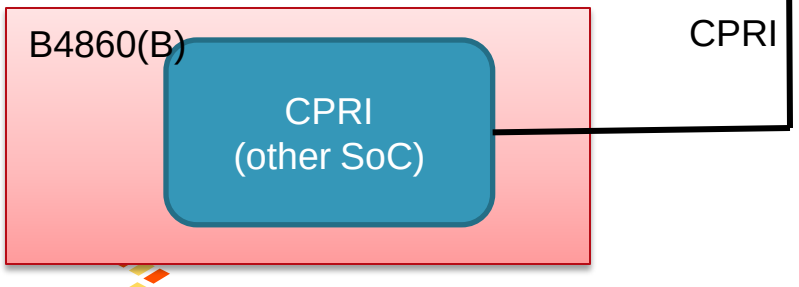
System example:





Each AxC is one of the following:

1. Local AxC
2. Forwarded AxC
3. Summed AxC



- Both SoCs have synchronized with offset 10ms frame sync and transmission
- Combining is an integral part of the pairing function (used to daisy chain two CPRI links)

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Timers in SoC

Total of 110 timers:

- Sixteen identical quad SoC timers, 32b version (total of 64 timers)
- One general-purpose 32-bit timer for RTOS support per each e6500 thread
- Four general-purpose 32-bit timers for RTOS support per each SC3900 core
- Eight timers in the MPIC (31-bit timers)
- One watchdog timer per each e6500 core
- One watchdog timer per each SC3900 core

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Quad Timers - Features

- Four 32-bit timers in each quad timer that serve as frequency dividers, clock generators, and event counters.
- Cascadable timers.
- Count up/down.
- Programmable count modulo.
- Count once or repeatedly.
- Counters are pre-loadable.
- Compare registers can be preloaded.
- Counters can share available inputs.
- Separate prescaler for each counter;
- each counter has capture and compare capability.
- providing ‘set-and-forget’ functionality for the CPRI and external events.
- Primary clock sources: system clock/2, SerDes TX/RX reference clock.
- Secondary clock sources: CPRI events, external clock input, IEEE 1588 clock.

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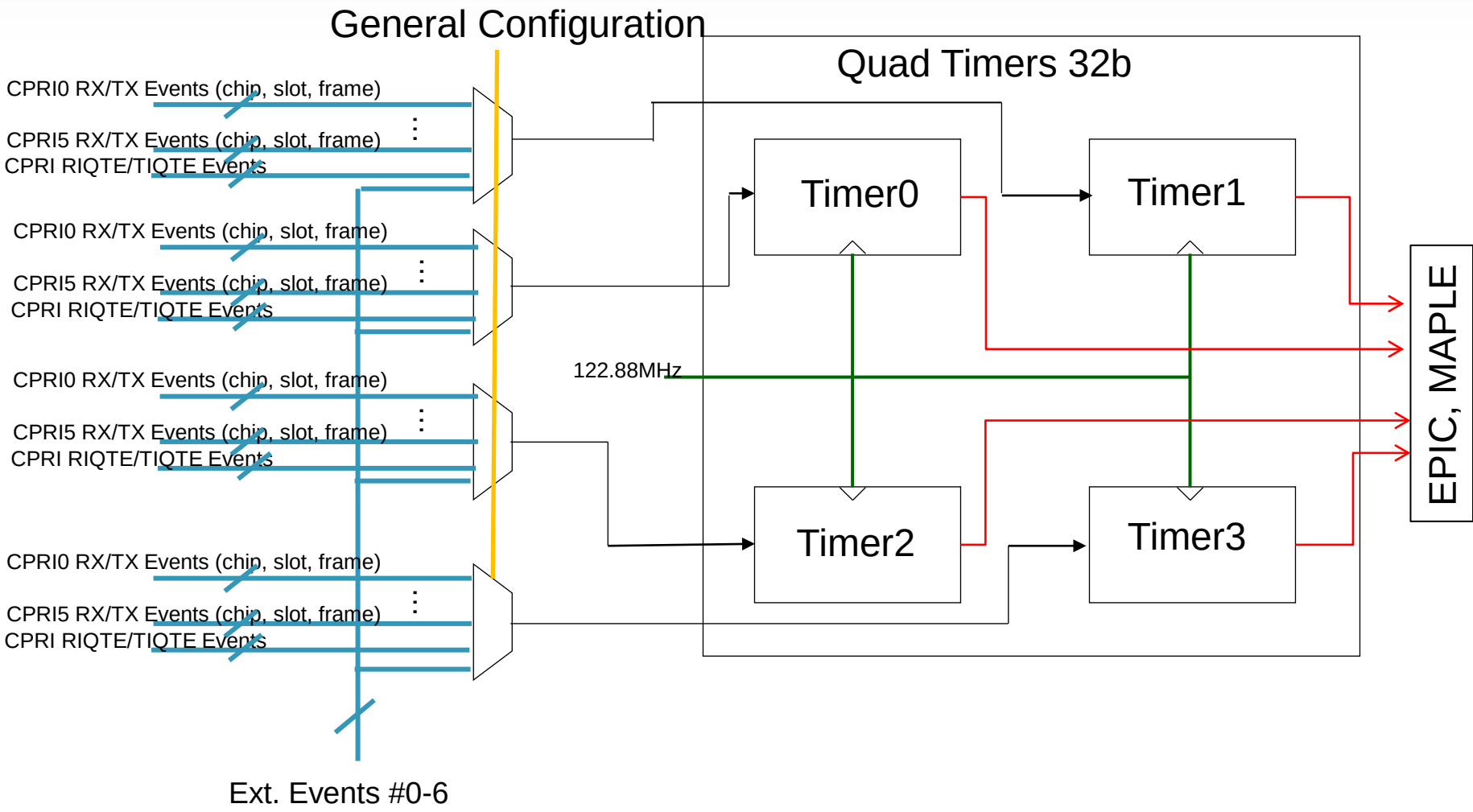
CPRI Events Connectivity with Timers



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Data Path Architecture (DPAA)

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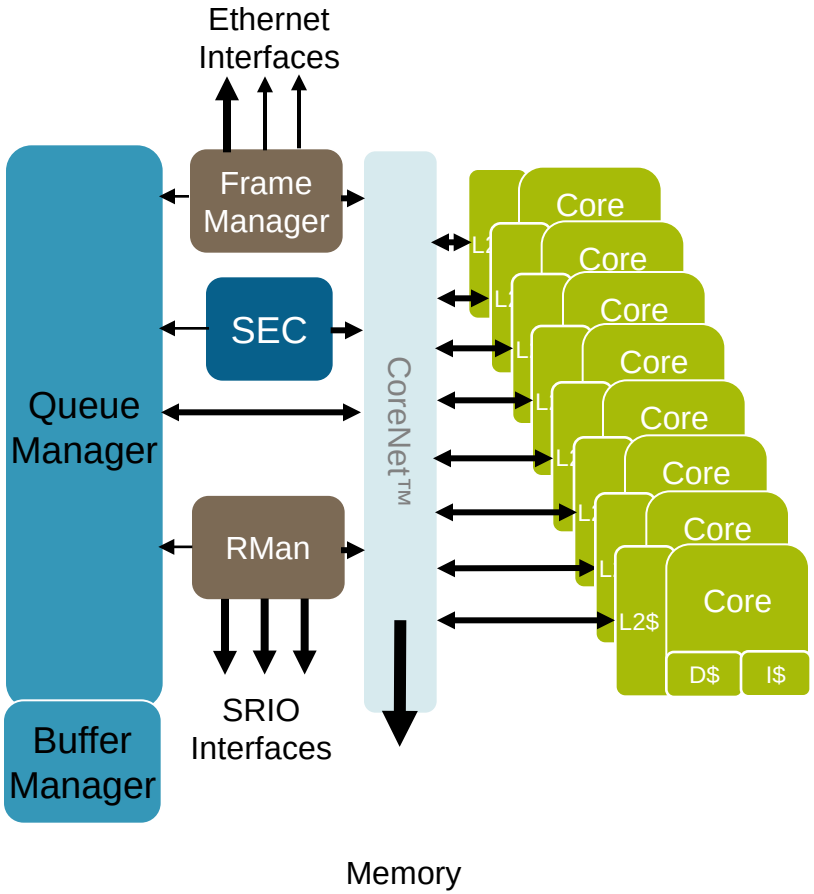
DPAA Purposes

- **Acceleration of frame/packet processing**
- **Classification and Distribution of data flows among cores and software partitions**
  - Load balancing through parse/classify/distribute
  - Load spreading through queues shared among multiple consumers
- **Abstract and manage efficiently Intercore communications and the access to shared resources** (NW interfaces, HW-Accelerators, Buffers, Queues)
- **Scalability and Portability**



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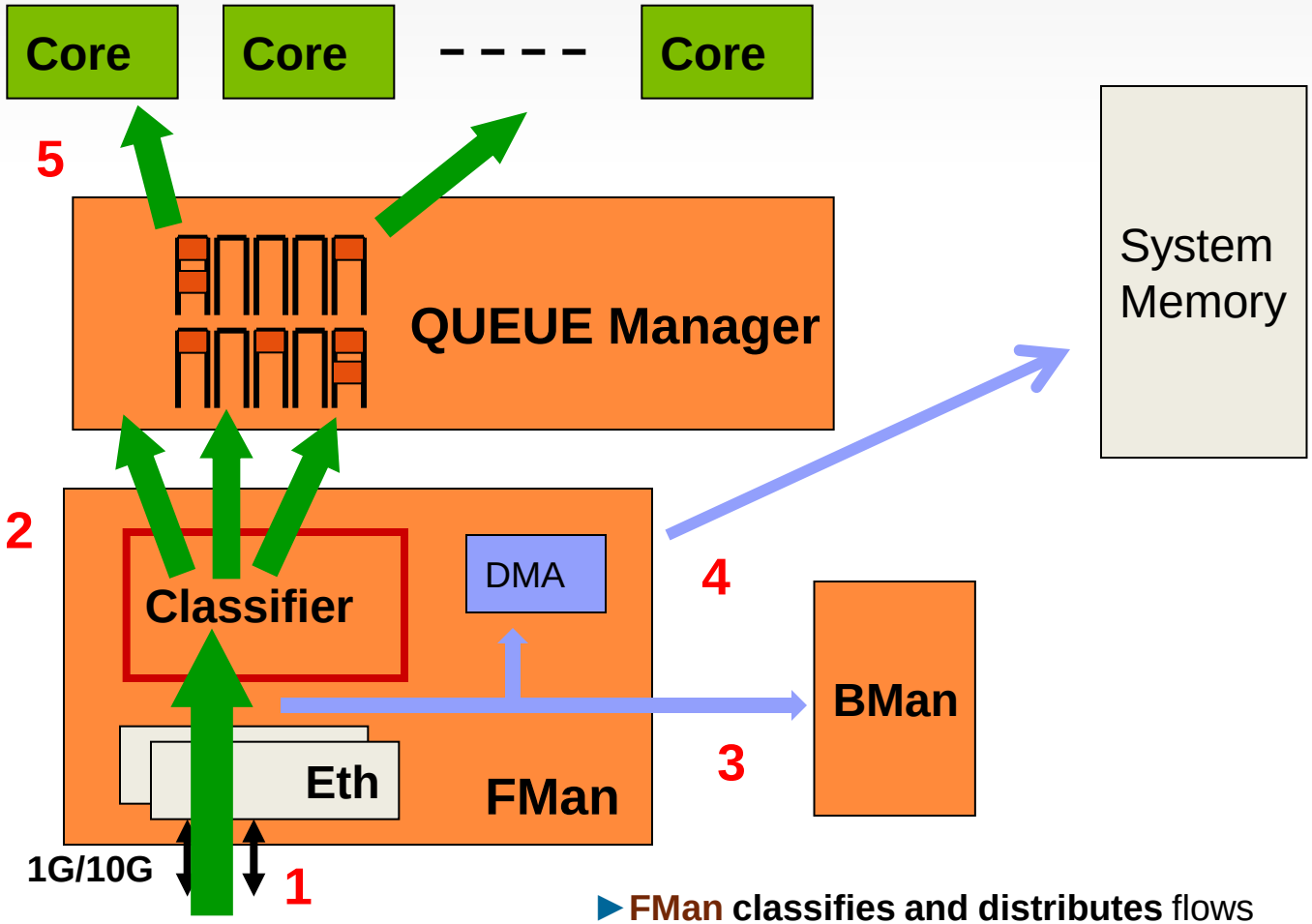
Data-flow pre-classification and distribution



Network Interfaces

- **FMan classifies and distributes** flows
- **BMan** provides **Buffer Pools services**
- **QMan** provides **multi-producer/consumer queues** services

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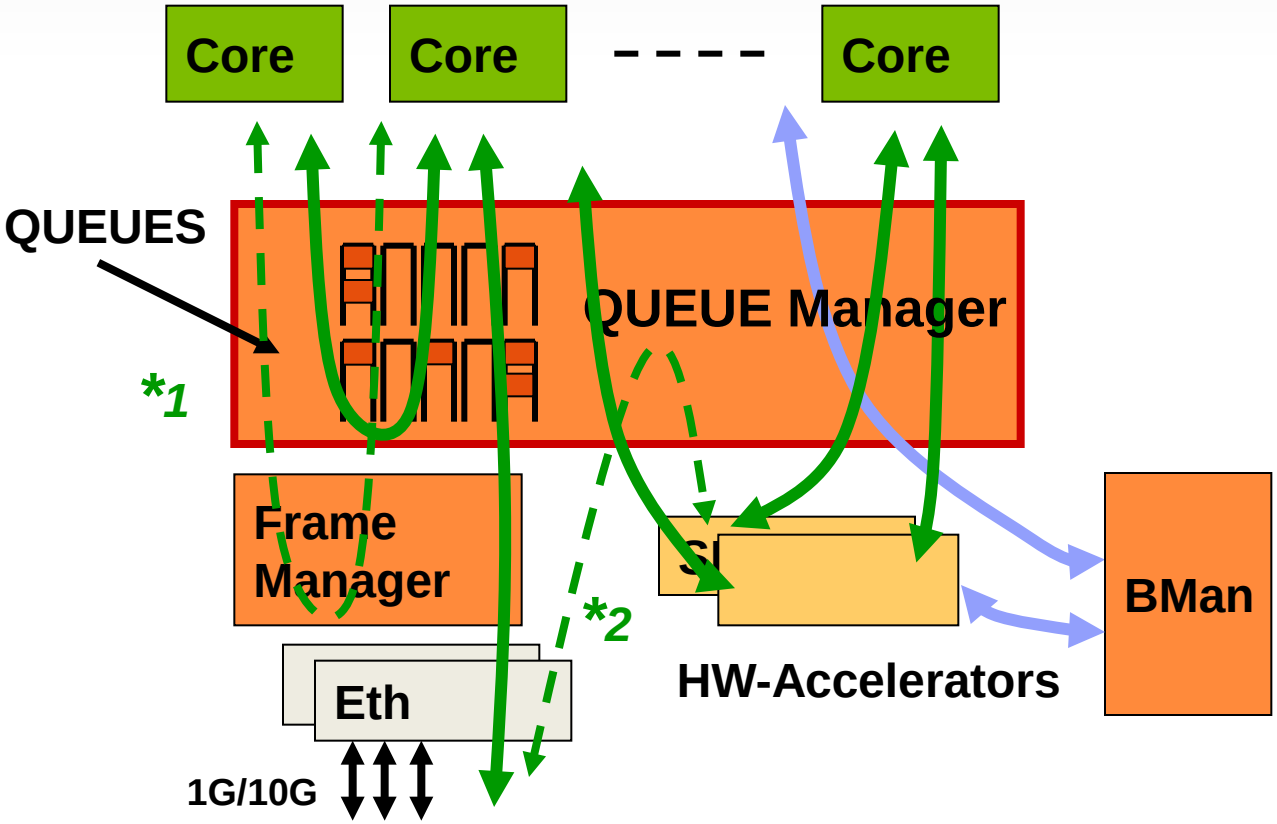
80

Managing the Multi-producer/Multi-consumer Model



Network Interfaces * *1) Shows FMan in off-line mode , 2) show autonomous path*

- ►**Cores and HW-accelerators** are Consumers and Producers
- ►**Queue Manager** acts as central exchange manager
- ► **All exchanges** between cores and HW-blocks are managed thru **queues**
- ► **Buffer Manager** eases and optimizes Buffer Pool Mgmt

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81

A few important comments …

- **BMan** does not make any data transfer (not a DMA), it manages pools of buffer pointers, servicing acquire/release requests from other blocks.

- **QMan** can manage (plenty of) Queues
  - Requires Queue organization (Hierarchy, Scheduling, Queue Mngt …)

- **QMan** services can be used (also) for Inter-core communication (for msg passing, work scheduling …)

- **Cores/SW** DO NOT ACCESS Queues directly (unlike BD rings …).
  - QMan instead provides specific interface/abstraction called **Portals** to service Queueing (from producers) and Dequeueing (from consumers)

- **FMan** frame processing ''services'' can be invoked off-line

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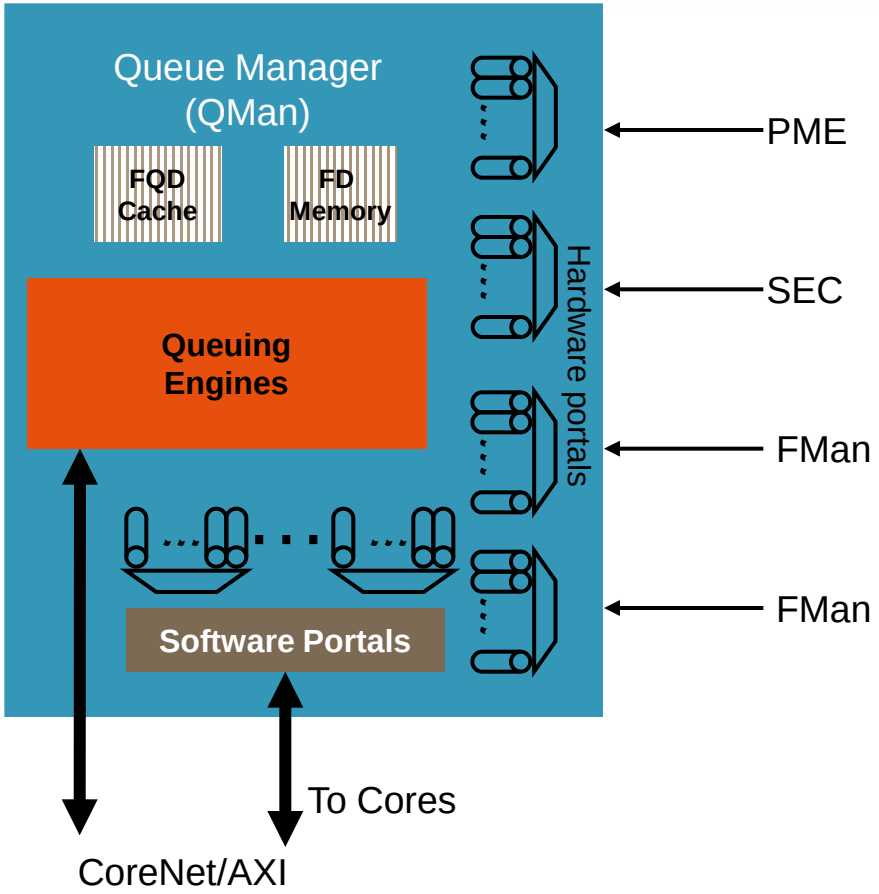
82

QMan overview

Queue Manager (QMan) supports:

- Low latency, prioritized queuing of descriptors between cores, network I/O and accelerators
- “Lockless” enqueue/dequeue interface
- Shared queues for load spreading and device “virtualization”
- Order restoration as well as order preservation through queue affinity
- Active queue management (WRED)
- Optimized core interface which can pre-position data/context/descriptors in core’s cache (with CoreNet)
- Delivery of per-queue accelerator specific commands and context information to offload accelerators along with dequeued descriptors



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Queue Manager (QMan) Software Portals

- Up to 25 software portals (B4860)
  - Accessing 16M queues, >50 channels, >400 work queues
- Software portals are memory mapped hardware components with 2 regions
  - cache-enabled (16KB)
  - cache-inhibited (4KB)
- The cache-enabled area of the portal contains the following major structures:
  - Enqueue Command Ring (EQCR)
  - Dequeue Response Ring (DQRR)
  - Message Ring (MR)
  - Management Command/Response Register (CR and RR0/1)

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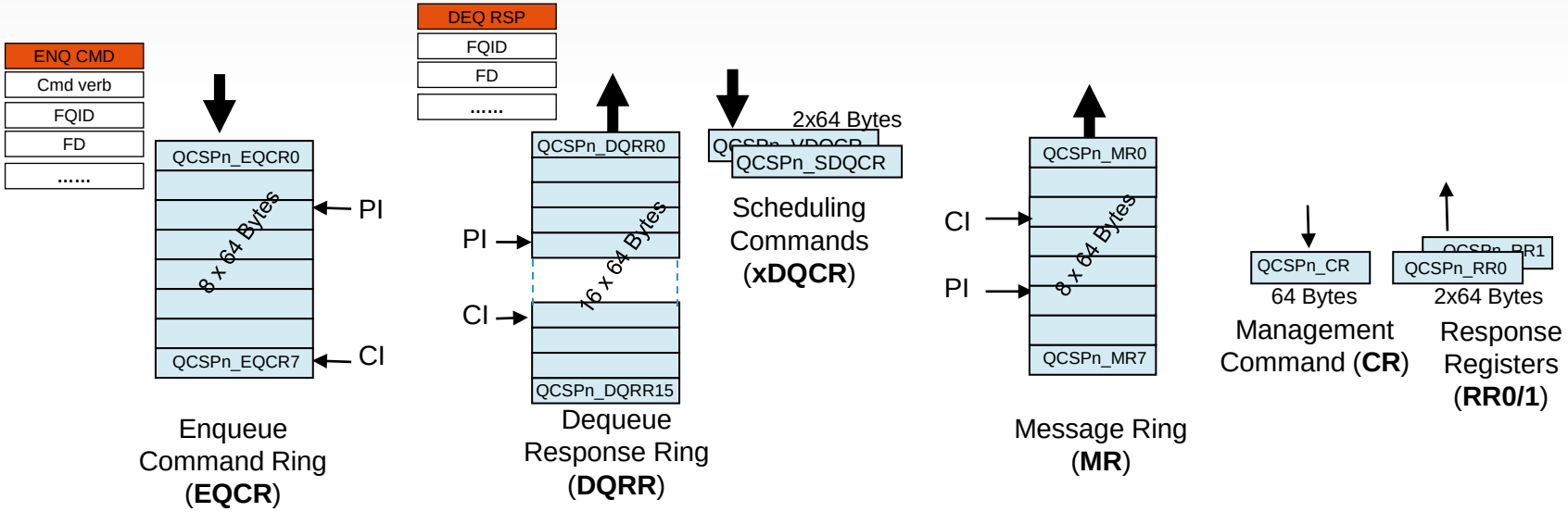
QMan Software Portal Components



- **Enqueue** frames into queues **EQCR**
- **Dequeue** frames from queueus **DQRR**
- **Notification** such error messages **MR**
- **Management** Initialize/query of FQs,WQ,Channel or Congestion Group **CR/RR0-1**
- **Interrupts ex:** data availability in EQCR

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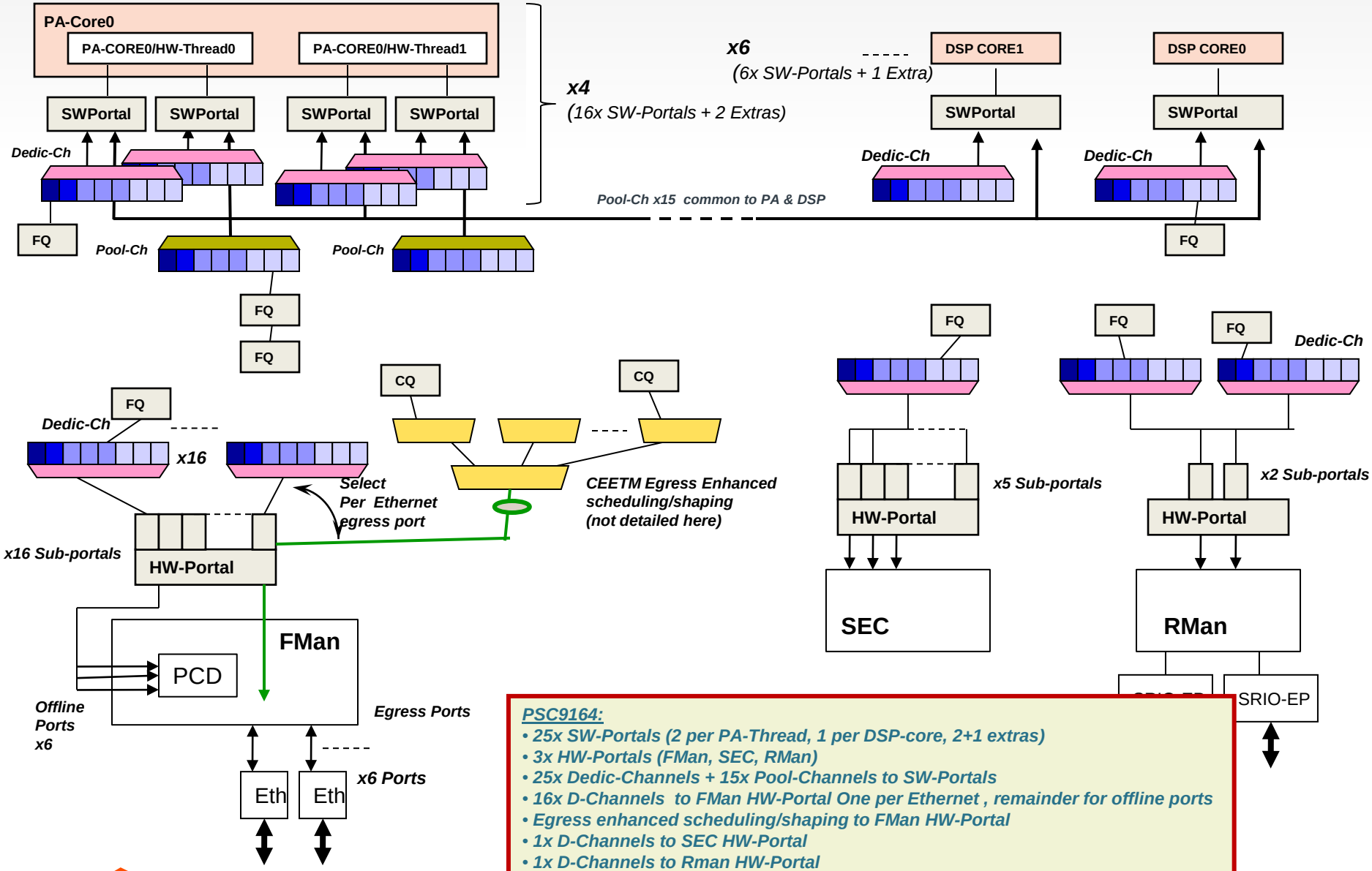
PSC9164 overall QMan portals & channels



PSC9164:

- 25x SW-Portals (2 per PA-Thread, 1 per DSP-core, 2+1 extras)
- 3x HW-Portals (FMan, SEC, RMan)
- 25x Dedic-Channels + 15x Pool-Channels to SW-Portals
- 16x D-Channels to FMan HW-Portal One per Ethernet , remainder for offline ports
- Egress enhanced scheduling/shaping to FMan HW-Portal
- 1x D-Channels to SEC HW-Portal
- 1x D-Channels to Rman HW-Portal

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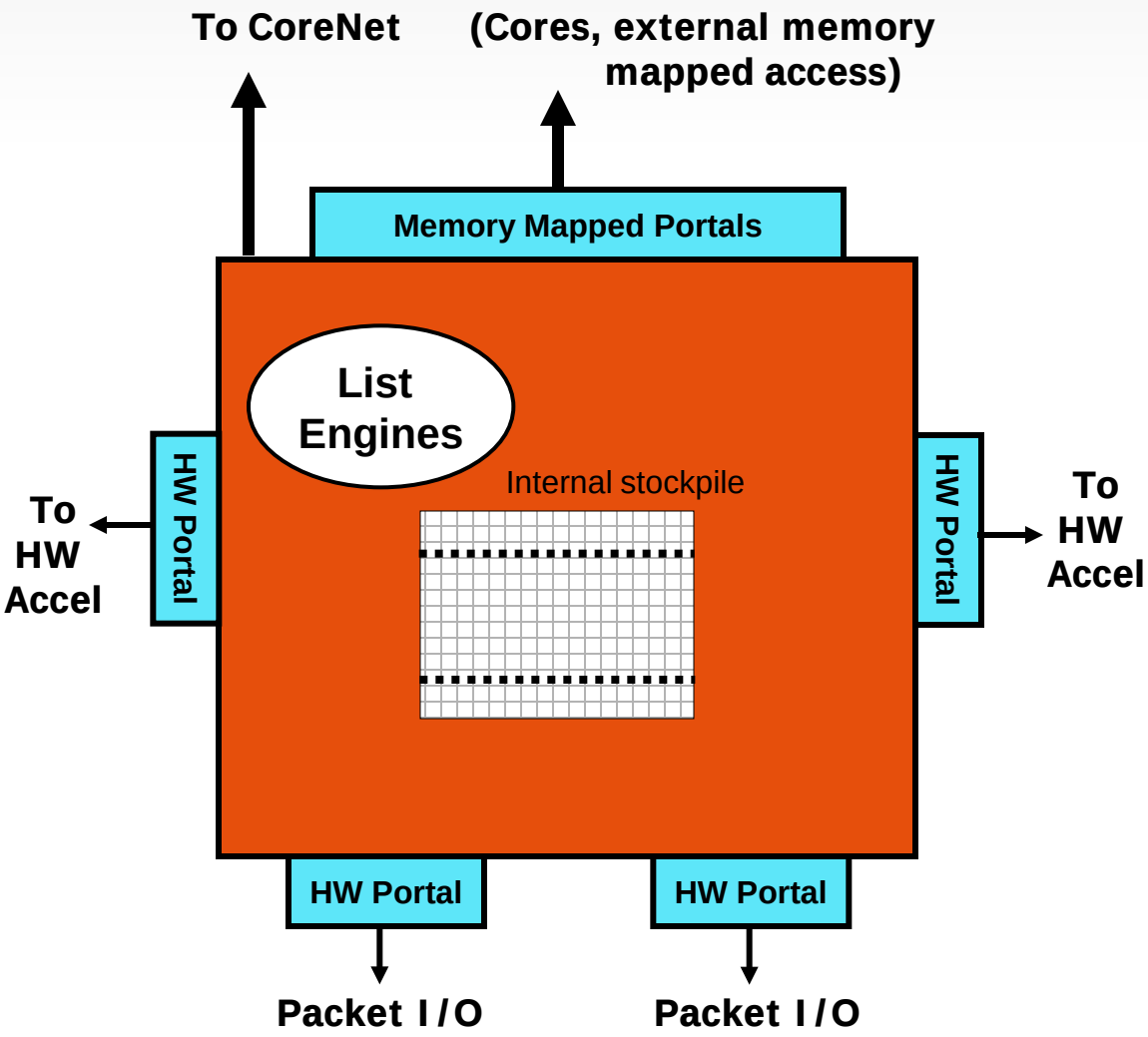
86

Buffer Manager



- BMan can manage 8-255 pools (64 current max implemented) of free buffers
  - Managed on behalf of software
  - Used by hardware
  - BMan does not “create” buffers nor does it “own” the memory where the buffers exist
  - BMan places no restrictions (alignment, size, addressability) on buffers
- BMan maintains a stockpile of buffers in internal memory
  - Reduce latency to acquire a buffer and external memory bandwidth
  - Pools overflow into LIFO lists in DRAM
- Per pool depletion thresholds with interrupt and/or notification
  - For software replenishment of pools
  - For loss-less flow control
- Hysteresis on all thresholds

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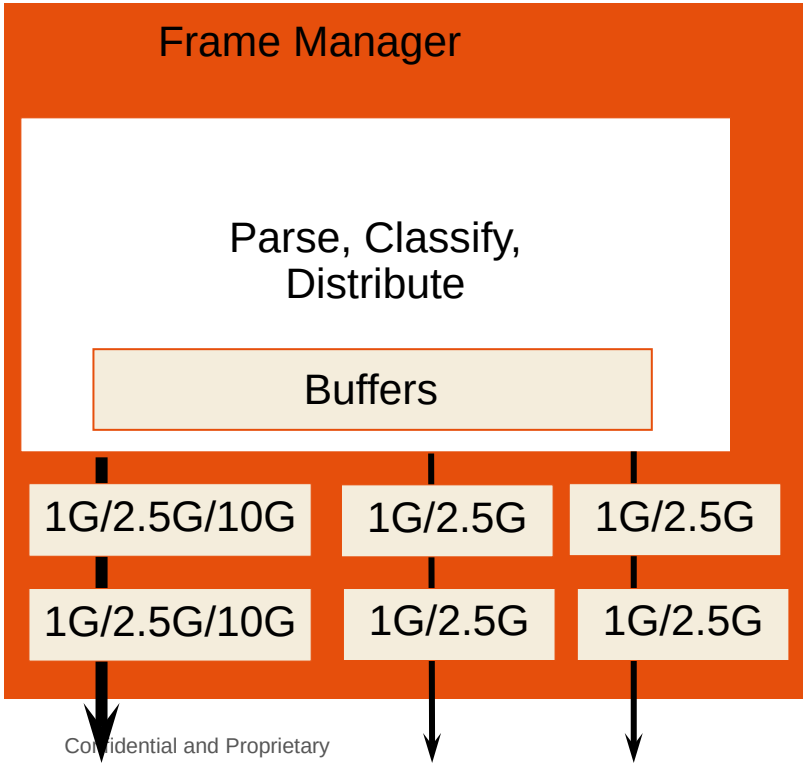
Frame manager

Frame Manager is responsible for preprocessing and moving Ethernet packets into and out of the datapath

- **Parsing**
  - Packet Parsing at wire speed
  - Supports standard protocols parsing and identification by HW (VLAN/IP/UDP/TCP/SCTP/PPPoE/PPP/MPLS/GRE/IPSec …)
  - Supports non-standard UDF header parsing for custom protocols
- **Classification / Distribution**
  - Coarse classification based on Key generation Hash and exact match lookup
  - Supports aggregated speed of 20Gbps, 30Mpps@667MHz
  - Lookups configured by user, can be chained
  - Classification result is frame queue ID, storage profile and policing profile.
- **Ingress Policing**
  - Two rate – three colour marking algorithm (rfc 2968 & 4115)
  - Up to 256 internal profiles

- **General**
  - Supports offline PCD on frames extracted from QMan
  - Supports “Independent” mode (no work with BMan & QMan, BD ring model)
  - Per port egress rate limiting
  - Statistics & Multicast support
  - Support for IEEE1588 thru HW-Timestamping



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Fman Enhancements relative to P4080

Enhancement	P4080	PSC9164	Comment
Rate	12G @ 600Mhz, 18Mpps	20G PCD@ 667Mhz , 30 Mpps	Internal architecture improvements.
Buffer pools selection	Port Based	Classification based through storage profiles	Better virtualization Bigger RX fifo able to hold the complete frame during classification
Fman memory	160K	384K	40K per 10G port: total 80K 25K per 1G/2.5K port: total 100K 12.5K per offline port: total 87.5 100K for classification tables
Offline Processing	no frame copy	frame copy according to classification & selected storage profile	better virtualization
Multicast	no special support	Support replication of frames	Performance impact of replication is the same as receiving/processing the frame multiple times
Fman controller	2 Riscs	4 Riscs	More performance for classification and Auto IPsec

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89

SEC (CAAM)

- Public Key Hardware Accelerators (PKHA)
  - RSA and Diffie-Hellman (to 4096b)
  - Elliptic curve cryptography (1023b)
- Data Encryption Standard Accelerators (DESA)
  - DES, 3DES (2K, 3K)
  - ECB, CBC, OFB modes
- Advanced Encryption Standard Accelerators (AESA)
  - Key lengths of 128-, 192-, and 256-bit
  - ECB, CBC, CTR, CCM, GCM, CMAC,
  - OFB, CFB, and XTS
- Message Digest Hardware Accelerators (MDHA)
  - SHA-1, SHA-2 256,384,512-bit digests
  - MD5 128-bit digest
  - HMAC with all algorithms
- Kasumi/F8 Hardware Accelerators (KFHA)
  - F8 , F9 as required for 3GPP
  - A5/3 for GSM and EDGE
  - GEA-3 for GPRS

- Snow 3G Hardware Accelerators
  - Implements Snow 3.0
- CRC Unit
  - Standard and user defined polynomials
- Random Number Generator, random IV generation
- ARC four execution unit
- ZUC integrity HW accelerator
- ZUC encryption HW accelerator
- Supports protocol processing for the following:
  - IPSec
  - 802.1ae (MACSEC)
  - SSL/TLS
  - 3GPP RLC
  - LTE PDCP
  - SRTP
  - 802.11i (WiFi)
  - 802.16e (WiMax)

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Serial RapidIO

- Two Serial RapidIO controllers
- Compliant with 2.0 standard plus selected 2.1 standard features
- Each controller supports
  - X1, X2, X4 @2.5 / 3.125 / 5 Gbaud rate
  - Full line rate of write type
  - Support Pass through
  - Direct access from the cores
- RMAN
  - Special block which is dedicated for doorbells, messages and streams
  - Handles 24 concurrent multi-segment messages/streams
  - Classification
  - Descriptor based both for inbound and outbound
  - Direct connection to QMAN and BMAN in order to offload cores.

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DMAs

- B4860 instantiates two OceAN DMAs
  - Transfer data between PCI/SRIO to the device memories
  - Transfer data between two locations in the memory

- Each DMA includes the following features
  - Eight channels
  - Advanced chaining and strides capabilities
  - Priority support
  - Can be activated using external signal

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