**《计算机原理与体系结构》实验报告**

**学号：16300240023 姓名：杨芗琳 学院：计算机科学技术学院 完成时间：2018.5.15**

1. 实验名称

设计实现Tomasulo算法

1. 实验目的

2.1 熟悉指令的动态调度方法;

2.2 熟悉 Tomasulo 算法；熟悉基于 Tomasulo 算法的前瞻执行算法

1. 实验过程

3.1分别使用Tomasulo算法、基于 Tomasulo算法的前瞻执行算法模拟执行下述指令

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 时间表 | | | | |
| 指令 | IS | EX | WB | （Commit）\* |
| LD F6,34(R2) | 1 | 2-4 | 5 | 6 |
| LD F2,45(R3) | 2 | 3-5 | 6 | 7 |
| MUL.D F0,F2,F4 | 3 | 7-17 | 18 | 19 |
| SUB.D F8,F6,F2 | 4 | 7-9 | 10 | 19 |
| DIV.D F10,F0,F6 | 5 | 19-59 | 60 | 61 |
| ADD.D F6,F8,F2 | 6 | 11-13 | 14 | 61 |
| SUB.D F10,F6,F2 | 7 | 15-17 | 18 | 61 |
| SD F10,24(R2) | 8 | 19-21 | 22 | 61 |

**Tomasulo算法**

1. MUL.D 指令将要写结果时（17->18）；

|  |  |  |  |
| --- | --- | --- | --- |
| 指令 | 指令状态表 | | |
| 流出/IS | 执行/EX | 写结果/WB |
| LD F6,34(R2) | √ | √ | √ |
| LD F2,45(R3) | √ | √ | √ |
| MUL.D F0,F2,F4 | √ | √ |  |
| SUB.D F8,F6,F2 | √ | √ | √ |
| DIV.D F10,F0,F6 | √ |  |  |
| ADD.D F6,F8,F2 | √ | √ | √ |
| SUB.D F10,F6,F2 | √ | √ |  |
| SD F10,24(R2) | √ |  |  |

图1：指令状态表（基于Tomasulo算法）

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 名称 | 保留站 | | | | | | |
| Busy | Op | Vj | Vk | Qj | Qk | A |
| Load1 | No |  |  |  |  |  |  |
| Load2 | No |  |  |  |  |  |  |
| Load3 | No |  |  |  |  |  |  |
| Store1 | Yes | S.D |  | Regs[R2] | Add3 |  | 24 |
| Store2 | No |  |  |  |  |  |  |
| Store3 | No |  |  |  |  |  |  |
| Add1 | No |  |  |  |  |  |  |
| Add2 | No |  |  |  |  |  |  |
| Add3 | Yes | SUB.D |  | Regs[F2] | Add2 |  |  |
| Mult1 | Yes | MUL.D | Mem[45+Regs[R3]] | Regs[F4] |  |  |  |
| Mult2 | Yes | DIV.D |  | Mem[34+Regs[R2]] | Mult1 |  |  |
| Mult3 | No |  |  |  |  |  |  |
| Branch1 | No |  |  |  |  |  |  |

图2：功能部件状态表（基于Tomasulo算法）

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 域 | 寄存器状态 | | | | | | | |
| F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
| Qi | Mult1 |  |  | Add2 |  | Add3 |  |  |

图3：结果寄存器状态表（基于Tomasulo算法）

2）DIV.D 指令将要写结果时(59->60)；

|  |  |  |  |
| --- | --- | --- | --- |
| 指令 | 指令状态表 | | |
| 流出/IS | 执行/EX | 写结果/WB |
| LD F6,34(R2) | √ | √ | √ |
| LD F2,45(R3) | √ | √ | √ |
| MUL.D F0,F2,F4 | √ | √ | √ |
| SUB.D F8,F6,F2 | √ | √ | √ |
| DIV.D F10,F0,F6 | √ | √ |  |
| ADD.D F6,F8,F2 | √ | √ | √ |
| SUB.D F10,F6,F2 | √ | √ | √ |
| ST F10,24(R2) | √ | √ | √ |

图4：指令状态表（基于Tomasulo算法）

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 名称 | 保留站 | | | | | | |
| Busy | Op | Vj | Vk | Qj | Qk | A |
| Load1 | No |  |  |  |  |  |  |
| Load2 | No |  |  |  |  |  |  |
| Load3 | No |  |  |  |  |  |  |
| Store1 | No |  |  |  |  |  |  |
| Store2 | No |  |  |  |  |  |  |
| Store3 | No |  |  |  |  |  |  |
| Add1 | No |  |  |  |  |  |  |
| Add2 | No |  |  |  |  |  |  |
| Add3 | No |  |  |  |  |  |  |
| Mult1 | No |  |  |  |  |  |  |
| Mult2 | Yes | DIV.D |  | Mem[34+Regs[R2]] | Mult1 |  |  |
| Mult3 | No |  |  |  |  |  |  |
| Branch1 | No |  |  |  |  |  |  |

图5：功能部件状态表（基于Tomasulo算法）

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 域 | 寄存器状态 | | | | | | | |
| F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
| Qi |  |  |  |  |  |  |  |  |

图6：结果寄存器状态表（基于Tomasulo算法）

**基于 Tomasulo算法的前瞻执行算法**

1. MUL.D 指令将要写结果时（17->18）；

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 指令 | 指令状态表 | | | |
| 流出/IS | 执行/EX | 写结果/WB | 确认/commit |
| LD F6,34(R2) | √ | √ | √ | √ |
| LD F2,45(R3) | √ | √ | √ | √ |
| MUL.D F0,F2,F4 | √ | √ |  |  |
| SUB.D F8,F6,F2 | √ | √ | √ |  |
| DIV.D F10,F0,F6 | √ |  |  |  |
| ADD.D F6,F8,F2 | √ | √ | √ |  |
| SUB.D F10,F6,F2 | √ | √ |  |  |
| ST F10,24(R2) | √ |  |  |  |

图7：指令状态表（基于Tomasulo算法的前瞻执行算法）

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 名称 | 保留站 | | | | | | | |
| Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
| Load1 | No |  |  |  |  |  |  |  |
| Load2 | No |  |  |  |  |  |  |  |
| Load3 | No |  |  |  |  |  |  |  |
| Store1 | Yes | S.D |  | Regs[R2] | #7 |  | #8 | 24 |
| Store2 | No |  |  |  |  |  |  |  |
| Store3 | No |  |  |  |  |  |  |  |
| Add1 | No |  |  |  |  |  |  |  |
| Add2 | No |  |  |  |  |  |  |  |
| Add3 | Yes | SUB.D |  | Regs[F2] | #6 |  | #7 |  |
| Mult1 | Yes | MUL.D | Mem[45+Regs[R3]] | Regs[F4] |  |  | #3 |  |
| Mult2 | Yes | DIV.D |  | Mem[34+Regs[R2]] | #3 |  | #5 |  |
| Mult3 | No |  |  |  |  |  |  |  |
| Branch1 | No |  |  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 编号 | ROB | | | | |
| Busy | 指令 | 状态 | 目的 | Value |
| 1 | No | LD F6,34(R2) | 确认 | F6 | Mem[34+Regs[R2]] |
| 2 | No | LD F2,45(R3) | 确认 | F2 | Mem[45+Regs[R3]] |
| 3 | Yes | MUL.D F0,F2,F4 | 执行 | F0 | #2\*Regs[F4] |
| 4 | Yes | SUB.D F8,F6,F2 | 写结果 | F8 | #1-#2 |
| 5 | Yes | DIV.D F10,F0,F6 | 指令流入 | F10 |  |
| 6 | Yes | ADD.D F6,F8,F2 | 写结果 | F6 | #4+#2 |
| 7 | Yes | SUB.D F10,F6,F2 | 执行 | F10 | #6-Regs[F2] |
| 8 | Yes | ST F10,24(R2) | 指令流入 | 24(R2) | #7 |

图8：功能部件状态表（基于Tomasulo算法的前瞻执行算法）

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 字段 | 寄存器状态 | | | | | | | |
| F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
| ROB项编号 | 3 |  |  | 6 | 4 | 7 |  |  |
| Qi | yes | no | no | yes | yes | yes | no | no |

图9：结果寄存器状态表（基于Tomasulo算法的前瞻执行算法）

1. DIV.D 指令将要写结果时(59->60)；

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 指令 | 指令状态表 | | | |
| 流出/IS | 执行/EX | 写结果/WB | 确认/commit |
| LD F6,34(R2) | √ | √ | √ | √ |
| LD F2,45(R3) | √ | √ | √ | √ |
| MUL.D F0,F2,F4 | √ | √ | √ | √ |
| SUB.D F8,F6,F2 | √ | √ | √ | √ |
| DIV.D F10,F0,F6 | √ | √ |  |  |
| ADD.D F6,F8,F2 | √ | √ | √ |  |
| SUB.D F10,F6,F2 | √ | √ | √ |  |
| ST F10,24(R2) | √ | √ | √ |  |

图10：指令状态表（基于Tomasulo算法的前瞻执行算法）

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 名称 | 保留站 | | | | | | | |
| Busy | Op | Vj | Vk | Qj | Qk | Dest | A |
| Load1 | No |  |  |  |  |  |  |  |
| Load2 | No |  |  |  |  |  |  |  |
| Load3 | No |  |  |  |  |  |  |  |
| Store1 | No |  |  |  |  |  |  |  |
| Store2 | No |  |  |  |  |  |  |  |
| Store3 | No |  |  |  |  |  |  |  |
| Add1 | No |  |  |  |  |  |  |  |
| Add2 | No |  |  |  |  |  |  |  |
| Add3 | No |  |  |  |  |  |  |  |
| Mult1 | No |  |  |  |  |  |  |  |
| Mult2 | Yes | DIV.D |  | Mem[34+Regs[R2]] | #3 |  | #5 |  |
| Mult3 | No |  |  |  |  |  |  |  |
| Branch1 | No |  |  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 编号 | ROB | | | | |
| Busy | 指令 | 状态 | 目的 | Value |
| 1 | No | LD F6,34(R2) | 确认 | F6 | Mem[34+Regs[R2]] |
| 2 | No | LD F2,45(R3) | 确认 | F2 | Mem[45+Regs[R3]] |
| 3 | No | MUL.D F0,F2,F4 | 确认 | F0 | #2\*Regs[F4] |
| 4 | No | SUB.D F8,F6,F2 | 确认 | F8 | #1-#2 |
| 5 | Yes | DIV.D F10,F0,F6 | 执行 | F10 |  |
| 6 | Yes | ADD.D F6,F8,F2 | 写结果 | F6 | #4+#2 |
| 7 | Yes | SUB.D F10,F6,F2 | 写结果 | F10 | #6-Regs[F2] |
| 8 | Yes | ST F10,24(R2) | 写结果 | 24(R2) | #7 |

图11：功能部件状态表（基于Tomasulo算法的前瞻执行算法）

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 字段 | 寄存器状态 | | | | | | | |
| F0 | F2 | F4 | F6 | F8 | F10 | … | F30 |
| ROB项编号 |  |  |  |  |  |  |  |  |
| Qi | no | no | no | no | no | no | no | no |

图12：结果寄存器状态表（基于Tomasulo算法的前瞻执行算法）