Control

	Instruction	Opcode	Funct	ALUFun[6]	Sign	PCSrc[3]	RegWrite	RegDst[2]	MemRead	MentoReg[2]	ALUSrc1	ALUSrc2	ExtOp	LuOp
R type	add	000_000	100_000	000_000	1	0	1	0	0	0	0	0	x	x
	add	000_000	100_001	000_000	0	0	1	0	0	0	0	0	x	x
	sub	000_000	100_010	000_001	1	0	1	0	0	0	0	0	x	x
	subs	000_000	100_011	000_001	0	0	1	0	0	0	0	0	x	x
	and	000_000	100_100	011_000	1	0	1	0	0	0	0	0	x	x
	or	000_000	100_101	011_110	0	0	1	0	0	0	0	0	x	x
	xor	000_000	100_110	010_110	1	0	1	0	0	0	0	0	x	x
	nor	000_000	100_111	010_001	0	0	1	0	0	0	0	0	x	x
	sll	000_000	000_000	100_000	1	0	1	0	0	0	1	0	x	x
	srl	000_000	000_010	100_001	1	0	1	0	0	0	1	0	x	x
	sea	000_000	000_011	100_011	0	0	1	0	0	0	1	0	x	x
	slt	000_000	101_010	110_101	1	0	1	0	0	0	0	0	x	x
	sltu	000_000	101_011	110_101	0	0	1	0	0	0	0	0	x	x
	sltu	000_000	101_011	110_101	0	0	1	0	0	0	0	0	x	x
	jr	000_000	001_000	x	x	3	0	x	0	0	x	x	x	x
	jalr	000_000	001_001	x	x	3	1	0	0	2	x	x	x	x
I type	lw	100_011	x	000_000	0	0	1	1	0	1	0	1	1	0
	sw	101_011	x	000_000	0	0	0	x	1	x	0	1	1	0
	lui	001_111	x	000_000	0	0	1	1	0	0	0	1	0	1
	addi	001_000	x	000_000	1	0	1	1	0	0	0	1	1	0
	addiu	001_001	x	000_000	0	0	1	1	0	0	0	1	0	0
	andi	001_100	x	011_000	1	0	1	1	0	0	0	1	0	0
	slti	001_010	x	110_101	1	0	1	1	0	0	0	1	1	0
	sltiu	001_011	x	110_101	0	0	1	1	0	0	0	1	0	0
	beq	000_100	x	110_011	1	1	0	x	0	x	0	0	1	0
	bne	000_101	x	110_001	1	1	0	x	0	x	0	0	1	0
	blez	000_110	x	111_101	1	1	0	x	0	x	0	0	1	0
	bgtz	000_111	x	111_111	1	1	0	x	0	x	0	0	1	0
	bltz	000_001	x	110_101	1	1	0	x	0	x	0	0	1	0
J type	j	000_010	x	x	x	2	0	x	0	x	x	x	x	x
	jal	000_011	x	x	x	2	1	2	0	2	x	x	x	x