

# NVCool: When Non-Volatile Caches Meet Cold Boot Attacks

Xiang Pan<sup>†</sup>, Anys Bacha<sup>‡</sup>, Spencer Rudolph, Li Zhou, Yinqian Zhang,  
and Radu Teodorescu

The Ohio State University, Uber<sup>†</sup>, University of Michigan<sup>‡</sup>

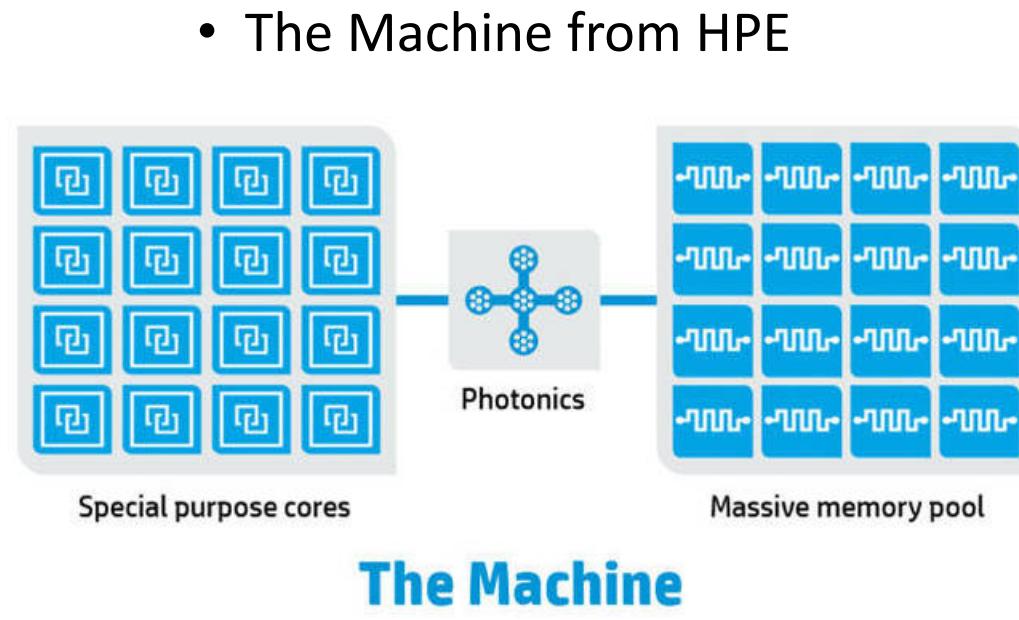
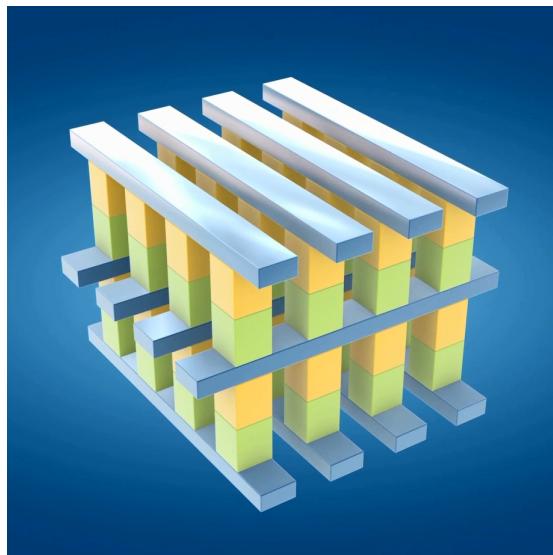


THE OHIO STATE UNIVERSITY



# Non-Volatile Memory is Coming

- Low power, high density, and good scalability make NVM attractive to industry companies
- 3D XPoint from Intel and Micron



- Crossbar and Everspin also make and sell NVM products

# Cold Boot Attack on DRAM

- Cooling DRAM to a certain low temperature can preserve its data for a short duration of time even without power supply



Halderman et al., Lest We Remember: Cold Boot Attacks on Encryption Keys, [citp.princeton.edu/research/memory](http://citp.princeton.edu/research/memory)

- Plug in the frozen DRAM DIMMs to a pre-prepared machine and run key search program to get secret keys
- Successfully conducted on both laptop and mobile computer systems



# Cold Boot Attack on NVM

- Trivial for NVM main memory but we focus on NVM caches
- NVM caches are vulnerable to cold boot attacks in a way SRAM caches are not
  - A few ms data retention time without power supply at cold temperatures
- Challenges
  - Caches only store a subset of data
  - Cache structure (set-associative) is very different from main memory (page)
  - Can we really find secrets from NVM caches?



# Outline

- Threat Model
- Cache-Aware AES Key Search
- Methodology
- Attack Analysis
- Countermeasure
- Conclusions



# Threat Model

- Attacker has physical access to the victim device
- Attacker has necessary equipments and knowledge to extract data from CPU caches



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# Threat Model

- What secrets can be found from cache?
  - Photos, emails, messages, disk encryption keys, ssh keys...
  - Anything stored in cache and useful to attacker
  - This work focuses on disk encryption keys as an example

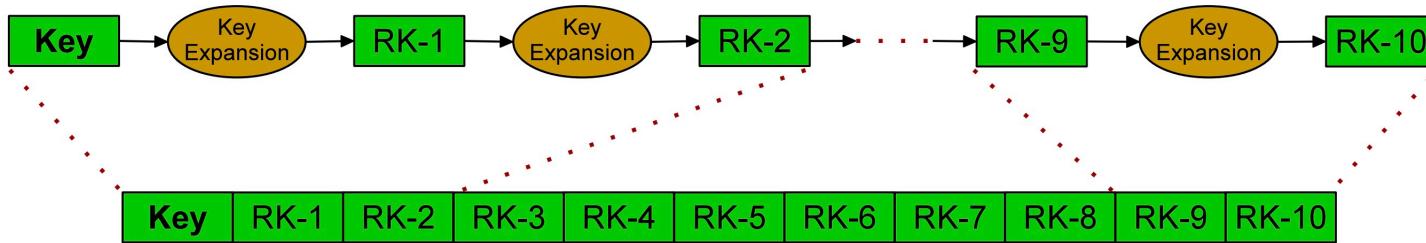


# Outline

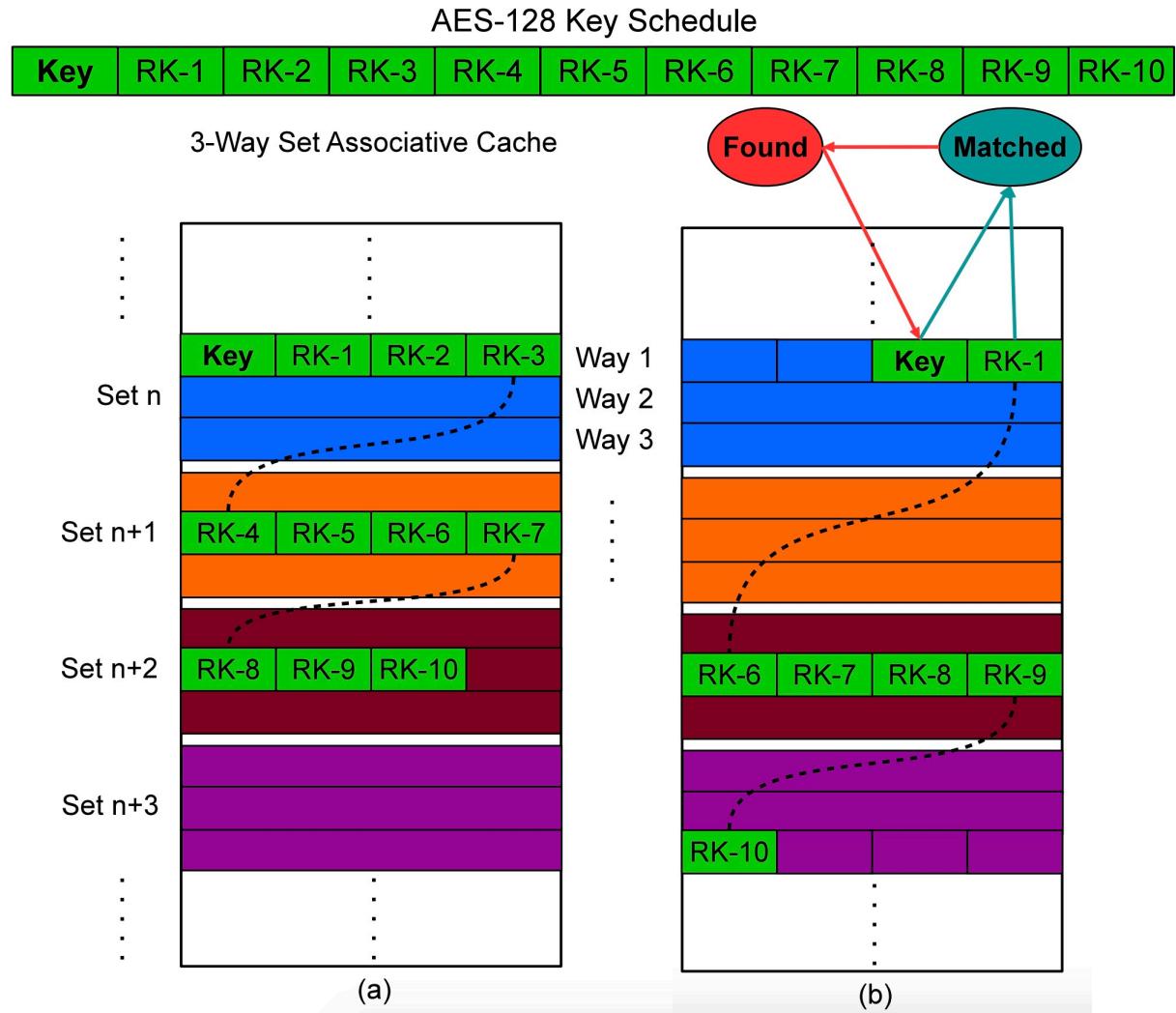
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# AES Key Schedule

- AES key search:
  - Original key needs to be expanded before encryption/decryption operations
- Current round key is deterministically computed from the previous round key
  - Scanning memory image sequentially can find the key if exists
- Challenges in cache-based approach:
  - Non-contiguous memory space
  - Incomplete key schedules



# Cache Aware AES Key Search



- Non-contiguous memory space
- Incomplete key schedules



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# Experimental Methodology

Software Configuration		Hardware Configuration	
Simulator	gem5	Cores	8 (out-of-order) ARMv8 (64-bit) 3GHz
OS	Ubuntu Trusty 14.04 64-bit	IL1/DL1 Size IL1/DL1 Block Size IL1/DL1 Associativity IL1/DL1 Latency Coherence Protocol	32KB 64B 8-way 2 cycles MESI
Disk Encryption Module	dm-crypt + LUKS	L2 Size	<u>2, 4, 8 (default), and 128MB</u>
Encryption Algorithm	AES-XTS with 128-bit key	L2 Block Size L2 Associativity L2 Latency	64B 16-way 20 cycles
Application	SPEC CPU2006	Memory Type	DDR3-1600 SDRAM [27]
Execution	1B insts to run	Memory Size	2GB
	1M insts to sample	Memory Page Size Memory Latency	4KB 300 cycles
		Disk Type	Solid-State Disk (SSD)
		Disk Latency	150us



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# Attack Scenarios

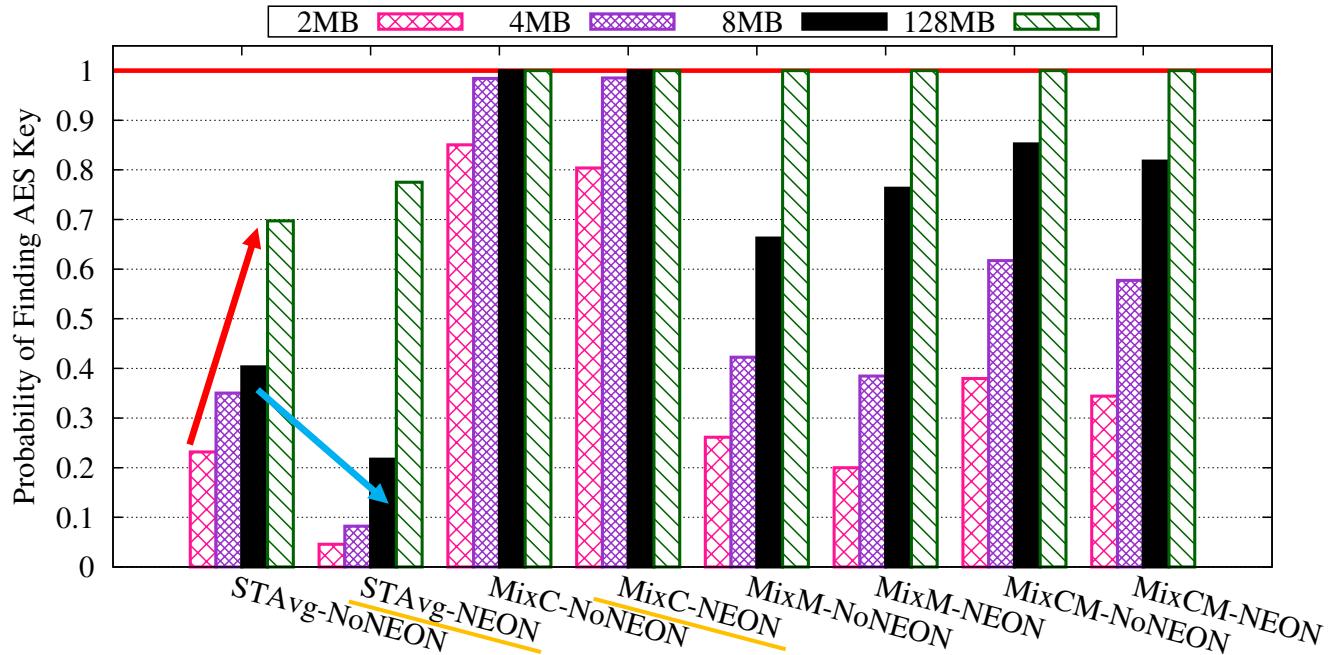
- Random Attack
  - Execution can be stopped at any given time to extract secrets from CPU caches
  - Due to power failures, disk failures, system crashes...
- Targeted Power-Off Attack
  - Conduct power-off operation on victim systems and extract secrets from CPU caches
  - Can be a normal power-off or a forced power-off

# Experiments and Benchmarks

NVCool Experiments	
<u>NoNEON</u>	System without ARM's cryptographic acceleration support
<u>NEON</u>	System with ARM's cryptographic acceleration support
STAvg	Geometric mean of single-threaded benchmarks from SPEC CPU2006

Mixed Benchmark Groups		
<u>mixC</u>	compute-bound	<i>calculix, dealII, gamess, gromacs, h264ref, namd, perlbench, povray</i>
<u>mixM</u>	memory-bound	<i>astar, cactusADM, GemsFDTD, lbm, mcf, milc, omnetpp, soplex</i>
<u>mixCM</u>	compute/memory	<i>dealII, gamess, namd, perlbench, astar, cactusADM, lbm, milc</i>

# Random Attack Analysis



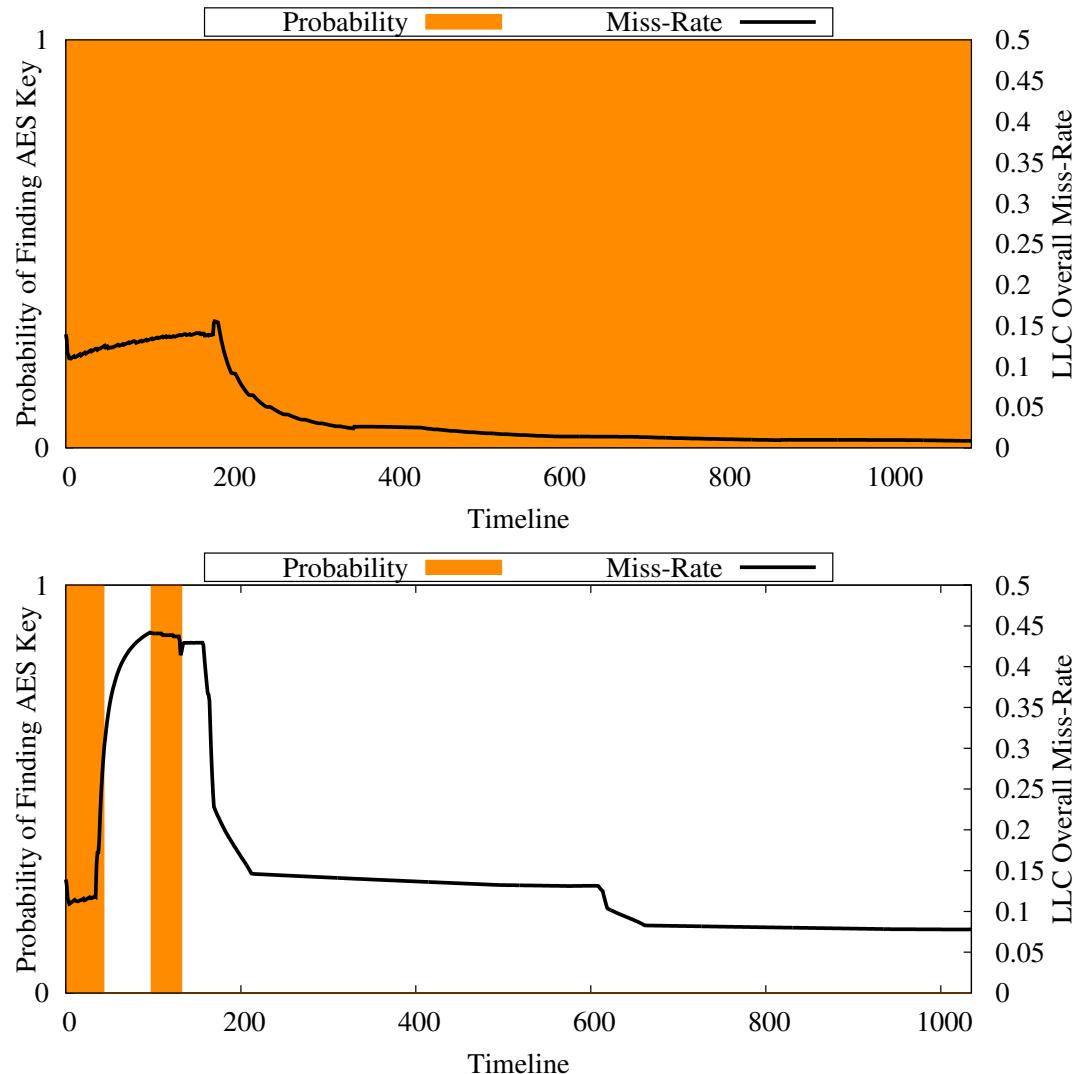
- Overall probability of finding AES keys in systems with different LLC sizes
- Larger caches increase the system vulnerability to random attack
- Systems running multi-programs are more vulnerable
- NoNEON systems are generally more vulnerable than NEON systems

# Random Attack Analysis

- Two factors:
  - Encryption disk accesses
  - Cache evictions

computation-  
bound: dealII

memory-  
bound: bzip2





# Power-Off Attack Analysis

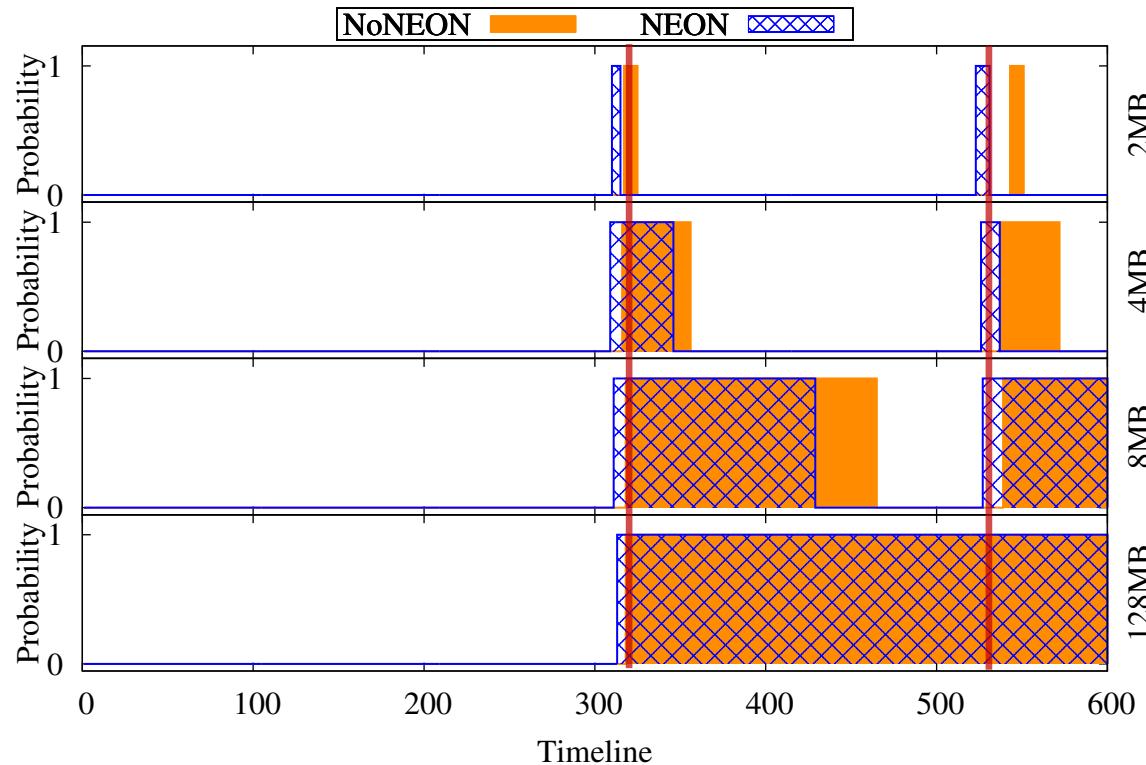
```
root@aarch64-gem5:/# poweroff
Session terminated, terminating shell...exit
...terminated.
* Stopping rsync daemon rsync
  [ OK ] // 1
* Asking all remaining processes to terminate...
  [ OK ] // 2
* All processes ended within 1 seconds...
  [ OK ] // 3
* Deactivating swap...
  [ OK ] // 4
* Unmounting local filesystems...
  [ OK ] // 5
* Stopping early crypto disks...
  [ OK ] // 6
* Will now halt // 7
[ 604.955626] reboot: System halted
```

- Two modes:

- Normal Power-Off:  
poweroff (-p)
- Force Power-Off:  
poweroff -f

# Power-Off Attack Analysis

Mode	Command	Keys exist in cache after power-off?			
		2MB	4MB	8MB	128MB
Normal Power-off	poweroff (-p)	N	N	Y	Y
Forced Power-off	poweroff -f	Y	Y	Y	Y





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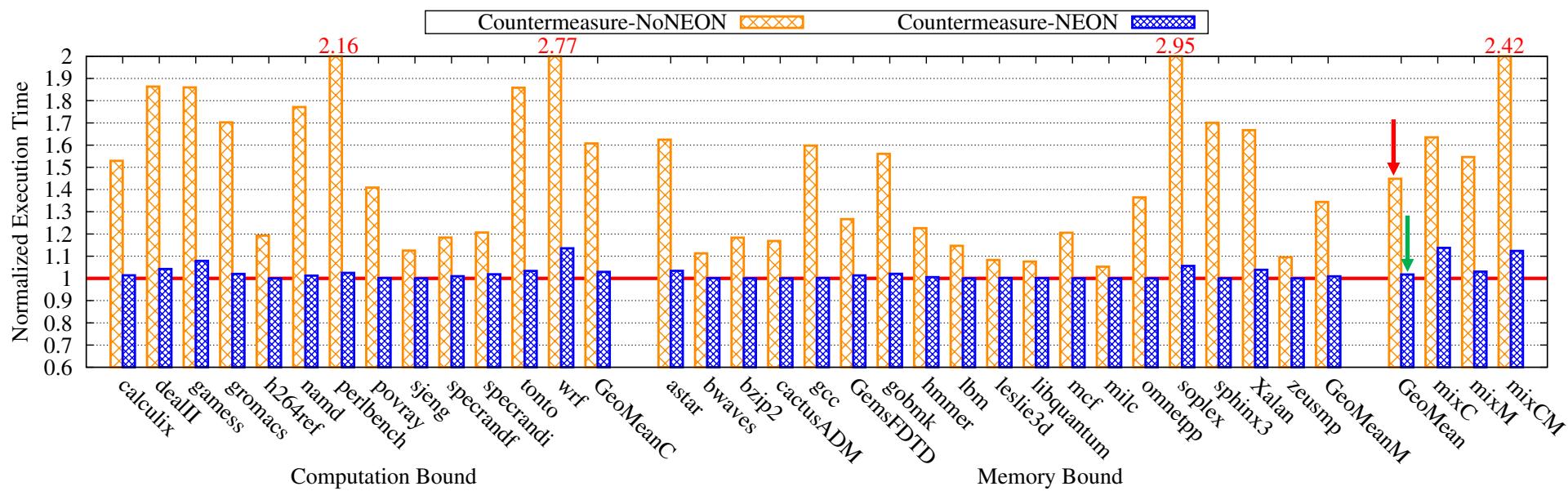
# Software-based Countermeasure

- Key idea: marking secret information as uncacheable
  - Walk through page table at kernel space; mark sensitive pages as uncacheable
- Effectiveness

	NoNEON	NEON	Countermeasure
Single-threaded Benchmark	23 - 70%	5 - 77%	<u>0%</u>
mixC	85 - 100%	80 - 100%	<u>0%</u>
mixM	26 - 100%	20 - 100%	<u>0%</u>
mixCM	38 - 100%	34 - 100%	<u>0%</u>
Normal Power-off	0 - 100%	0 - 100%	<u>0%</u>
Forced Power-off	100%	100%	<u>0%</u>

# Performance Analysis

- Performance Overhead



- NoNEON systems show high performance overhead
- NEON systems show less than 3% average performance overhead
- Performance optimizations are discussed in the paper



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# Conclusions

- Non-volatile caches are vulnerable to cold boot attacks
- Two attacks on disk encryption keys are successfully conducted — random attacks and targeted power-off attacks
- A software-based countermeasure that allocates sensitive information into uncacheable memory pages is developed and shown effective
- We hope this work will serve as a starting point for future studies on the security vulnerabilities of NVM caches and their countermeasures



# Questions?

# Thank you!